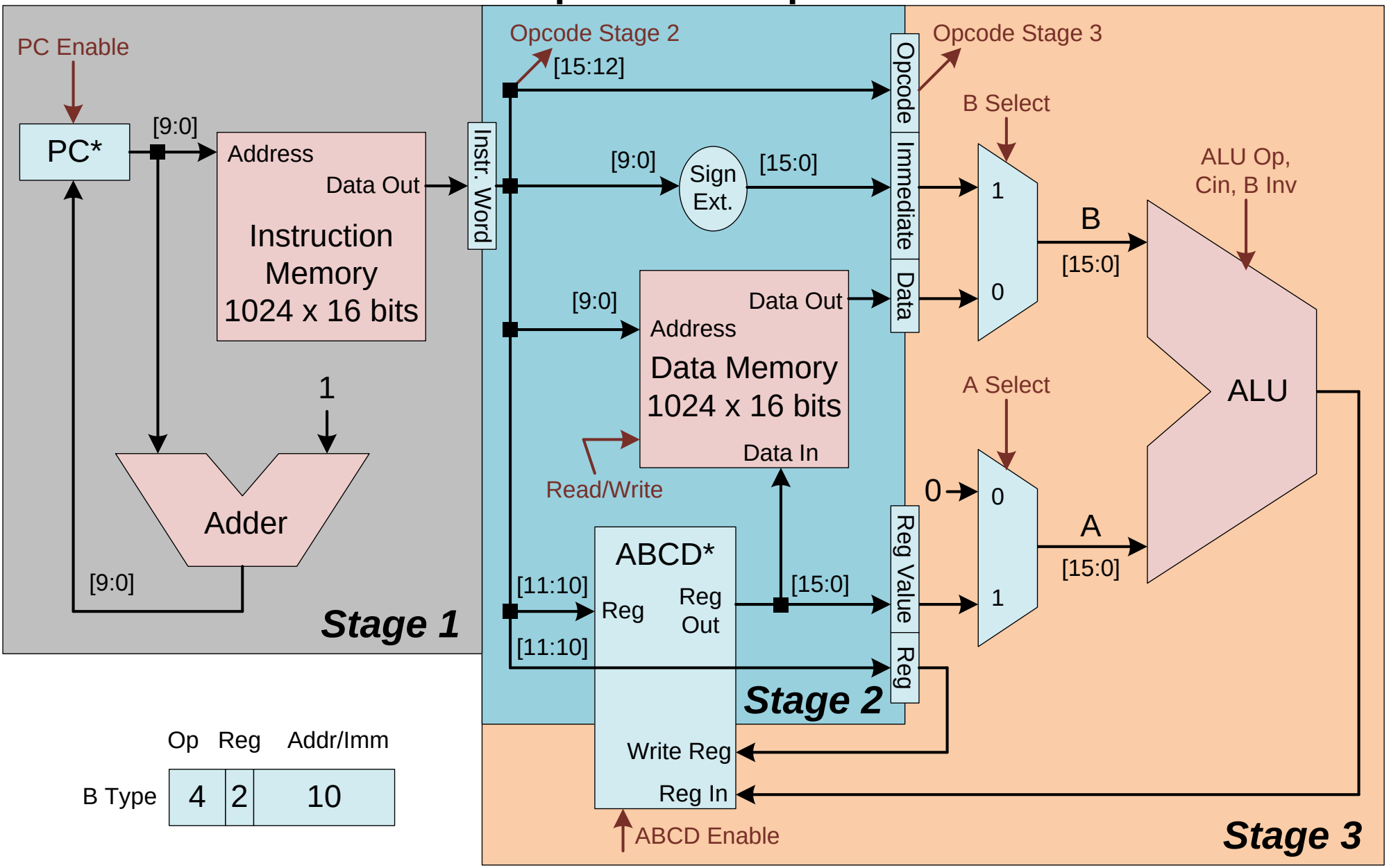
Pipelined Datapath



	Op	Reg	Addr/Imm
B Type	4	2	10

**Assume CLK and RESET control signals go to all registers*