

John Sarris Burke

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Computer Engineer with skills in Computer Architecture seeking challenging positions in hardware security and high performance applications

Education

Boston University College of Engineering, Boston, MA

Master of Engineering in Computer Engineering, September 2017 : GPA – 3.35/4.0

Bachelor of Science in Electrical Engineering, September 2011: GPA – 3.05/4.0

Technical Skills

Programming	C, C++, Python, Perl, Scala, MATLAB, Rust, Assembly (RISC-V and x86)
Skillset	GNU and Windows Compilers and Debuggers, Embedded and Baremetal development
Hardware	Verilog, System Verilog, Bluespec Language and Simulation tools, Chisel
Hardware	Xilinx, Synopsys, and Cadence Tools, Verilator, FPGA development
Additional	Tagged Processor Designs, Hardware and Software Security,
Capabilities	Multi-Threading, and High Performance Programming and Profiling

Work and Research Experience

Charles Stark Draper Laboratory

Cambridge, MA, October 2017 to Present

Embedded Hardware Security Research and Development Engineer

- ◊ Development, simulation, and testing of Draper's Inherently Secure Processor
- ◊ Introduced and enhanced open-source Rocket-Chip, Bluespec Flute and Piccolo
- ◊ Low level software development with PicoRV32 and SiFive Cores

Boston University

Boston, MA, May 2017 to October 2017

Research with BU Integrated Circuits and Systems Group (ICSG)

- ◊ Mapped the RISC-V Berkely Out of Order Machine onto FPGA with the Rocket Chip Generator
- ◊ Utilized and developed skills with RISC-V cross compiler, emulators, Linux, and related tools

MEDITECH

Framingham, MA, November 2011 to January 2017

System Analyst

- ◊ Developed TruCode Interface, in-house portion of the Site Information Retrieval Tool, other tools

Boston University

Boston, MA, September 2009 to May 2011

Undergraduate Teaching Assistant

- ◊ Assisted Professor teaching MATLAB to Engineering students
- ◊ Graded exams and quizzes, managed labs, recitations, and office hours

Relevant Projects

Boston University, Computer Architecture: Multicore Tiny RISC-V Processor

- ◊ Made a Quadcore CPU in Verilog using a restricted RISC-V ISA, private L1i caches, shared L1d
- ◊ Verified with PyMTL and by cross-compiling a parallel hybrid Merge-Quick sort written in C

Boston University, High Performance Programming: N-Body Simulation

- ◊ Designed an N-Body Gravitational simulation using the Barnes-Hut algorithm
- ◊ Multi-threaded C code with investigation of Intel Intrinsics and a simpler model in CUDA

Boston University, Machine Learning: Yelp Review Prediction

- ◊ Constructed Machine Learning systems to predict Yelp Ratings from review text
- ◊ Used scikit-learn's SVM and MLP to predict with 40 percent higher accuracy than random selection

Boston University, Senior Capstone: Magnetic Environment Sensor for the Naval Undersea Warfare Center

- ◊ Team project to create a device to sample and process magnetic fields and return frequency content
- ◊ Project started with initial design phases until a functional prototype

Philanthropy

Served several times in Mississippi for Hurricane Katrina Relief, impoverished areas of West Virginia. Often assist at Saint Francis House in Boston.