Invention Disclosure Form

Pu Justin Yang

October 23, 2024

Disclosure and Record of Invention

To be completed by the inventors:

Invention Title:

Development of p-adic Logic Gates and p-adic-Based Computers

Date Submitted:

October 23, 2024

Inventor #1

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1. Describe the problem that is being solved by the invention.

Current computers are limited by binary logic, which restricts the efficiency of complex arithmetic operations and number-theoretic algorithms. Binary systems also struggle with modular arithmetic and cryptographic computations that could benefit from more advanced number systems. This invention introduces **p-adic logic gates** and **p-adic-based computers** to leverage the

properties of p-adic numbers, improving performance in tasks such as cryptography, number theory, and quantum computing.

2. Describe how the problem is currently being addressed.

Currently, computers operate using binary logic, where computations are based on two states (0 and 1). Modular arithmetic, as required in cryptographic applications, is performed inefficiently using binary systems. Floating-point arithmetic also struggles with precision for certain mathematical applications, particularly in fields like cryptography or number theory. Although some modular arithmetic is optimized in existing cryptographic processors, no dedicated hardware exists to handle p-adic logic and computation directly.

3. List known prior art related to the invention.

- **Binary Logic Systems**: Traditional binary logic gates (AND, OR, XOR) are well-established in modern computing but do not handle p-adic arithmetic efficiently.
- **Cryptographic Hardware**: There are processors optimized for modular arithmetic (e.g., RSA encryption), but they are still based on binary logic.
- **p-adic Number Theory**: Research on p-adic numbers and their applications in mathematics is well-developed, but no prior implementation of p-adic logic gates in hardware has been made.

4. List the advantage(s) of the invention over the current solution(s).

- **Efficiency in Modular Arithmetic**: p-adic logic gates natively handle modular arithmetic, making cryptographic algorithms faster and more efficient.
- **Precision in Number Theory**: p-adic numbers have infinite expansions that can be truncated with controlled precision, allowing for highly accurate computations in number theory and cryptography.
- **Quantum and Neuromorphic Applications**: p-adic-based logic gates may have natural synergies with quantum and neuromorphic computing, where multiple states and non-binary systems are essential.

5. Provide a complete description of the invention, append any supporting description, drawings, tables, and data to this disclosure.

The invention is a **p-adic logic gate system**, which replaces traditional binary logic gates with gates that operate on **p-adic digits**. For a prime p, p-adic numbers are expressed as infinite expansions in powers of p. The system includes:
- **p-adic AND Gate**: This gate computes the minimum of two p-adic digits.
- **p-adic OR Gate**: This gate computes the maximum of two p-adic digits.
- **p-adic NOT Gate**: This gate inverts a p-adic digit using modular arithmetic.
- **p-adic XOR Gate**: This gate performs addition modulo p between two p-adic digits.

In addition to individual gates, the invention includes a full **p-adic-based computer architecture** capable of processing p-adic numbers and performing p-adic arithmetic efficiently. This architecture would consist of:
- **Custom Arithmetic Logic Units (ALUs)** for p-adic addition, subtraction, multiplication, and division.
- **Memory models** designed to handle infinite p-adic expansions with truncation strategies.
- **Efficient carry propagation circuits** to manage p-adic arithmetic's unique carry behavior.

6. List the title(s) and nature of any supplemental document(s) appended to this disclosure, or indicate not applicable (n/a).

- Appendix 1: p-adic Number Theory Overview
- Appendix 2: Circuit Design for p-adic Logic Gates

7. Could one of ordinary skill in the art make and use the invention based solely upon the disclosure provided with respect to Sections #5 and #6 above? (Y/N)

Yes, with expertise in both modular arithmetic and circuit design, one could implement this invention.

8. Is there a working prototype of the invention? (Y/N)

No. A hypothetical prototype could be built using **FPGAs** or **ASICs** designed for modular arithmetic.

9. List all known company projects or products that can use or benefit from the invention.

- **Cryptographic Hardware Companies** (e.g., those working on RSA and elliptic curve cryptography).
- **Quantum Computing Research Labs** interested in multi-valued logic systems.
- **Number Theory Research Labs** focusing on advanced modular arithmetic systems.

10. Would it be possible to reverse-engineer the invention? (Y/N)

No. The complexity of p-adic arithmetic makes reverse engineering challenging without the specific design details.

11. List date(s) of any prior or planned disclosure(s) of the invention and to whom, or indicate not applicable (n/a).

Not applicable.

12. List date(s) of any offers for sale of the invention and to whom, or indicate not applicable (n/a).

Not applicable.

13. List date(s) of any prior or planned public or commercial use of the invention, or indicate not applicable (n/a).

Not applicable.

14. List any joint developer(s) of the invention, or indicate not applicable (n/a).

Not applicable.