Metamodel:

Module:
-if more than one module is created Simulation will be set true use Simulation if you want to test the i2c with testbenches

Option:	Master	Slave:	Masterslave:	Description:
Clk_stretching:	variable	variable	supported	Slave can pull down clk
Multimaster:	variable	X	supported	Multiple Masters supported
ID:	X	variable	variable	ID of the device if not added, a register in the CSC for a variable ID will be generated
word_length_reg	variable	variable	variable	Register to set word_length if not set, word_length will be 8 bit
Prescalar_reg_size:	variable	variable	variable	Size of prescalar_reg Standard= 16bit
Bytetrans_reg_size	variable	variable	variable	Size of Register which stores number of bytes send standard = 8bit

FIFO:
- if FIFO is not added a 1 byte DataBuffer will be generated
- Depth has to be a power of 2

Option:	Master	Slave:	Masterslave:	Description:
ReceiveDepth:	variable	variable	variable	Depth of Receive FIFO standard = 256
SendDepth:	variable	variable	variable	Depth of Send FIFO standard = 256

Interuppt:

Option:	Master	Slave:	Masterslave:	Description:
TransFinished:	variable	variable	variable	Sends Interrupt if Transmission is finished
DataProcess:	variable	variable	variable	Sends Interrupt if Data has to be processed
Error:	variable	not supported	variable	Sends Interrupt if an Error occurred (desynch not included)
CrAddress:	not supported	variable	variable	Sends Interrupt if Address is correct (Slave)
Edge:	variable	variable	variable	Determines Edge for Interrupt (Rising,Falling,Both)