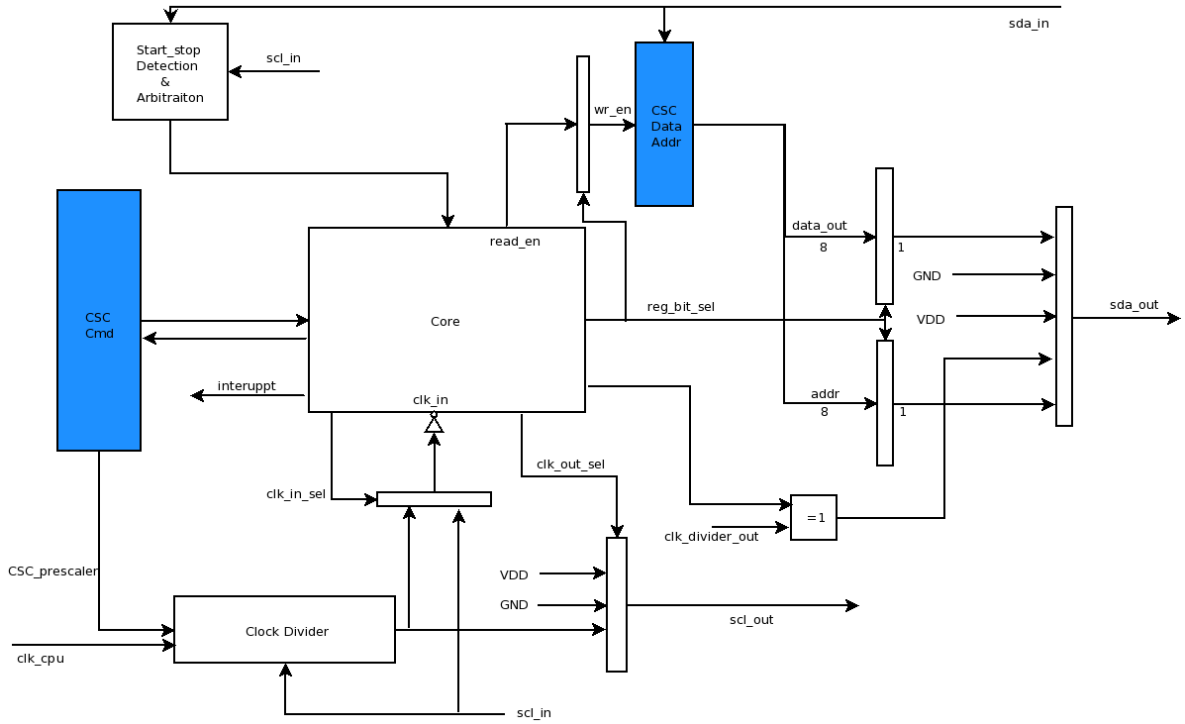
I2C-Peripheral Documentation:

Features:

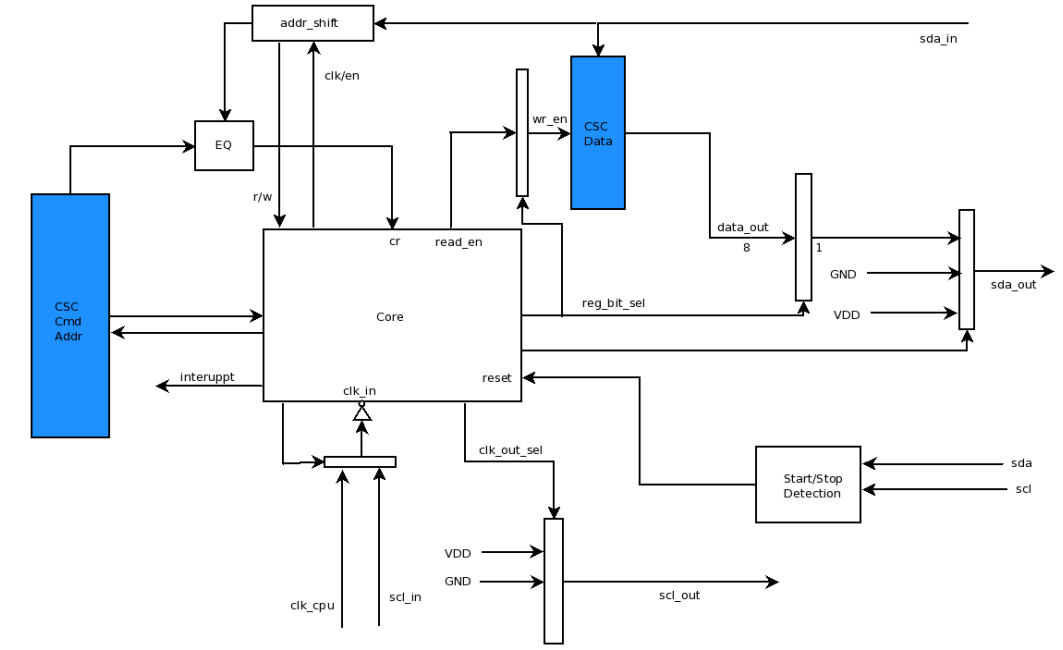
For supported features please use the document describing the metamodel.
The different models don’t support sending a start byte or using a 10bit address.

Implementation:

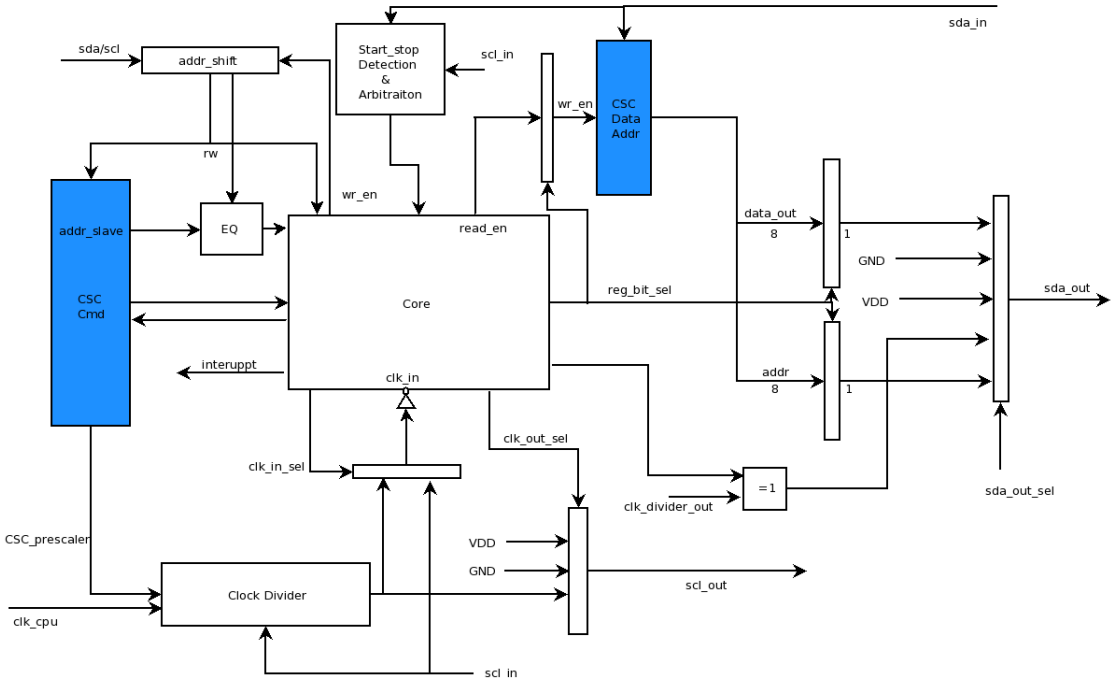
The Schematics show a simplified Structure of the three different Types in the most complicated configuration, the different components will be described later in this documents.
Multimaster:



Slave with clockstretching:



MasterSlave:



CSCInterface:

Cmd & Status :

Name	Description	M	S	MS
rw	Set if write, reset if read			
slave	Set if module in slave mode			
cr	Set if received address matches internal			
StartReset	Set if you want to start another Transmission after the first using the repeated start condition			
Busy	Is set if the master is currently transmitting			
Error	Is set if an error occurs, won't be reset from master			
Abort	Set if you want to abort the Transmission will be reset by master			
Go	Set if you want to start a Transmission will be reset by master			

Data:

To enable a smoother Transmission the user can generate a FIFO, if not a simple byte sized databuffer with a status bit will be generated. If you write to the databuffer you have to set the status bit and if you are reading a byte you have to reset the bit. The FIFO contains two separated FIFOs one for the data to be send and one for the data to be received. There are two status signals which are set if the respective FIFO is full/empty (depends on the direction), and a wr_en and a rd_en signal to enable reading/writing a byte.

Address:

Master:
The outgoing address is stored in a byte sized register, the LSB is the r/w bit (write = '0')
Slave:
Depending on the Metamodel the 7-bit address is stored in the CSC or in a RAM.

Bytenumber- and prescaler:

The Bytenumberregister stores the number of bytes to transmit and the prescalerregister contains the value of the prescaler. The Size of both registers can be freely chosen by the user. The Slave doesn't have a prescaler.
(max 32 bit)

Wordlength :

If generated it can be used to send data words shorter than 8bits, the word length is
8 – int(Wordlengthregister).

Core:

The Core contains a finite state machine and two counters. One counter counts the number of bytes send the other counter determines the current bit in the dataword/adrressbyte they both compare the output with the desired number. The fsm is a Mealy Machine and is based on PLA-Design and will be presented in more detail in a different document

Clkdivider:

The clkdivider slows down the incoming clock, and in the case of a multimaster it follows the i2c-protocoll to synchronize clocks of multiple masters. The Slave has no clkdivider.

Arbitration & start-stop-detection:

In the master determines whether the bus is blocked or the transmission has desynched. In the slave it detects a start condition and sends a pulse to the core. In the masterslave it does both.

Interrupt:

The interrupt is generated by the core, and can be triggered by different events, which are chosen by the user. The edge of the interrupt can also be determined.