

A 4mW-RX 7mW-TX IEEE 802.11ah Fully-Integrated RF Transceiver

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Abstract—An IEEE 802.11ah-compliant RF transceiver with a direct-conversion receiver and a fully-digital polar transmitter is presented. For the receiver, a current-mode RF front-end covers the mandatory modes worldwide from 755MHz to 928MHz. The digitally-assisted analog baseband achieves variable gains and bandwidths with an automatic gain/DC-offset calibration. Implemented in 40nm CMOS with 1V supply, this receiver achieves -104dBm sensitivity in the 1MHz MCS0 mode (i.e., 300kbps). It fulfills the adjacent channel rejection requirements with at least 17dB margin. The digital polar transmitter achieves -31dB EVM and 10dB spectral mask margin.

Index Terms—IoT, IEEE 802.11ah, Wi-Fi HaLow, transceiver, receiver.

I. INTRODUCTION

Wi-Fi HaLow, or IEEE 802.11ah, is a new flavor in the Wi-Fi family of standards. It is optimized to the requirements of sensor node communication, where power consumption needs to be at least one order of magnitude lower than current Wi-Fi devices. In addition, it brings Wi-Fi to the sub-GHz bands, which helps in extending the communication range. The standard defines multiple data rates and a sensitivity as low as -98dBm for the lowest data rate mode of 150kbps (i.e., MCS10). Different from other IoT standards that employ constant envelope modulation for higher power efficiency but at the cost of spectral efficiency and channel robustness, IEEE 802.11ah adapts OFDM modulation schemes with 1/2MHz mandatory and 4/8/16MHz optional bandwidths. An 11ah-compliant RF transceiver (TRX) has to fulfil competitive specifications without compromising the power consumption. Especially on the receiver (RX) side, the flexibility to support different sub-GHz bands in different countries/areas with -98dBm sensitivity puts constraints on the noise and LNA matching; the 16dB-adjacent/32dB-alternate channel rejection (ACR) requires extensive interference filtering which is challenging with low-power implementation. The support of advanced OFDM modulation also needs co-optimization of the receiver analog baseband (ABB) and digital baseband (DBB) for automatic gain/DC-offset calibration.

In this paper, an ultra-low power 11ah-compliant RF transceiver is presented. The second generation fully-digital polar transmitter (TX) updated from [1] further

improves the EVM to -31dB with 10dB spectral mask margin. The digitally-assisted receiver achieves 6dB noise figure for the sub-GHz bands worldwide from 755MHz to 928MHz. The co-optimization of the ABB and DBB enables a RX-input dynamic range from -18dBm to -104dBm with a data rate of 300kbps for the MCS0 mode. The 33dB/43dB ACR is achieved by programmable low-pass filters (LPFs) with extra digital filtering. This RF transceiver fulfills IEEE 802.11ah standard under the 1/2MHz MSC 0-4 modes with 4.4mW-RX and 7.2mW-TX power consumption.

II. SYSTEM ARCHITECTURE

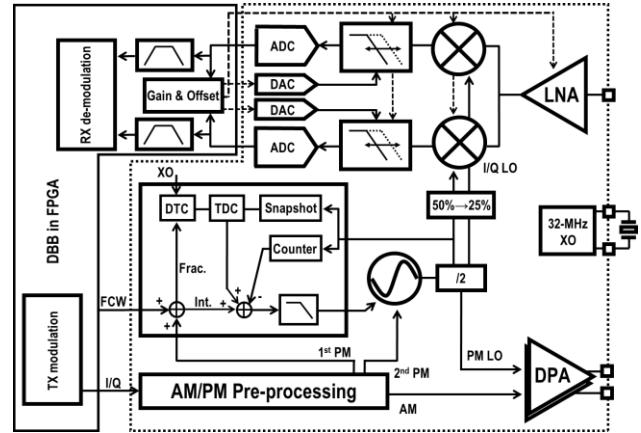


Fig. 1. A top-view of the IEEE 802.11ah transceiver.

The 11ah-compliant transceiver is illustrated in Fig. 1. A low-power direct-conversion (zero-IF) receiver architecture is used according to the specifications defined in IEEE 802.11ah, such as the omission of sub-carriers at the centre of the OFDM spectrum. The current-mode LNA has configurable centre frequencies and gains. Together with quadrature passive mixers, the RF front-end achieves good linearity with low flicker noise. After being down-converted to baseband, the received signals are filtered with 3rd-order LPFs. Two 9b successive approximation (SAR) ADCs [2] run at a configurable sampling rate of 6.4/8/10.6/16MHz. Such high dynamic range enables further signal enhancements in the digital domain, including interference filtering.

The direct-conversion architecture makes the receiver vulnerable to static or dynamic DC-offset. When the LPF has a high gain, a small DC-offset at the input could saturate the LPF output stage, or shift the ADC input level out of its optimal operation point. Conventional DC-offset removal techniques using AC-coupling or servo-loop in the legacy Wi-Fi (i.e., 11b/g/n) are not feasible in 11ah, this is due to the 10 \times narrower sub-carrier spacing which leads to a large chip area. In this work, a DC-offset trimming DAC is added in each of the LPF to remove the large static DC-offset. In addition, the dynamic DC-offset is removed in the digital domain with an area-efficient digital band-pass filter (BPF).

The all-digital PLL (ADPLL) [1] provides an RF single-tone signal at twice of the carrier frequency, and a low-power divider generates the quadrature LOs for mixers. In the receiver mode, since the oscillator phase is locked within the detection range of the time-to-digital converter (TDC), the integral part of the PLL phase detection (mainly, the counter) can be switched off to save power [3]. The second generation fully-digital polar transmitter is updated from [1]. Increased signal resolution and filter suppression in the digital AM/PM pre-processing module further improve the EVM and spectral purity.

III. TRX IMPLEMENTATION

A. The current-mode RF front-end

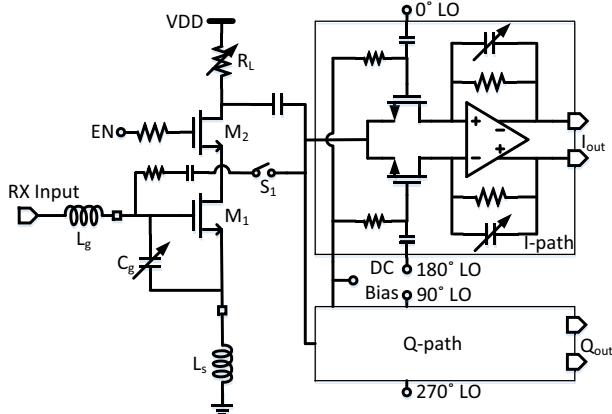


Fig. 2. The schematic of the LNA with quadrature mixers

The implementation of the tunable LNA with passive mixers is shown in Fig. 2. A single-ended source-degenerated topology is applied for the LNA with two off-chip inductors. Since the matching network is narrowband, a 3b programmable capacitor bank C_g is used to match the LNA input impedance at different centre frequencies. The LNA load is resistive instead of inductive to save area. Compared to an active PMOS load, a passive resistor provides higher impedance with lower noise. However,

the DC current can cause a large voltage drop, which limits the output voltage headroom and degrades the front-end linearity. In this work, these imperfections are eliminated by the current-mode operation. Because of the feedback in the trans-impedance amplifier (TIA, the output stage of each mixer), its input is virtually grounded. The reciprocity of the passive mixing up-converts the TIA input impedance from DC to the LO frequency at the LNA output. Since the LNA load itself presents a high impedance, the RF current will flow into the mixers without introducing a large voltage swing at the LNA output. As the mixers are directly connected to the LNA by an AC-coupling capacitor, to improve the reverse isolation, a cascode transistor M_2 is added. In the low-gain mode, M_2 also serves as a switch to disconnect M_1 from the LNA output, while the additional RC path is switched on by S_1 .

The passive mixers consist of four-path NMOS switches with TIAs for the I/Q branches. The TIAs are configured as low-pass to provide additional interference suppression before the following baseband stage. 25% duty-cycle LO signals are applied to achieve 6dB higher conversion gain and also better noise performance [4]. With a proper DC bias provided to achieve a higher overdrive voltage, the NMOS switches can be switched on with low resistance, and switched off with low leakage.

B. The digitally-assisted analog baseband

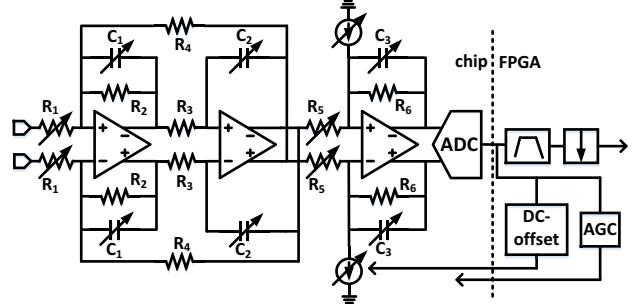


Fig. 3. The implementation of the ABB with part of the DBB (only one branch is shown).

The detailed implementation of the ABB together with part of the DBB is shown in Fig. 3. Each baseband LPF is made of a Tow-Thomas bi-quad section (the 1st and 2nd order) followed by a single-pole stage (the 3rd order). The benefit of this architecture is that the DC gain, cut-off frequency, and Q-factor can be set independently. The gain is tuned by changing resistors R_1 and R_5 , and the bandwidth is tuned by simultaneously changing the three capacitors C_1 , C_2 and C_3 , according to Equation 1-4.

$$G_{1,2} = \frac{R_2}{R_1} \quad (1)$$

$$G_3 = \frac{R_6}{R_5} \quad (2)$$

$$\omega_{1,2} = \frac{1}{\sqrt{R_3 R_4 C_1 C_2}} \quad (3)$$

$$\omega_3 = \frac{1}{R_6 C_3} \quad (4)$$

After the LPFs, 9b SAR ADCs interface the baseband signal to the digital domain. An automatic gain control (AGC) loop together with a DC-offset calibration algorithm is triggered during the preamble period of received packets. The AGC loop first sets the circuits to the highest gain mode, and then reduces the gain starting from the LPFs to the LNA according to the signal strength. The DC-offset is compensated by injecting a differential current at the input of the 3rd-order op-amp. The differential current is generated by an 8b current-mode DAC which covers the entire LPF dynamic range. It is worth to mention that the interaction between the AGC and the DC-offset calibration has to be carefully taken into consideration, as the DC-offset varies with different gain settings. The gain and DC-offset correction automatically calibrate during the initial part of the short training field (STF) and are frozen for the remainder of the frame. The BPF removes the residual and dynamic DC-offset, it also provides additional filtering to further suppress interferences and aliases. Then, the signals are down-sampled to 1/2MHz for de-modulation.

C. Low-power divider design

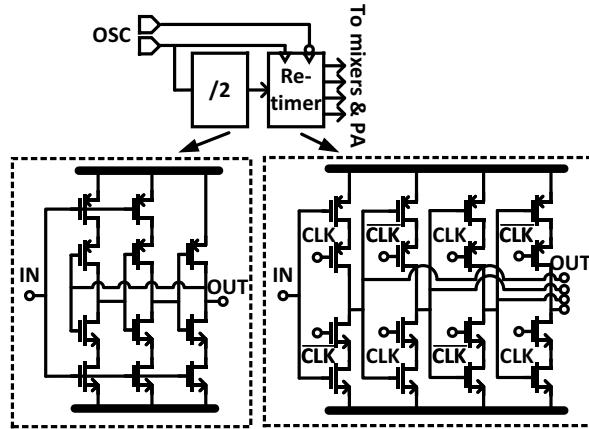


Fig. 4. The schematic of the low-power divider.

As mentioned above, the digital circuits of the polar transmitter are improved for EVM and spectral mask margin. On the RF side, a new divider is implemented for lower power consumption, which is shown in Fig. 4. This power-optimized solution splits the frequency division into two stages: a low-power divider similar to [5] followed by a low-power retiming circuit to generate the 4-phase LOs and restore the phase noise performance from the original RF oscillator. The /2 divider is based on a 3-stage ring oscillator with controlled phase propagation. The following re-timer is composed of 4 dynamic latches, it converts the single-phase divider output to 4-phase LOs

for the mixers and PA. Compared to the divider in [1], this one also eliminates the extra start-up circuits, and make the architecture concise and robust.

IV. MEASUREMENT

This IEEE 802.11ah RF transceiver is fabricated in 40nm CMOS, with 1V supply. As shown in Fig.5, it occupies 1.5×1.6mm². The die is packaged in QFN48.

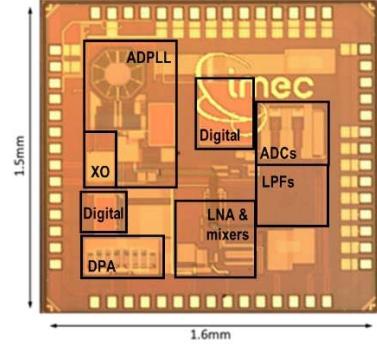


Fig. 5. Die photo of the proposed transceiver.

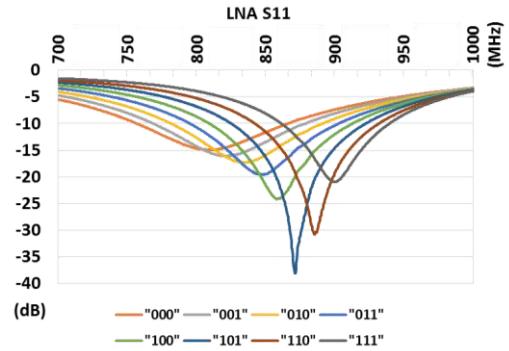


Fig. 6. Measured S11 curves of the LNA.

The frequency response of the LNA input matching is shown in Fig. 6. With the 3b programmable capacitor, better than -10dB S11 is achieved between 755MHz and 928MHz, which is sufficient to cover most of the sub-GHz bands around the world.

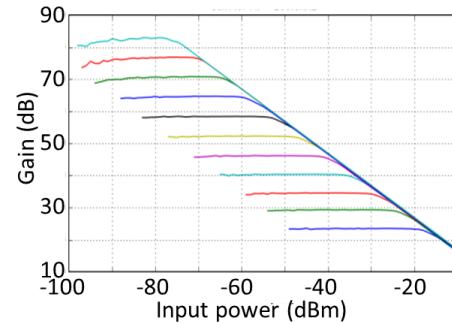


Fig. 7. Receiver gain curves in different gain modes.

The AGC loop relies on accurate gain steps that are implemented in the receiver circuits. All the gain modes are swept and plotted in Fig. 7. This receiver has a

variable gain from 83dB to 23dB with 6dB steps. The 1dB compression point of the minimal gain mode is -18dBm.

The receiver sensitivity is defined as the minimal input power for 10% packet error rate (PER) in 11ah. As plotted in Fig. 8(a), the proposed receiver achieves a dynamic range from -18dBm to -104dBm in the 1MHz MCS0 mode. The ACR performance is also evaluated and shown in Fig. 8(b), the combination of the analog LPFs together with the digital BPFs achieves total 33dB suppression for adjacent interferences, which is 17dB better than the standard requirements.

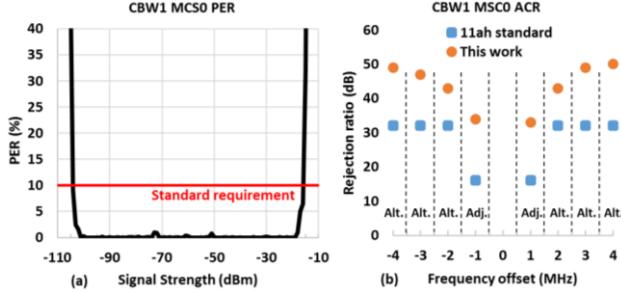


Fig. 8. (a) Rx dynamic range; (b) Rx ACR performance.

The transmitter EVM and spectral purity is also evaluated through the Keysight WLAN analyzer and is shown in Fig. 9 (with cable loss included). Compared to [1], by optimizing the digital AM/PM pre-processing module, the EVM is improved by 4dB, and the sprectal mask margin is 5dB better. Finally, the power breakdown of the transceiver is illustrated in Fig. 10.

