Low Power IEEE 802.11ah Receiver System-Level Design Aiming for IoT Applications

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ABSTRACT

Internet of Things (IoT) is a topic of growing interest and intensive research in industry, technological centers and academy, where data communication is one of its most relevant aspects. Since IoT is an open field for new applications, it does not have yet a standard communication protocol. This paper presents the system level design of a Wi-Fi receiver supporting the novel low power standard IEEE 802.11ah with focus on IoT applications. Theoretical performance analysis as well as system level design strategies are presented. Individual blocks of the receiver chain are specified as a condition for future circuit-level design. Simulation results validate the proposed system specifications attending the 802.11ah standard. The presented receiver provides 80.5dB maximum gain, 9 dB minimum noise figure and 69.4 dB of dynamic range. Those performance parameters lead to -99.4 dBm sensitivity, 21 dB and 51 dB for adjacent and non-adjacent maximum channel rejection.

Categories and Subject Descriptors

B.7.0 [**Integrated Circuits**]: General

Keywords

Internet of Things (IoT), Wi-Fi HaLow, IEEE 802.11ah, Low Power, Receiver

1. INTRODUCTION

The concept of Internet of Things, also known as Internet of Everything (IoE), has been a growing discussion topic both in academic community and industry [8] [9]. The main idea behind this concept is the ability of data storage and exchange by a wide variety of devices or sensors, connecting a large number of smart objects. The Internet of Things finds applications in many different fields, as wearables, health care, automobilistic industry, smart buildings and smart cities [11].

Many communication standards have been developed to deal with the demands of IoT applications. Some of which are Bluetooth Low Energy (BLE), Zigbee, LoRaWAN and Wi-Fi HaLow (IEEE 802.11ah) [5]. The last one is a promising alternative for IoT devices, since it is still an emerging standard based on the widely used Wi-Fi network communication protocol. Whereas the standard is still evolving, suitable low power radio systems are desired for Wi-Fi HaLow usage.

In this paper, system level design of a receiver for the novel 802.11ah standard is presented. The paper is organized as follows: Section 2 presents a brief introduction of the standard and its requirements. In Section 3, specifications for the receiver and its blocks are calculated from the communication protocol. Section 4 reports tests performed for verification of the receiver, while simulation results of the system fulfilling all communication demands are shown in Section 5. Finally, Section 6 presents concluding remarks.

2. THE IEEE 802.11AH STANDARD

The IEEE 802.11 standard is the baseline for internet Wi-Fi communication technology. The base standard was released in 1997 and is nowadays widely adopted for wireless connectivity of digital devices. It has been developed to allow high data rates and top performance for a small number of connected devices, but not for Wireless Sensor Network (WSN) and IoT applications, which in turn require a large number of units besides low transmission data rates and power consumption. Nowadays there are some different standards that fulfill these objectives, but the IoT market is expanding and none of them has been established as an global answer [5]. Considering this scenario, the IEEE 802.11ah Task Group was formed in 2010 in order to create an amendment to the 802.11 standard addressing the demand for WSN and IoT purposes.

The Wi-Fi HaLow solution defines its specification over a set of unlicensed sub-1GHz bands that are available in

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Table 1: Mandatory Modulation Coding Schemes

	MCS10	MCS0	MCS1	MCS2	Unit
Modulation	BPSK	BPSK	QPSK	QPSK	-
Code Rate	1/4	1/2	1/2	3/4	-
Data Rate (1MHz)	0.150	0.300	0.600	0.900	Mpbs
Data Rate (2MHz)	-	0.650	1.300	1.950	Mpbs
Sensitivity (1MHz)	-98	-95	-92	-90	dBm
Sensitivity (2MHz)	-	-92	-89	-87	dBm
ACR	19	16	13	11	dB
NACR	35	32	29	27	dB

most territories, such as United States, Europe and Japan. Although sub-1GHz bands are more limited in terms of bandwidth availability, they are suitable for IoT applications which consists of a high number of low-rate, low-power and long distance devices [1], thus presenting all characteristics to support WSN. The carrier frequency of about 900 MHz allows long distance (up to 1km) in low-traffic band. A hierarchical identification structure enables a network up to 6,000 devices connected to an Access Point (AP). Low-power strategies and fast and short transmissions (approximately 100 bytes per data package) complete these features.

Since regulation of the sub-1GHz varies between different regions, so does the operation range of IEEE 802.11ah. A frequency range between 863MHz and 930MHz enables operation in Europe, United States, Japan and Brazil. Five different channel bandwidths are supported, with 1 MHz and 2 MHz bandwidths mandatory and widely adopted. The standard employs eleven modulation coding schemes (MCS) [6], ten of which are equivalent to the modulation coding schemes in IEEE802.11ac standard. A new version of the MCS0, with half the corresponding code rate, is introduced as MCS10 for improvement in robustness. Table 1 gathers characteristics and requirements of each MCS, including values of adjacent channel rejection (ACR) and non-adjacent channel rejection (NACR) power levels. All MCS require a maximum packet error rate (PER) of 10%, considering a package formed by 256 octects. The maximum RF input power level supported by the standard is -30 dBm for any modulation scheme.

3. SYSTEM AND BLOCKS SPECIFICATIONS

3.1 Receiver Architecture and Intermediary Frequency

There are two main RF receiver architectures: heterodyne and homodyne. In the first case, the demodulated signal is down-converted to a certain intermediary frequency (IF), and, in the latter, to DC level. Further, heterodyne architectures can also be subdivided in low-IF and high-IF solutions. In a low-IF receiver, the intermediary frequency is typically up to three times the signal bandwidth.

The direct-conversion architecture is not appropriate for a narrow band system because of the effect of flicker noise (also called 1/f noise) at low frequencies and the crosstalk between the local oscillator (LO) and the RF input signal [3]. Due to the necessity of multiple frequency conversions and high quality filters, the classic heterodyne high-IF is also not adequate for implementation as an integrated circuit solution aiming low power. The most suitable architecture for an on-chip 802.11ah system is, then, heterodyne low-IF architecture.

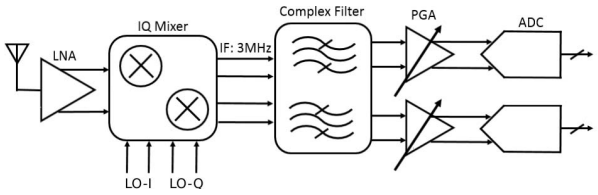

Figure 1: Receiver Architecture

The system intermediary frequency is then defined based on the corner frequency of the technology process, to avoid significant flicker noise contribution. Since the receiver under study aims a future design in a 130 nm CMOS technology, which presents a corner frequency around 2 MHz, the IF was chosen equal to 3 MHz, suitable for both mandatory bandwidths. The low-IF architecture needs, however, an image rejection strategy. To overcome this issue, the complex filtering procedure was selected and is explored further in subsection 3.4. Figure 1 represents the block diagram of the final receiver architecture.

3.2 Required SNR and Noise Figure

Receiver sensitivity is defined as the minimum signal power level that a receiver can detect with acceptable quality, which is the minimum signal-to-noise ratio (SNR) that the system can tolerate with an established error rate [10]. The relation between minimum SNR and error rate depends on type of modulation, error correction mechanisms and quality of the digital decoder system [12]. Thus system signal bandwidth, SNR and noise figure (NF) present limitations to the receiver sensitivity, which can be expressed as [10]:

$$P_{sen} = -174dBm/Hz + NF + 10logBW + SNR_{min} \quad (1)$$

Where P_{sen} is the sensitivity, NF is the receiver total noise figure, BW is the signal bandwidth, SNR_{min} is the minimum required SNR and the term $-174dBm/Hz$ is the equivalent 300 K thermal noise of an 50 Ω input impedance. The worst case for NF, according to equation (1), is the minimum sensitivity required by MCS10, with a bandwidth of 1 MHz. The minimum SNR needed was defined from simulation as around 5 dB (as described in Sections 4 and 5) and corroborated with results found in [12]. For such a signal quality, NF should then be less than 11 dB. Considering an implementation margin of 2 dB, the receiver total noise figure resulted in 9 dB.

3.3 Intermodulation, Linearity and Adjacent Channel Rejection

The linearity of the receiver can be expressed by the second and third order intermodulation points (IIP2 and IIP3) and by the 1 dB compression point [10]. Different constraints apply to each parameter.

The out-of-band IIP3 is defined by the maximum acceptable channel corruption, which happens due to the adjacent and the non-adjacent channels an can be estimated in dB

by equation (2) [10].

$$IIP3_{dB} = 20 \cdot log\sqrt{\frac{4}{3} \cdot \left|\frac{\alpha_1}{\alpha_3}\right|} \quad (2)$$

Terms α_1 and α_3 are, respectively, receiver linear gain and third order coefficient of the receiver non-linear gain Taylor expansion (3rd harmonic). Channel corruption is expressed by IM3, which corresponds to the difference between signal power level and interferer power level that appears on the frequency of interest, due to the adjacent and the non-adjacent channels. It can be written as in equation (3), in which A_0, A_1 and A_2 are the power levels of the desired signal, of the adjacent channel and of the non-adjacent channel, respectively. These amplitudes are defined by channel rejection requirements shown in Table 1 and are equal to -95 dBm, -76 dBm and -60 dBm.

$$IM3 = 20 \cdot log\left|\frac{3\alpha_3 A_1^2 A_2}{4\alpha_1 A_0}\right| \quad (3)$$

For this purpose an IM3 of 15 dB is considered as an acceptable interference. Thus, the out-of-band IIP3, calculated by equations (2) and (3) is equal to -51 dBm.

The in-band IIP3 is related to the input signal dynamic range and to the 1 dB compression point (IP1dB). To assure that the receiver operates without saturation, it is necessary to consider the peak-to-average ratio (PAR) of the input signal. The minimum input-referred compression point is thus given by equation (4).

$$IP1dB = Pin_{max} + PAR \quad (4)$$

Where Pin_{max} is the maximum input power.

For an OFDM process with 56 subcarriers, the PAR is approximately equal to 10 dB [4]. As despicted in Figure 1, the chosen architecture employs a gain control, which will be explored further in Subsection 3.5. Considering the maximum input level requested by the first gain step mode (-80.5 dBm), so the compression point is -70.5 dBm. The IIP3 is approximately 10 dB higher than IP1dB. Thus, the in-band IIP3 requirement is -60.5 dBm and the receiver linearity (for the first gain step) is then limited by the out-of-band IIP3, which is -51 dBm. This comparison between in-band and out-of-band IIP3 requirements is repeated for each gain mode of the receiver to define its linearity, and shown on Table 2.

Another effect of non-linearity that must be considered is the second-order intermodulation products. They can appear due to the local oscillator frequency self-mixing or from external interference mixing products. They affect multicarrier systems because of the overlap between different subcarriers. It is shown in [7] that the second order effects can be tolerated by a 802.11a receiver if the IIP2 remains higher than 0 dBm.

The required channel rejection determines the necessary filter order. The system should be able to reject an adjacent channel by 19 dB and a non-adjacent channel by 35 dB at MCS0 (1 MHz channel bandwidth). Considering a butterworth filter model, 19 dB of rejection with 1MHz from the corner frequency demands a 5th order filter, and 35 dBm of rejection with 2MHz from the corner frequency requires a 4th order filter. Thus, the proposed filter is a 6th order one divided in three cascaded 2nd order blocks, or biquads, since they exhibit better image rejection ration than two cascaded stages of first order ones [2].

3.4 I/Q Mismatch

One of the requirements of the low-IF architecture is image rejection. The image is an interference that appears on the frequency translation process. The mixing operation between the desired signal and the local oscillator signal occurs for an undesired image signal as well. A possible solution that is widely used for image rejection is the employment of a complex filter after the frequency translation, which does not require two mixing operations. This is done in the analog domain instead of the more common digital domain for low-power receivers because it reduces the necessary signal back-off at the ADC, a block which power consumption depends heavily on the dynamic range. The implementation of a complex analog filter instead of a common I/Q channel selection filter does not increase this block power significantly, thus, the receiver can achieve lower overall power with this architecture. In this type of circuit the image suppression depends on the accuracy of the amplitude and phase of the oscillator signals and also on the gain difference and phase delays between the I and Q paths of the receiver. The Image Rejection Ratio (IRR) in this architecture can be estimated by equation (5) [10].

$$IRR = \frac{4}{\left(\frac{\Delta A}{A}\right)^2 + \theta^2} \quad (5)$$

Where $\Delta A/A$ is the amplitude mismatch, and θ is the phase mismatch between in-phase and quadrature signals. The image channel is considered to be up to 35 dB above the desired one and the same power consideration is made for the non-adjacent channel rejection. Considering a desired margin of 10 dB between the signal and the interferer at baseband, the IRR shall be 45 dB. To achieve this value an amplitude mismatch of 0.07dB and a phase mismatch of 0.45° are required.

3.5 Dynamic Range, Gain Control and ADC Resolution

Considering the minimum and maximum input level for the IEEE 802.11ah standard -98 dBm (MCS10) and -30 dBm, respectively, the receiver dynamic range is 68 dB. A gain control is necessary in order to narrow the input signal variations at the analog-to-digital converter (ADC) and relax its resolution specification. This control is mainly performed by a block the programmable gain amplifier (PGA), but also by the low noise amplifier (LNA).

The ADC full scale (FS) was first set to 1 V_{pp} for differential signals, which corresponds to 1 dBm for a 50 Ω reference impedance. With a 10 dB PAR, the necessary receiver gain is 89dB, in order to achieve the 1 dBm level at the end of the chain at the minimum power level (-98 dBm). For a -30 dBm input, the gain shall be 21 dB.

A 3-bit control was chosen for the PGA and 1-bit control for the LNA, leading to a 8.5 dB step size with 8 steps, represented in Figure 2. By changing the receiver gain according to the input level, noise and linearity requirements can be better adjusted for each level, defining 8 gain modes, as detailed in Table 2. HG and LG stand for high and low gain, respectively, and are related to the LNA.

The ADC resolution was chosen based on the worst case SNR degradation. A maximum SNR degradation of 0.5 dB due to AD conversion was regarded as acceptable for an SNR input of 8.5 dB. Considering that a 7-bit resolution leads to a signal degradation of 0.42 dB, a 8-bit resolution ADC was

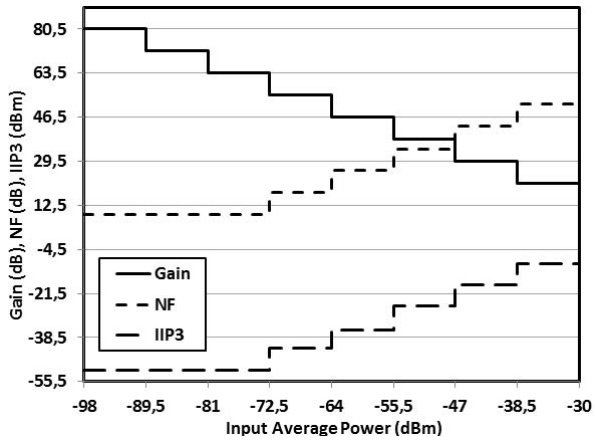

Figure 2: Receiver specifications for 8 different gain modes

defined thus allowing an implementation error margin of 1 bit.

3.6 Blocks specifications

System requirements for a 802.11ah receiver were calculated in the previous subsections. They are summarized in Table 3. With these characteristics, specifications for each internal block of the architecture shown in Figure 1 can be devised. Some of these are directly taken from the receiver top specifications, such as filter order and ADC resolution. Yet gain, noise and linearity characteristics ought to be distributed between receiver blocks. To accomplish this, the cascaded effect of the noise figure was estimated by the Friis' Formula in equation (6), and the cascaded IIP3, by equation (7).

$$F = 1 + (F_1 - 1) + \frac{F_2 - 1}{G - 1} + ... + \frac{F_n - 1}{G_1 \cdot ... \cdot G_{n-1}} \quad (6)$$

$$\frac{1}{A^2_{IP3}} \approx \frac{1}{A^2_{IP3,1}} + \frac{G^2_1}{A^2_{IP3,2}} + ... + \frac{G^2_1 \cdot ... \cdot G^2_{n-1}}{A^2_{IP3,n}} \quad (7)$$

F and A_{IP3} are the total noise factor and total intermodulation third order amplitude. F_i, A_{IP3}, i and G_i are respectively noise factor, third order amplitude and power gain of the i-th cascaded stage.

Initially, the receiver was divided in two stages: RF front-end (LNA and Mixer) and baseband (BB) stage (Filter and PGA). The distribution of specifications was made based on the established performance found in literature, considering trade-offs between gain, linearity and noise. Since the input dynamic range is quite large, two gain modes were defined for the RF front-end and eight gain modes for the baseband, as mentioned previously. Resulting specifications for RF and BB stages were then divided between gain-switched LNA and Mixer and between three cascaded programmable filter and PGA stages, respectively. PGA stages perform both the filtering process and the gain control. For clarity, top baseband characteristics are presented, instead of individual internal blocks, in Table 2. Mixer specifications remain the same for all gain modes: 12 dB for gain, 15 dB for NF and 0 dBm for IIP3, and were not specified in the aforementioned table.

4. SYSTEM SIMULATION

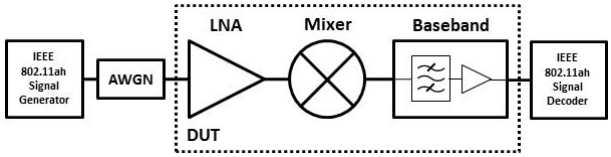

Figure 3: Receiver system modeling

In order to verify receiver and its internal block specifications, the complete system was simulated with software SystemVue 2016.08, which contains a dedicated IEEE 802.11ah library. SystemVue has model sources and receivers that emulate the digital signal processing used to code and decode the standard modulated signals, meaning receiver architecture and block specifications can be validated under protocol restrains.

Two test-benches were built, one to determine the minimum SNR required and another to perform validation tests of the designed receiver, defined by the communication protocol. The first one consists only of a 802.11ah transmitter model with variable power, an additive white Gaussian noise channel and an ideal decoder. The second test-bench has a 802.ah signal generator with two transmitter blocks (for main channel signal and optional interferer), an additive white Gaussian noise channel, the designed receiver and the digital baseband verification model. The system modeling is depicted in Figure 3. All blocks were modeled with variable non-idealities, such as NF and IIP3, and I/Q mismatch for the mixer. The depicted baseband stage is composed by three cascaded blocks, each one containing a second order filter and a variable gain amplifier. The 8-bit quantization is realized at the decoder block. Results for both tests are discussed in Section 5.

In digital modulation, the quality of a given signal after baseband processing can be described by the rate of the bits (or defined packages of bits) which suffered modification during reception and decoding. These rates are bit error rate (BER) and package error rate (PER). However, they must be translated to a correspondent signal-to-noise ratio before analog-to-digital conversion, in order to define receiver specifications.

The 802.11ah standard determine as acceptable a PER of 10%, considering a package formed by 256 octects. The first test verifies the relation between SNR and PER for different modulation coding schemes. The transmitter power is swept from noise floor level (corresponding to SNR = 0) to a power 14 dB higher (SNR = 14 dB). The signal proceeds to the 802.11ah baseband model, which recovers the coded bits. These are compared with the original generated bits in order to evaluate the error rate. The objective of this test is the verification of the quality needed by the decoder as a way to correctly design the receiver.

The second testbench allows an estimate of sensitivity and channel rejection (for both alternate and non-adjacent channels). A performance evaluation at the highest power level can also be realized to verify system linearity. The sensitivity test is conducted by varying the input power and checking the PER at the end of the receiver chain for a 10% minimum and is performed for all MCS. Channel rejection can be verified by applying two signals to the receiver, a desired one and an interferer, with powers specified as in

Table 2: Receiver blocks specifications

		LNA			Baseband		
Input Power (dBm)	**Mode RF/BB**	**Gain (dB)**	**NF (dB)**	**IIP3 (dBm)**	**Gain (dB)**	**NF (dB)**	**IIP3 (dBm)**
-98 to -89.5	HG/000	14	5	-29	54	31.5	-25
-89.5 to -81	HG/001	14	5	-29	46	31.5	-25
-81 to -72.5	HG/010	14	5	-29	37.5	31.5	-25
-72.5 to -64	LG/010	5.5	13	-4.5	37.5	31.5	-25
-64 to -55.5	LG/011	5.5	13	-4.5	29	43	-18
-55.5 to -47	LG/100	5.5	13	-4.5	20.5	51.5	-9
-47 to -38.5	LG/101	5.5	13	-4.5	12	60.5	0
-38.5 to -30	LG/110	5.5	13	-4.5	3.5	69	-12

Table 3: Receiver specifications summary

Receiver Spec	**Min**	**Typ**	**Max**	**Unit**
Intermediary Frequency	-	3	-	MHz
Gain	21	-	80.5	dB
Noise Figure	9	-	-	dB
Ip1dB	-41	-	-	dBm
IIP2	0	-	-	dBm
IIP3	-51	-	-	dBm
I/Q Amplitude Mismatch	-	-	0.07	dB
I/Q Phase Mismatch	-	-	0.45	◦
Filter Order	6	-	-	-
PGA Step Size	-	8.5	-	dB
ADC Resolution	-	8	-	bits

Table 1 and following evaluation of the package error rate delivered.

5. SIMULATION RESULTS

The SystemVue IEEE 802.11ah digital baseband model was verified to obtain the correct PER and SNR relation. Results for this test are shown in Figure 4 (a) for MCS at 1 MHz bandwidths and in Figure 4 (b) for MCS at 2 MHz bandwidths. The minimum SNR required for a package error rate below 10% occurs for MCS0 at 2 MHz and is 4.75 dB. However, the sensitivity demanded by MCS10 at 1 MHz is 6 dB lower, hence, the SNR needed for this case (5 dB) determines the minimum noise figure of the receiver.

The proposed receiver is modeled in SystemVue and submitted to an envelope simulation with 1000 transmitted packages in order to evaluate the PER for the various required performances. The first performed test concerns about the sensitivity of the receiver. All mandatory modulation coding schemes were tested for the input powers specified in Table 1 without any interferer. Under these conditions only MCS10 and MCS0 at 1 MHz presented significant PER (higher than 1e-6). The error rates are respectively 0.7% and 3.3%. The input power was swept between -103 dBm and -98 dBm in order to evaluate the maximum sensitivity achieved. The minimum input power with acceptable PER is -99.4 dBm, result which is shown in Figure 5

Channel rejection tests were realized following the specifications for each MCS to set the interferer and main channel power. The non-adjacent channel rejection is verified with no significant package error rate, i.e., all required tests by the standard lead to a PER lower than 1e-6. The two highest error rates found in adjacent channel rejection tests were 0.3% for MCS2 at 2MHz and 0.2% for MCS10. The maximum channel rejection achieved by the proposed receiver was determined by setting the main channel power as -95 dBm and varying the interferer channel power until the

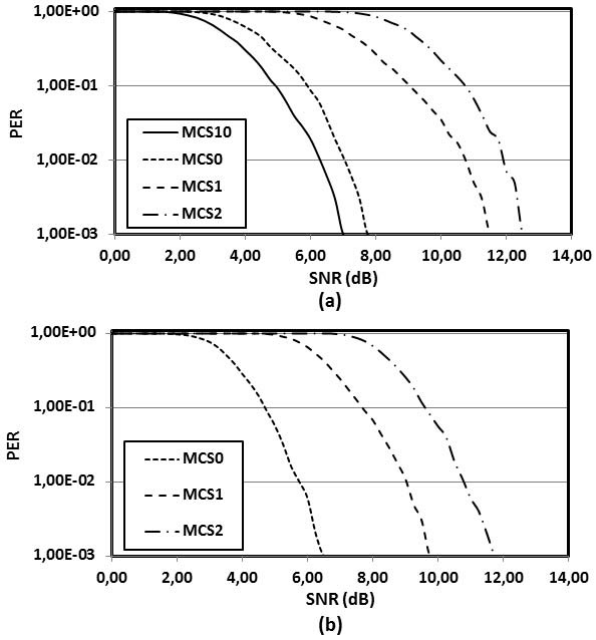

Figure 4: Simulated PER and SNR relation of supported modulation coding schemes at (a)1 MHz and (b)2 MHz

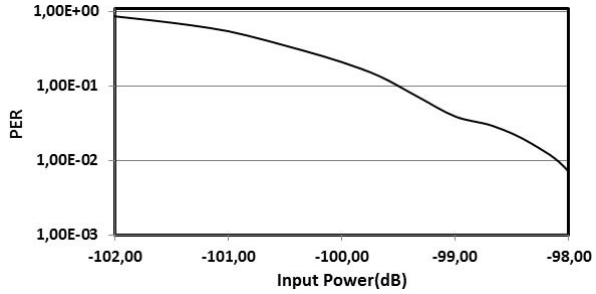

Figure 5: Simulated PER as function of the input power

PER reaches 10%. The ACR is 25 dB and the NACR is 40 dB. Figure 6 shows the input signal spectra for the MCS10 NACR test and of the signal at the end of the receiver chain, exhibiting the performed channel rejection.

The receiver performance is also validated for the several gain modes specified in Section 3 and for I/Q impairments. Each mode was submitted to its lower and higher power lev-

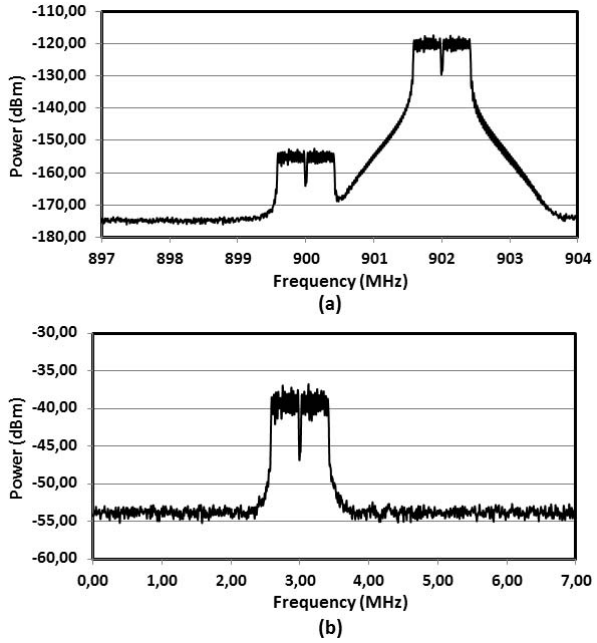

Figure 6: Simulated signal spectrum at receiver (a) input and (b) output

els and all different MCS and the error rate was evaluated. The maximum PER noticed occurs for the gain range from -98 dBm to -89.5m dB and is equal to 3.3%, showing no significant error due to non-linearity and compression when compared to noise requirements. Each performed test was realized with the I/Q amplitude and phase mismatches described in section 3.

6. CONCLUSIONS

A system level design for a receiver supporting the novel IEEE 802.11ah standard focused on IoT low power implementations was presented. Basic design concepts of a generic heterodyne low-IF receiver were introduced and then applied to the specific study case. The performance specifications were spread between RF front-end and the following analog blocks as discussed. In order to achieve the desired performance for the entire required dynamic range (from -98 dBm to -30 dBm), a PGA with 8 gain modes was devised and specified. The complete receiver system was simulated under the conditions specified by the communication standard. The proposed receiver provides 80.5 dB maximum gain, 9 dB minimum noise figure and 69.4 dB dynamic range. Those lead to -99.4 dBm sensitivity, 21 dB and 51 dB for adjacent and alternate maximum channel rejection. The next task is the design of the RF and analog blocks in a 130 nm technology aiming the fabrication and tests.

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