

# ProtoDUNE-SP Central Trigger Board

## Capabilities and Proposed Trigger Scheme

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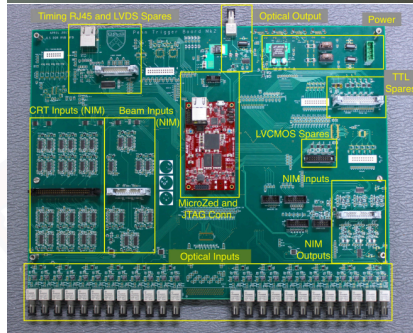
University of Pennsylvania

A large, faint watermark of the University of Pennsylvania seal is visible in the background, tilted diagonally. The seal features a shield with a ship, a lion, and an open book, with the word 'UNIVERSITY' and the year '1681' also present.

# The Central Trigger Board (CTB)

- Second (revised) iteration of trigger electronics used in DUNE 35-ton
- Uses a MicroZed
  - Zynq-7000 SoC
  - ~100 I/O ports
  - Dual-core ARM processor
  - Gigabit ethernet
  - 1GB of RAM
- **Motherboard** implements hardware interface with different systems
- FPGA implements trigger logic, interface with timing
- CPU/Software manages FPGA configuration and communication with DAQ software

This board decides when we have something worth recording



Jon Sensenig

# Definitions

**Channel** Input to the CTB. Each subsystem has several channels.

**Coincidence Window** Time period (in clock cycles) that each individual input is shaped to permit coincidences

**Reshape time** Same as above. Historically also known as **trigger gate**

**Delay** Time period (in clock cycles) that a signal is delayed before being passed to the trigger logic.

**Prescale** Number of triggers that are ignored before accepting one and propagating it to trigger distribution

**LLT Low Level Trigger.** Trigger at subsystem level (PDS, CRT, BI)

**HLT High Level Trigger.** Global trigger, built from LLTs.

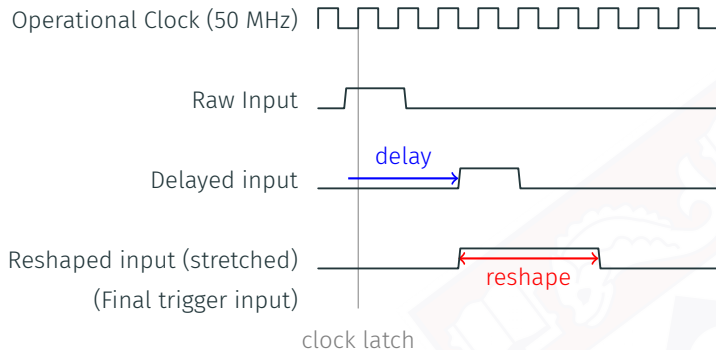
**Board Reader** artDAQ interface to the CTB (config and data handling)

**Calibration Stream** Aka **Monitoring Stream**. Data stream for monitoring of CTB activity. Likely outside artDAQ.

## Important Remarks

The CTB is a synchronous system. Asynchronous inputs are latched and processing is begun on rise of the operational clock (50 MHz)

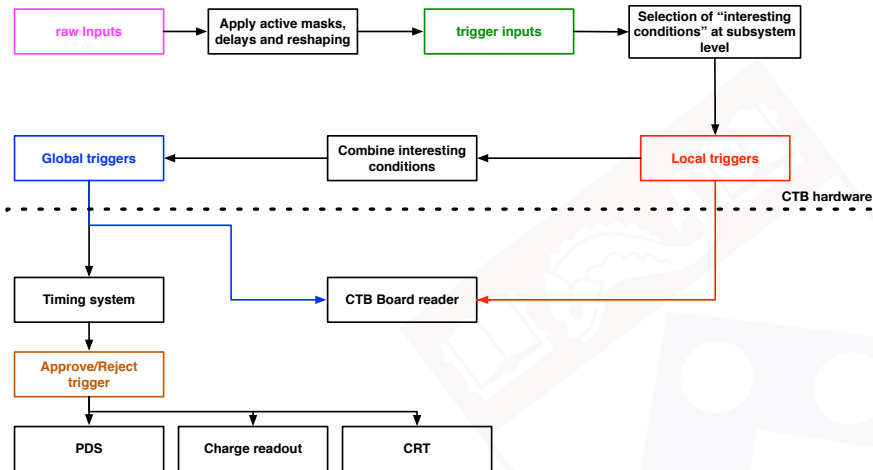
# Trigger inputs



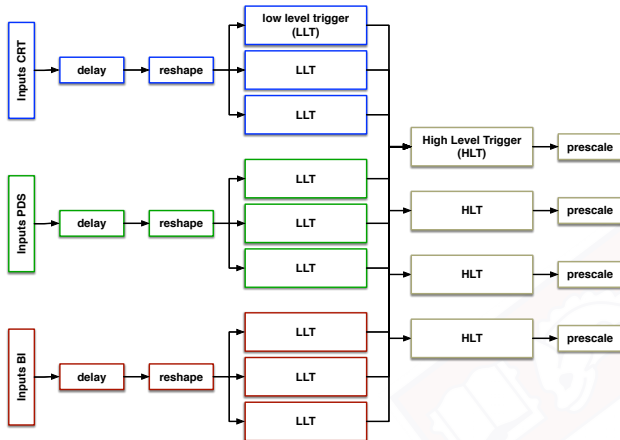
# CTB trigger design principles

- Use multi-layered trigger
  - Multiple LLTs (each dedicated to a single input subsystem)
  - Produce HLT (global triggers), by combining one or more LLT
- Each subsystem can have several LLTs
- The CTB can produce several types HLTs
- Only the HLTs are passed on to the timing system
- The timing system can **veto** any trigger from being propagated
  - For example, if another trigger was issued recently, if the charge readout is busy, etc
- Both LLTs and HLTs are recorded/reported to the board reader
  - So we can recover at least the history of everything the CTB "saw", even if a global trigger was not issued
  - **Everything that the CTB sends downstream is timestamped**
- Planning to also produce **random triggers**.
  - Zero bias. Trigger on noise, when there are no real triggers.
  - The very first trigger to be put in place (next week)

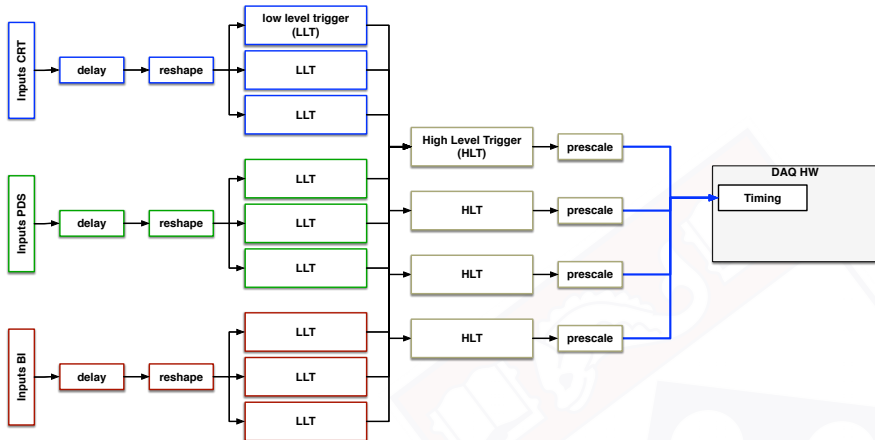
## How the CTB works



# How the CTB works (a more technical view)

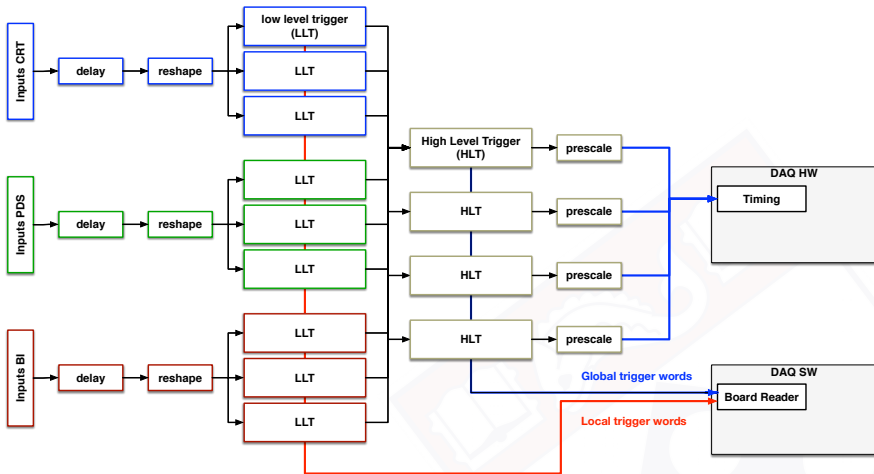


# How the CTB works (a more technical view)





# How the CTB works (a more technical view)



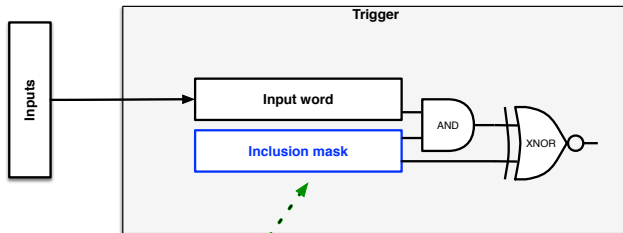
## How to build triggers?

- Possibilities are endless. Have to draw the line somewhere.
  - Current design allows for a lot of flexibility
  - Well defined use cases are still necessary
- Two generic types of triggers:
  - Mask Based** A bitmask indicates which inputs can contribute to a trigger
  - Count Based** Number of active inputs activate a trigger

- Each of these types represents a distinct firmware block.
- Can have multiple instances (both per subsystem and globally), and exact configuration is performed at run start.
- However, the number of each type of triggers must be defined beforehand for each subsystem
- Need input from the physics groups!!!
- CTB inputs are not "raw" inputs. In some cases they may have already built-in coincidences (eg. CRT)

- A bitmask indicates which inputs can contribute to a trigger
- At subsystem level (LLT), the bitmask represents the different subsystem inputs
- At high level (HLT), the bitmask represents the different LLTs
- Masks can be either **inclusive** (all masked inputs must match), or **simple** (any of masked bits enables a trigger)

## Mask based triggers (inclusive trigger)



All of masked channels must be on

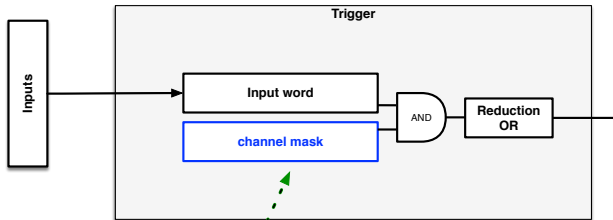
### Examples

**LLT/BI** Beam is on and Cherenkov detector X has a signal

**LLT/CRT** +X plane has signal **AND** -X plane has signal (horizontal, through going muon)

**HLT** BI is on, Cherenkov X is on, and through going muon on CRT  
(LLT BI 1 LLT CRT 1)

# Mask based triggers (simple trigger)



Any of the masked channels must be on

## Examples

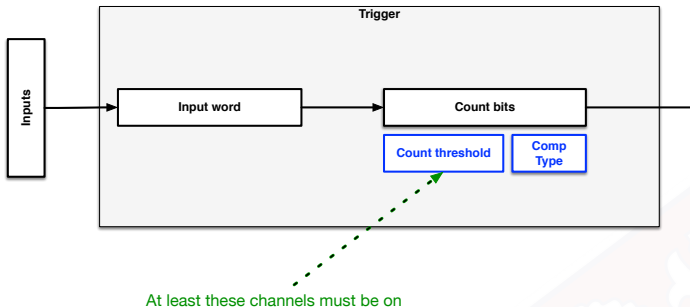
LLT/CRT Any CRT horizontal panel is on

LLT/PDS Any SSP is on

HLT Should be avoided its use as it is too broad and will likely cause large number of triggers

- This is the equivalent of saying "fire a trigger whether any of these conditions happen."

## Count based triggers (only for PDS)



- Only planned to be used on the PDS subsystem
- Expensive in terms of logic

### Examples

LLT/PDS At least/exactly/no more than N SSPs on

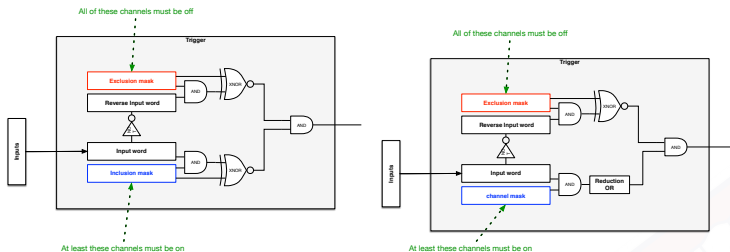
- These triggers are completely dependent on the configured LLTs for each subsystem
  - Use cases are more complex
- Triggers should consist mostly of mask based triggers
- **There is one hardcoded LLT in the HLT mask: beam ON/OFF**

## Examples

- Beam on and no more than 2 SSPs on
- Beam on, Cherenkov A on and at least 4 SSPs on
- Any vertical CRT and any number of SSPs on

While drafting this, one extra use case was found...

# Excluding triggers (only for HLTs)



All of requested asserted LLTs were ON, and **ALL** the requested deasserted LLTs were OFF

## Examples

- All top CRTs and any PDS **but no beam**
  - Note that this implies the following LLTs
    - LLT on CRT selecting all top CRTs
    - LLT on PDS selecting any PDS
    - LLT on BI selecting **at least** the beam gate
- To be used sparingly! Clear requirements needed.



## Examples of Low Level Triggers

- Beam ON and BI detectors 1,3 and 5
- Any of beam detectors A, B, C and D
- At least N PDs
- Exactly N PDs
- Planes A and B of CRT
- Any horizontal/vertical panel of CRT

## Important!!!

Low level triggers are internal CTB constructs. They are **not** distributed to the other systems.

- But they can be if an appropriate HLT mask is defined (commissioning use case)
- They are still recorded to artDAQ through the CTB data stream (regardless of global trigger)

## Examples of High Level Triggers

- Through going muon on horizontal CRT planes and PDS but NO beam

LLT1 Beam ON (built-in)

LLT2 At least 1 PDS

LLT3 Any CRTs on one side of the cryostat

LLT4 Any CRTs on other side of the cryostat

HLT Mask in : LLT2-4, Exclude LLT1

- Beam event

LLT1 Beam ON

LLT2 At least 1 PDS

HLT Mask in : LLT1 and 2

By using exclusion of triggers, we can negate any of the LLTs

**Important!!!**

High Level Triggers can be prescaled.

## Examples of what not to do

- $x$  CRTs and  $y$  SSPs
  - Counting triggers not planned for the CRT
- A CRT and a SSP **OR**  $X$  CRTs and BI
  - Logic including both AND and OR in HTLs
  - Doing this using both LLTs and HLTs is possible
- Beam on,  $x$  SSPs  $n$  ns later and  $y$  SSPs  $m$  ns after that
  - Delays are applied at channel level (and are common to all triggers)
- Build a HLT from prescaled LLTs
  - Hard to evaluate efficiencies. Prescales only possible on HLTs

This is also likely to be the order they will be put in place on the CTB

1. Zero/Minimal bias triggers (commissioning of board and board reader)
2. CRT triggers (to use for commissioning before beam). Ignore beam instrumentation.
  - Front-to-back triggers (through-going muons)
  - Vertical muons (are there CRTs on top of cryostat?)
  - Stopped muons (fire one side of cryostat and not the other)
  - Muons through the APA (fire both sides but selecting specific panels to have guaranteed APA crossing)
3. Beam (un)correlated triggers
  - Beam spill (simplest trigger)
  - Beam and selection BI detectors (looking for specific beam composition)
$$\begin{aligned}e^- & Chkv_1 \wedge Chkv_2 \\ \pi & \neg Chkv_1 \wedge Chkv_2 \\ K/p & \neg Chkv_1 \wedge \neg Chkv_2\end{aligned}$$
4. Triggers with PDS
  - Mostly to study the PDS system in combination with other systems

- The trigger is very flexible and allows to do almost anything
- Logic available is limited, so priorities have to be defined
- Plan is to put in as many triggers as requested, while logic is available
  - When we run out of logic, we'll need to start to prioritize
- CTB is in place and basic firmware is written
  - Planning to test some basic triggers next week (using controlled inputs)
  - Communication hurdles with timing system are now solved.
  - Focus on constructing triggers and commissioning
- Formal documentation detailing the trigger structure is being drafted

### Call for feedback

Decisions are being made. Time for changes is limited, so any extra requests are **urgent** (and not guaranteed to be feasible).

## Support Slides

