Display Component Specification

Abstract
This document provides the component specification for an LCD module for use as the main display in a consumer electronics product.

Revision 03

Last updated
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1. Revision History

Revision	Date	Author	RCO	Description
01	08/17/2016	XiaoPing Bai	014744	Release for HVT
02	2/14/2017	Patrick Qu	015437	Release for DVT Updated brightness spec to 420nits (typ), 350nits (min)
03	4/11/17	Patrick Qu	016975	Release for PVT Update ppi to 225

2. Light Level Document Description

This document specifies the performance and design requirements for a display module to be integrated into a mobile consumer electronics product by Amazon Lab126.

a. Audience and usage

- Display vendors: Document requirements for display product to be supplied to Amazon Lab126.
- Commodity manager: Provide a basis for identifying suitable components.
- Quality Management: Canonical reference to determine if components conform to Amazon Lab126 requirements.
- Hardware/Software Engineering: Reference for integration of display component.

b. Design Change Approval

This document describes a display performance and quality requirements for a tablet in Amazon. No element of the displays may change without the written permission from Amazon and an appropriate testing and qualification. Furthermore, any requests or discussion for changes to the displays must be signed off by the responsible lead display engineer and informed to display EPM, GCM, and OPM.

3. Normative Reference

Product Documents	05-011436	DWG,GEN,DISPLAY,SUEZ
Product Documents	05-010883	SPEC,INCOMING INSPECTION,DISPLAY,SUEZ
Product Documents	05-011437	DISPLAY COMPONENT SPECIFICATION,SUEZ

4. Introduction

This display is a color Active Matrix Liquid Crystal Display (AMLCD) of glass construction in normally black mode. The display consists of 1200 (x RGB Stripe) x 1920 pixels with 16,777,216 colors. The display interface is MIPI.

The display module is a 10.1" portrait vertical color LCD with 1200x1920 pixels with a 225 dpi pixel density. The peak brightness is 410nits typical (at the center of the LCM), and a color gamut of 72% NTSC typical. It is a conventional In-plane-Switching (IPS), normally black display with a viewing angle of 80^0 (without wide viewing compensation).

This AMLCD module uses amorphous Silicon (a-Si) Thin Film Transistor (TFT) as the active circuit elements, driving fringe field switching (FFS). The gate driver is integrated on the TFT glass. The source driver resides on the two driver IC that is mounted onto the LCD glass directly thru a Chip-On-Glass (COG) bonding process. The power IC is mounted onto PCB thru a Flexible-On-Glass (FOG) bonding process and a Flexible - On-PCB (FOB).

This active area is 10.1" inches in diagonal size at WUXGA resolution (1200 vertical (x RGB) x1920 horizontal). Each pixel is divided into three sub-pixels laid out as RGB or dots that are arranged in vertical stripes. Gray scale or the luminance of the sub-pixels is determined with an 8-bit gray scale with spatial dithering signal, thus presenting a palette of 24-bit.

This module consists of a LED backlight assembly, mechanical housings and support, TFT-LCD panel, and a PCB with minimal number of external components to minimize required component area. It will be assembled to a multi-point capacitive touch panel (CTP) with lamination.

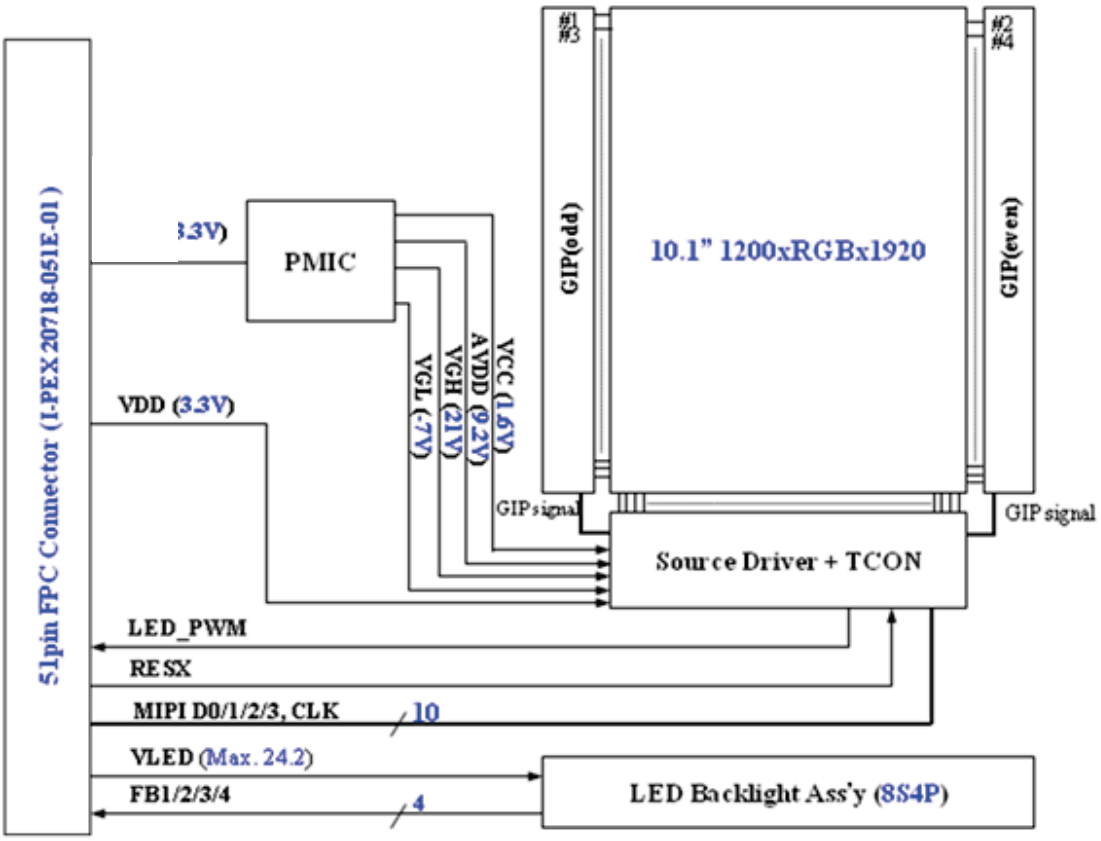
NT51021 driver IC supports MIPI high-speed serial interface for both display data and command/control interface. This driver IC supports streaming video mode only.

5. Physical Specifications

Items	Specifications
Display Technology	a-Si TFT, Transmissive
Panel Technology	1P2D
Pixel Resolution	1200 (x RGB) x 1920 WUXGA
Pixel Pitch (um)	112.80
Pixel Configuration	RGB
Color Depth (24 bit)	16,777,216 (16.7M)
Active Area (mm)	135.36(H)*216.576(V)
Glass Thickness (mm) (TFT/CF)	0.4 mm / 0.4 mm
Pixel Orientation/Drawing	Square
Module outline (mm)	143.0(H) x227.926(V)x 2.50mm(typical) 4.40 mm (maximum thickness, WPCBA);
Top Polarizer	Hard Coat
Bottom Polarizer	APF
Panel Interface	1 port 4 lane MIPI
Power Supply VDD3.3 (V)	3.3 V
LCD Power Consumption (mw)	500mW (Max) – White
Back Light LED Configuration	4P8S
Backlight Power Consumption	2.1 W Max
Driver IC	NT51021
Operating Temp	0°C to +60°C
Storage Temp	- 20°C to +70°C
COG ledge protection	Tuffy or resin on COG ledge
Weight	145g Max (without liner)

6. Electrical Specifications

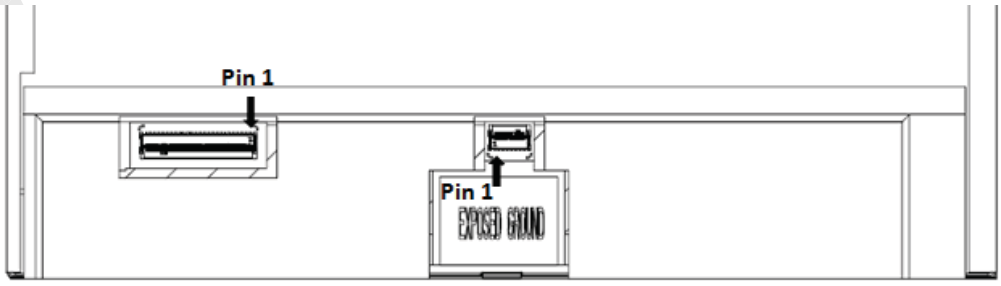
6.1 Block Diagram



6.2 Connector Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	27	GND	Ground
2	TP_INT	Interrupt pin for TP	28	CLK-	MIPI
3	TP_RST	Reset pin for TP	29	GND	Ground
4	TP_SCL	I2C Clock for TP	30	D2+	MIPI
5	TP_SDA	I2C Data for TP	31	GND	Ground
6	TP_1.8V	Typ 1.8V for TP	32	D2-	MIPI
7	GND	GND	33	GND	Ground
8	TP_3.3V	Typ 3.3V for TP	34	D3+	MIPI
9	GND	GND	35	GND	Ground
10	LCM_ID0	GND	36	D3-	MIPI
11	NC	No Connection	37	GND	Ground
12	NC	No connection	38	LED_PWM_OUT	PWM control for BL driver
13	VDD_3.3 V	3.3V input for driver IC	39	RST(GRB)	LCM Reset signal from system
14	VDD_3.3 V		40	LCM_SCL	I2C Clock for LCM
15	VDD_3.3 V		41	LCM_SDA	I2C Data for LCM
16	NC	No connection	42	NC	No Connection
17	GND	Ground	43	TP_SYNC	ESD recovery
18	D0+	MIPI	44	LCM_ID1	High
19	GND	Ground	45	LED1-	Cathode for light bar
20	D0-	MIPI	46	LED2-	Cathode for light bar
21	GND	Ground	47	LED3-	Cathode for light bar
22	D1+	MIPI	48	LED4-	Cathode for light bar
23	GND	Ground	49	NC	No connection
24	D1-	MIPI	50	LED+	Anode for light bar
25	GND	Ground	51	LED+	Anode for light bar
26	CLK+	MIPI			

FPCA Pin Orientation



6.3 Absolute Maximum Rating

Parameter	Symbol	Minimum	Max	Units
Supply Voltage	VDD3V3	-0.3	5.0	V
LED Forward current	$I_{LED\ (per\ LED)}$		20	mA

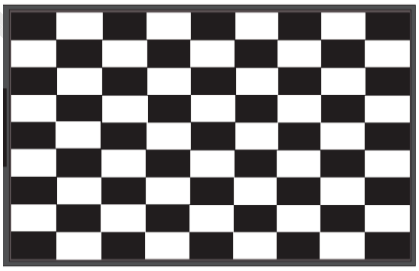
6.4 Display Modes for Power Measurement

Items	Min	Typical	Max	Conditions
Panel Normal Mode (mW)			500	$T_{ambient}$= 25°C (White Pattern);Vdd=3.3V
Standby Mode(mW)		200		$T_{ambient}$= 25°C
Backlight LED (W)			2.1	$T_{ambient}$= 25°C, 20mA per chain.

Standby Mode and Normal Mode Pattern are defined as below

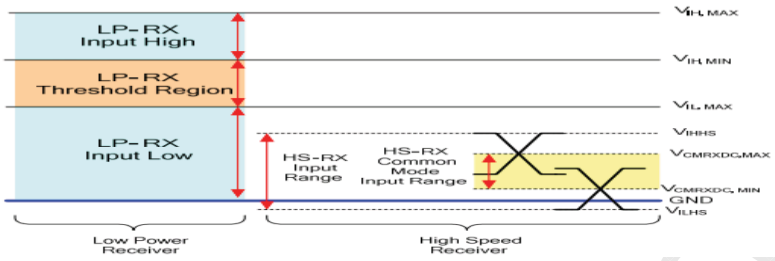
-Standby mode (All black pattern) -Normal mode (9x9 mosaic pattern)

6.5 DC Characteristics over Operating Voltage and Temperature Range



Item		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Voltage		VDD_IO	3.0	3.3	3.6	V	
Ripple Voltage		VRP	-	-	300	mV	
Inrush Current		IRUSH	-	-	1.5	A	
LEDPWMOUT	High Level	VOH	0.7*VDD	-	VDD	V	
	Low Level	VOL	0		0.3*VDD	V	
BLU Power Consumption		P_{BLU}		1920	2100	mW	
VDD Current in Normal Mode		I_{VDD}			150	mA	
Frame frequency		fFrame		60		HZ	

6.6 MIPI Characteristics

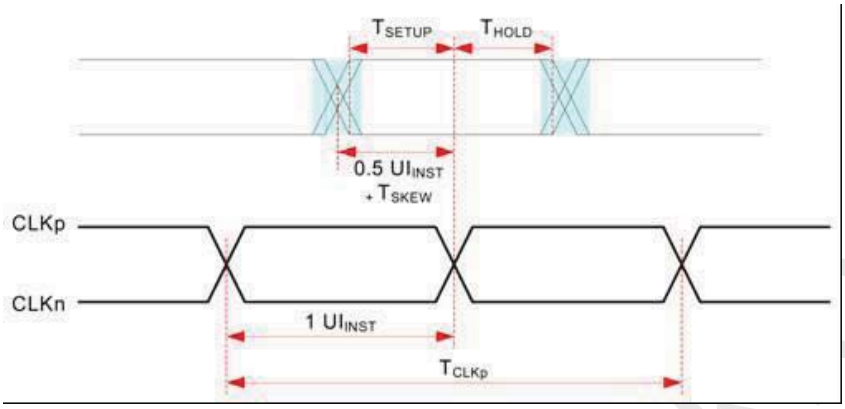


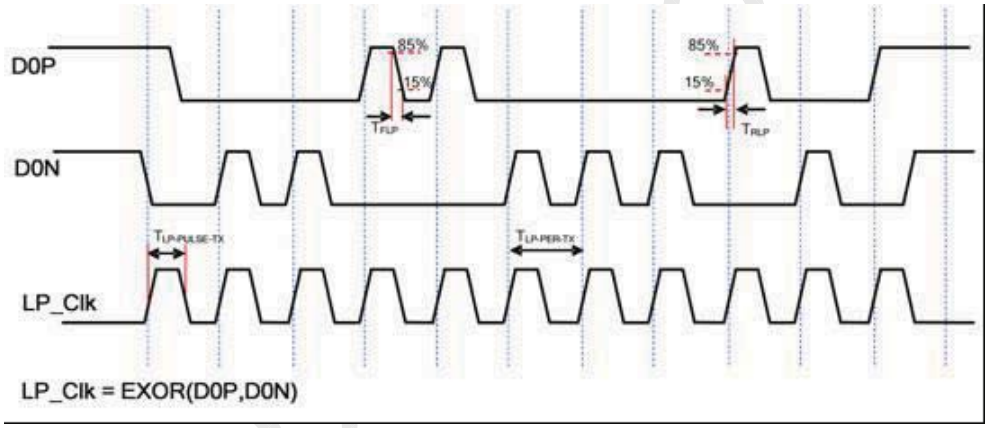
Parameter	Symbol	Min	Typ	Max	Unit	Condition
MIPI digital operation current	IVCCIF	-	-	24	mA	-
MIPI digital stand-by current	IVCCIFST	-	200	-	uA	-
MIPI Characteristics for High Speed Receiver						

6.6.1 DC Characteristics

Single-ended input low voltage	VILHS	-40	-	-		
Single-ended input high voltage	VIHHS	-	-	460	mV	
Common-mode voltage	VCMRXDC	155	-	330	mV	
Differential input impedance	ZID	80	100	125	Ω	
HS transmit differential voltage(VOD=VDP-VDN)	|VOD|	85	200	250	mV	
MIPI Characteristics for Low Power Receiver						
Pad signal voltage range	VI	-50	-	1350	mV	
Ground shift	VGNDSH	-50	-	50	mV	
Output low level	VOL	-150	-	150	mV	
Output high level	VOH	1.1	1.2	1.3	V	

6.6.2 AC/Timing Characteristics over Operating voltage and Temperature Range:





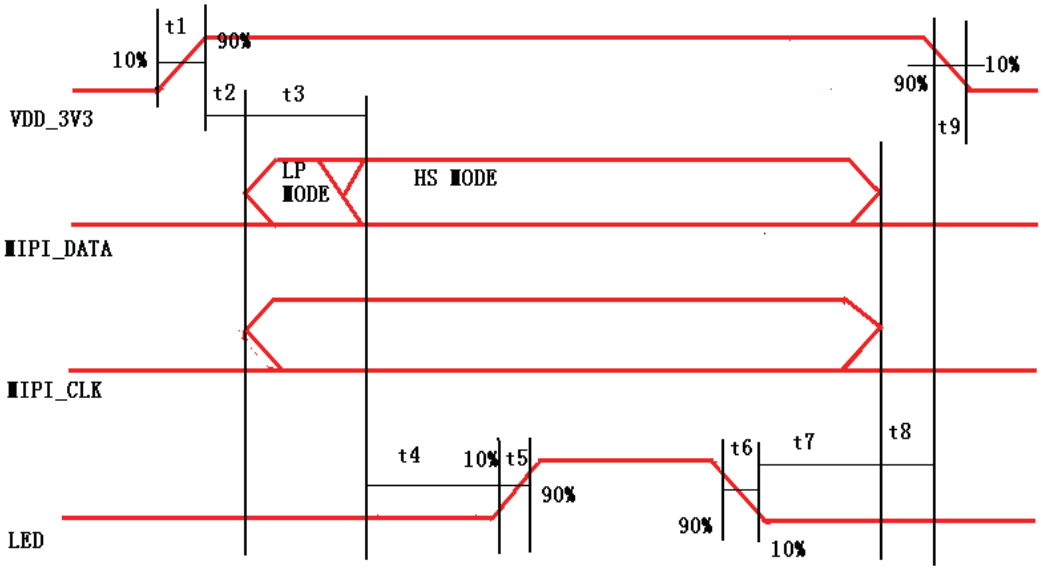
MIPI AC Characteristic

Number	Characteristics	Symbol	Min	Typ	Max	Units
6.4.1	DSI CLK Frequency (HS)	F_{CLKP_HS}	125		250	MHz
6.4.2	DSI CLK Cycle Time (HS)	T_{CLKP_HS}	4		8	ns
6.4.3	DSI Data Transfer Rate (HS)	U_{IINST}	40		500	Mbps
6.4.4	DSI CLK Frequency (LP)	$F_{LP\text{-}PER\text{-}TX}$			10	MHz
6.4.5	DSI CLK Cycle Time (LP)	$T_{LP\text{-}PER\text{-}TX}$	100			ns
6.4.6	DSI Data Transfer Rate (LP)	$T_{LP\text{-}PULSE\text{-}TX}$			10	Mbps
6.4.7	DSI Data to DSI CLK Setup Time	T_{SETUP}	0.15			UI
6.4.8	DSI Data to DSI CLK Hold Time	T_{HOLD}	0.15			UI
6.4.9	LP timing period(client to host)	T_{LPX}	50		75	ns
6.410	Allowable LP timing (host to client)	T_{LPX}	50		75	ns

6.6.3 MIPI timing

ITEM			SYNBOL	min	typ	max	UNIT
LCD	Frame Rate		-	-	60	-	Hz
	Pixels Rate		-	156.8	156.8	159.9	MHz
Timing	MipiCLK	Frequency	fCLK	490	490	498	MHz
		Period	Tclk	2.01	2.04	2.04	ns
	Horizontal	Horizontal total time	tHP	1343	1343	1366	tCLK
		Horizontal Active time	tHadr		1200		tCLK
		Horizontal Pulse Width	tHsync	1	1	1	tCLK
		Horizontal Back Porch	tHBP	32	32	32	tCLK
		Horizontal Front Porch	tHFP	110	110	133	tCLK
	Vertical	Vertical total time	tvp	1946	1946	1951	tH
		Vertical Active time	tVadr		1920		tH
		Vertical Pulse Width	tVsync	1	1	1	tH
		Vertical Back Porch	tVBP	14	14	14	tH
		Vertical Front Porch	tVFP	11	11	16	tH
Bit Rate			TX SPD (MBPS)	980	980	995	Mbps
Lane				-	4	-	Lane

6.7 Power-on/off Sequence & Timing



Parameter	Value				Remark
	Min.	Typ.	Max.	Unit	
t1	0.1	-	20	ms	
t2	1	-	20	ms	
t3	20	-	40	ms	
t4	200	-	-	ms	
t5	0.1	-	20	ms	
t6	0.1		20	ms	
t7	200	-	-	ms	
t8	0	-	20	ms	
t9	0.1	-	20	ms	

6.8 Display Registers Support

Any use of undocumented registers and/or settings may compromise display performance temporarily, and may possibly cause permanent damage to the display module.
In order to read registers with more than two parameters you must first set Maximum Return Packet size (data type 37h).

Command Summary

Cmd/Register	Function	Read/Write	# of parameters
01h	Software Reset	W	0
10h	Sleep in	W	0
11h	Sleep out	W	0

(xxh) NOP: No Operation

MIPI Interface		d7	d6	d5	d4	d3	d2	d1	d0	Type
CMD	Parameter									

Equation to calculate Lane clock speed (@ 60 Hz data rate) in Hz, for N lines per packet

$$\frac{\frac{1280}{N}\times\left(\left(800\times 24+\left(7\times 8\right)\right)\times N\right)+32}{\left(0.0166667-BlankingTime\right)\times 4}$$

Address Parameter

Packet Transfer Size Calculations for Multiple Packet Transactions per Transmission, single transaction per frame

Item	Time(sec)	UI	Comment
1 frame @ 60 Hz	0.0166667		Frame Time 1/60
Blanking Time (VFP+VBP)	0.000805		Selected Blanking Time
Active time	0.016667 – 0.000805=0.015861		Frame Time – Blanking Time
Packing overhead		32+ N*56	4*8(Eotp) + N * (4 header + 2 checksum + 1 command)*8

6.9 Driver IC ID Bit Programming

ID0 = 0; ID1 = 1

6.10 Initialization Code

VDD_IO Power On
↓
2ms >T0 > 0ms
↓
VBAT_SYS Power On
↓
60ms＞T1&T2 > 30ms
↓
8F = A5
↓
83 = 00
↓
84 = 00
↓
8C = 8E
↓
CD = 6C
↓
C0 = 8B
↓
C8 = F0
↓
97 = 00
↓
8B = 10
↓
A9 = 20
↓
FA = 12
↓
FD = 1B
↓
83 = AA
↓
84 = 11
↓

A9 = 4B
↓
85 = 04
↓
86 = 08
↓
9C = 10
C0=01
C1=05
C2=18
C3=29
C4=35
C5=3E
C6=4B
C7=56
C8=5B
C9=CC
CA=D7
CB=EF
CC=F9
CD=00
CE=F7
CF=F9
D0=FF
D1=12
D2=27
D3=4C
D4=56
D5=BA
D6=BE
D7=C9
D8=CF
D9=DA
DA=E5
DB=F4
DC=FD
DD=FF
DE=10
DF=2F

E0=1B
E1=1F
E2=32
E3=43
E4=4F
E5=58
E6=63
E7=6A
E8=77
E9=EA
EA=E7
EB=FB
EC=03
ED=F8
EE=F7
EF=F9
F0=F7
F1=02
F2=17
F3=34
F4=3E
F5=A2
F6=A2
F7=AD
F8=B9
F9=C2
FA=CB
FB=DA
FC=E3
FD=FF
FE=08
FF=2F
83=BB
84=22
C0=01
C1=05
C2=18
C3=29
C4=35

C5=3E
C6=4B
C7=56
C8=5B
C9=CC
CA=D7
CB=EF
CC=F9
CD=00
CE=F7
CF=F9
D0=FF
D1=12
D2=27
D3=4C
D4=56
D5=BA
D6=BE
D7=C9
D8=CF
D9=DA
DA=E5
DB=F4
DC=FD
DD=FF
DE=10
DF=2F
E0=1B
E1=1F
E2=32
E3=43
E4=4F
E5=58
E6=63
E7=6A
E8=77
E9=EA
EA=E7
EB=FB

EC=03
ED=F8
EE=F7
EF=F9
F0=F7
F1=02
F2=17
F3=34
F4=3E
F5=A2
F6=A2
F7=AD
F8=B9
F9=C2
FA=CB
FB=DA
FC=E3
FD=FF
FE=08
FF=2F
83=CC
84=33
C0=01
C1=05
C2=18
C3=29
C4=35
C5=3E
C6=4B
C7=56
C8=5B
C9=CC
CA=D7
CB=EF
CC=F9
CD=00
CE=F7
CF=F9
D0=FF

D1=12
D2=27
D3=4C
D4=56
D5=BA
D6=BE
D7=C9
D8=CF
D9=DA
DA=E5
DB=F4
DC=FD
DD=FF
DE=10
DF=2F
E0=1B
E1=1F
E2=32
E3=43
E4=4F
E5=58
E6=63
E7=6A
E8=77
E9=EA
EA=E7
EB=FB
EC=03
ED=F8
EE=F7
EF=F9
F0=F7
F1=02
F2=17
F3=34
F4=3E
F5=A2
F6=A2
F7=AD

F8=B9
F9=C2
FA=CB
FB=DA
FC=E3
FD=FF
FE=08
FF=2F
11H
↓
8F = 00
↓
Display On

6.11 Scan Direction

6.11.1 Normal Mode

Default programming, does not require programmingfor register 0x90h = 0xFF

6.11.2 Inverted Mode

Inverted operation programming for register 0x90h = 0xFC, required to be set during initialization

6.12 Design for RF and Regulatory Compatibility

This LCD module will be integrated into a product that will have wireless communication capability. It will be one of the major non-shielded noise emitting electrical components in the entire product and will be in close proximity to a variety of antennas of various wireless devices. The display module must be designed to minimize RF emission from its power supply and TFT driving circuits and layout.

All the power supplies must be decoupled properly and signals should be terminated properly. Proper shielding will be required whenever appropriate by low impedance FPC ground layer and/or external metallic shielding. All metallic parts and housing of the module must be grounded via low impedance paths, preferably metal-to-metal contact.

There is no specific pass/fail target on the component level, but the LCD module must satisfy system level performance and regulatory criteria.

6.13 ESD Testing

Follow the Display Component Spec for ESD Test, **05-009460**.

6.14 Black Light LED Driver Setting

TBD

7 Optical Specifications

7.1 General Optical Specifications

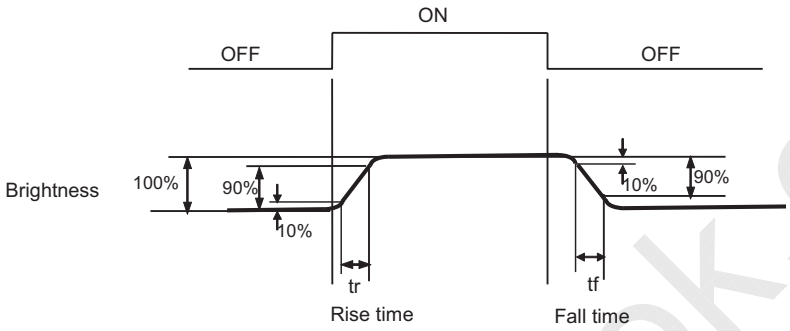
All optical tests are to be performed in compliance to the IDMS V1.03 (Information Display Measurement Standard) released on June 1,2012, as found at http://www.icdm-sid.org/downloads/idms1.html unless specified.

	Item	Specification	Remarks	Test Procedure in IDMS v1.03
1.1	Luminance at center of screen	350 nits min, 410 nits typical	This is assuming LED current of 20mA.	5.3
1.2	White Chromaticity	0.3127+/-0.03, 0.3290+/-0.03	CIE x,y.	5.3
1.3	Color Gamut	Min 65%,Typ 72% NTSC	CIE x,y. (Actual color points and gamut to be measured & reported per IDMS test 5.14).	5.18.1
1.4	Red Chromaticity	(0.643+/-0.03, 0.337+/-0.03)	CIE x,y.	5.4
1.5	Green Chromaticity	(0.303+/-0.03, 0.605+/-0.03)	CIE x,y.	5.4
1.6	Blue Chromaticity	(0.150+/-0.03, 0.057+/-0.03)	CIE x,y.	5.4
1.7	Contrast Ratio	700:1 Min	According to the actual measurement	5.10
1.8	Luminance Uniformity 13 points	70% minimum	On Full-screen white	8.1 (Add additional 4 points at H/3, W/3 from each corner)
1.9	Color Uniformity 13 points	Duv≤0.03	On Full-screen white	8.1(Add additional 4 points at H/3, W/3 from each corner)
1.10	Gamma Curve	2.2+/-0.3	R, G, B and gray scale gamma must meet spec	6.2, 6.3
1.11	Cell Transmittance	4.6% MIN , 5.1% TYP		10.4
1.12	Burn-in	± 1 L*	Follow OE spec method below	

All optical measurements will be taken after the display has been subjected to the electrical specifications. Additional optical measurements as specified by test methods and specifications below needs to be followed & reported at all times:

7.2 Optical Switching Time

Temp	Symbol	Typ	Max	Unit
0º C	Response Time (B/W) (tr + tf)	60	80	ms
+25º C	Response Time (B/W) (tr + tf)	30	35	ms



Gray to gray response time is measured from one gray level to the next 64 levels higher or lower. It is expected that RT_GG will not be significantly worse than black-white response time for this module and that RT_GG will meet the response time specified in this section. Worst case RT_GG must be reported and the overall result should be reported as below.

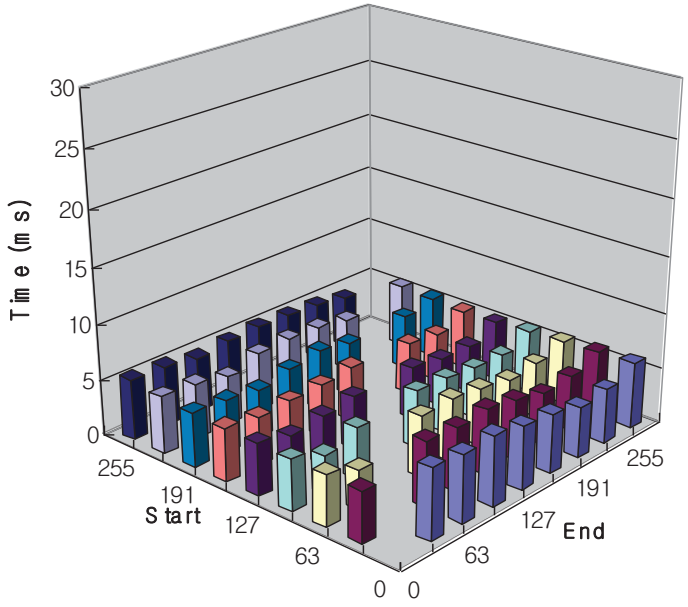


Figure 7.2 Grey-to-Grey response time spec limit

7.3 Optical Properties of the Display

7.3.1 Measurements of Transmissive Optical Properties

The transmissive properties of the display shall be measured using the specific auxiliary lighting that is designed for the display module, unless otherwise stated. The measurement shall be done at detector placed at θ=0°, φ=90°. The auxiliary lighting shall be driven according to IDMS1 (Information Display Measurement Standard) released on June 1,2012 and there shall be no ambient light present.

7.3.2 Brightness Uniformity

13 spots will be tested for the brightness uniformity as described above. The uniformity is calculated as the ratio of the minimum to maximum luminance. The uniformity shall meet the spec as follows.

Display White Uniformity at 25°C		
Minimum	Typical	Maximum
70%	80%	-

The display should have even illumination with no auxiliary lighting “hot spots”. There should not be any visible hotspots, light streaking, Moiré patterns, Newton Rings, mura, and other visible artifacts.

7.3.3 Transmittance of Display Driven White at Room Temperature

The driven white transmittance is defined as the percentage of the auxiliary light passing through the display when all its pixels are driven white. It shall be measured using the standard backlight. The transmittance The transmittance (including the APCF effect) of the display with all pixels driven white shall meet the spec as follows.

Minimum	Typical	Maximum
4.6%	5.1%	-

7.3.4Transmissive Contrast Ratio as a function of Temperature

The transmissive contrast of the display is defined as photometric luminance of display with all pixels driven white divided by the photometric luminance of display with all pixels driven black when the auxiliary lighting on.

$$CR = L_{white}/L_{black}$$

Temperature	Contrast Ratio	
	Min	Typical
0°C	600:1	800:1
25C°	700:1	900:1
50°C	600:1	800:1

7.3.5ISO-contrast Ratio at Room Temperature

It should be measured at 25° C with the lighting on with the observer (detector) at all φ from 0° and 360° and θ up to 80°. The contrast ratio must meet the following conditions:

Contrast ratio	Min Theta	Typical Theta	Phi
10:1	40	80	0°, 90°, 180°, 270°
10:1	30	70	45°, 135°, 225°, 315°

7.3.6Time to Half Luminance

The minimum time to half luminance for the LED back-lighting is 30,000 hours at 25°C.

7.3.7Crosstalk

The appearance of 50% gray pixels that are interfered by the neighbor black pixels shall not be appreciably different from those 50% gray pixels without interfering with the black pixels. Luminance for cross-talk calculation shall be measured in the central area of the display using the test patterns defined below. Crosstalk is defined as follows.

$$\text{Vertical Crosstalk} = \frac{\text{Luminance at REF - Luminance at VINF}}{\text{Luminance at REF}} \times 100\%$$

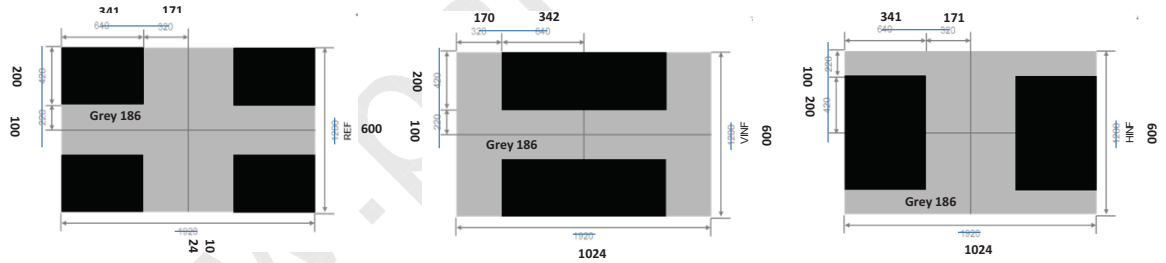


Figure 7.3.1 X-talk Test Pattern for WUXGA

Both Horizontal and Vertical Cross-talk shall meet the following specificaiton.

Cross Talk @ 25°C		
Minimum	Typical	Maximum
-	-	2.5%

Note that crosstalk should not exceed º for any cases.

7.3.8 Flicker

The flicker level shall be measured using photodiode or PMT in a range from 5Hz to 80Hz after panel **VCOM** tuning. The peak flicker level must be measured **less than-30dB**at the center of the screen.

Flicker(dB)		
Minimum	Typical	Maximum
-	-	-30

7.4 Backlight profile

The FWHM (Full Width Half Maximum) of the angular distribution of the backlight should meet the following requirement.

Temperature 25° C	Horizontal			Vertical		
	Min	Typical	Max	Min	Typical	Max
FWHM	65°	90°	-	65°	90°	-

7.5 Burn In (Image Retention)

Image retention is also called Burn-in, Ghosting, or Image sticking. It is a phenomenon seen on a display that the previous image, after long period of time being static displayed on the screen, can be still seen when the display is refreshed to next image. Image retention above certain level is consider an optical defect on Amazon's products. Display vendors shall design and manufacture the displays for Amazon to meet image retention spec as follows.
Measurements must be made in a dark environment (less than 0.01 lux) and the display is driven at typical brightness .Turn off any image enhancement features and automatic backlight dimming and controls. Exposure time of the test instrument needs to be adjusted appropriately to ensure fast & accurate low luminance measurements. Measurement procedure is defined in the diagram below. Measure and record the time and luminance on the last Grey 32 test image every 5 seconds for 5 minutes.

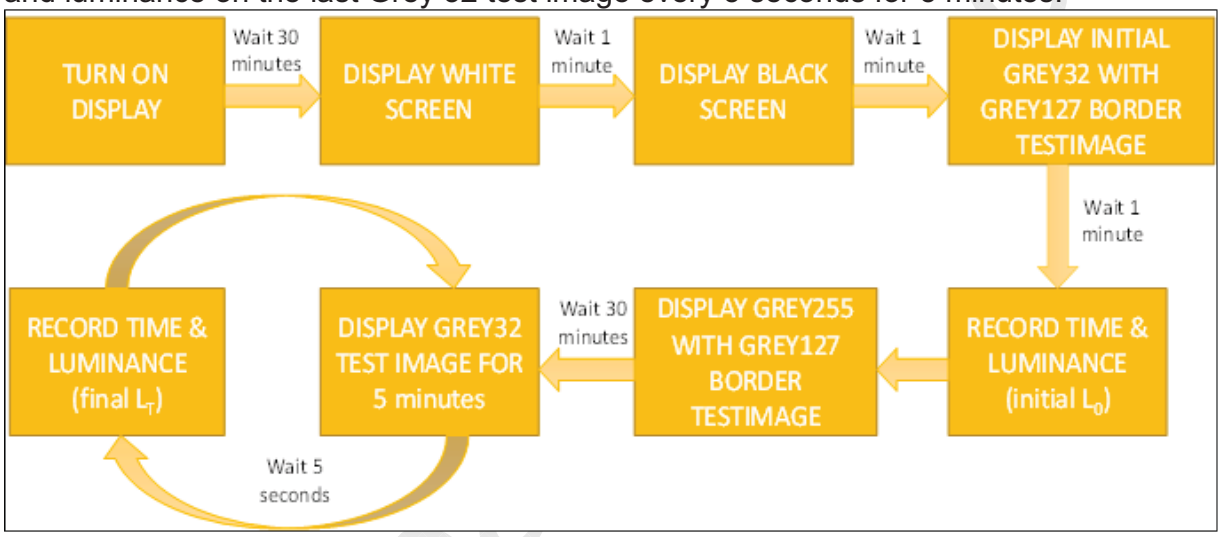
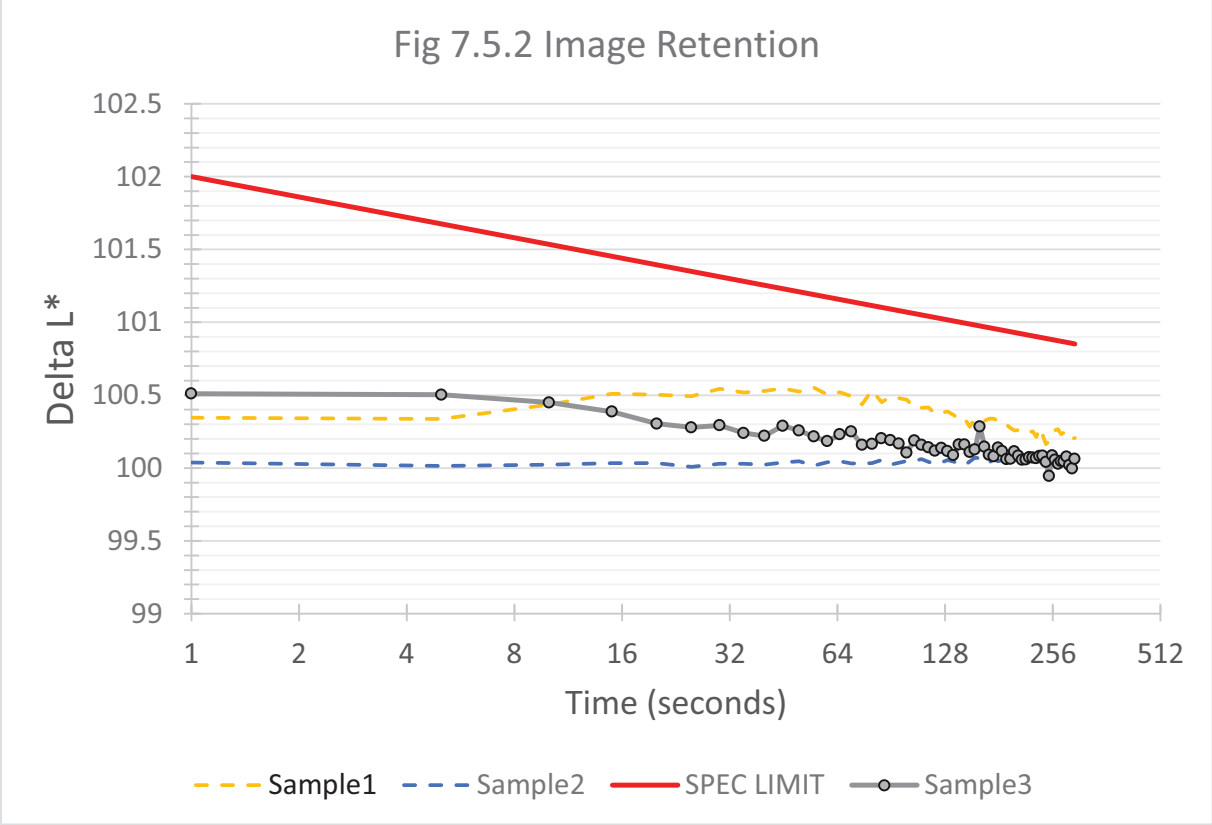


Figure 7.5.1 Image Retention Test Method

L* value is calculated for each Grey32 Measurements (relative to Initial Grey32 measurements) from the raw data reported by the vendor. Follow the formula below to calculate ΔL* at each time point and plot it out per Fig 7.5.2.



$$L^* = 116 * \left({}^{Y}/_{Yn}\right)^{\frac{1}{3}}$$

Where, Yn = Luminance of Initial Grey32 Image at t = 0 min
Y = Luminance of Initial Grey32 Image at t = 5 min.

$$\Delta L^* = L^*_T - L^*_0$$

Follow the “Image Retention” worksheet in the OE Workbook to report the measurement data and result. ΔL* or slope of ΔL* v/s Log (time) must be lower than the threshold limit shown in Fig 7.5.3below.

The measured L* for grey 32 after 30 minutes of burn-in must not exceed or change more than 1 L* value from its initial value. The final grey 32 value must be less than 0.05 L* value of its initial measurement after 5 minutes.

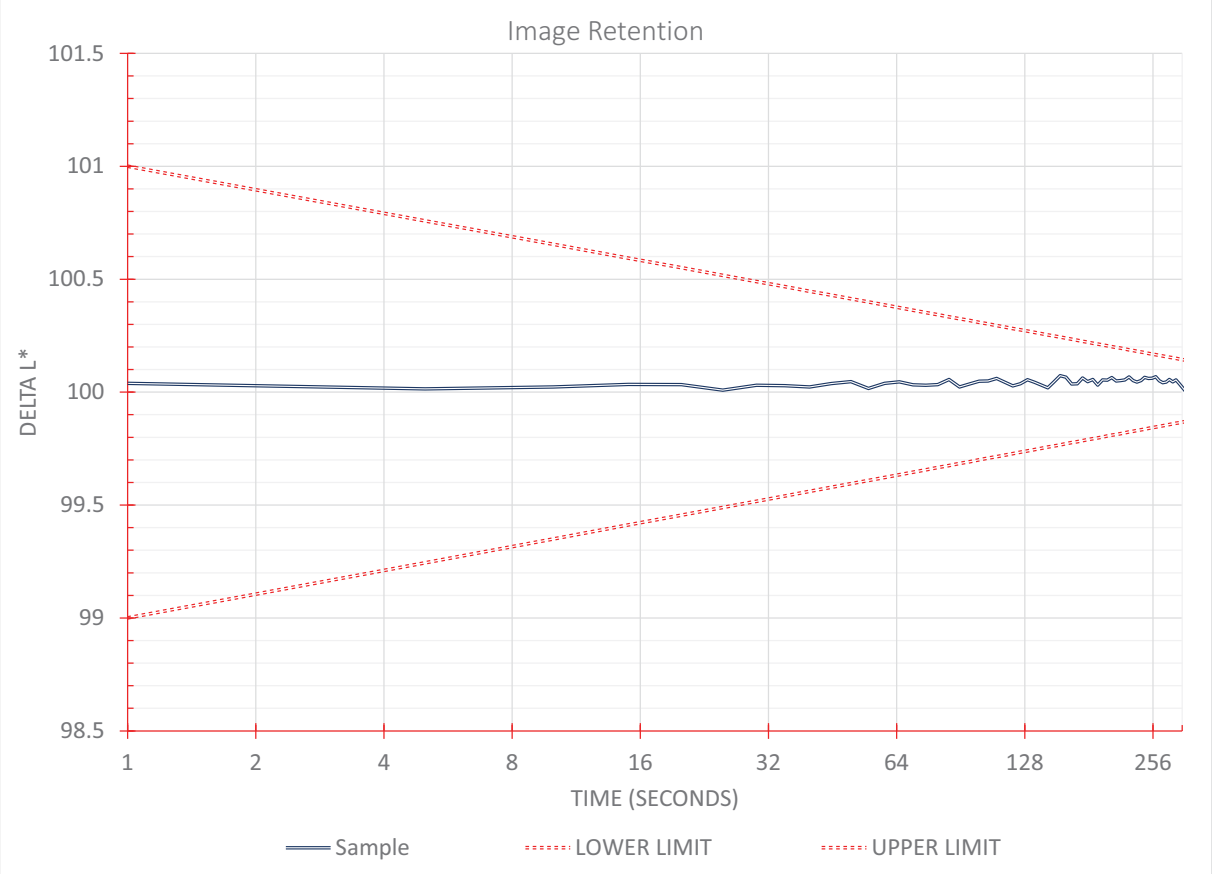


Figure 7.5.3 Spec limit for Image Retention Performance after 30 min test

8. Mechanical Requirements

6.1 Pixel Count of the Display

1200(24bit) x 1920

6.2 Pixel Pitch and Maximum Gap in between Pixels

0.1128mm pixel pitch

6.3 CD Mechanical Layout and Dimensions

LCD mechanical layout and dimensions are defined in Amazon MCO Sub-assembly TP-LCM module05-0080xx. Critical dimensions are marked **[FAI]** in the above drawing print. Refer the drawing for detailed information.

6.4 COG ITO Runner Encapsulation Requirements:

On modules in which COG (Chip on Glass) technology is used, the exposed ITO runners must be completely encapsulated. A neutral curing electronic grade silicone RTV should be used. The material must be tested for ion content to verify the material itself is not a source of contamination. The supplier will provide a certified chemical analysis of the ion content of the encapsulate material.

9. Visual Inspection &Defects

Refer to document "*Incoming Inspection Standard for Suez Display Component*" 05-010883