INNOLUX 群創光電

PRODUCT SPECIFICATION

Doc. Number:

□ Tentative Specification
■ Preliminary Specification
□ Approval Specification

MODEL NO.: P101KDA
SUFFIX: AB0

Customer: Amazon

APPROVED BY **SIGNATURE**

Name / Title
Note :

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

INNOLUX 群創光電

PRODUCT SPECIFICATION

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
0.0	2017/12/08	All	Spec Ver.0.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

P101KDA-AB0 is a 10.1" (10.1" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 51 pins MIPI interface. This module supports 1200 x 1920 WUXGA mode.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	10.1" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1200 x R.G.B. x 1920	pixel	-
Pixel Pitch	0.1128 (H) x 0.1128 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216 (8bit color depth)	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating (3H), Glare	-	-
Luminance, White	440	Cd/m2	Typ.
Power Consumption	2.556 W (Max.) (Panel 0.5 W @ White (Max.), BLU 2.056W (Max.))		(1)

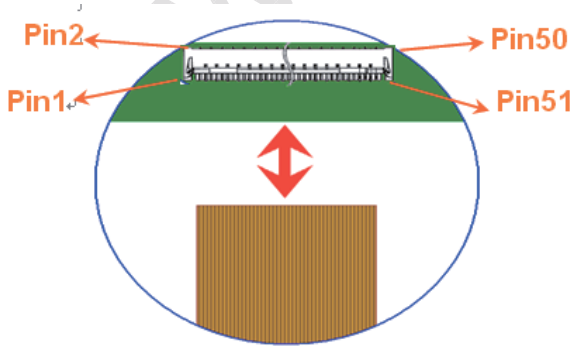
Note (1) The specified power consumption (without LED converter efficiency) is under the conditions at VDDI = 3.3 V, fv = 60 Hz, Brightness = 440 nits, I_{F_LED} = 21 mA and Ta = 25 ± 2 ºC, whereas white pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	227.63	227.93	228.23	mm	(1)
	Vertical (V)	142.7	143	143.3	mm	
	Thickness (T)	2.3 (w/o PCBA)	2.5 (w/o PCBA)	2.7 (w/o PCBA) 4.4 (w/ PCBA)	mm	
Active Area	Horizontal		216.576		mm	
	Vertical		135.36		mm	
Weight	-	-		144	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer to Appendix Outline Drawing for detail design.

Connector Part No.: **I-PEX 20718-051E-01**

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+70	ºC	(1)
Operating Ambient Temperature	T_{OP}	-10	+60	ºC	(1), (2)

Note (1) (a) 90 %RH Max.

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) The temperature of panel surface should be -10 ºC min. and 60 ºC max.

3.2 ELECTRICAL ABSOLUTE RATINGS

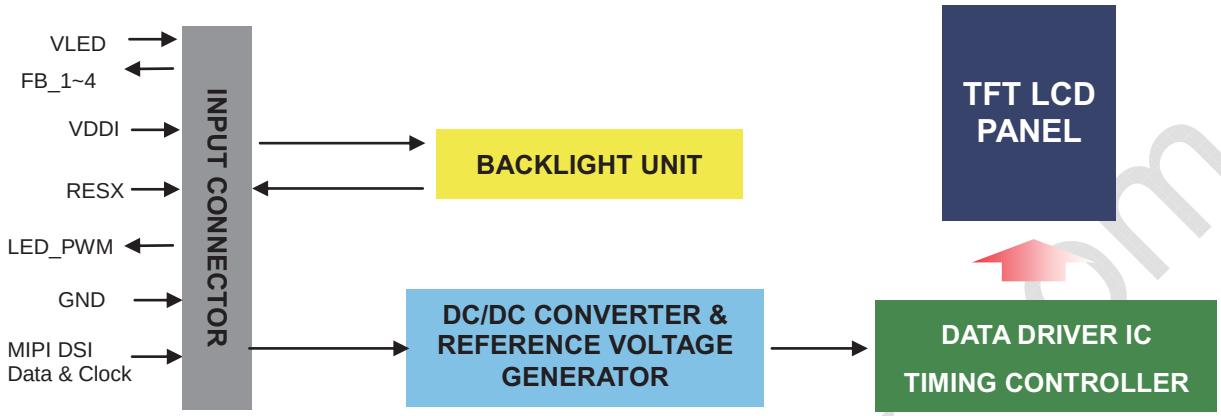
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VDDI	3.0	3.6	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2 INTERFACE CONNECTIONS

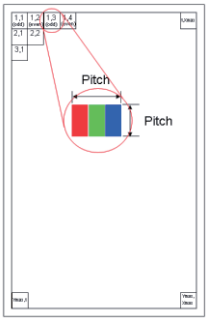
PIN ASSIGNMENT

Pin No.	Symbol	I/O	Description	Remark
1	GND	P	Ground	
2	TP_INT	-	NC	
3	TP_RST	-	NC	
4	TP_SCL	-	NC	
5	TP_SDA	-	NC	
6	TP_1.8V	-	NC	
7	GND	P	Ground	
8	TP_3.3V	-	NC	
9	GND	P	Ground	
10	GND	P	Ground	
11	NC	P	INX use for MTP, no connection for system	
12	NC	-	No connection,	
13	VDD_3.3 V	P	3.3 V input	3.0 ~3.6 V
14	VDD_3.3 V	P	3.3 V input	3.0 ~3.6 V
15	VDD_3.3 V	P	3.3 V input	3.0 ~3.6 V
16	NC	-	No connection,	
17	GND	P	Ground	
18	D0+	I	MIPI differential data0 input (Positive)	
19	GND	P	Ground	
20	D0-	I	MIPI differential data0 input (Negative)	
21	GND	P	Ground	
22	D1+	I	MIPI differential data1 input (Positive)	

23	GND	P	Ground	
24	D1-	I	MIPI differential data1 input (Negative)	
25	GND	P	Ground	
26	CLK+	I	MIPI differential clock input (Positive)	
27	GND	P	Ground	
28	CLK-	I	MIPI differential clock input (Negative)	
29	GND	P	Ground	
30	D2+	I	MIPI differential data2 input (Positive)	
31	GND	P	Ground	
32	D2-	I	MIPI differential data2 input (Negative)	
33	GND	P	Ground	
34	D3+	I	MIPI differential data3 input (Positive)	
35	GND	P	Ground	
36	D3-	I	MIPI differential data3 input (Negative)	
37	GND	P	Ground	
38	LED_PWM_OUT	O	PWM control signal for LED driver	
39	RST(GRB)	I	Device reset signal	
40	SCL	I	I2C signal	
41	SDA	I	I2C signal	
42	NC	I	INX use for WPN, no connection for system	
43	TP_SYNC	O		
44	ID1(GND)		ID	
45	LED1-	O	Cathode for light bar	
46	LED2-	O	Cathode for light bar	
47	LED3-	O	Cathode for light bar	
48	LED4-	O	Cathode for light bar	
49	NC	-	No connection,	
50	LED+	P	Anode for light bar	
51	LED+	P	Anode for light bar	

Note (1) The first pixel is odd as shown in the following figure.

Note (2) Normal operation/BIST pattern selection. (Control by MIPI LP Command)



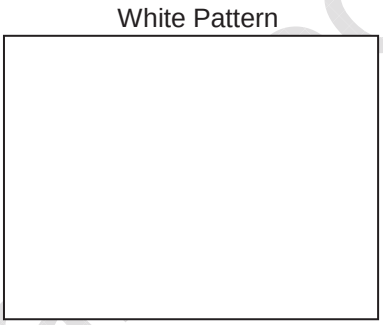
4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELECTRICAL SPECIFICATION

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Power Supply Voltage		VDDI	3.0	3.3	3.6	V	
Logic High Level Input Voltage		V_{IH1}	0.7xVDD		VDD	V	For I/O circuit
Logic Low Level Input Voltage		V_{IL1}	0		0.3xVDD	V	
Power Supply Current	White	I_{VDDI}		0.15		A	Note (2)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) The specified power supply current is under the conditions at VDDI = 3.3 V ,Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power-dissipation check pattern is displayed below.



4.3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Forward Current	I_B		21		mA	Note (1)
Forward Current Voltage	V_f		2.96	3.06	V	
Power Consumption	P_{BL}	-	1.988	2.056	mW	Note (2)

Note (1) 8 LEDs are connected in series; each LED forward current is 21mA.

Note (2) I_B=21mA, $P_{BL} = I_{B\ x\ LED\ Q'ty} \times V_{BL}$, V_{BL} is backlight forward voltage.

4.4 MIPI DSI INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1. MIPI Interface DC characteristic

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
MIPI digital operation current	I_{VCCIF}	VCC=VCC_IF=1.5V, Data Rate=500Mbps,	-	-	24	mA
MIPI digital stand-by current	$I_{VCCIFST}$	VCC_IF input current. All input signal are stopped.	-	200	-	uA
MIPI Characteristics for High Speed Receiver						
Single-endedl input low voltage	V_{ILHS}		-40	-	-	mV
Single-endedl input high voltage	V_{IHHS}		-	-	460	mV
Common-mode voltage	V_{CMRXDC}		155	-	330	mV
Differential input impedance	Z_{ID}		80	100	125	ohm
Differential input high threshold	V_{IDTH}			-	70	mV
Differential input low threshold	V_{IDTL}		70	-	-	mV
MIPI Characteristics for Low Power Mode						
Pad signal voltage range	V_I		-50	-	1350	mV
Ground shift	V_{GNDSH}		-50	-	50	mV
Input low level	VIL		-150		150	mV
Input high level	VIH		1.1	1.2	1.3	V

Note 1) VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C

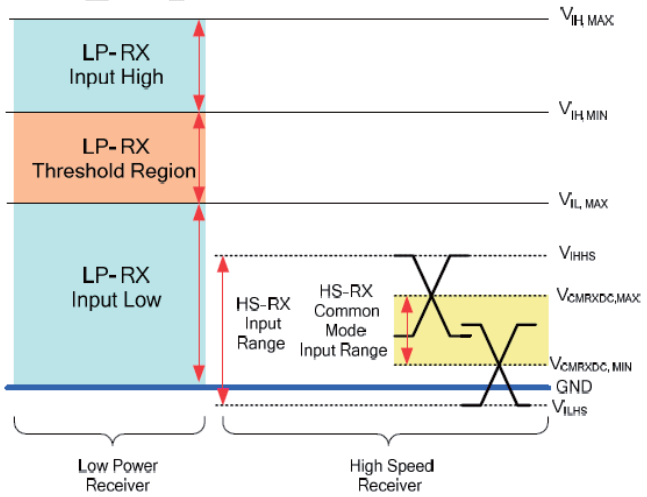


Figure :MIPI DC Diagram

4.4.2 MIPI AC Characteristic

4.4.2.1 LP Transmission

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	25	ns
Pulse width of the LP exclusive-OR clock	$T_{LP\text{-}PULSE\text{-}TX}$	50	-	-	ns
Period of the LP exclusive-OR clock	$T_{LP\text{-}PER\text{-}TX}$	100			ns

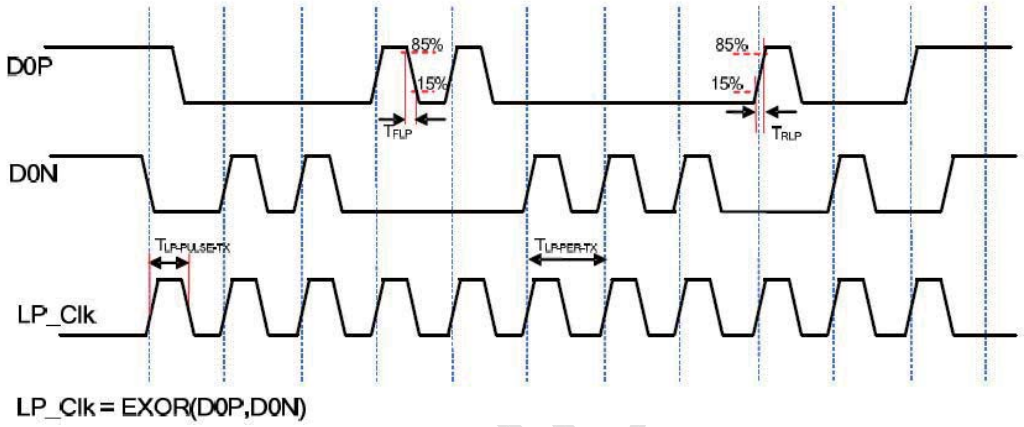


Figure :LP Transmitter Timing Definitions

4.4.3 High Speed Transmission

4.4.3.1 Data-Clock Timing Specifications

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
UI instantaneous	UI_{INST}	1.0	-	12.5	ns
Data to Clock Setup Time	T_{SETUP}	0.25	-	-	UI_{INST}
Data to Clock Hold Time	T_{HOLD}	0.25	-	-	UI_{INST}

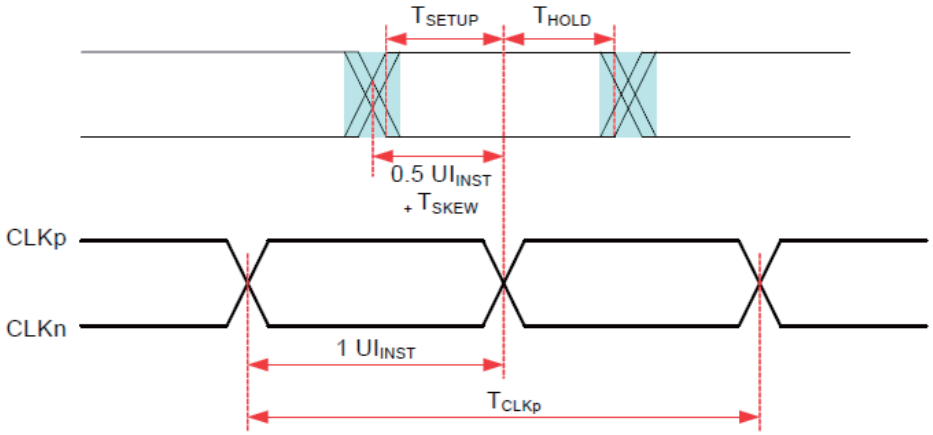


Figure : Data to Clock Timing Definitions

4.4.3.2 High-Speed Data Transmission in Bursts

4.4.3.2.1 High-Speed Data Transmission Operation Timing Parameters

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}	-	-	105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	8UI	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI	-	-	ns

Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. UI means Unit Interval, equal to one half HS clock period on the Clock Lane.
3. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

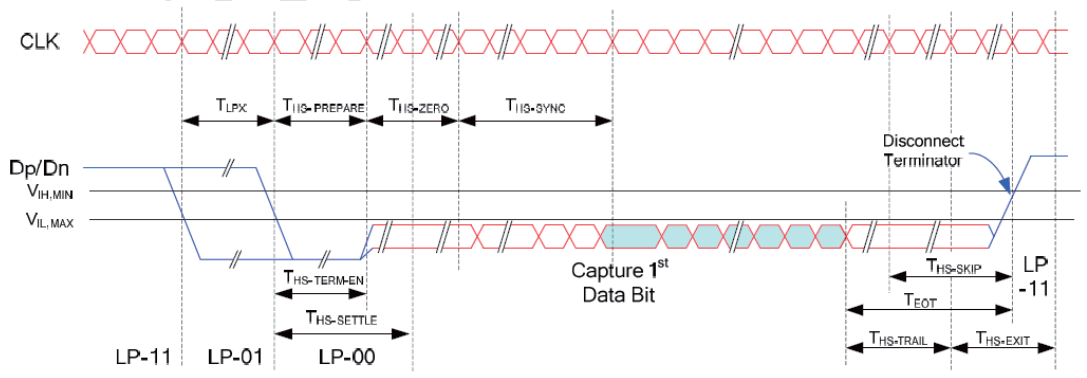


Figure : High-Speed Data Transmission in Bursts

4.4.3.3 High-Speed Clock Transmission

4.4.3.3.1 Switching the Clock Lane Operation Timing Parameters

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock Transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns

Note:

The DSI host processor shall support continuous clock on the Clock Lane for NT chip that require it, so the host processor needs to keep the HS serial clock running.

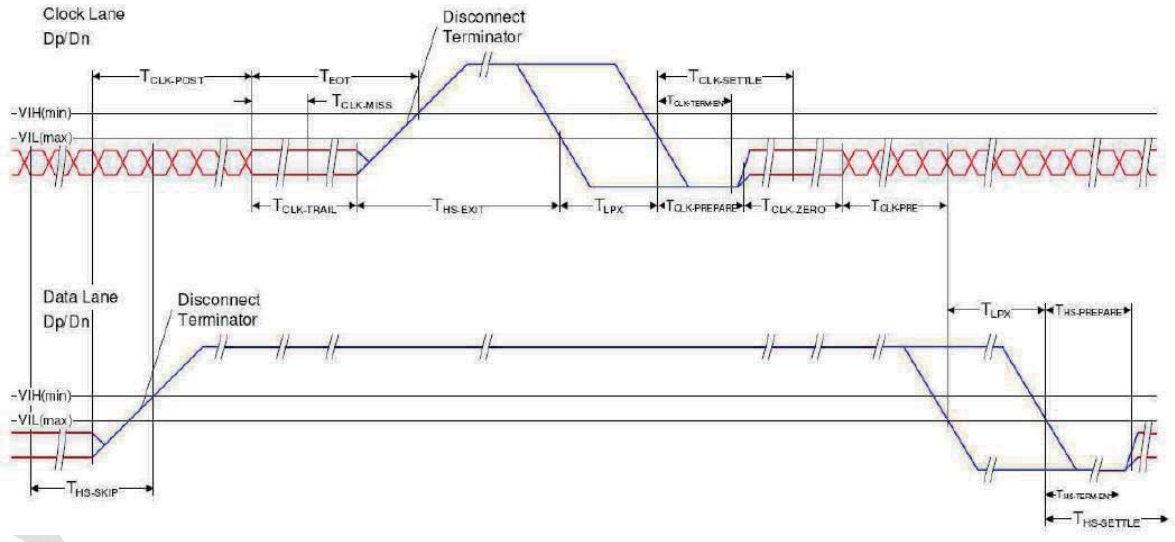
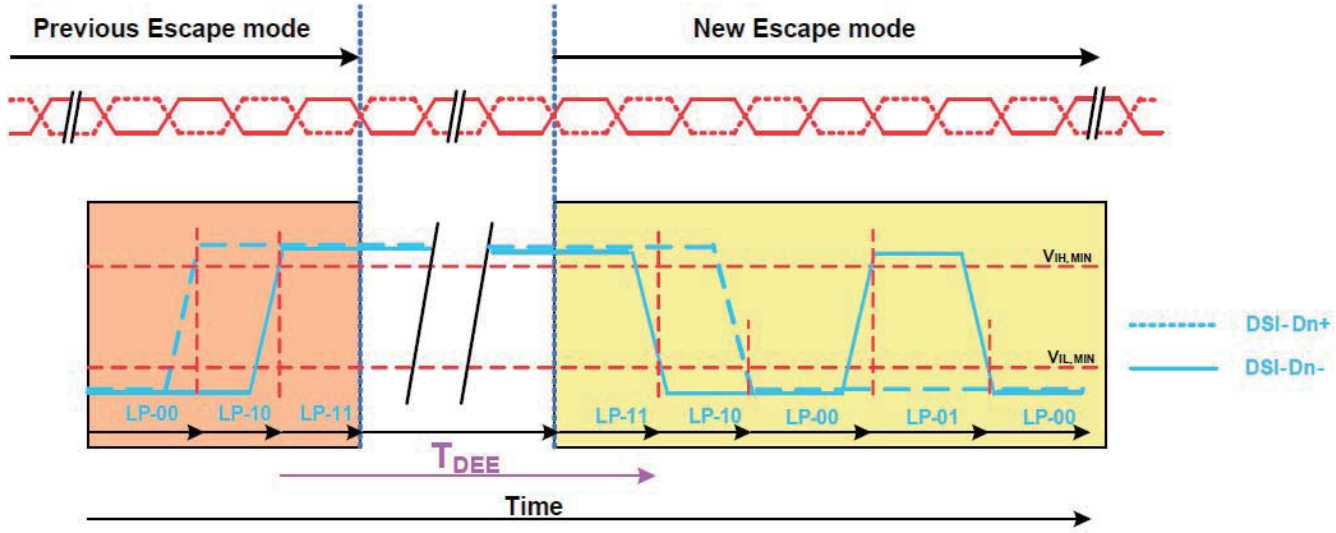


Figure :Switching the Clock Lane between Clock Transmission and Low-Power Mode

4.4.3.4 LP11 timing request between data transformation

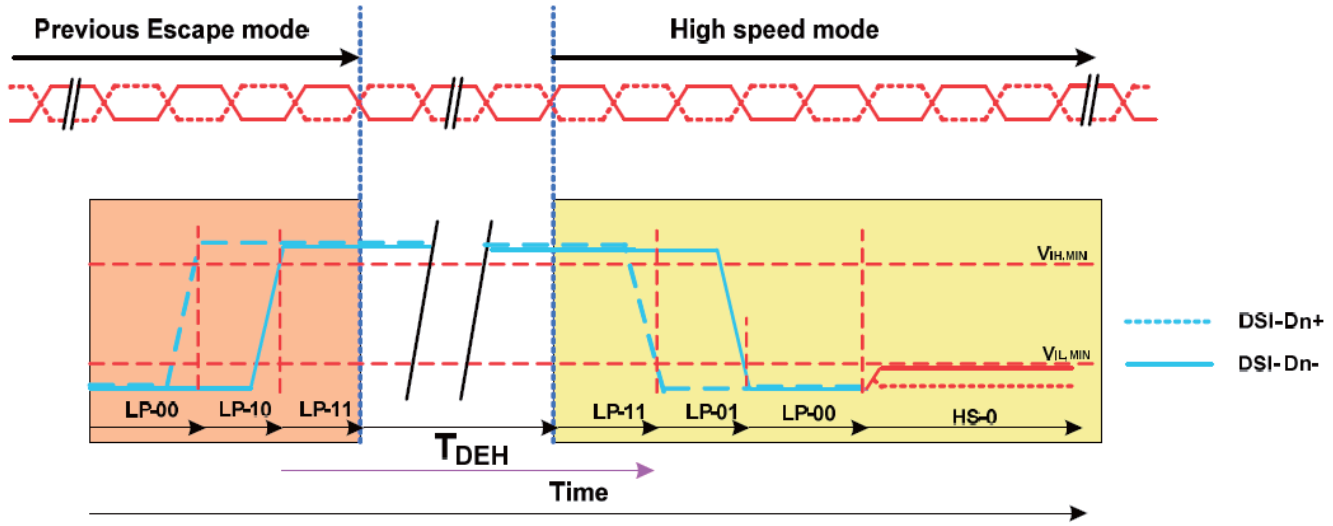
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP - LP, LP - HS, HS - LP, and HS – HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP - LP command



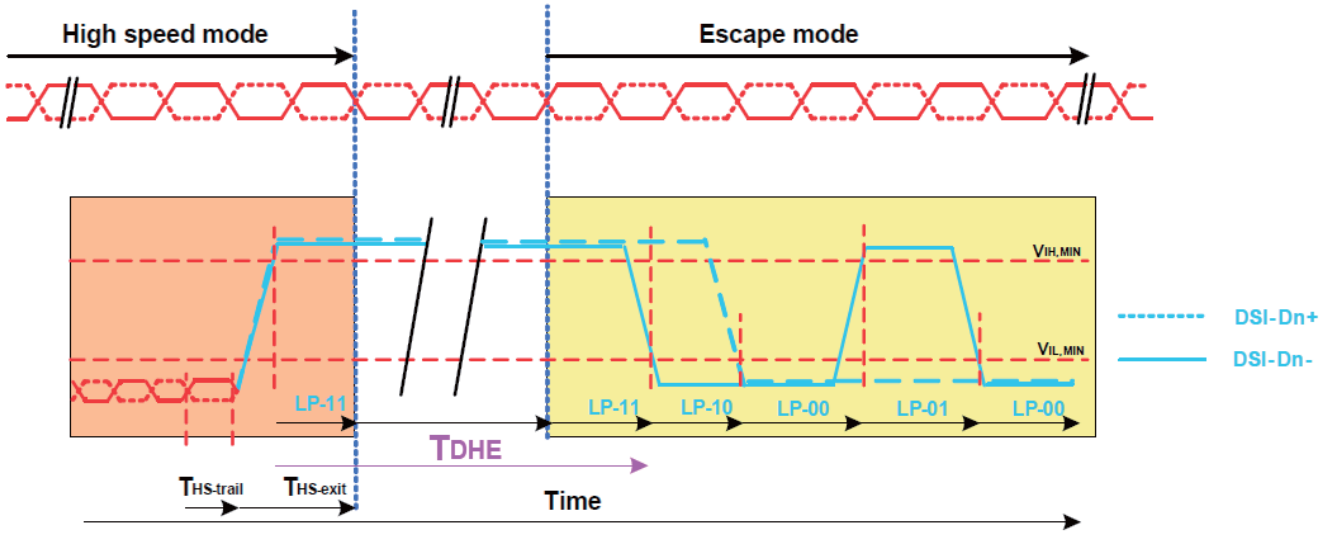
Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the new Escape Mode Entry	T_{DEE}	150	-	-	ns

(2)Timing between LP - HS command



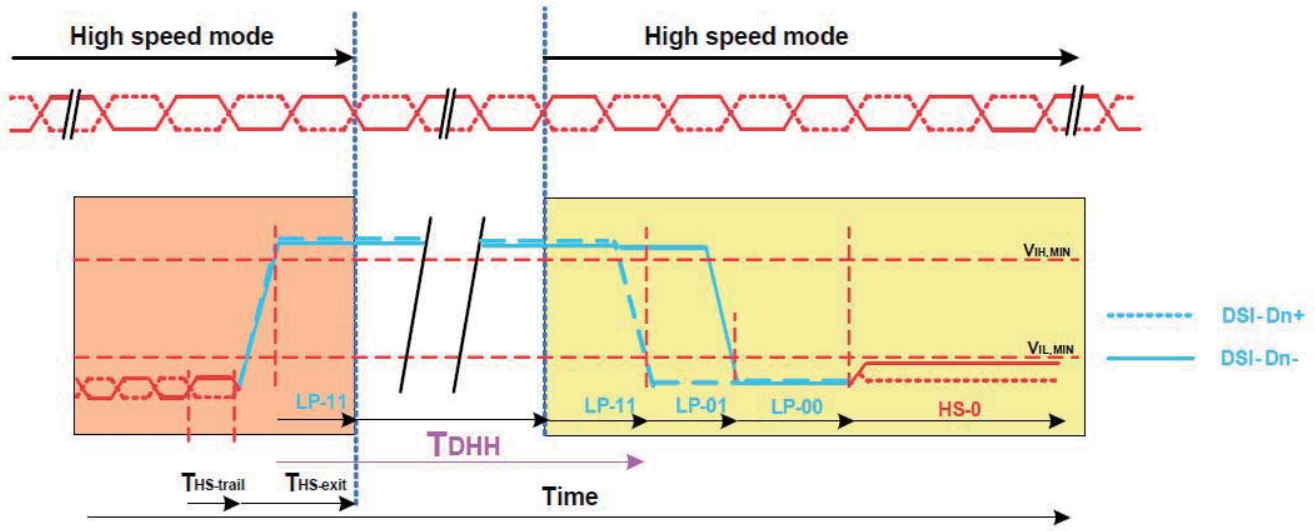
Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Entering High Speed Mode	T_{DEH}	Max(150,32UI)	-	-	ns

(3)Timing between HS - LP command



Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Escape Mode Entry	T_{DHE}	Max(150,32UI)	-	-	ns

(4)Timing between HS - HS command



Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Entering High Speed Mode	T_{DHH}	Max(150,32UI)	-	-	ns

4.5 MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display Controller may include local registers. Systems using Command Mode write to, and read from the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.
Note: The NT51021 IC only supports Video Mode operation.

4.5.1 MIPI Lane Configuration

	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Unidirectional Lane ■ Forward High-Speed ■ Forward Escape Mode ■ Forward LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

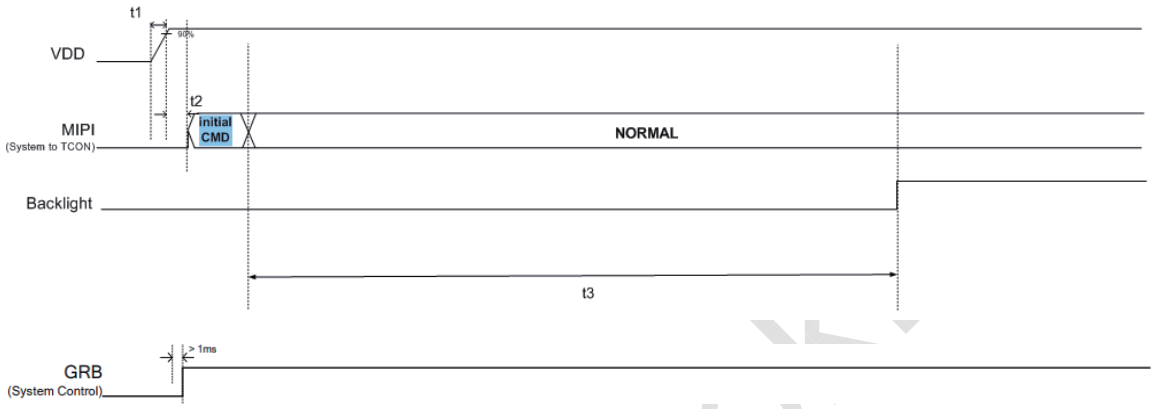
The connection between host device and display module is as reference.

4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

a. Power on:

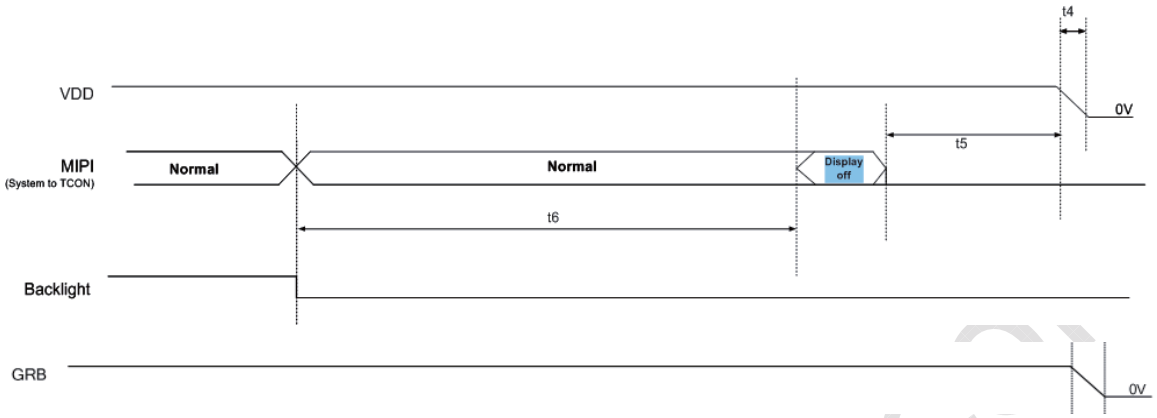
VDDI=3.0 ~ 3.6 V



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t1	-	-	2	ms	
t2	25	-	-	ms	
t3	100	-	-	ms	

b. Power off:

VDDI=3.0~3.6V,



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t4	0	-	-	ms	
t5	100	-	-	ms	
t6	20	-	-	ms	

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

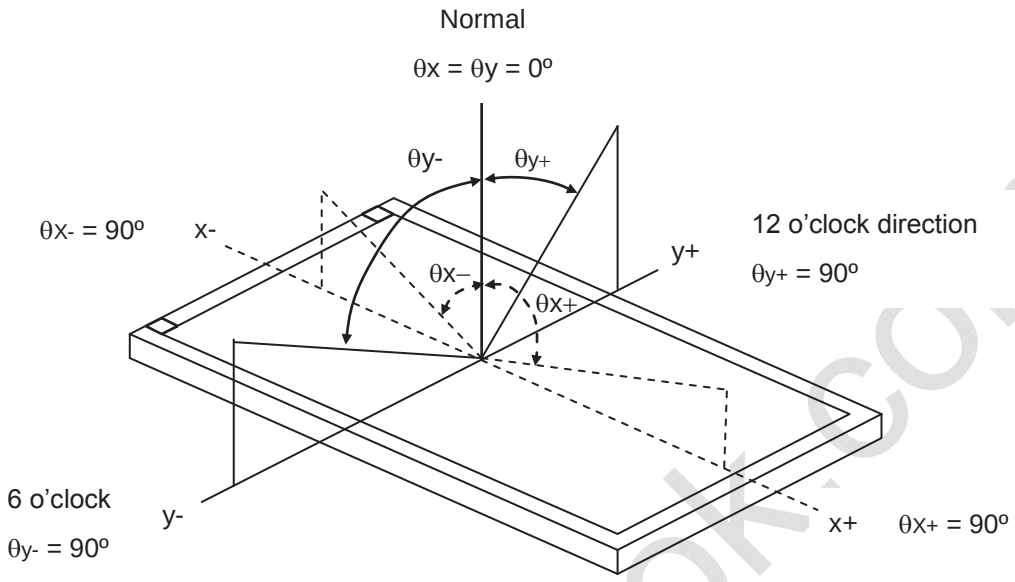
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	(3.0)	V
Input Signal	According to typical value in "4.3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	88	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θY =0° Viewing Normal Angle	800	1000	-	-	(2), (5) ,(7)
Response Time (Tr+Tf)		T		-	25	35	ms	(3) ,(7)
CP Luminance of White		LCP		350	440	-	Cd/m2	(4), (6) ,(7)
Color Coordinate	White	Wx		0.283	0.313	0.343	-	
		Wy		0.299	0.329	0.359	-	
Color Gamut Color		NTSC		65	70		%	
Luminance Uniformity		U_L		75	80		%	(6)
Viewing Angle	Horizontal	θ_{X+}		-	80	-	Deg.	(1), (5), (7)
		θ_{X-}		-	80	-		
	Vertical	θ_{Y+}		-	80	-		
		θ_{Y-}		-	80	-		
Flicker		dB	θx=0°, θY =0° Viewing Normal Angle		-30	-20		(8)
Crosstalk		%				2.5		(9)
Gamma				1.9	2.2	2.5		
White Variation of 13 Points		δW_{13p}		70	75	-	%	(5), (6), (7)

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression：

Contrast Ratio (CR) = L255 / L0

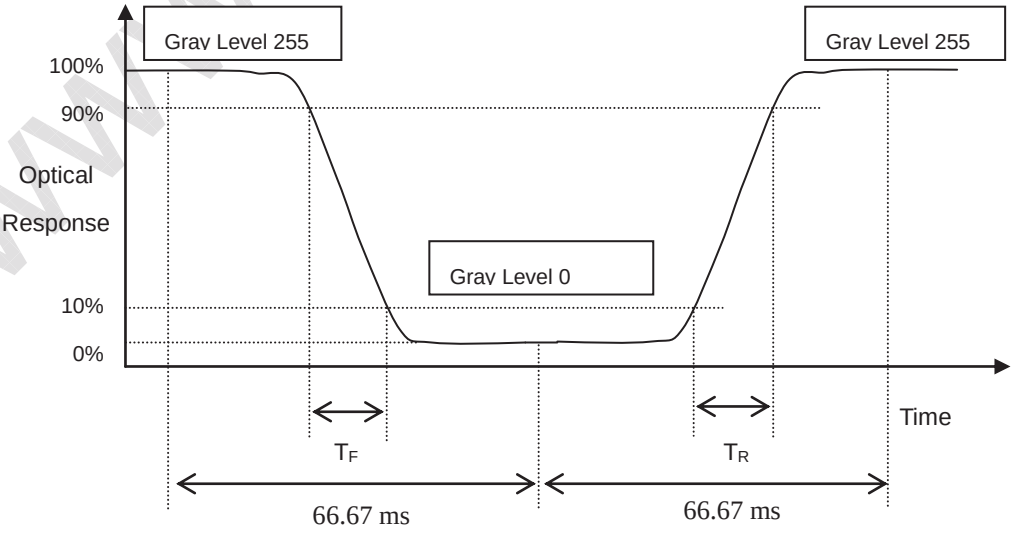
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Center Point Luminance of White (L_{CP}):

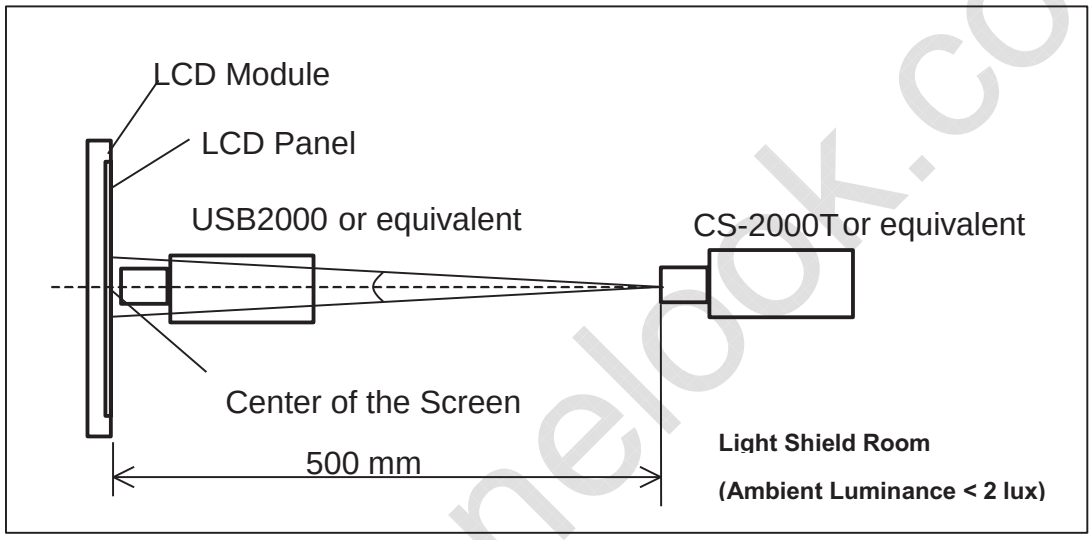
Measure the luminance of gray level 255 at center point

L_{CP} = L(5)

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

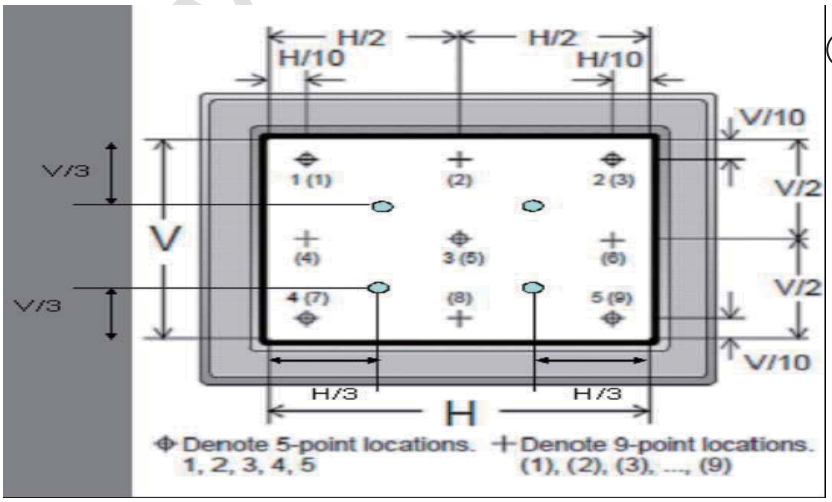
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 13 points

δW_{13p} = {Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}*100%



(X) : Test Point

X=1 to 13

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note (8) Flicker

No visual flicker will be allowed. The flicker level should be measured on GS127, The output signal is measured by Minolta CA210 immediately while Vcom is optimized. The flicker is essentially a ratio of the Amplitude in the frequency spectrum at 30 Hz (A30) and 0 Hz (A0), i.e.,

$$F = 20 \text{ Log } (A30 / A0).$$

Note (9) Crosstalk

Three luminance values are measured at the same position (i.e. A , B, and C).

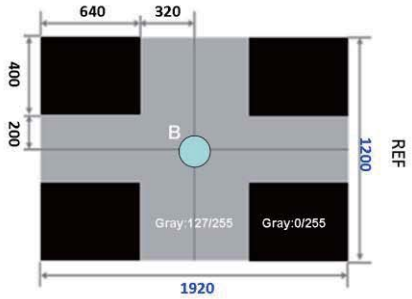
The cross-talk, is defined as,

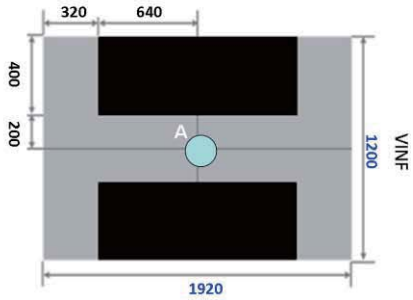
$$C(H) = | (L(A) – L(B) | / L(B) • 100\%,$$

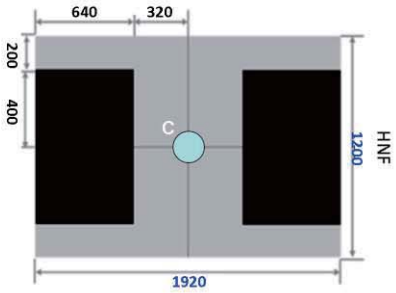
$$C(V) = | (L(C) – L(B) | / L(B) • 100\%,$$

Where, L (A, B, C) = Luminance in Position A, B, C

$$\text{Crosstalk} = \max (C(H), C(V))$$







6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	70ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	60ºC, 240 hours	
Low Temperature Operation Test	-10ºC, 240 hours	
High Temperature & High Humidity Storage Test	50ºC, RH 90%, 240hours	
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	

Note (1) criteria : Normal display image with no mura and extra line defect.
(should be checked with 6% ND filter and within 45° viewing angle from vertical)

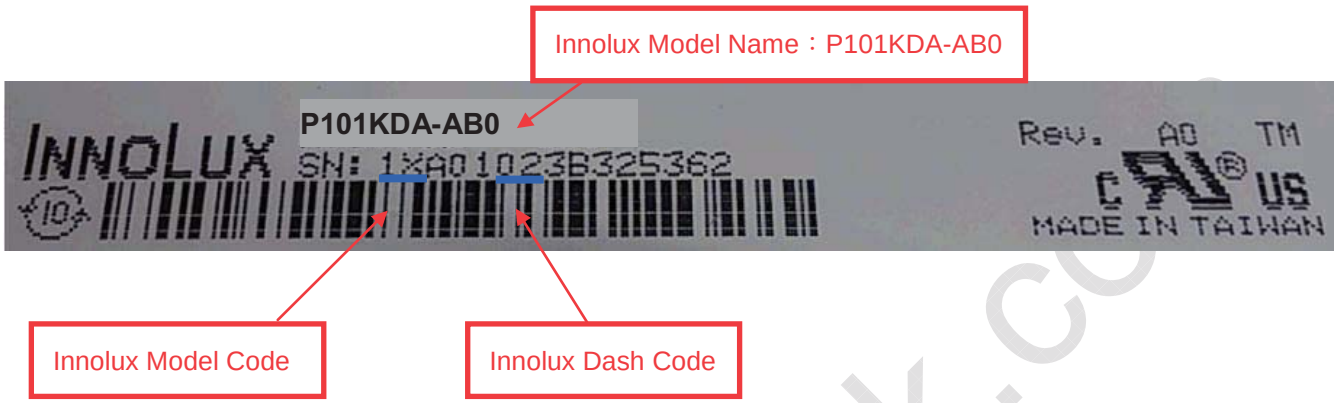
Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



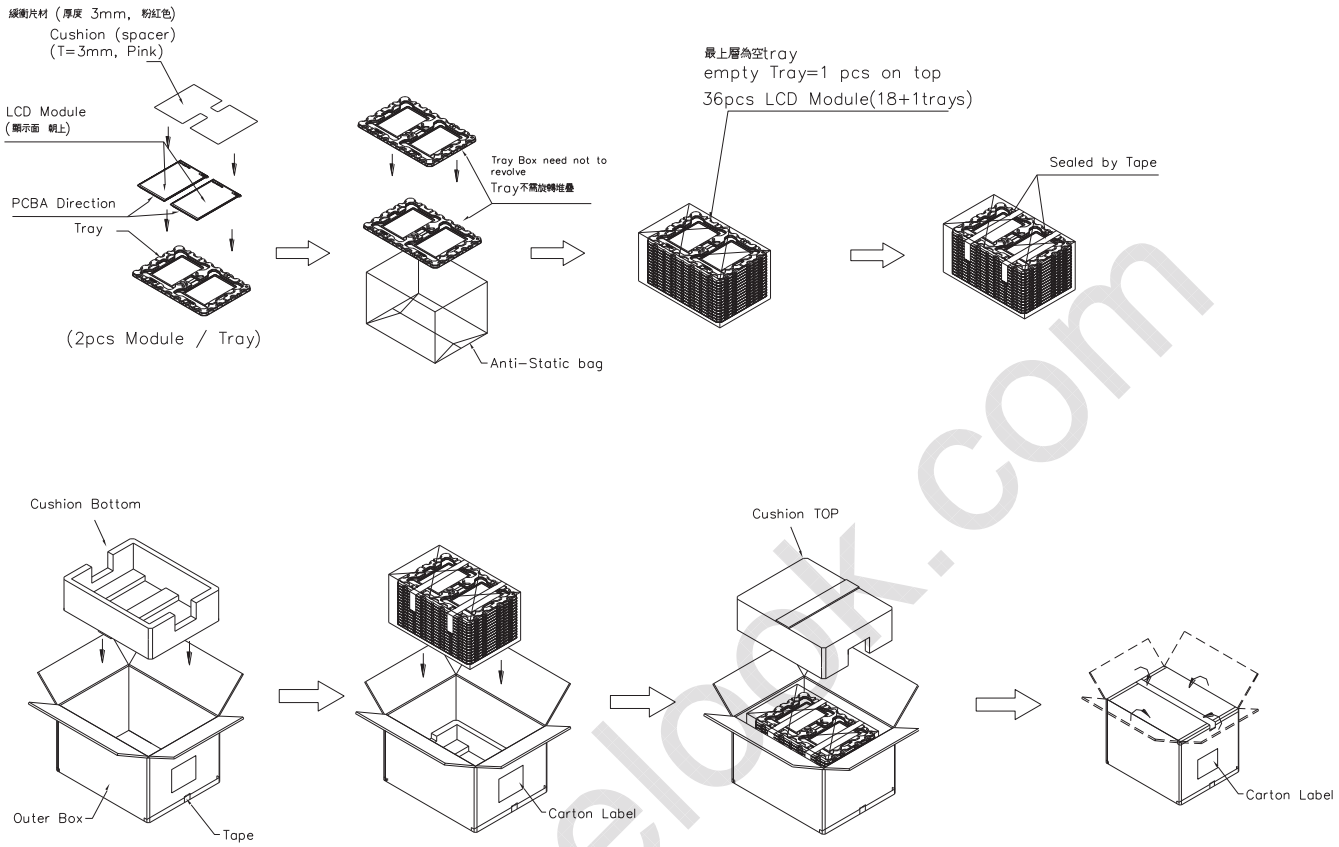
(a) Model Name: P101KDA-AB0

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: XX X X X XX Y M D L N N N N

- Serial No. (系統帶出)
- Product Line (grade, 系統帶出)
- Year, Month, Date (系統帶出)
- INX Internal Use (廠別 Code, 系統帶出)
- INX Internal Use (Product ID, 系統帶出)
- Revision (系統帶出, 跟著 BOM 版次變更)
- INX Internal Use (Model Code, 系統帶出, 固定不變)

7.2 CARTON



(1) Box Dimensions : 590(L)*390(W)*320(H)
(2) 36 Modules/Carton

Figure. 7-2 Packing method

7.3 PALLET

(1) 16 box(max.) / 1pallet
(2) Pallet stack 1200(L) x 800(W) x 1425(H) mm

Sea / Land Transportation
(40ft /40ft HQ Container)
Air Transportation

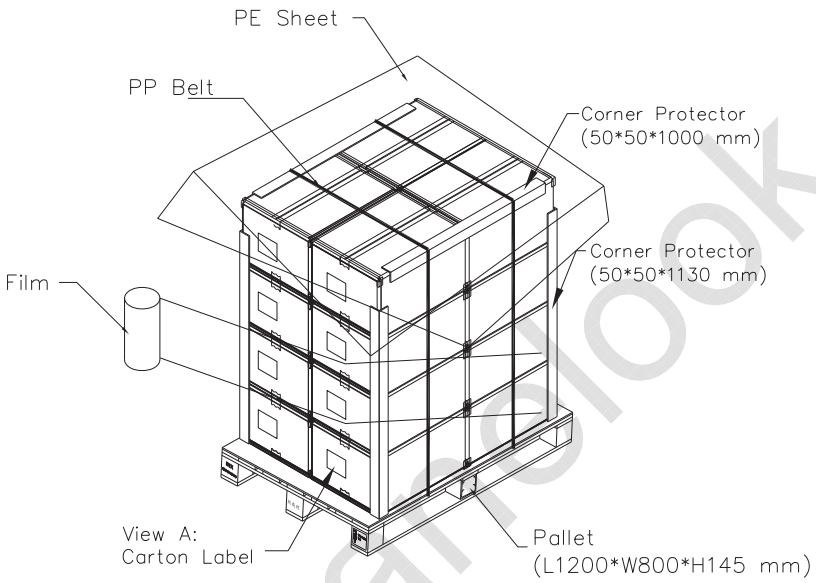


Figure. 7-3 Packing method

7.4 UN-PACKAGING METHOD

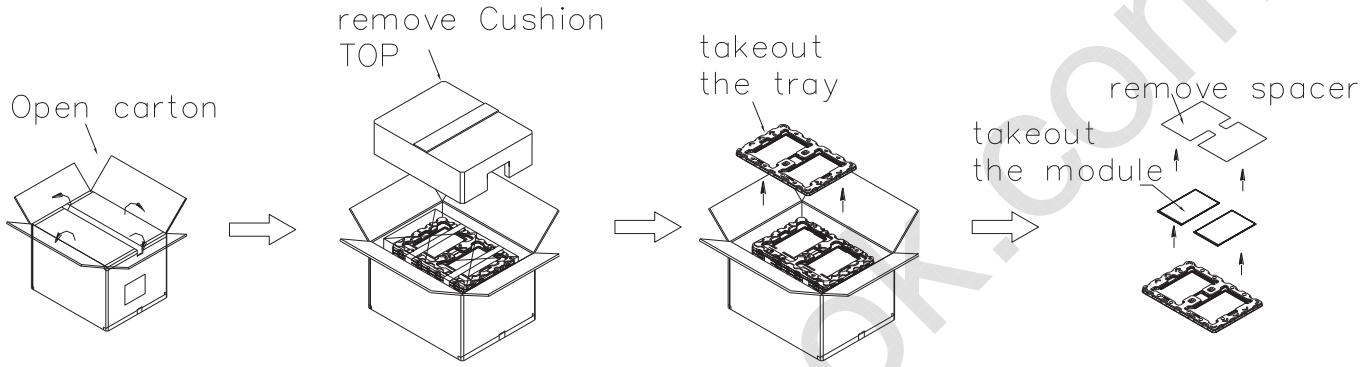


Figure. 7-4 Un-Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly.

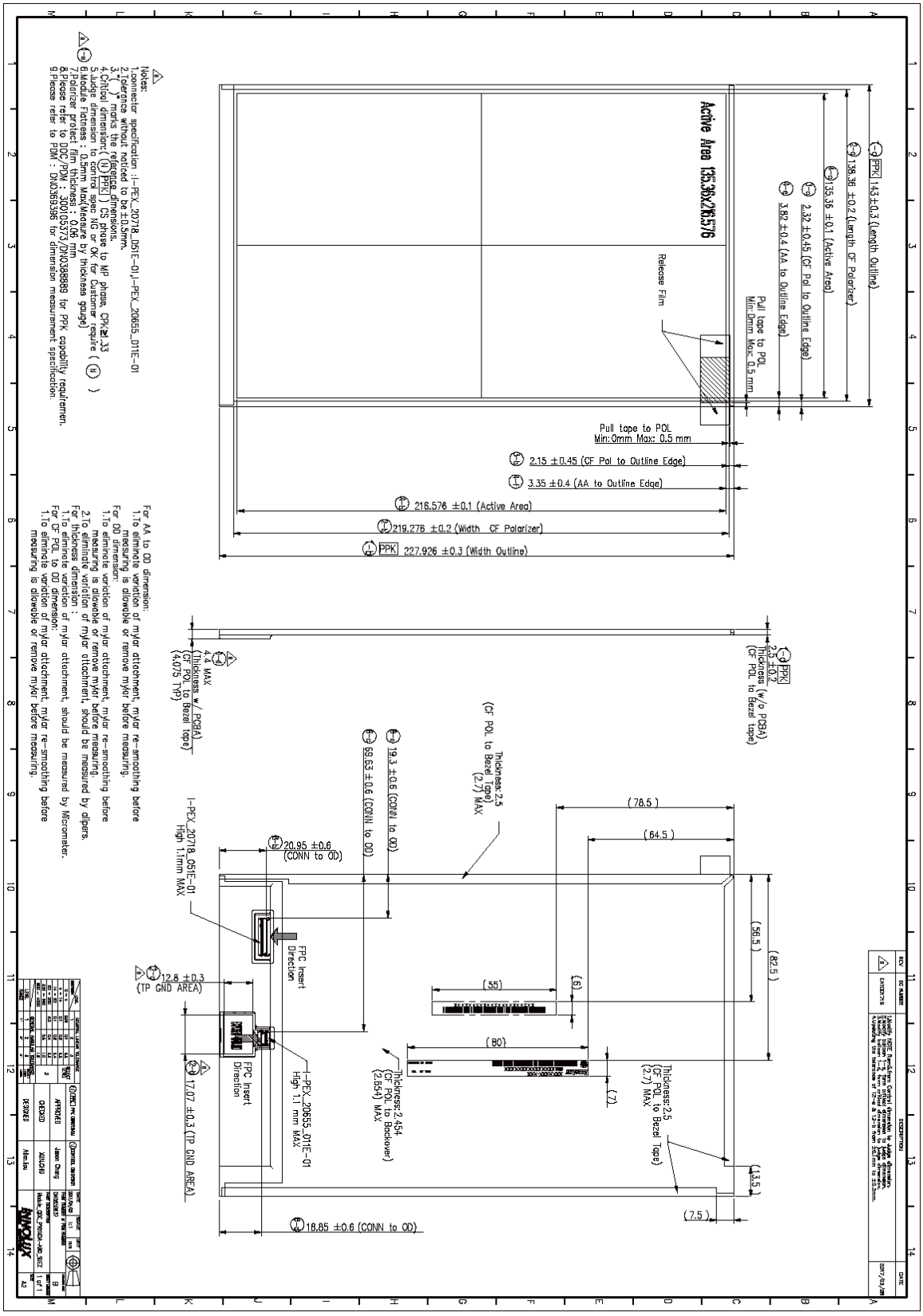
8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) Do not disassemble the module or insert anything into the Backlight unit.

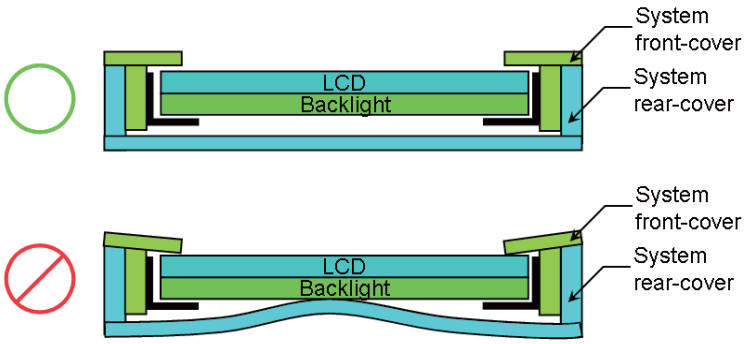
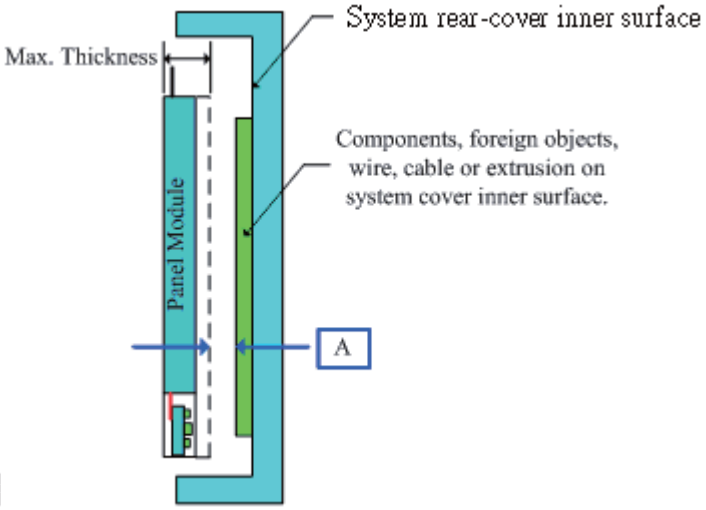
Appendix 1：OUTLINE DRAWING

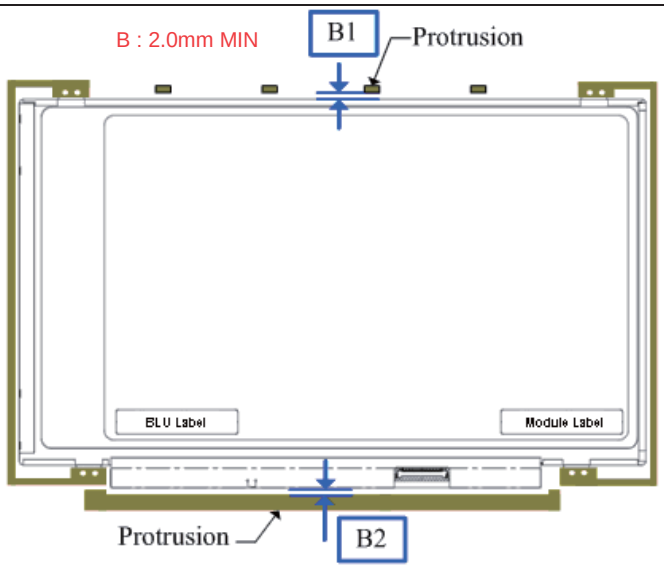


Appendix 2：NT51021B REGISTER SETTING

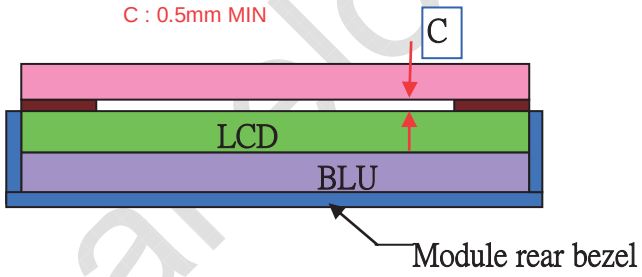
Command/ Function	R/W	Parameter
0x8F	W	0xA5
0x01	W	0x00
0x8F	W	0xA5
0x8C	W	0x80
0xC7	W	0x50
0xC5	W	0x50
0x85	W	0x04
0x86	W	0x08
0xA9	W	0x20
0x83	W	0xAA
0x84	W	0x11
0x9C	W	0x10
0xA9	W	0x4B
0x8F	W	0x00

Appendix 3：SYSTEM COVER DESIGN GUIDANCE

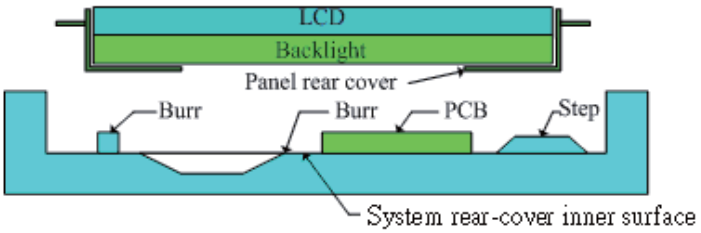
1.	Permanent deformation of system cover after reliability test
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
2.	Design gap A between panel & any components on system rear-cover
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Flatness of panel and system rear-cover should be taken into account for gap design.
3	Design gap B1 & B2 between panel & protrusions



Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.
4	Design gap C between touch panel & panel surface.



Definition	Air gap design between touch panel & panel surface is needed to prevent pooling, newton ring or glass broken. Compression ration of double side tape may cause pooling issue or newton ring. This phenomenon is obvious during pooling inspection procedure. To remain sufficient gap between touch panel and panel surface is recommended.
5	System rear-cover inner surface examination



Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
6	Tape/sponge design on system inner surface

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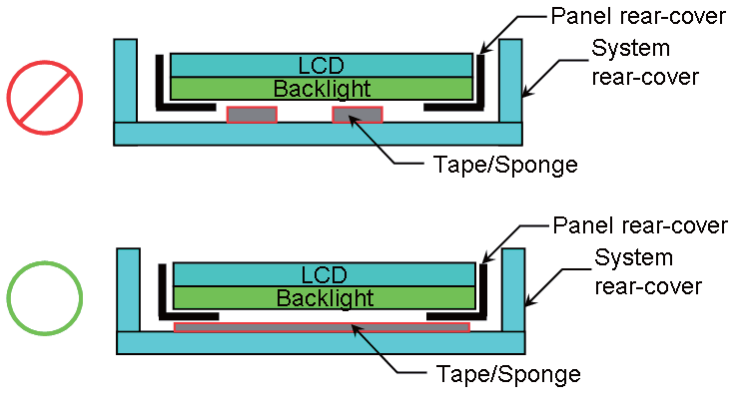
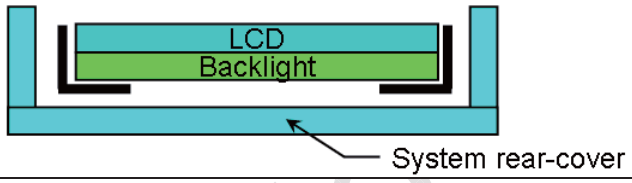
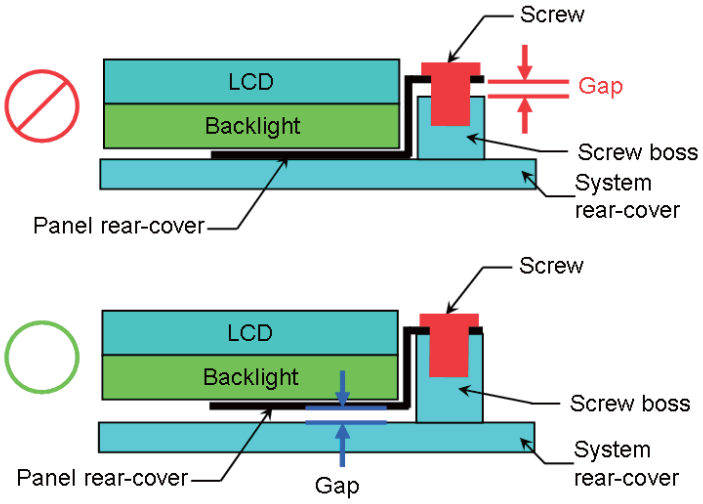
PRODUCT SPECIFICATION



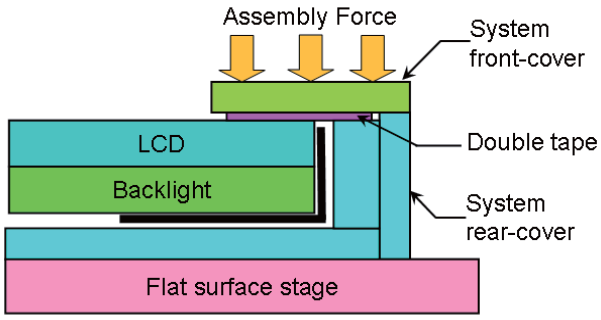
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
7	Material used for system rear-cover



Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
8	Screw boss height design



Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
9	Assembly SOP examination for touch panel with double side tape design

	
Definition	To prevent panel crack during touch panel assembly process with double tape design, it is only allowed to give slight pressure with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.