**Statement of Work**

**Project 38: Cross-Agency Applications/Architectures Analysis**

**Dated 6/15/2020**

**Dat**

Sept 2011 – Sept 2012

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# Overview

The goal of the project is to create, develop, and evaluate novel technologies and evidence for the value to serve the computing needs of the NSA and DOE simulation and data analysis. This SOW focuses on the analysis of DOE HPDA applications to identify similarities with LPS HPDA/Graph applications, and also to produce a predictive model to analyze potential technology paths to improving performance or scale of these target problems by a factor of 10x or more.

**Period of Performance:** July 1, 2020 - October 1, 2020 with ROM projections for FY21 1-year budget

The effort includes:

1. Establish benchmark codes and datasets to baseline performance on current state-of-the-art systems. Focus is on DOE graph and HPDA applications (focus area bioinformatics)
2. Instrument codes and collect performance data to build a predictive analytic model that enables evaluation of architectural alternatives.
3. Compare to LPS-supplied graph applications and identify overlaps/similarities.

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1. Evaluate Wafer Scale Integration Approach and impact on Graphs

**Costs:**

$384k for July 1-October 1, 2020 (3 month period),

$1.079M for FY21 (Oct 1, 2020 – Sept 30, 2021, 12 months)

## **WP1: Collect and Evaluate SC-relevant HPDA workloads and Compare alignment with LPS HPDA workloads and examples** *(LBL, ANL)*

We will analyze the HPDA workloads from bioinformatics applications in the SC space and compare with LPS examples to determine alignment between the HPDA requirements for graph applications supplied by LPS. The final report will deliver packaged benchmarks for the SC-relevant applications, a comparison of similarities with the LPS Graph/HPDA examples, and a predictive performance model that demonstrates the opportunities for performance improvement based on Project38 technologies. *This is a companion to the ANL-led WP2 activity, which focuses on the recoding engine aspects.*

**Time Period: July 1-October 1, 2020 (with prorated estimates for last months of FY20).**

**Budget:** 3 month total is $204*k (note summer salary only during summer months for faculty participants)****.***

***Participants***

Shaikh Arifuzzaman (MSU visiting faculty at LBNL) $46k summer salary + Student MD Abdul Motaleb Faysal at $12.5k/month,

Julian Shun (MIT/LBL) $53k,

Thom Popovici (Postdoc working for Shalf) $12.5k/month,

Shalf+Michelogiannakis ($15k/month)

ANL: 0.2 Bustamante ($5k/month)

**Deliverable at endpoint:** *A skeleton software/hardware design and projected performance. Report on the commonalities for these applications. All benchmark results and data will be documented in a final report.*

**Work Packages:**

1. **Collect challenge application codes and datasets (WP1.1)**
   * **Ensure they build and run on HPC systems Cori and Theta**
   * **Target SC bioinformatics & related graph applications** (HipMCL protein similarity, ANL CANDLE genomic sequence similarity, and HipMer/MetaHipMER sequence alignment)
   * **Target LPS HPDA applications:** Will be identified based on alignment with DOE-SC HPDA applications.

**Deliverables:** *Fully functioning benchmark codes to represent application requirements for challenge applications. A selection of LPS-provided HPDA applications based on alignment with SC apps. A baseline performance on contemporary HPC architectures.*

1. **Diagnose code barriers/bottlenecks: And what are the commonalities (what are common barriers and motifs that we can design against) (WP1.2)**
   * *Instrument code to identify resource requirements and limitations*
   * *Note: Although we understand the code behavior on contemporary systems in extreme detail, we have not thought in terms of what resources does the code* ***require*** *if the system was better suited. This part will require additional data collection to establish extended resource requirements.*

***Deliverable****: full code analysis with prioritized list of barriers and potential hardware/software remedies.*

1. **Develop predictive analytic model to explore design alternatives (WP1.3):**
   * Explore architecture alternatives using models as an exploration tool
   * Use higher-fidelity “simulator” models where required

**Deliverable**: Projections for how much improvement could be derived from alternative hardware and algorithm configurations (P38 alternatives)

## **WP2: Report on the IUSG Architecture Synergies with Graph-analytics applications.**

Explore Graph Analytics applications (partner with PNNL) to identify opportunities for efficient encodings (compute, storage, movement). Use prior P38/Recode design infrastructure to explore, but focus is on new requirements and new architectural features -- insights from this new problem space.

**Time Period: July 1-October 1, 2021 (with prorated estimates for last 3 months of FY20).**

**ANL:** 3 month total is $150k

* 1 Graduate students ($60k)
* Bustamante 0.25 FTE ($60k)
* Fractional Chien, Bair, Finkel FTE ($30k)

**Deliverables: *(each will be documented with a presentation and report)***

***Work Packages;***

1. Work with algorithm designers and software implementation developers to design novel, dense encodings (WP2.1)
2. Design and implement encodings and and data orchestration on Recode infrastructure to explore potential performance improvements for graph analytics algorithms (WP2.2)
3. Enhance the LLVM-based low-level compiler for Recode as needed; develop higher-level compiler for parallel graph algorithms (perhaps based on GraphIt (<https://graphit-lang.org/>) and/or TACO (<http://tensor-compiler.org/>). (WP2.3)
4. Propose new architectural features / designs for Project 38 Innovative USG architecture based on insights from graph analytics workloads (WP2.4)

## **WP3: Assess Impact of Op-level Synchronization and Wafer-scale integration for Project 38**

Write kernel codes to assess and analyze Cerebras CS-1 (cerebras.net) architecture features using regular (stencil), then irregular (graph) structures. Evaluate effectiveness of fine-grained parallelism, network integration, WSI, etc.. Specific targets include finite difference solvers, and graph algorithms such as community detection (Vite) and maximum influence (Ripples). Understanding Op-level synchronization and WSI opportunities and limitations to inform new architectures (WSI or not, Cerebras or other avenues) and the larger architecture design space that falls within the P38 mission.

**ANL:** 3 month total to end of fiscal year is $130k

* 2 Graduate students ($120k)
* Fractional Chien FTE ($10k)

**Deliverables:*(each will be documented with a presentation except where software artifact is noted)***

1. Work with Cerebras team (and very limited software tools) to build high-performance codes on CS-1 (WP3.1)
2. Understanding and evaluate benefits of and how to exploit the CS-1’s fine-grained synchronization and communication mechanisms for future P38 accelerators (WP3.2)
3. Assess benefits of wafer-scale architecture approach (or variations) for graph analytics applications (WP3.3)
4. Build a high-level analytical performance model of both operation-level synchronization and WSI technologies (WP3.4)

Supplemental: Estimated FY21 work packages and Costs Projections

Total Projected for FY21 (October 1 2020-October 1, 2021): $1.079M

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| Extending WP1 into FY21 | **Design and Refine Project 38 Innov-USG architecture based on Workloads Study and FG&WSI Learnings**  **Deliverable**: Detailed Architecture development and delivery of fully-functioning simulator/model of proposed Innovative USG Architecture   * Develop and document design specification (ANL, LBL) * Develop simulator/architectural model (may need uplift to bring in Sandia for SST aspects) * Base software (ANL for system software and compiler, GraphBlas + MIT C-Trees for algorithm/framework) * Potentially merge back together with PNNL. (use PNNL cost estimates)   **Schedule:** 1 year (fiscal year boundary) | **LBNL**: Thom Popovici (75% postdoc $150k), John Shalf ($75k) George Michelogiannakis ($75k), Shaikh Arifuzzaman ($46k + $120k for one graduate student), Julian Shun ($53k summer salary)  **Total FY21**: $519K |
| Extending WP2 into FY21 | **Rigorous Simulation and Performance Evaluation of Updated Innovative USG Project 38 Architecture for Graph Analytics**  Based on results of performance modeling and growing software infrastructure, build a detailed simulation of the overall IUSG Project 38 architecture and evaluate potential benefits for graph analytics   * Release LLVM-based compiler and higher-level compiler for graph algorithms. * Build Recode software libraries for chosen graph encodings and operations * Detailed performance evaluation of architecture features using Graph Analytics Kernel on Updated Innovative USG Project 38 Architecture | **ANL**: 1 graduate students ($120K), Bustamante 0.35 ($84K), fractional Chien, Finkel FTE ($40K)  **Total FY21:** $244k |

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| **Extending WP3 into FY21** | **Design Novel Project 38 Innov-USG architecture based on FG&WSI Learnings**  Based on results of analysis, and the implementation learnings, explore implications for Innovative-USG architecture   * Implications of Wafer-scale for design of memory hierarchy structures - PE, node, large-scale system * Viability and desirability of Operation-level synchronization, network integration, etc. for future P38 architectures * Propose new architectures (synthesis)     Build a high-level analytical performance model of novel Project 38 architecture mechanisms and design   * Evaluate potential benefit on stencil and graph applications * Adapt prototype of a high-level Graph compiler from to enable experiments on lower-level Cerebras software tools | ANL: 2 graduate students ($240K), Bustamante 0.15 ($36K), fractional Chien, Finkel FTE ($40K)  **Total FY21:** $316k |