

MOD-5 COUNTER USING VERILOG

- DESIGN SOURCE USED IN VIVADO

The screenshot shows the Vivado 2016.4 interface with the following details:

- Title Bar:** counter - /afs/itd.ac.in/user/e/een212026/eclab_21/counter/counter.vr - Vivado 2016.4@dirac1
- Top Menu:** File, Edit, Flow, Tools, Window, Layout, View, Run, Help
- Toolbar:** Default Layout, New, Open, Save, Undo, Redo, 10 us, Synthesis Out-of-date, more info
- Flow Navigator:** Project Manager, IP Integrator, Simulation, RTL Analysis, Synthesis, Implementation, Program and Debug.
- Behavioral Simulation Tab:** Functional - sim_1 - testbench
- Object List:** counter.v x testbench.v
- Code Editor:** Displays the Verilog code for the counter module:

```
module counter(
    input clk,
    input rst,
    output reg [2:0] count
);
    reg [2:0] next_count;
    always @(posedge clk, negedge rst)
    begin
        if(rst==0)
            begin
                count<=0;
            end
        else
            begin
                count<=next_count;
            end
    end
    always @*
    begin
        if(count==5)
            count<=0;
        else
            next_count<=count+1;
    end
endmodule
```
- Tcl Console:** A small window at the bottom left.
- System Icons:** Taskbar icons for File Explorer, Control Panel, Mail, Internet Explorer, and others.
- Bottom Status Bar:** 29°C, ENG, 17.10.2021, 12:17.

- SIMULATION SOURCE USED IN VIVADO

The screenshot shows the Vivado 2016.4 interface with the following details:

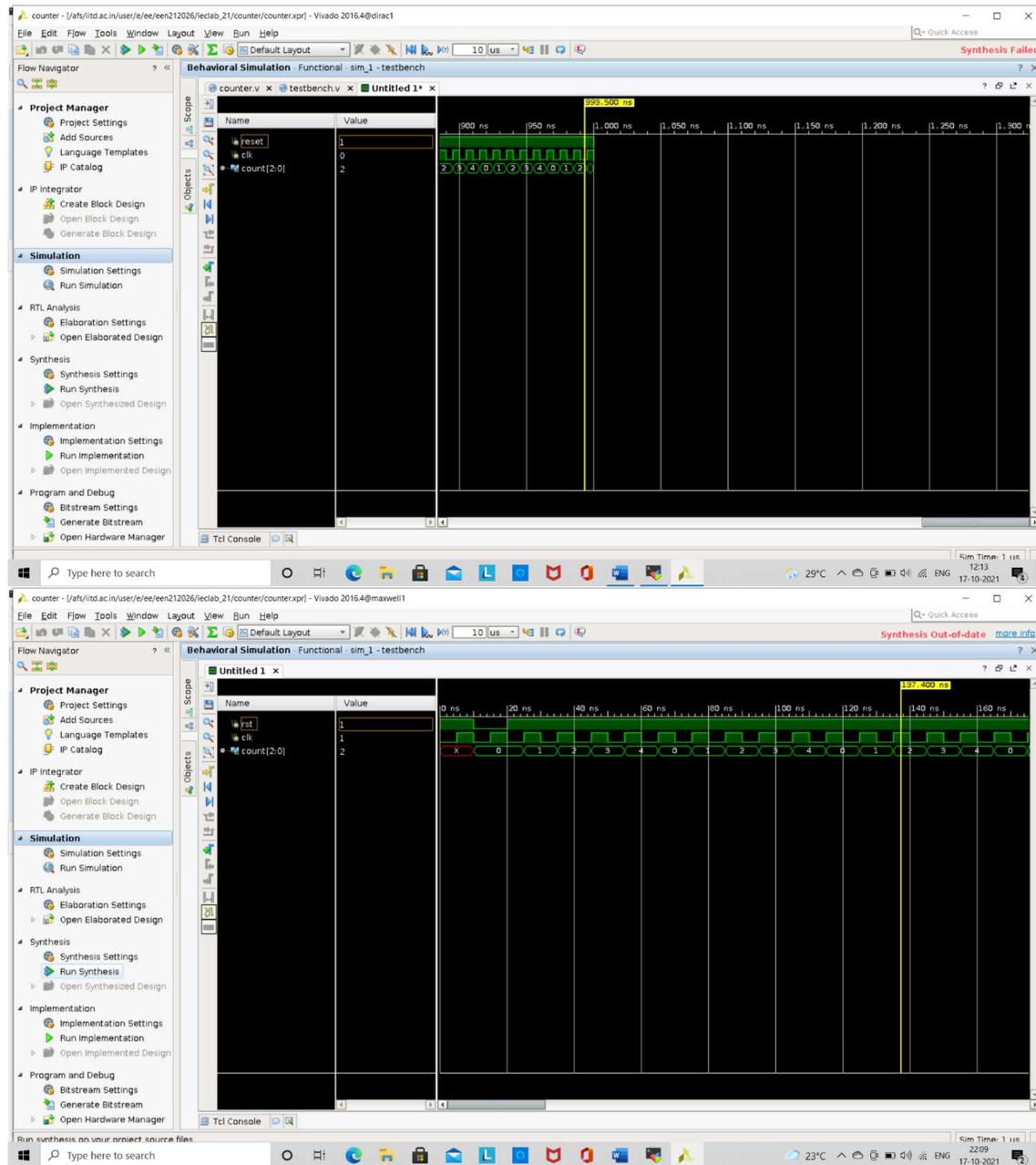
- Title Bar:** counter - /afs/itid.ac.in/user/e/ee/en212026/eclab_21/counter/counter.xpr - Vivado 2016.4@dirac
- Top Menu:** File, Edit, Flow, Tools, Window, Layout, View, Run, Help
- Toolbar:** Default Layout, New, Open, Save, Undo, Redo, 10 us, More Info, Synthesis Out-of-date, more info
- Flow Navigator:** Project Manager, IP Integrator, Simulation, RTL Analysis, Synthesis, Implementation, Program and Debug.
- Objects View:** Shows the current file structure:
 - counter.v (selected)
 - @ testbench.v
 - /afs/itid.ac.in/user/e/ee/en212026/eclab_21/counter/counter.srcs/sim_1/new/testbench.v
- Code Editor:** Displays the Verilog code for the testbench:

```
// Company: 
// Engineer: 
//
// Create Date: 10/18/2021 04:42:00 PM
//
// Design Name: 
// Module Name: testbench
//
// Project Name: 
// Target Devices: 
//
// Tool Versions: 
//
// Description: 
//
// Dependencies: 
//
// Revision: 
// Revision 0.01 - File Created
// Additional Comments: 
//
// 
module testbench();
    reg rst, clk;
    wire [2:0] count;

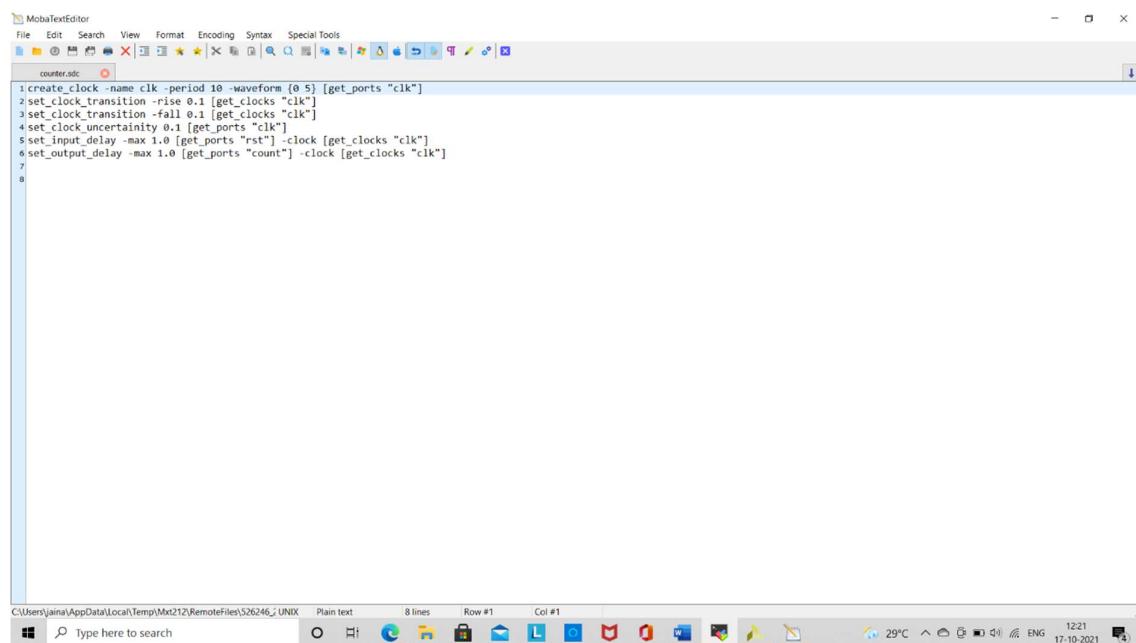
    counter #(clk, rst, count);
endmodule

always #5
    clk=~clk;
initial
begin
    $readmemh("data.dat", count);
    $dump(1, count);
    clk=1;
    rst=0;
    $display("rst = %b", rst);
    rst=1;
end
endmodule
```
- Tcl Console:** Shows the command `source ./testbench.v`.
- Bottom Status Bar:** 33.6, Insert, Version, 29°C, ENG, 12:18, 17.10.2021

- OUTPUT OF SIMULATION IN VIVADO

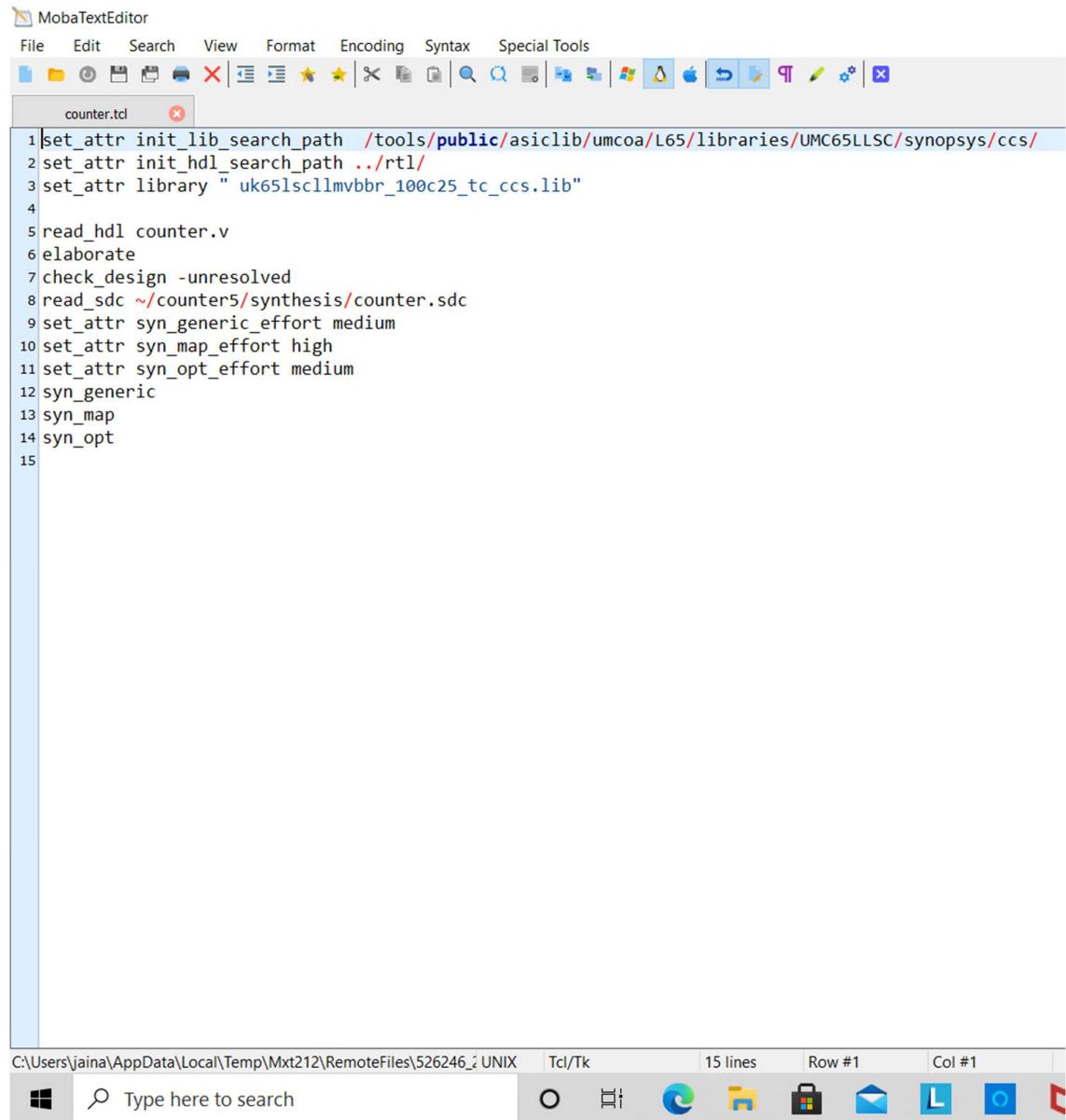


● SDC FILE USED



```
1 create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
2 set_clock_transition -rise 0.1 [get_clocks "clk"]
3 set_clock_transition -fall 0.1 [get_clocks "clk"]
4 set_clock_uncertainty 0.1 [get_clocks "clk"]
5 set_input_delay -max 1.0 [get_ports "rst"] -clock [get_clocks "clk"]
6 set_output_delay -max 1.0 [get_ports "count"] -clock [get_clocks "clk"]
7
8
```

- **TCL FILE USED**

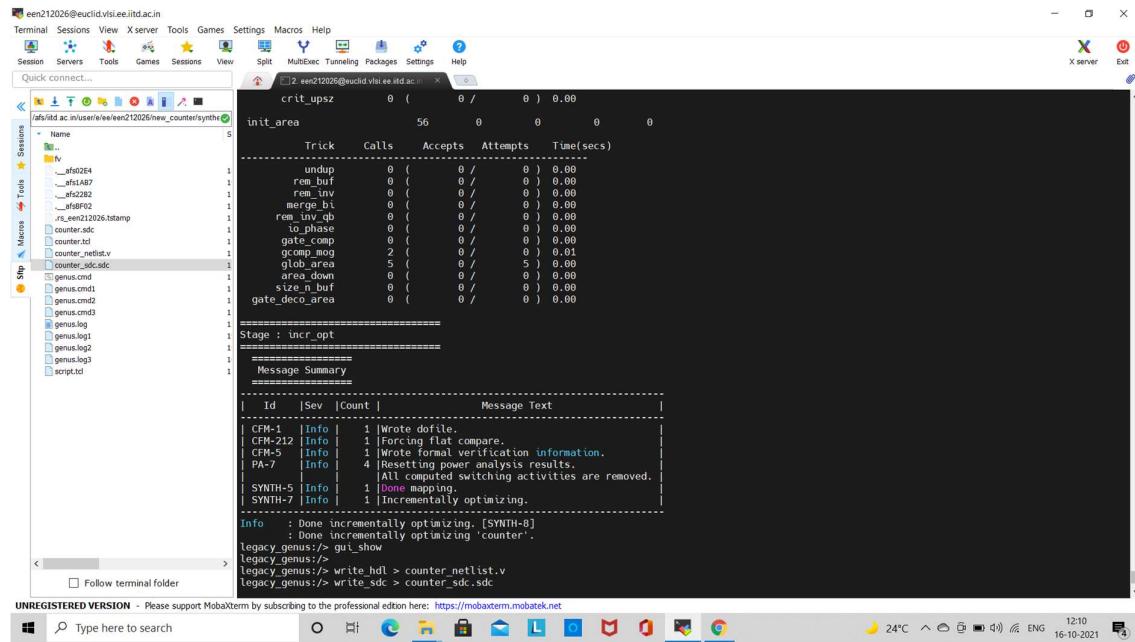


The screenshot shows a window titled "MobaTextEditor" with a menu bar including File, Edit, Search, View, Format, Encoding, Syntax, and Special Tools. Below the menu is a toolbar with various icons. The main area displays a file named "counter.tcl" containing the following TCL script:

```
1 set_attr init_lib_search_path /tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs/
2 set_attr init_hdl_search_path ../rtl/
3 set_attr library " uk65lscl1mvbbbr_100c25_tc_ccs.lib"
4
5 read_hdl counter.v
6 elaborate
7 check_design -unresolved
8 read_sdc ~/counter5/synthesis/counter.sdc
9 set_attr syn_generic_effort medium
10 set_attr syn_map_effort high
11 set_attr syn_opt_effort medium
12 syn_generic
13 syn_map
14 syn_opt
15
```

At the bottom of the window, there is a status bar showing the path "C:\Users\jaina\AppData\Local\Temp\Mxt212\RemoteFiles\526246_2 UNIX", the word "Tcl/Tk", and line counts "15 lines", "Row #1", and "Col #1".

● GENERATING NETLIST(.v) AND CONSTRAINT(.sdc) FILE IN GENUS FOR SYNTHESIS



The screenshot shows the MobaXterm interface with a terminal window titled 'een212026@euclid.vlsiee.iit.ac.in'. The user has run the command 'genus' to generate synthesis files. The output shows the progress of the synthesis process, including the creation of a netlist and constraint files.

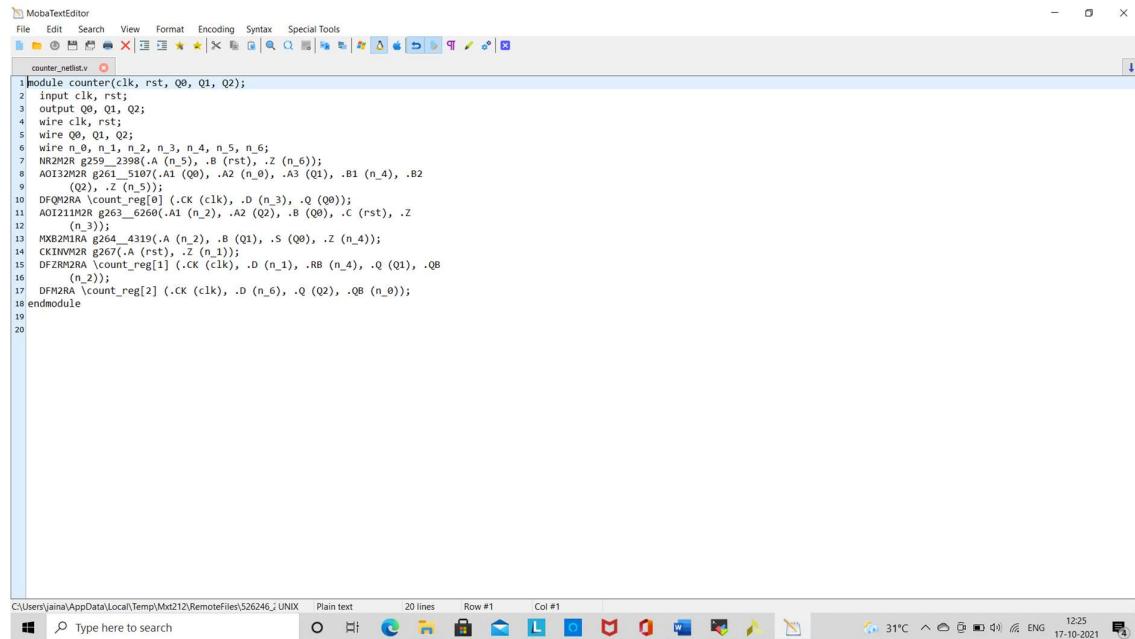
```

een212026@euclid.vlsiee.iit.ac.in ~
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
< /afs/iit.ac.in/vlsiee/een212026/new_countersynth>
Sessions
Tools Macros Step Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Name
  -_af602E4
  -_af602F7
  -_af602F8
  -_af602F9
  -_rs sen212026.tstamp
  -counter.sdc
  -counter.tcl
  -counter.netlist.v
  -counter.sdc
  -genus.cmd
  -genus.cmd2
  -genus.cmd3
  -genus.log
  -genus.log2
  -genus.log3
  -script.tcl
S
init_area      56   0   0   0   0
      Trick   Calls   Accepts   Attempts   Time(secs)
1 undup          0   (   0 /   0 )  0.00
1 rem_buf        0   (   0 /   0 )  0.00
1 rem_inv        0   (   0 /   0 )  0.00
1 merge_b1       0   (   0 /   0 )  0.00
1 rem_inv_gb     0   (   0 /   0 )  0.00
1 io_phase       0   (   0 /   0 )  0.00
1 gate_comp     0   (   0 /   0 )  0.00
1 gcomp_mog     2   (   0 /   0 )  0.00
1 global_taps    5   (   0 /   5 )  0.00
1 area_down      0   (   0 /   0 )  0.00
1 size_n_buf     0   (   0 /   0 )  0.00
1 gate_deco_area 0   (   0 /   0 )  0.00
1
=====
Stage : incr_opt
=====
=====
Message Summary
=====
| Id | Sev | Count | Message Text
|---|---|---|
| CFM-1 | Info | 1 | Wrote dofile.
| CFM-212 | Info | 1 | Forcing flat compare.
| CFM-5 | Info | 1 | Wrote formal verification information.
| PA-7 | Info | 4 | Resetting power analysis results.
| PA-8 | Info | 1 | All computed switching activities are removed.
| SYNTH-5 | Info | 1 | Incrementally optimizing.
| SYNTH-7 | Info | 1 | Incrementally optimizing.

Info : Done incrementally optimizing. [SYNTH-8]
Info : Done incrementally optimizing 'counter'.
legacy_genus:/> gui_show
legacy_genus:/> write_hdl > counter.netlist.v
legacy_genus:/> write_sdc > counter_sdc.sdc
legacy_genus:/> write_sdc > counter_sdc.sdc
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
24°C ⌂ ENG 12:10 16-10-2021

```

NETLIST FILE GENERATED BY GENUS



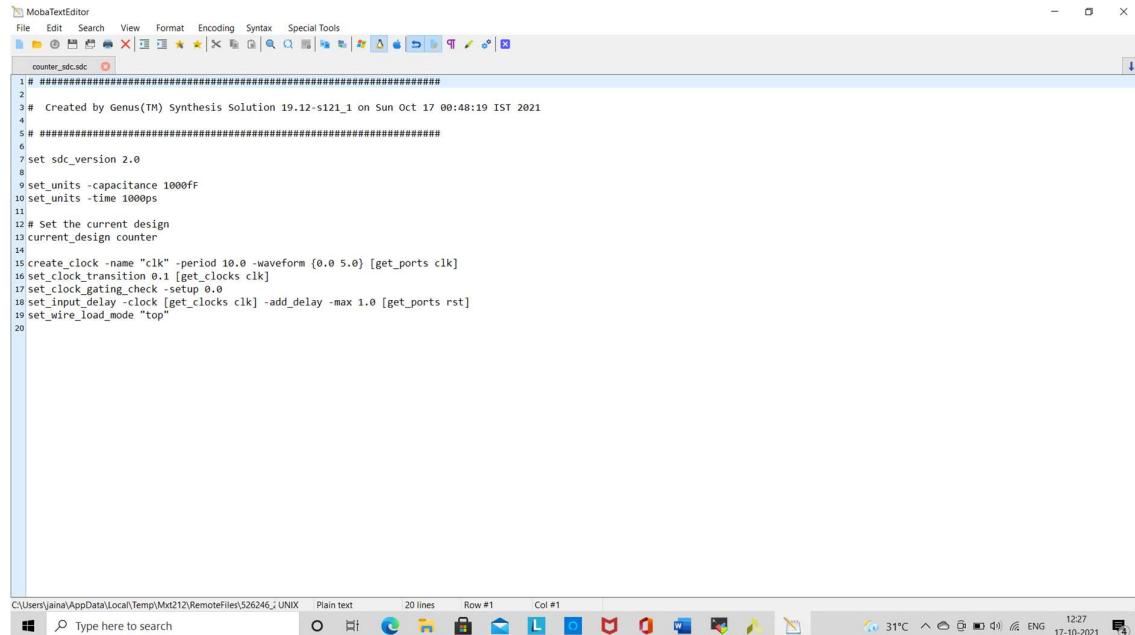
The screenshot shows the MobaTextEditor interface displaying the generated Verilog netlist file 'counter.netlist.v'. The code defines a module 'counter' with various wires and logic blocks such as D flip-flops and multiplexers.

```

MobaTextEditor
File Edit Search View Format Encoding Syntax Special Tools
File Edit Search View Format Encoding Syntax Special Tools
counter.netlist.v
1 module counter(clk, rst, Q0, Q1, Q2);
2   input clk, rst;
3   output Q0, Q1, Q2;
4   wire clk, rst;
5   wire Q0, Q1, Q2;
6   wire n_0, n_1, n_2, n_3, n_4, n_5, n_6;
7   NR2M2R g259_2398(A {n_5}), .B(rst), .Z(n_6);
8   AO132M2R g261_5107(.A1(Q0)), .A2(n_0), .A3(Q1), .B1(n_4), .B2
9   (Q2), .Z(n_5);
10  DFQ2RA \count_reg[0] (.CK(clk), .D(n_3), .Q(Q0));
11  AOI211M2R g263_6260(.A1(n_2), .A2(Q2), .B(Q0), .C(rst), .Z
12  (n_3));
13  MXB2H1RA g264_4319(.A(n_2), .B(Q1), .S(Q0), .Z(n_4));
14  CK1INV2R g267(.A(rst), .Z(n_1));
15  DF2RM2RA \count_reg[1] (.CK(clk), .D(n_1), .RB(n_4), .Q(Q1), .QB
16  (n_2));
17  DFMR2RA \count_reg[2] (.CK(clk), .D(n_6), .Q(Q2), .QB(n_0));
18 endmodule
20

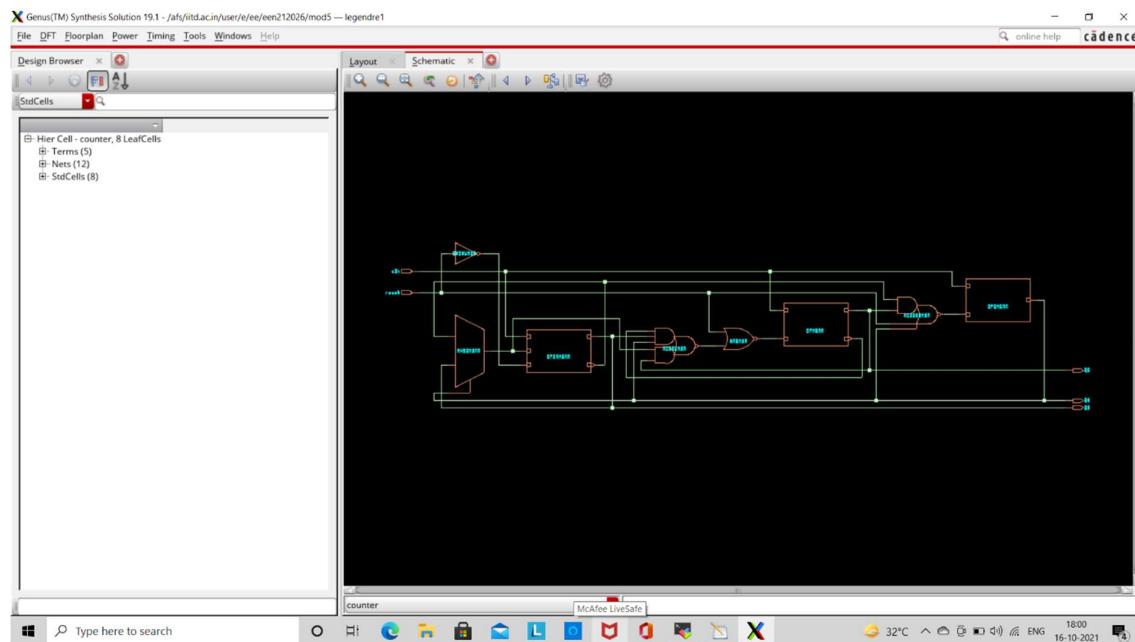
```

SDC FILE GENERATED BY GENUS



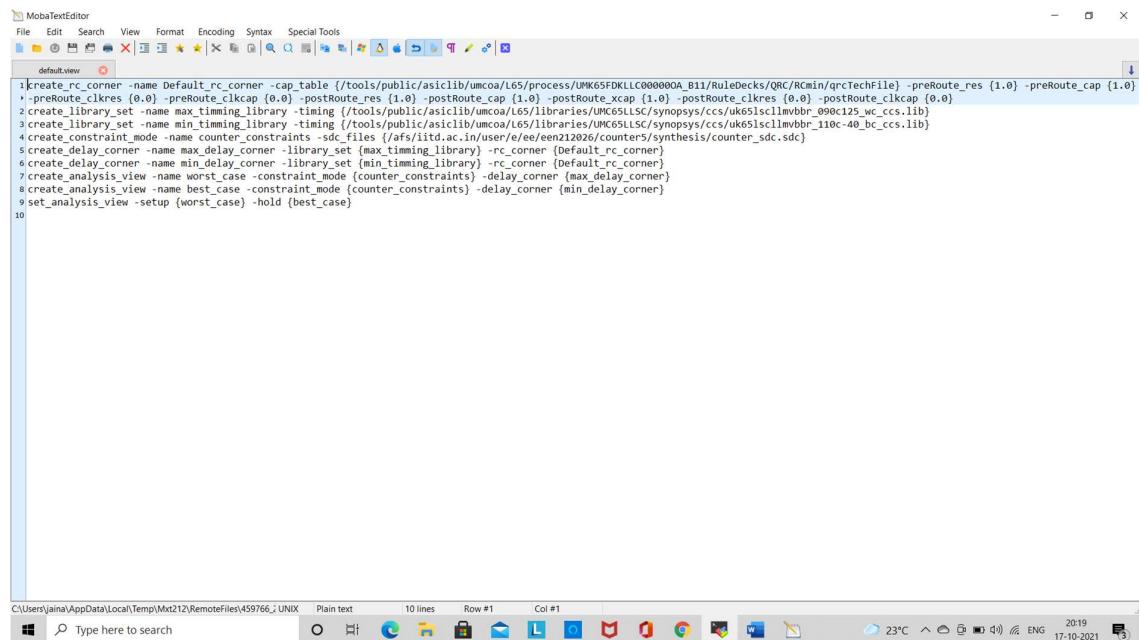
```
1 # #####  
2  
3 # Created by Genus(TM) Synthesis Solution 19.12-s121_1 on Sun Oct 17 00:48:19 IST 2021  
4  
5 # #####  
6  
7 set sdc_version 2.0  
8  
9 set_units -capacitance 1000ff  
10 set_units -time 1000ps  
11  
12 # Set the current design  
13 current_design counter  
14  
15 create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]  
16 set_clock_transition 0.1 [get_clocks clk]  
17 set_clock_gating_check -setup 0.0  
18 set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports rst]  
19 set_wire_load_mode "top"  
20
```

● GENUS SCHEMATIC



PHYSICAL DESIGN IN INNOVUS

- **MMMC FILE USED(.view)**

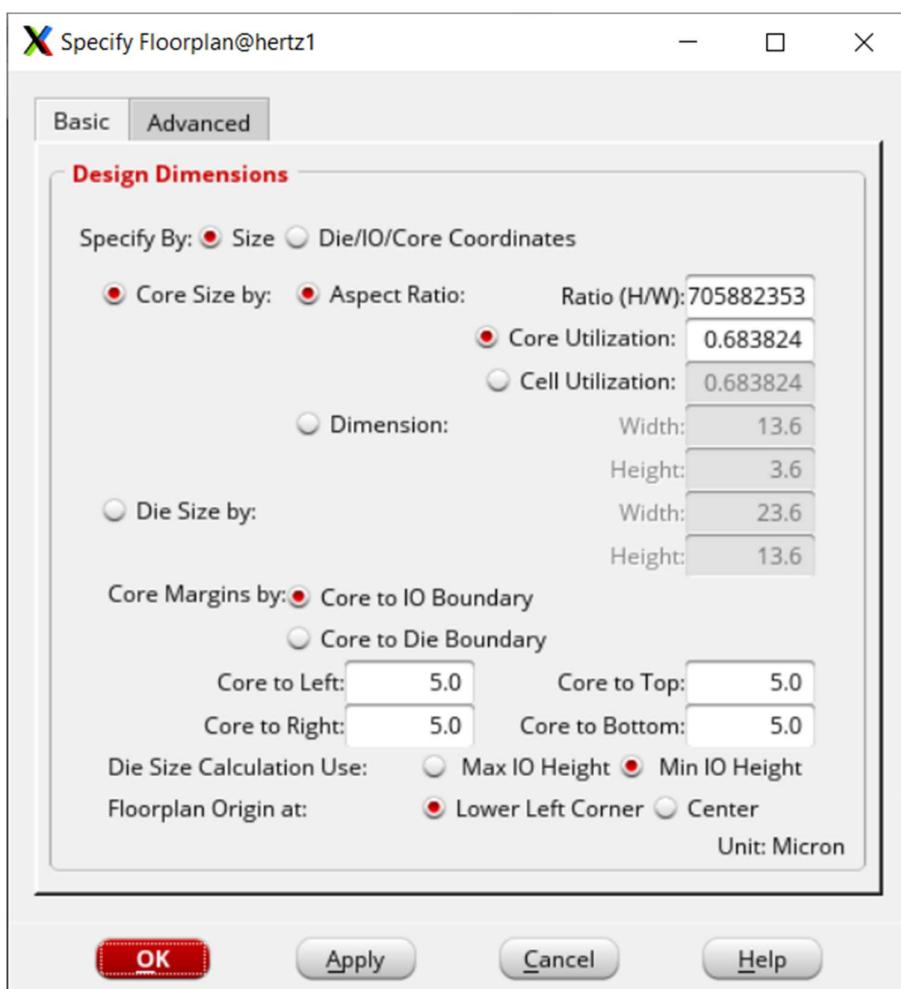


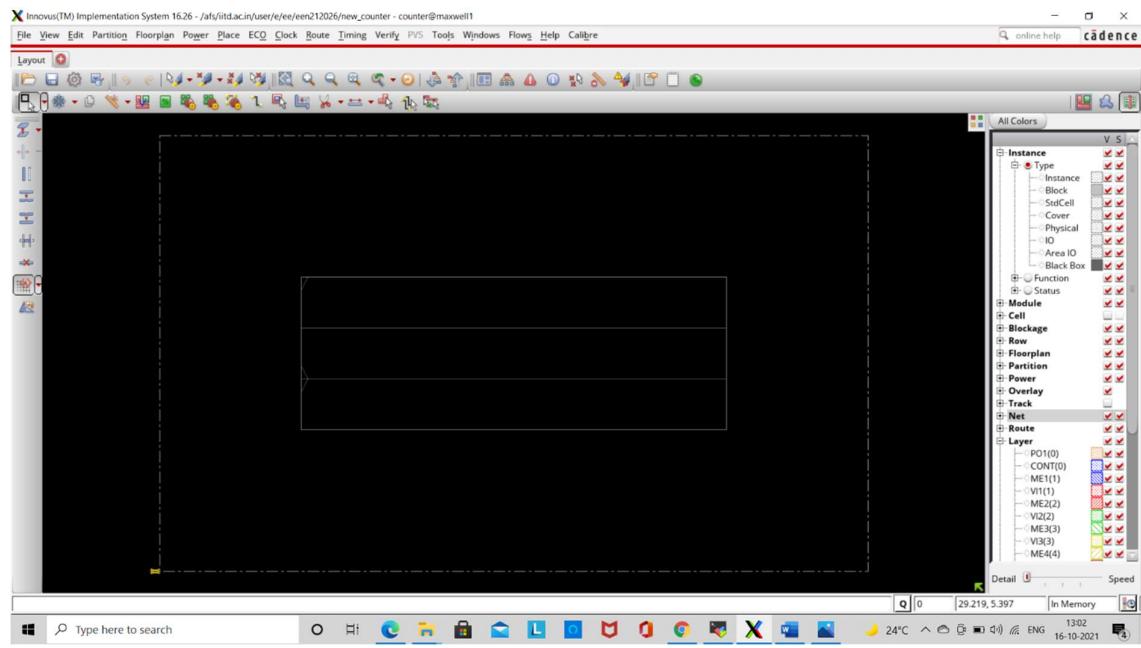
The screenshot shows a MobaTextEditor window displaying a text file named "default.view". The file contains the following content:

```
1#create_rc_corner -name Default_rc_Corner -cap_table {/tools/public/asiclib/umcos/lcs/process/UMCG5FDKLLC000000A_E11/RuleDecks/QPC/QCmin/qrcTechFile} -preroute_res {1.0} -preRoute_cap {1.0}
2:-preRoute_clkres {0.0} -preRoute_clkcap {0.0} -postRoute_res {1.0} -postRoute_cap {1.0} -postRoute_clkres {0.0} -postRoute_clkcap {0.0}
3:create_library_set -name min_timing_library -timing {/tools/public/asiclib/umcos/lss/libraries/UMCG5LSC/synopsys/ccs/uks61sc11mwbrr_090c125_wc_ccs.lib}
4:create_constraint_mode -name counter_constraints -sdc_files {/afs/iitd.ac.in/user/e/ee/eon212026/counters/synthesis/counter_sdc.sdc}
5:create_delay_corner -name max_delay_corner -library_set {max_timing_library} -rc_corner {Default_rc_Corner}
6:create_delay_corner -name min_delay_corner -library_set {min_timing_library} -rc_corner {Default_rc_Corner}
7:create_analysis_view -name worst_case -constraint_mode {counter_constraints} -delay_corner {max_delay_corner}
8:create_analysis_view -name best_case -constraint_mode {counter_constraints} -delay_corner {min_delay_corner}
9;set_analysis_view -setup {worst_case} -hold {best_case}
```

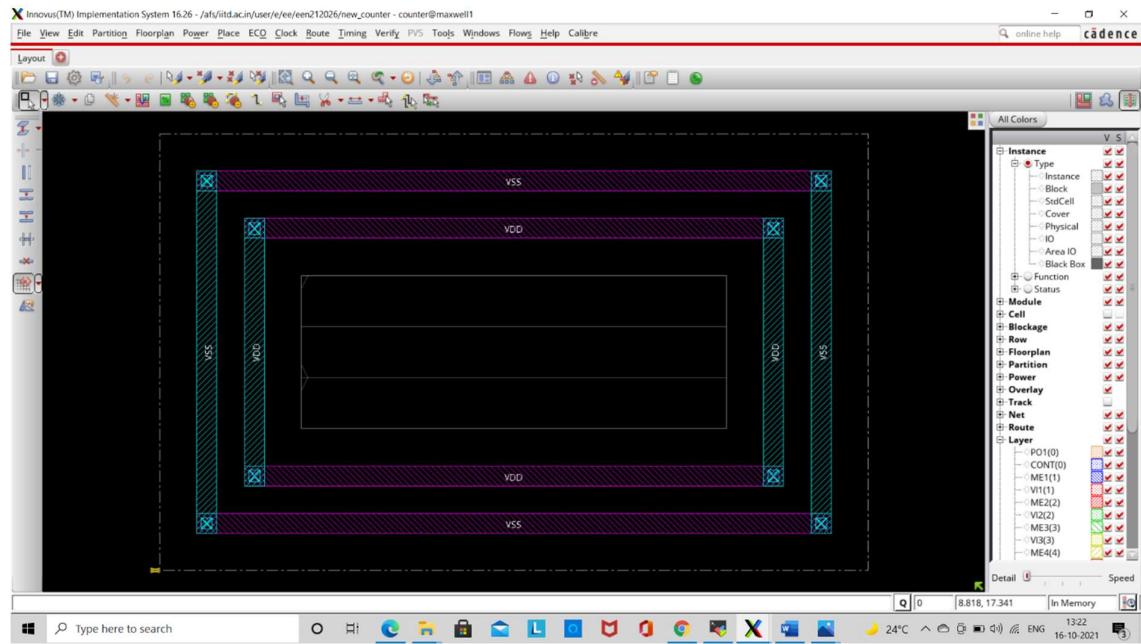
The code defines various synthesis parameters such as route constraints, timing libraries, and analysis views.

- FLOORPLANNING IN INNOVUS

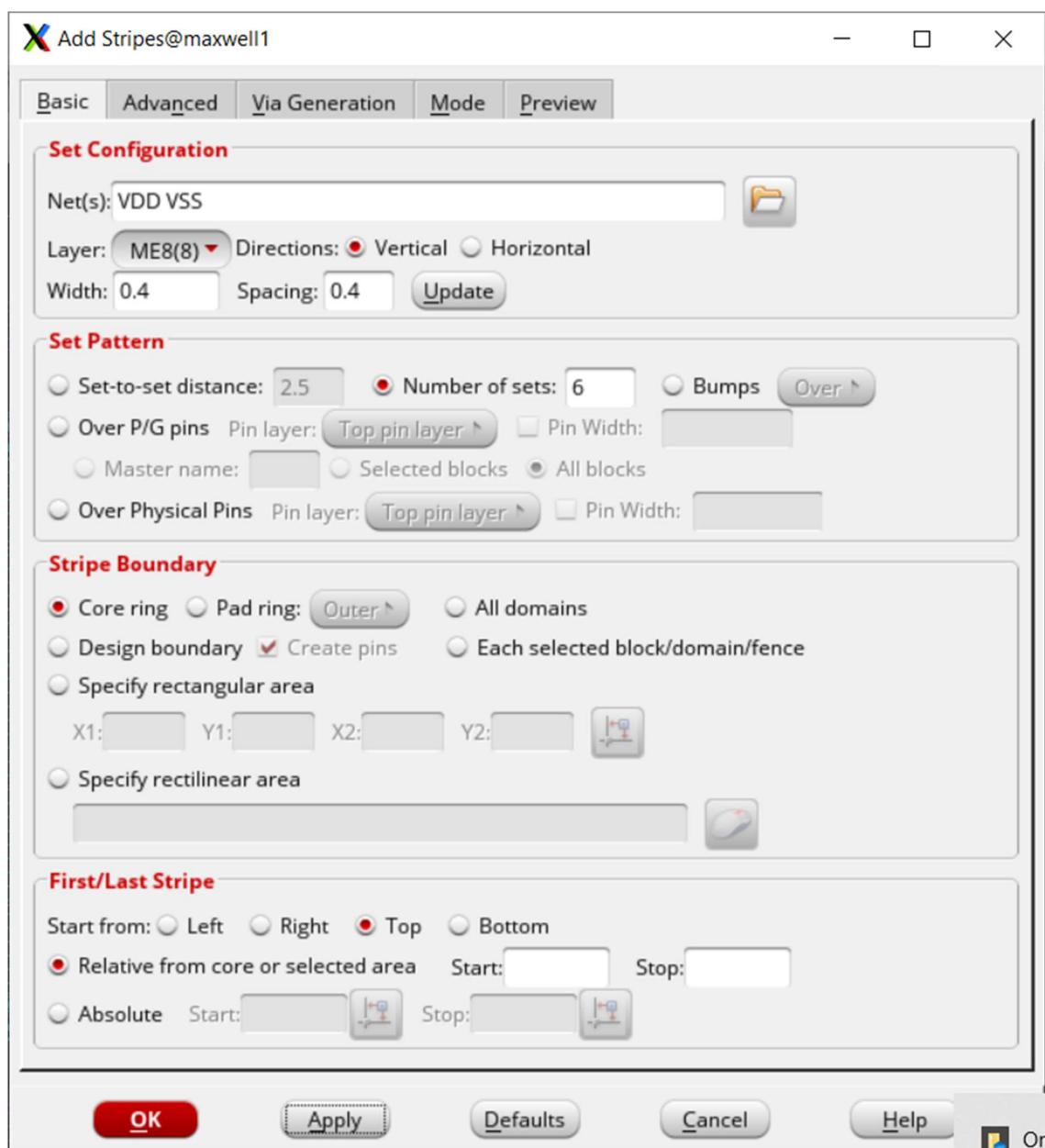




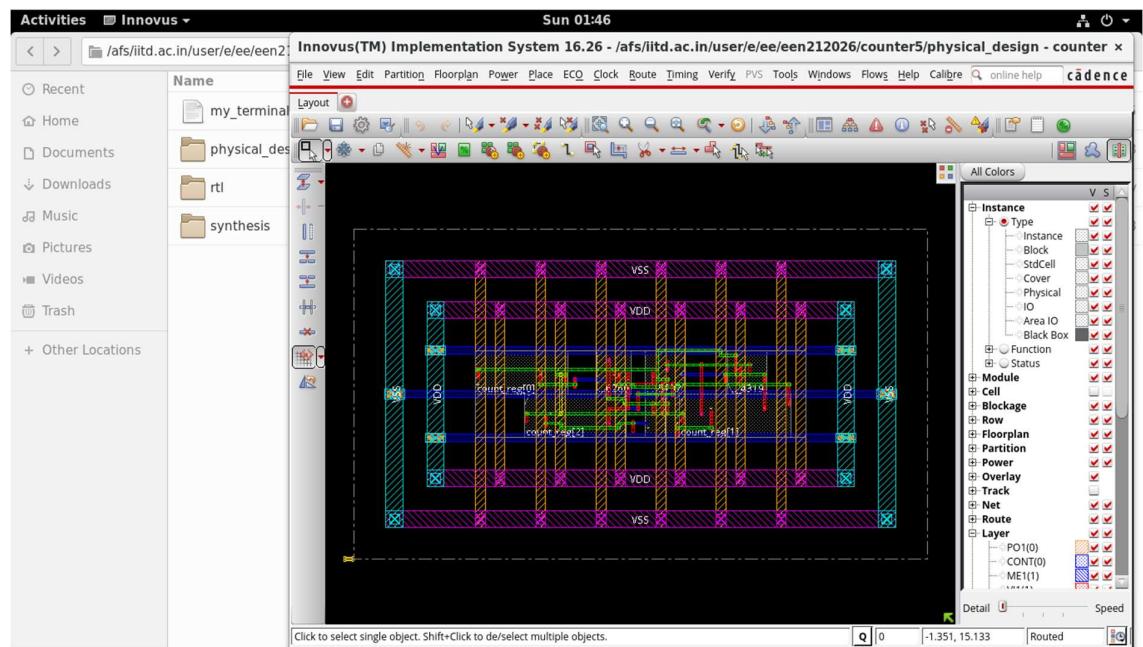
● ADDING POWER RINGS



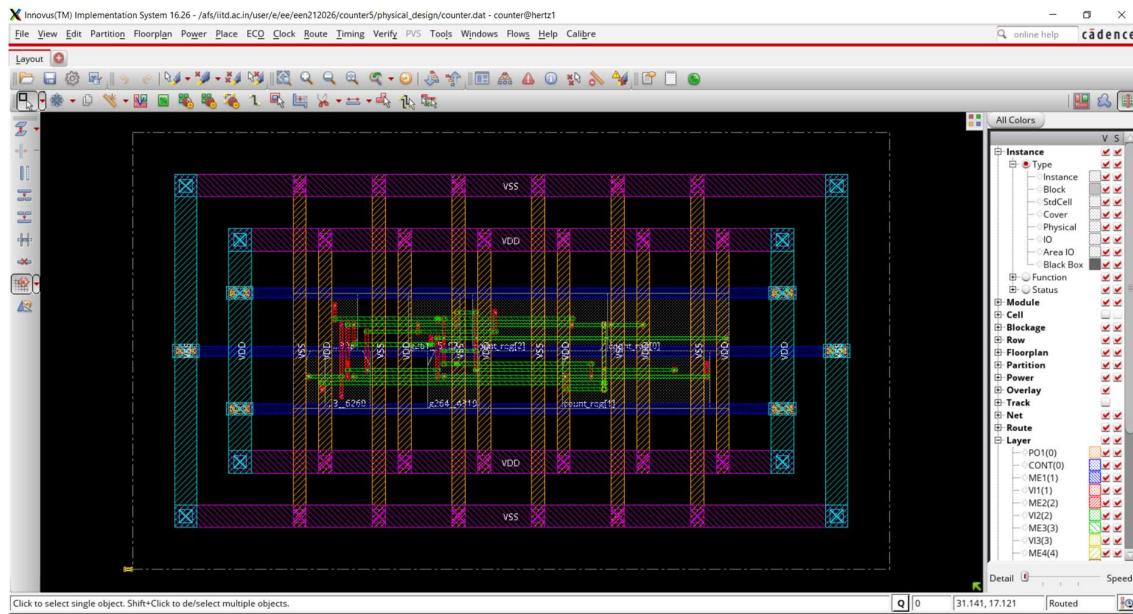
- ADDING POWER STRIPES



- ROUTING (---> SPECIAL ROUTING) AND PLACING STANDARD CELLS



● NANO ROUTING



● TIMING REPORT

timeDesign Summary

Hold views included:

best_case

+-----+	+-----+	+-----+
Hold mode all reg2reg default		
+-----+	+-----+	+-----+
WNS (ns) : 0.095 0.095 0.000		
TNS (ns): 0.000 0.000 0.000		

Violating Paths:	0	0	0	
All Paths:	3	3	0	
+-----+-----+-----+-----+				

Density: 68.382%

Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports

Total CPU time: 0.74 sec

Total Real time: 0.0 sec

Total Memory Usage: 1937.765625 Mbytes

timeDesign Summary

Setup views included:

worst_case

+-----+-----+-----+-----+				
Setup mode	all	reg2reg	default	
+-----+-----+-----+-----+				
WNS (ns):	8.829	9.198	8.829	
TNS (ns):	0.000	0.000	0.000	
Violating Paths:	0	0	0	
All Paths:	4	3	3	
+-----+-----+-----+-----+				

+-----+-----+-----+			
	Real	Total	
+-----+-----+-----+			
DRVs			

	Nr nets(terms)	Worst Vio	Nr nets(terms)	
max_cap	0 (0)	0.000	0 (0)	
max_tran	0 (0)	0.000	0 (0)	
max_fanout	0 (0)	0	0 (0)	
max_length	0 (0)	0	0 (0)	

Density: 68.382%

Routing Overflow: 0.00% H and 0.00% V

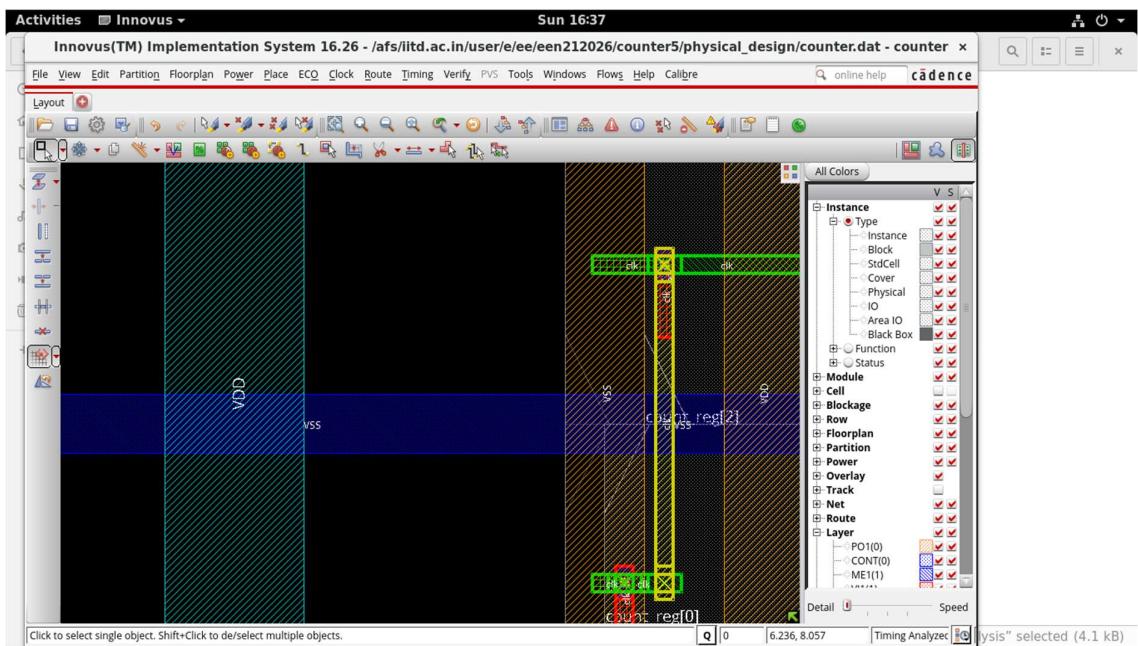
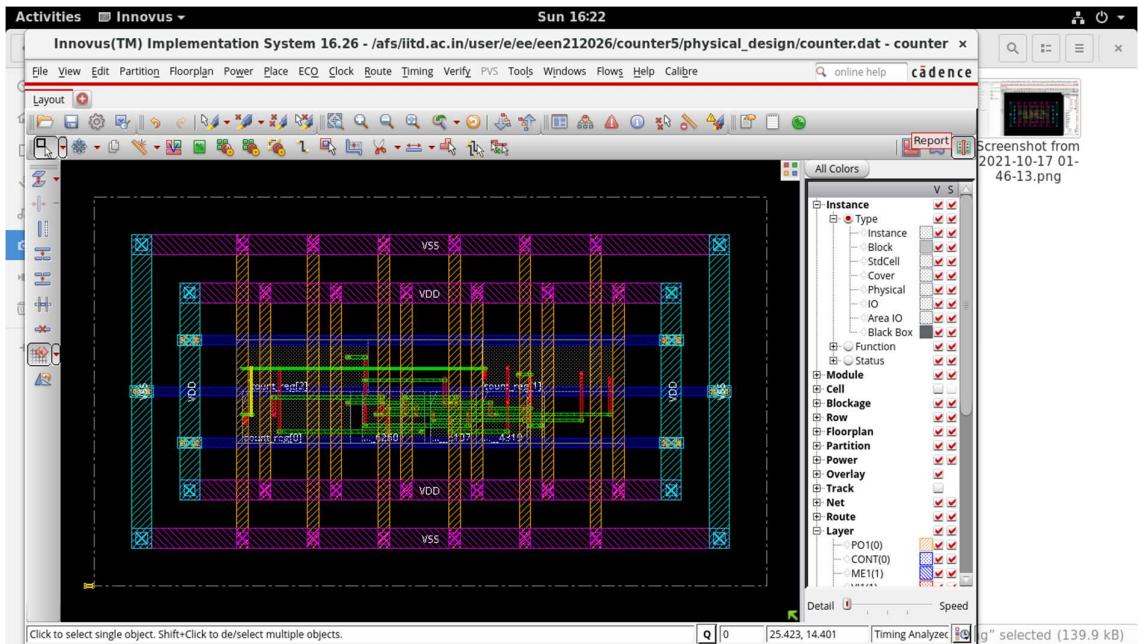
Reported timing to dir timingReports

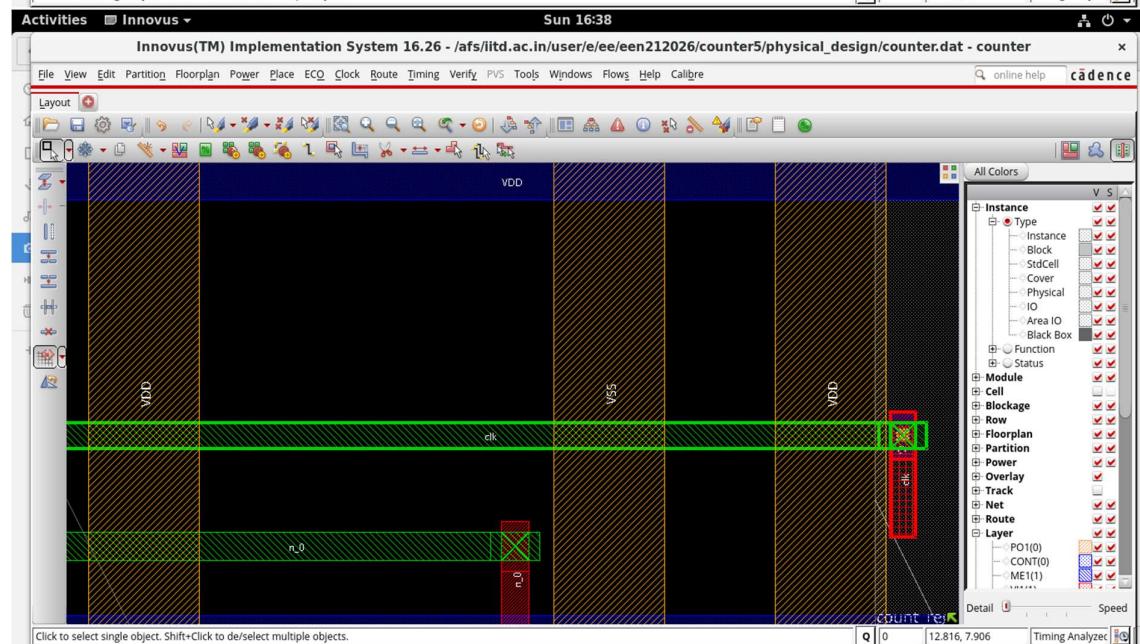
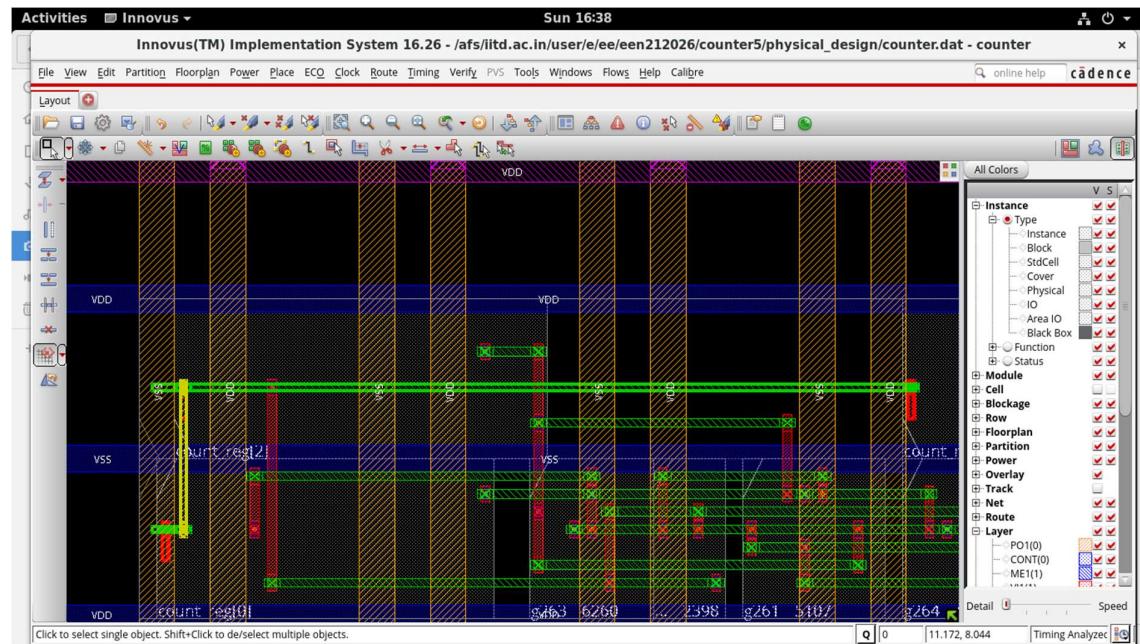
Total CPU time: 0.71 sec

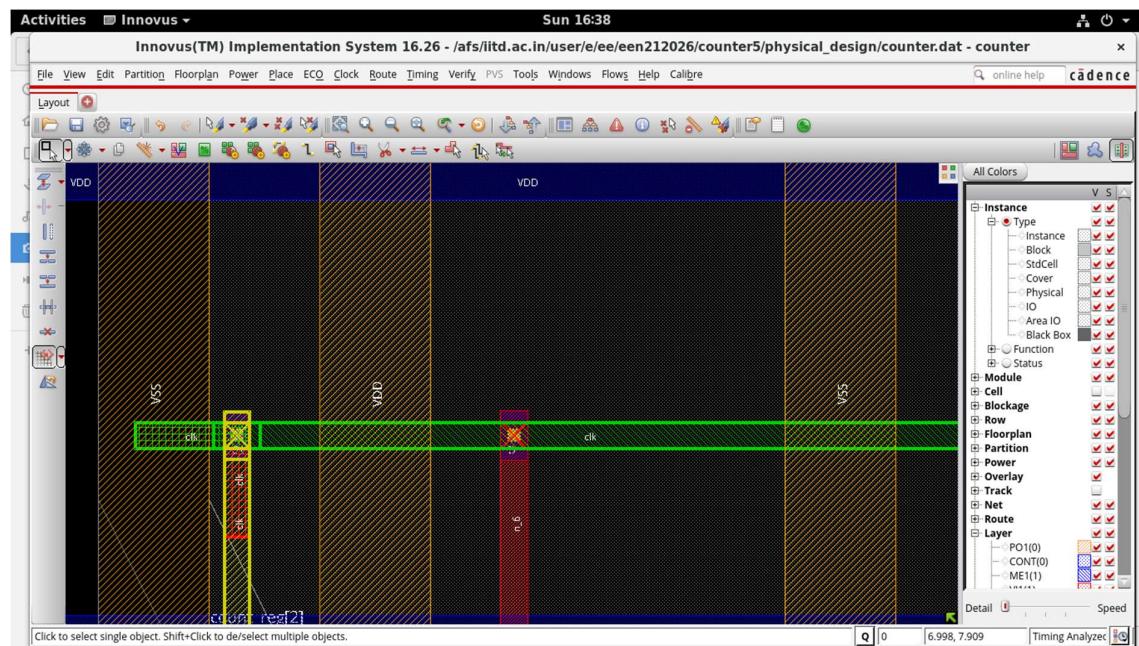
Total Real time: 1.0 sec

Total Memory Usage: 1956.921875 Mbytes

- AFTER CLOCK TREE SYNTHESIS







- TIMING REPORT AFTER CTS

```
-----  
timeDesign Summary  
-----  
Setup views included:  
worst_case  
+  
+-----+-----+-----+-----+  
| Setup mode | all | reg2reg | default |  
+-----+-----+-----+-----+  
| WNS (ns): | 8.795 | 9.208 | 8.795 |  
| TNS (ns): | 0.000 | 0.000 | 0.000 |  
| Violating Paths: | 0 | 0 | 0 |  
| All Paths: | 4 | 3 | 3 |  
+-----+-----+-----+-----+  
+-----+-----+-----+-----+  
| DRVs | Real | Total |  
| | Nr nets(terms) | Worst Vio | Nr nets(terms)  
+-----+-----+-----+-----+  
| max_cap | 0 (0) | 0.000 | 0 (0) |  
| max_tran | 0 (0) | 0.000 | 0 (0) |  
| max_fanout | 0 (0) | 0 | 0 (0) |  
| max_length | 0 (0) | 0 | 0 (0) |  
+-----+-----+-----+-----+  
Density: 68.382%
```

```
File Edit View Search Terminal Help
Total number of fetched objects 12
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End' delay calculation. (MEM=2297.51 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.5 real=0:00:01.0 totSessionCpu=0:09:54 mem=2297.5M)

-----
timeDesign Summary
-----
23
4Hold views included:
best_case

+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+
|          WNS (ns): 0.092 | 0.092 | 0.000 |
|          TNS (ns): 0.000 | 0.000 | 0.000 |
| Violating Paths: 0 | 0 | 0 |
| All Paths: 3 | 3 | 0 |
+-----+-----+-----+

Density: 68.382%
Routing Overflow: 0.00% H and 0.00% V

-----
Reported timing to dir timingReports
Total CPU time: 0.89 sec
Total Real time: 1.0 sec
Total Memory Usage: 2220.125 Mbytes
innovus 3> 
```

- POWER ANALYSIS

```

MobaTextEditor
File Edit Search View Format Encoding Syntax Special Tools
power_analysis
1 **ccept_design ... cpu = 0:00:25, real = 0:00:25, mem = 2309.1M, totSessionCpu=0:15:25 **
2 innovus 4> innovus 4> report_power
3
4 Power Net Detected:
5   Voltage Name
6   0.00V VSS
7   0.90V VDD
8
9 Begin Power Analysis
10
11   0.00V VSS
12   0.90V VDD
13
14 Begin Static Power Report Generation
15 -----
16 * Innovus 16.26-s040_1 (64bit) 03/14/2018 00:26 (Linux 2.6.18-194.el5)
17 *
18 *
19 * Date & Time: 2021-Oct-17 16:31:20 (2021-Oct-17 11:01:20 GMT)
20 *
21 *
22 *
23 * Design: counter
24 *
25 * Liberty Libraries used:
26 *   worst_case: /afs/iitd.ac.in/user/e/een212026/counters/physical_design/counter.dat/libs/lib/typ/uk65lscllmvbbr_090c125_wc_ccs.lib
27 *
28 * Power Domain used:
29 *
30 *   Power View : worst_case
31 *
32 *   User-Defined Activity : N.A.
33 *
34 *   Activity File: N.A.
35 *
36 *   Hierarchical Global Activity: N.A.
37 *
38 *   Global Activity: N.A.
39 *
40 *   Sequential Element Activity: 0.200000
C:\Users\jaina\AppData\Local\Temp\Myx212\RemoteFiles\459766_1.UNIX Plain text 106 lines Row #93 Col #66
Windows Type here to search 23°C ENG 19:38 17-10-2021

MobaTextEditor
File Edit Search View Format Encoding Syntax Special Tools
power_analysis
40 * Sequential Element Activity: 0.200000
41 * Primary Input Activity: 0.200000
42 *
43 *
44 * Default icg ratio: N.A.
45 *
46 * Global Comb ClockGate Ratio: N.A.
47 *
48 * Power Units = 1mW
49 *
50 * Time Units = 1e-09 secs
51 *
52 * report_power
53 *
54 *
55 *
56 *
57 Total Power
58 -----
59 Total Internal Power: 0.00167713 91.7823%
60 Total Switching Power: 0.00014353 7.8549%
61 Total Leakage Power: 0.00000663 0.3629%
62 Total Power: 0.00182729
63 *
64 *
65 *
66 Group Internal Power Switching Power Leakage Power Total Power (%) Percentage
67 *
68 -----
69 Sequential 0.001557 8.418e-05 5.003e-06 0.001647 90.12
70 Macro 0 0 0 0 0 0
71 IO 0 0 0 0 0 0
72 Combinational 0.0001196 5.935e-05 1.628e-06 0.0001806 9.884
73 Clock (Combinational) 0 0 0 0 0 0
74 Clock (Sequential) 0 0 0 0 0 0
75 *
76 Total 0.001677 0.0001435 6.63e-06 0.001827 100
77 *
78 *
79
C:\Users\jaina\AppData\Local\Temp\Myx212\RemoteFiles\459766_2.UNIX Plain text 106 lines Row #93 Col #66
Windows Type here to search 23°C ENG 19:39 17-10-2021

```

```

File Edit Search View Format Encoding Syntax Special Tools
power_analysis

67
68 Sequential          Power    Power    Power    Power (%) 
69   0.001557 8.418e-05 5.003e-06 0.001647 90.12
70 I/O                 0         0         0         0         0
71 IO                 0         0         0         0         0
72 Combinational       0.0001196 5.935e-05 1.628e-06 0.0001806 9.884
73 Clock (Combinational) 0         0         0         0         0
74 Clock (Sequential) 0         0         0         0         0
75
76 Total               0.001677 0.0001435 6.63e-06 0.001827 100
77
78
79 Rail                Voltage Internal Switching Leakage Total Percentage
80   Rail              Power   Power   Power   Power (%) 
81   Default           0.9     0.001677 0.0001435 6.63e-06 0.001827 100
82
83
84
85
86
87 ** Power Distribution Summary:
88 *   Highest Average Power:      count_reg[1] (DFZRM2RA):  0.0005616
89 *   Highest Leakage Power:     count_reg[2] (DFM2RA):  1.868e-06
90 *   Total Cap: 1.6496e-14 F
91 *   Total instances in design:  8
92 *   Total instances in design with no power:  0
93 *   Total instances in design with no activity:  0
94
95 *   Total Fillers and Decap:  0
96
97
98 ** WARN: (VOLTUS_POWR-2041): There are some instances in the design which are not connected to any power or ground nets.
99 These instances will be added to default power/ground rail uti files.
100 Use 'itaputil list <uti-file>' command to get the list of instances.
101
102 Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
103 mem(process/total)=1526.47MB/1526.47MB)
104
105
106

```

C:\Users\jaina\AppData\Local\Temp\lMxt212\RemoteFiles\459766_2 UNIX Plain text 106 lines Row #105 Col #1

Windows Start Task View File Explorer Mail Edge Microsoft Store Microsoft Edge Google Chrome Paint Photos File History 23°C ENG 19:39 17-10-2021

****ALL FILES USED ABOVE ARE PRESENT IN THE GIVEN PATH****

"/afs/iitd.ac.in/user/e/ee/een212026/counter5/"

****INNOVUS LOG FILE*****

"/afs/iitd.ac.in/user/e/ee/een212026/counter5/physical_design/innovus.log1"