```
##################################################
##                              ##
##      C A L I B R E   S Y S T E M      ##
##                              ##
##         L V S   R E P O R T          ##
##                              ##
##################################################
```

REPORT FILE NAME: counter.lvs.report

LAYOUT NAME: /afs/iitd.ac.in/user/e/ee/een212026/ieclab_21/lvs/counter.sp ('counter')

SOURCE NAME: /afs/iitd.ac.in/user/e/ee/een212026/ieclab_21/lvs/counter.src.net ('counter')

RULE FILE: /afs/iitd.ac.in/user/e/ee/een212026/ieclab_21/lvs/___G-DF-LOGIC_MIXED_MODE65N-LL_LOW_K_CALIBRE-LVS-1.6-P4.txt___

RULE FILE TITLE: UMC Calibre LVS 65nm LOGIC/MIXED MODE Low Leakage Low-K Process

CREATION TIME: Sat Sep 25 11:42:24 2021

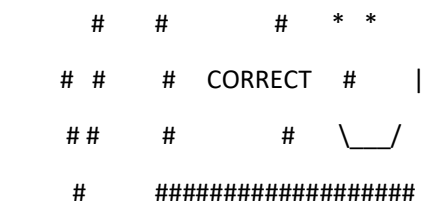
CURRENT DIRECTORY: /afs/iitd.ac.in/user/e/ee/een212026/ieclab_21/lvs

USER NAME: een212026

CALIBRE VERSION: v2020.4_34.17 Tue Dec 1 16:11:11 PST 2020

OVERALL COMPARISON RESULTS

```
#     ###################     _ _
```



****

CELL SUMMARY

****

Result	Layout	Source
CORRECT	counter	counter

****

LVS PARAMETERS

****

o LVS Setup:

// LVS COMPONENT TYPE PROPERTY

// LVS COMPONENT SUBTYPE PROPERTY

// LVS PIN NAME PROPERTY

```
LVS POWER NAME                  "?VCC?" "?VDD?"
LVS GROUND NAME                 "?GND?" "?VSS?"
LVS CELL SUPPLY                 NO
LVS RECOGNIZE GATES             ALL
// LVS HCELL REPORT
LVS IGNORE PORTS                NO
LVS CHECK PORT NAMES            YES
LVS IGNORE TRIVIAL NAMED PORTS  NO
LVS BUILTIN DEVICE PIN SWAP     NO
LVS ALL CAPACITOR PINS SWAPPABLE NO
LVS DISCARD PINS BY DEVICE      NO
LVS SOFT SUBSTRATE PINS         NO
LVS INJECT LOGIC                NO
LVS EXPAND UNBALANCED CELLS     YES
LVS FLATTEN INSIDE CELL         NO
LVS EXPAND SEED PROMOTIONS      YES
LVS PRESERVE PARAMETERIZED CELLS NO
LVS GLOBALS ARE PORTS           YES
LVS REVERSE WL                  NO
LVS SPICE PREFER PINS           NO
LVS SPICE SLASH IS SPACE        YES
LVS SPICE ALLOW FLOATING PINS   YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS NO
LVS SPICE CONDITIONAL LDD       NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS NO
// LVS SPICE EXCLUDE CELL SOURCE
// LVS SPICE EXCLUDE CELL LAYOUT
LVS SPICE IMPLIED MOS AREA      NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS      NO
```

LVS SPICE REDEFINE PARAM NO

LVS SPICE REPLICATE DEVICES YES

LVS SPICE SCALE X PARAMETERS NO

LVS SPICE STRICT WL NO

// LVS SPICE OPTION

LVS STRICT SUBTYPES NO

LVS EXACT SUBTYPES NO

LAYOUT CASE NO

SOURCE CASE NO

LVS COMPARE CASE NO

LVS COMPARE CASE STRICT NO

LVS DOWNCASE DEVICE NO

LVS REPORT MAXIMUM 50

LVS PROPERTY RESOLUTION MAXIMUM 32

// LVS SIGNATURE MAXIMUM

// LVS FILTER UNUSED OPTION

// LVS REPORT OPTION

LVS REPORT UNITS YES

// LVS NON USER NAME PORT

// LVS NON USER NAME NET

// LVS NON USER NAME INSTANCE

// LVS IGNORE DEVICE PIN

// LVS PREFER NETS FILTER SOURCE

// LVS PREFER NETS FILTER LAYOUT

LVS PREFER PORT NETS NO

LVS EXPAND ON ERROR NO

// Reduction

LVS REDUCE SERIES MOS NO

LVS REDUCE PARALLEL MOS YES

```
LVS REDUCE SEMI SERIES MOS            NO
LVS REDUCE SPLIT GATES                YES
LVS REDUCE PARALLEL BIPOLAR           YES
LVS REDUCE SERIES CAPACITORS          YES
LVS REDUCE PARALLEL CAPACITORS        YES
LVS REDUCE SERIES RESISTORS           YES
LVS REDUCE PARALLEL RESISTORS         YES
LVS REDUCE PARALLEL DIODES            YES

LVS REDUCE  C(MIMCAPS_20F_MM)  PARALLEL NO
LVS REDUCE  C(NCAP_12_LL)  PARALLEL NO
LVS REDUCE  C(PCAP_12_LL)  PARALLEL NO
LVS REDUCE  C(NCAP_25_LL)  PARALLEL NO
LVS REDUCE  C(PCAP_25_LL)  PARALLEL NO
LVS REDUCTION PRIORITY                PARALLEL

LVS SHORT EQUIVALENT NODES            NO

// Trace Property

TRACE PROPERTY  n_12_llrvtrf  lf lf 3
TRACE PROPERTY  n_12_llrvtrf  wf wf 3
TRACE PROPERTY  n_12_llrvtrf  nf nf 0
TRACE PROPERTY  n_12_llrvtrf  con con 0
TRACE PROPERTY  p_12_llrvtrf  lf lf 3
TRACE PROPERTY  p_12_llrvtrf  wf wf 3
TRACE PROPERTY  p_12_llrvtrf  nf nf 0
TRACE PROPERTY  p_12_llrvtrf  con con 0
TRACE PROPERTY  n_bpw_12_llrvtrf  lf lf 3
TRACE PROPERTY  n_bpw_12_llrvtrf  wf wf 3
TRACE PROPERTY  n_bpw_12_llrvtrf  nf nf 0
```

TRACE PROPERTY n_bpw_12_llrvtrf con con 0

TRACE PROPERTY n_12_llhvtrf lf lf 3

TRACE PROPERTY n_12_llhvtrf wf wf 3

TRACE PROPERTY n_12_llhvtrf nf nf 0

TRACE PROPERTY n_12_llhvtrf con con 0

TRACE PROPERTY p_12_llhvtrf lf lf 3

TRACE PROPERTY p_12_llhvtrf wf wf 3

TRACE PROPERTY p_12_llhvtrf nf nf 0

TRACE PROPERTY p_12_llhvtrf con con 0

TRACE PROPERTY n_bpw_12_llhvtrf lf lf 3

TRACE PROPERTY n_bpw_12_llhvtrf wf wf 3

TRACE PROPERTY n_bpw_12_llhvtrf nf nf 0

TRACE PROPERTY n_bpw_12_llhvtrf con con 0

TRACE PROPERTY n_12_lllvtrf lf lf 3

TRACE PROPERTY n_12_lllvtrf wf wf 3

TRACE PROPERTY n_12_lllvtrf nf nf 0

TRACE PROPERTY n_12_lllvtrf con con 0

TRACE PROPERTY p_12_lllvtrf lf lf 3

TRACE PROPERTY p_12_lllvtrf wf wf 3

TRACE PROPERTY p_12_lllvtrf nf nf 0

TRACE PROPERTY p_12_lllvtrf con con 0

TRACE PROPERTY n_bpw_12_lllvtrf lf lf 3

TRACE PROPERTY n_bpw_12_lllvtrf wf wf 3

TRACE PROPERTY n_bpw_12_lllvtrf nf nf 0

TRACE PROPERTY n_bpw_12_lllvtrf con con 0

TRACE PROPERTY n_25_llrf lf lf 3

TRACE PROPERTY n_25_llrf wf wf 3

TRACE PROPERTY n_25_llrf nf nf 0

TRACE PROPERTY n_25_llrf con con 0

TRACE PROPERTY p_25_llrf lf lf 3

TRACE PROPERTY p_25_llrf wf wf 3

TRACE PROPERTY p_25_llrf nf nf 0

TRACE PROPERTY p_25_llrf con con 0

TRACE PROPERTY n_bpw_25_llrf lf lf 3

TRACE PROPERTY n_bpw_25_llrf wf wf 3

TRACE PROPERTY n_bpw_25_llrf nf nf 0

TRACE PROPERTY n_bpw_25_llrf con con 0

TRACE PROPERTY r(rsnpo_efuse) r r 3

TRACE PROPERTY r(rsppo_efuse) r r 3

TRACE PROPERTY rnnpo_nw_llrf r r 3

TRACE PROPERTY rnnpo_nw_llrf l l 3

TRACE PROPERTY rnnpo_nw_llrf w w 3

TRACE PROPERTY rnnpo_llrf r r 3

TRACE PROPERTY rnnpo_llrf l l 3

TRACE PROPERTY rnnpo_llrf w w 3

TRACE PROPERTY rnppo_nw_llrf r r 3

TRACE PROPERTY rnppo_nw_llrf l l 3

TRACE PROPERTY rnppo_nw_llrf w w 3

TRACE PROPERTY rnppo_llrf r r 3

TRACE PROPERTY rnppo_llrf l l 3

TRACE PROPERTY rnppo_llrf w w 3

TRACE PROPERTY rnhr_nw_llrf r r 3

TRACE PROPERTY rnhr_nw_llrf l l 3

TRACE PROPERTY rnhr_nw_llrf w w 3

TRACE PROPERTY rnhr_llrf r r 3

TRACE PROPERTY rnhr_llrf l l 3

TRACE PROPERTY rnhr_llrf w w 3

TRACE PROPERTY r(fuse) r r 3

TRACE PROPERTY r(ral) r r 3

TRACE PROPERTY varmis_12_llrf lf lf 3

TRACE PROPERTY varmis_12_llrf wf wf 3

TRACE PROPERTY varmis_12_llrf nf nf 0

TRACE PROPERTY varmis_12_llrf array array 0

TRACE PROPERTY varmis_25_llrf lf lf 3

TRACE PROPERTY varmis_25_llrf wf wf 3

TRACE PROPERTY varmis_25_llrf nf nf 0

TRACE PROPERTY varmis_25_llrf array array 0

TRACE PROPERTY vardiop_llrf l l 3

TRACE PROPERTY vardiop_llrf wp wp 3

TRACE PROPERTY vardiop_llrf nf nf 0

TRACE PROPERTY vardiop_llrf c c 3

TRACE PROPERTY d(dionw_ll) a a 3

TRACE PROPERTY d(dionw_ll) p p 3

TRACE PROPERTY d(diodnw_ll) a a 3

TRACE PROPERTY d(diodnw_ll) p p 3

TRACE PROPERTY d(diodp_ll) a a 3

TRACE PROPERTY d(diodp_ll) p p 3

TRACE PROPERTY momcaps_sy_mmkf nf nf 0

TRACE PROPERTY momcaps_sy_mmkf l l 3

TRACE PROPERTY momcaps_sy_mmkf nm nm 0

TRACE PROPERTY momcaps_sy_mmkf bm bm 0

TRACE PROPERTY momcaps_as_mmkf nf nf 0

TRACE PROPERTY momcaps_as_mmkf l l 3

TRACE PROPERTY momcaps_as_mmkf nm nm 0

TRACE PROPERTY momcaps_as_mmkf bm bm 0

TRACE PROPERTY momcaps_symesh_mmkf nf nf 0

TRACE PROPERTY momcaps_symesh_mmkf mh mh 0

TRACE PROPERTY momcaps_symesh_mmkf nm nm 0

TRACE PROPERTY momcaps_symesh_mmkf bm bm 0

TRACE PROPERTY momcaps_symesh_mmkf l l 3

TRACE PROPERTY momcaps_asmesh_mmkf nf nf 0

TRACE PROPERTY momcaps_asmesh_mmkf mh mh 0

TRACE PROPERTY momcaps_asmesh_mmkf nm nm 0

TRACE PROPERTY momcaps_asmesh_mmkf bm bm 0

TRACE PROPERTY momcaps_asmesh_mmkf l l 3

TRACE PROPERTY momcaps_array_vp3_rfvcl bm bm 0

TRACE PROPERTY momcaps_array_vp3_rfvcl ns ns 0

TRACE PROPERTY momcaps_array_vp3_rfvcl nf nf 0

TRACE PROPERTY momcaps_array_vp3_rfvcl array array 0

TRACE PROPERTY momcaps_array_vp3_rfvcl lf lf 3

TRACE PROPERTY momcaps_array_vp4_rfvcl bm bm 0

TRACE PROPERTY momcaps_array_vp4_rfvcl ns ns 0

TRACE PROPERTY momcaps_array_vp4_rfvcl nf nf 0

TRACE PROPERTY momcaps_array_vp4_rfvcl array array 0

TRACE PROPERTY momcaps_array_vp4_rfvcl lf lf 3

TRACE PROPERTY momcaps_array_vp5_rfvcl bm bm 0

TRACE PROPERTY momcaps_array_vp5_rfvcl ns ns 0

TRACE PROPERTY momcaps_array_vp5_rfvcl nf nf 0

TRACE PROPERTY momcaps_array_vp5_rfvcl array array 0

TRACE PROPERTY momcaps_array_vp5_rfvcl lf lf 3

TRACE PROPERTY momcaps_array_vp5_rfvcl sh sh 0

TRACE PROPERTY l_slcr30k_rfvil s s 3

TRACE PROPERTY l_slcr30k_rfvil w w 3

TRACE PROPERTY l_slcr30k_rfvil od od 3

TRACE PROPERTY l_slcr30k_rfvil nt nt 0

TRACE PROPERTY l_syct30k_rfvil nt nt 0

TRACE PROPERTY l_syct30k_rfvil s s 3

TRACE PROPERTY l_syct30k_rfvil w w 3

TRACE PROPERTY l_syct30k_rfvil od od 3

TRACE PROPERTY l_sy30k_rfvil nt nt 0

TRACE PROPERTY l_sy30k_rfvil s s 3

TRACE PROPERTY l_sy30k_rfvil w w 3

TRACE PROPERTY l_sy30k_rfvil od od 3

TRACE PROPERTY l_sqsk_rfvil nt nt 0

TRACE PROPERTY l_sqsk_rfvil s s 3

TRACE PROPERTY l_sqsk_rfvil w w 3

TRACE PROPERTY l_sqsk_rfvil od od 3

TRACE PROPERTY l_sqsk_rfvil ns ns 0

TRACE PROPERTY l_sqsk_rfvil bm bm 0

TRACE PROPERTY mimcaps_20f_nwell_rfkf l l 3

TRACE PROPERTY mimcaps_20f_nwell_rfkf w w 3

TRACE PROPERTY mimcaps_20f_psub_rfkf l l 3

TRACE PROPERTY mimcaps_20f_psub_rfkf w w 3

TRACE PROPERTY mimcaps_20f_m1_rfkf l l 3

TRACE PROPERTY mimcaps_20f_m1_rfkf w w 3

TRACE PROPERTY c(mimcaps_20f_mm) c c 3

TRACE PROPERTY l_sq_trans_rfvil nt_in nt_in 0

TRACE PROPERTY l_sq_trans_rfvil nt_out nt_out 0

TRACE PROPERTY l_sq_trans_rfvil w w 3

TRACE PROPERTY l_sq_trans_rfvil od od 3

TRACE PROPERTY l_sqctin_trans_rfvil nt_in nt_in 0

TRACE PROPERTY l_sqctin_trans_rfvil nt_out nt_out 0

TRACE PROPERTY l_sqctin_trans_rfvil w w 3

TRACE PROPERTY l_sqctin_trans_rfvil od od 3

TRACE PROPERTY l_sqctout_trans_rfvil nt_in nt_in 0

TRACE PROPERTY l_sqctout_trans_rfvil nt_out nt_out 0

TRACE PROPERTY l_sqctout_trans_rfvil w w 3

TRACE PROPERTY l_sqctout_trans_rfvil od od 3

TRACE PROPERTY l_sqctinout_trans_rfvil nt_in nt_in 0

TRACE PROPERTY l_sqctinout_trans_rfvil nt_out nt_out 0

TRACE PROPERTY l_sqctinout_trans_rfvil w w 3

TRACE PROPERTY l_sqctinout_trans_rfvil od od 3

TRACE PROPERTY l_occtout_trans_rfvil nt_in nt_in 0

TRACE PROPERTY l_occtout_trans_rfvil w w 3

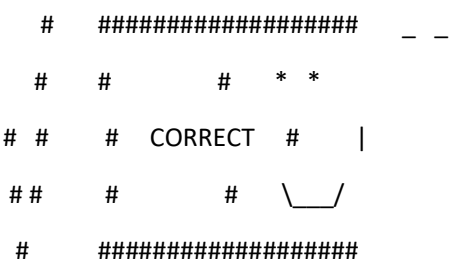
TRACE PROPERTY l_occtout_trans_rfvil od od 3

TRACE PROPERTY pad_rf index_layer index_layer 0

TRACE PROPERTY pad_rf index_thick index_thick 0

TRACE PROPERTY pad_rf index_pad index_pad 0

CELL COMPARISON RESULTS (TOP LEVEL)



LAYOUT CELL NAME: counter

SOURCE CELL NAME: counter

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	9	9	
Nets:	63	63	

Instances:	60	60	MN (4 pins)
	60	60	MP (4 pins)
Total Inst:	120	120	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	9	9	
Nets:	32	32	
Instances:	4	4	INV (2 pins)
	19	19	NAND2 (3 pins)
	6	6	NAND3 (4 pins)
Total Inst:	29	29	

****

INFORMATION AND WARNINGS

****

Matched	Matched	Unmatched	Unmatched	Component

	Layout	Source	Layout	Source	Type
Ports:	9	9	0	0	
Nets:	32	32	0	0	
Instances:	4	4	0	0	INV
	19	19	0	0	NAND2
	6	6	0	0	NAND3
Total Inst:	29	29	0	0	

o Initial Correspondence Points:

Ports: VDD GND QABAR CLK QA QBBAR QC QB QCBAR

o Voltage Names Matched by Wildcard:

Power Names from Layout:

VDD

Ground Names from Layout:

GND

Power Names from Source:

VDD

Ground Names from Source:

GND

****
****

SUMMARY

****
****

Total CPU Time: 0 sec

Total Elapsed Time: 0 sec