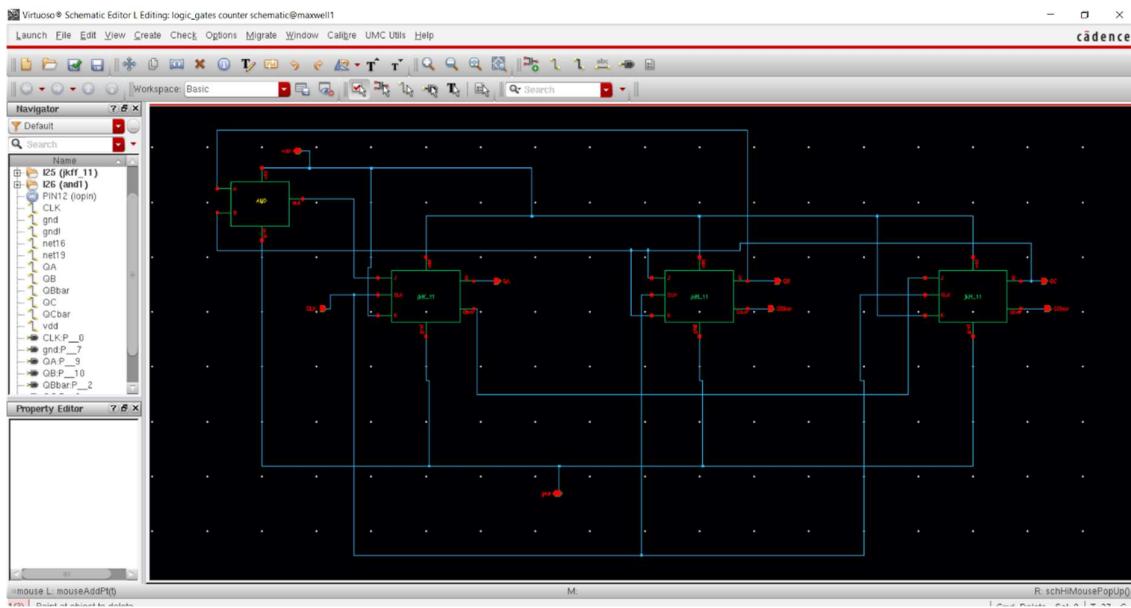
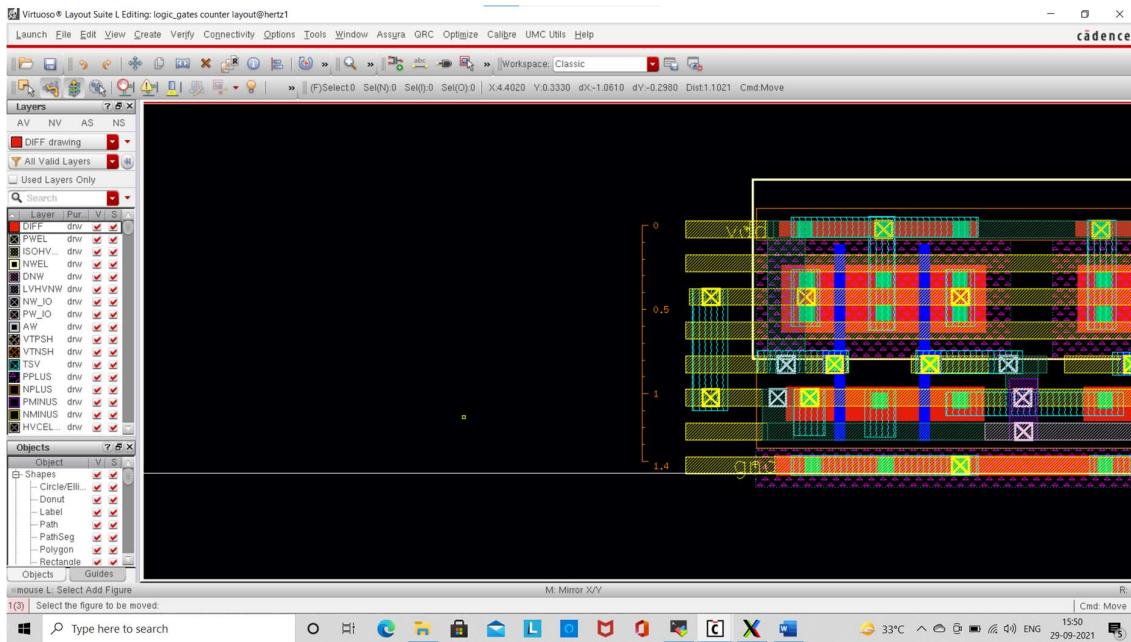
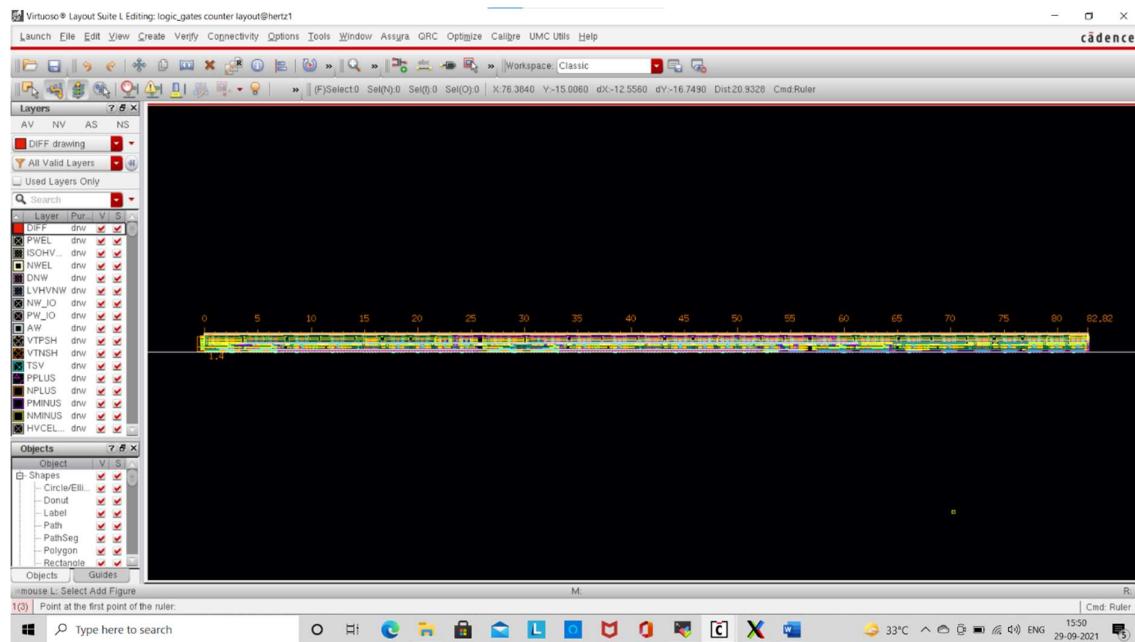


## MOD-5 COUNTER USING JK FLIP FLOP



**Layout with all scales:**



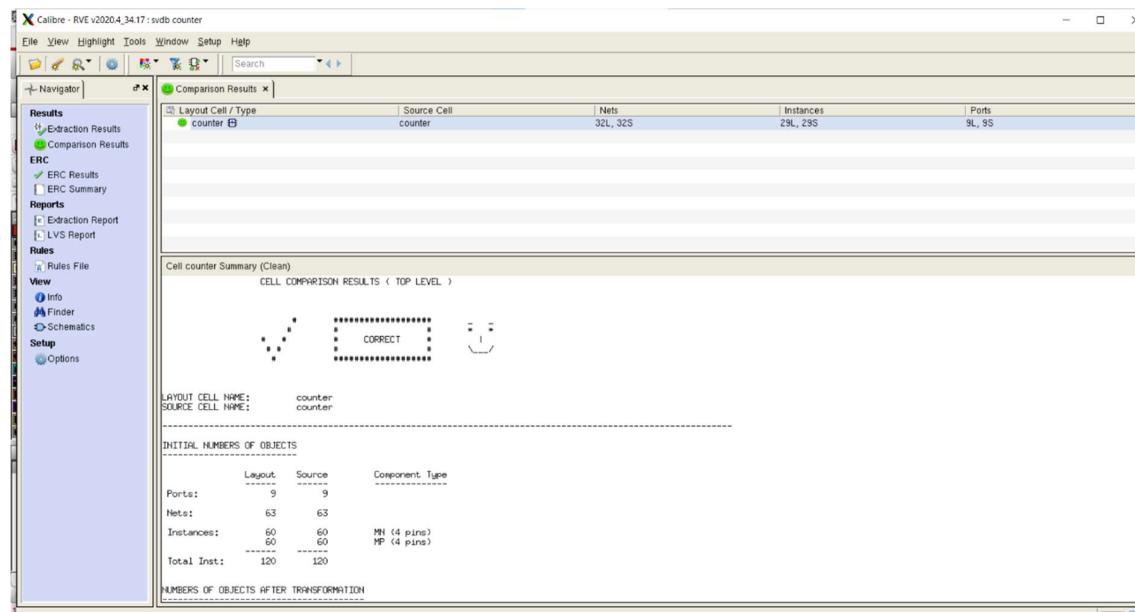


Height = 14um

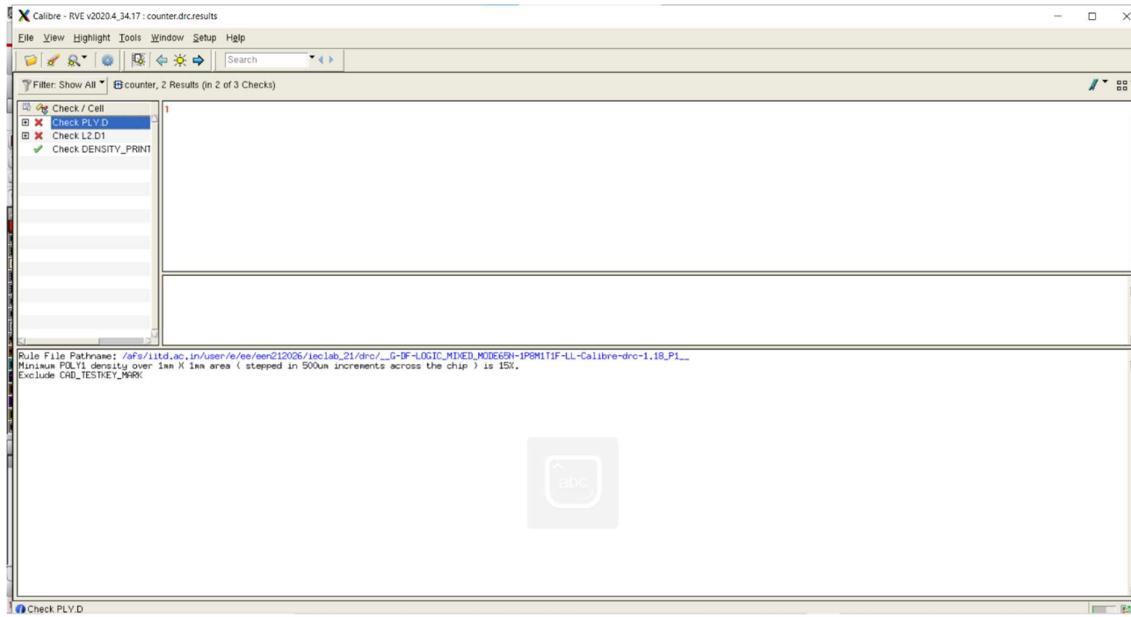
Width (width of N-Well) = 82.82um

Area of layout = 115.948 um sq.

## LVS RESULTS



## DRC Results

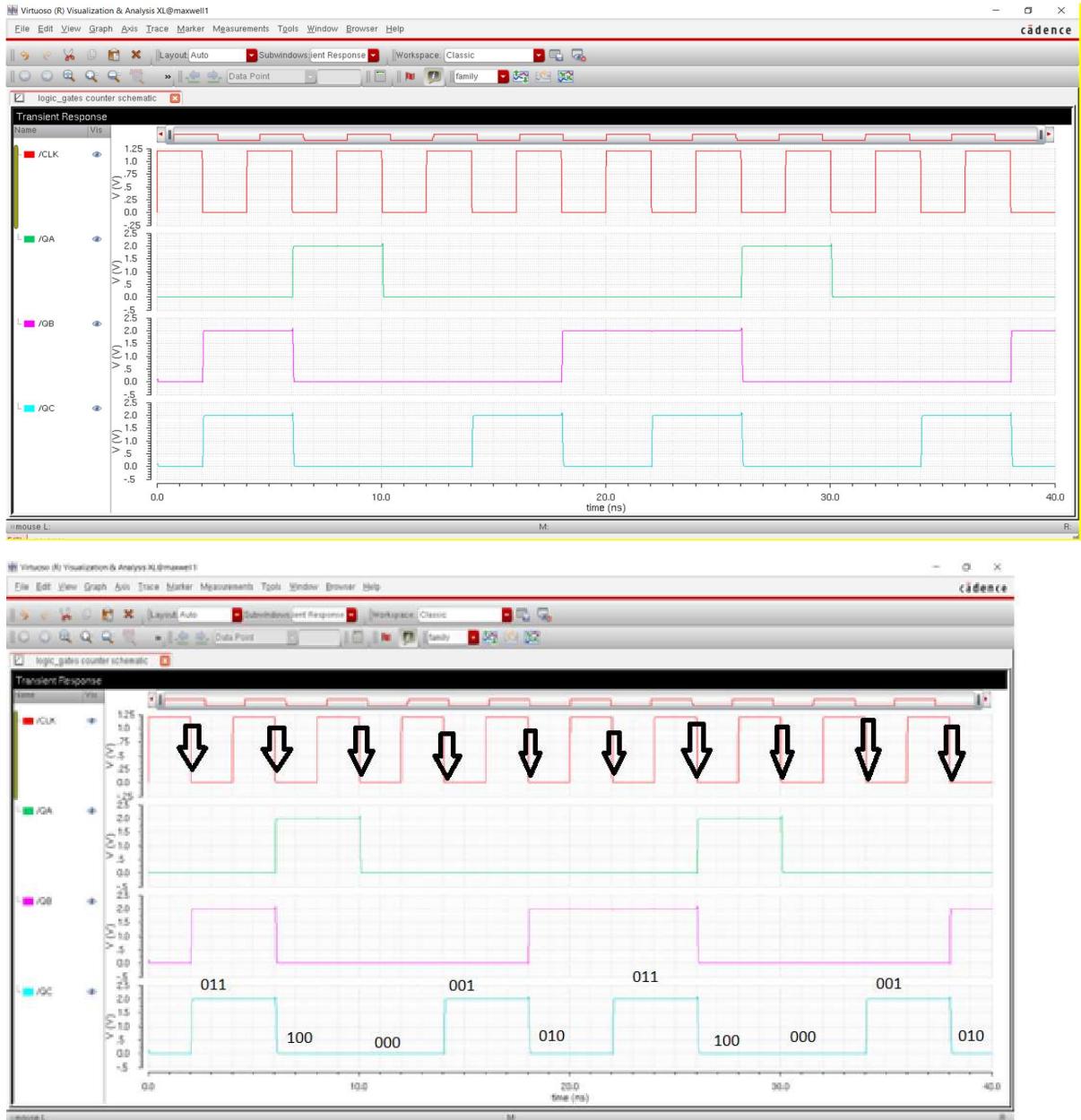


\*\* Density errors are there.

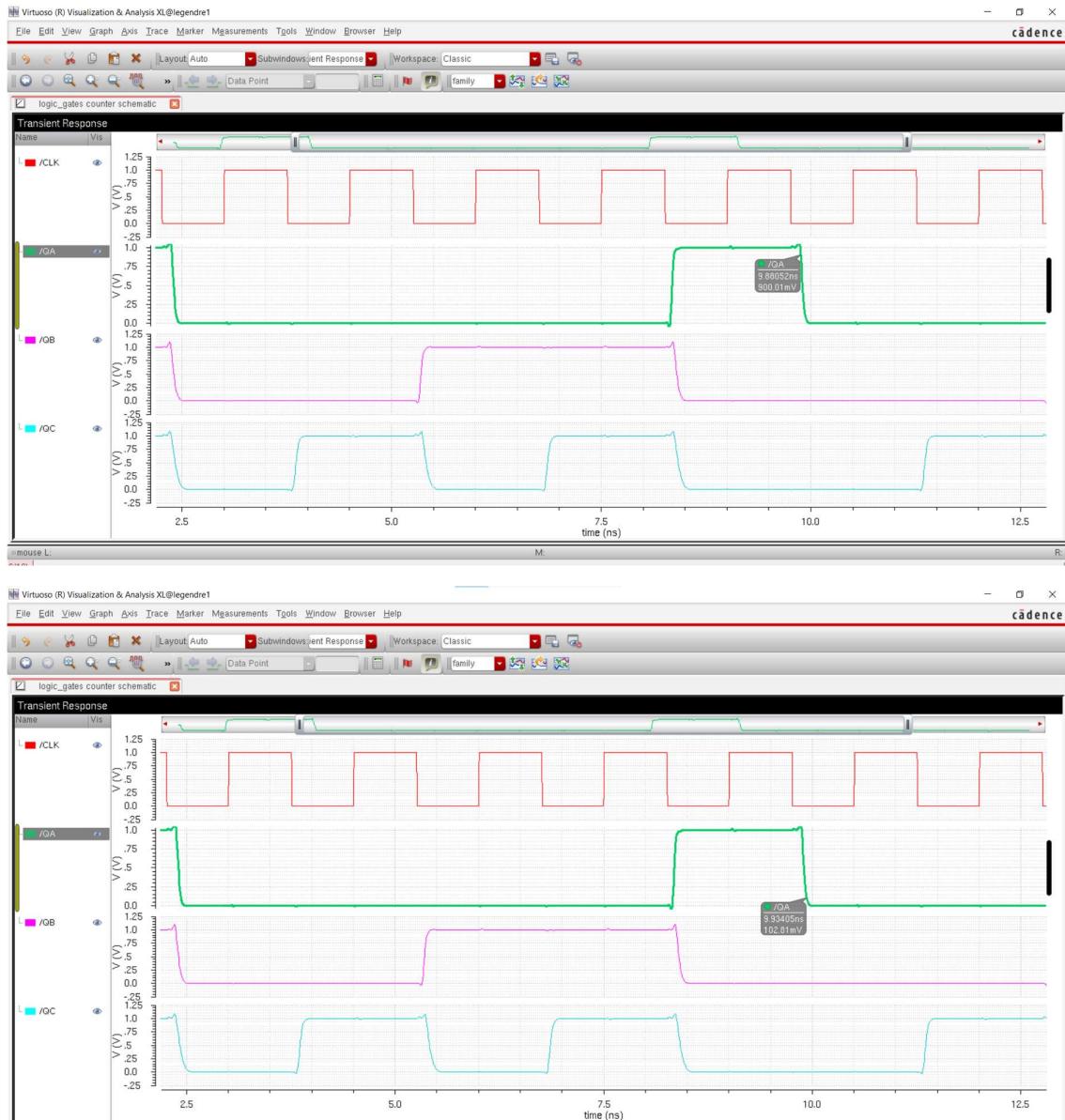
## PRE-LAYOUT EXTRACTION ANALYSIS

Output at different frequencies:

(i) 250MHz

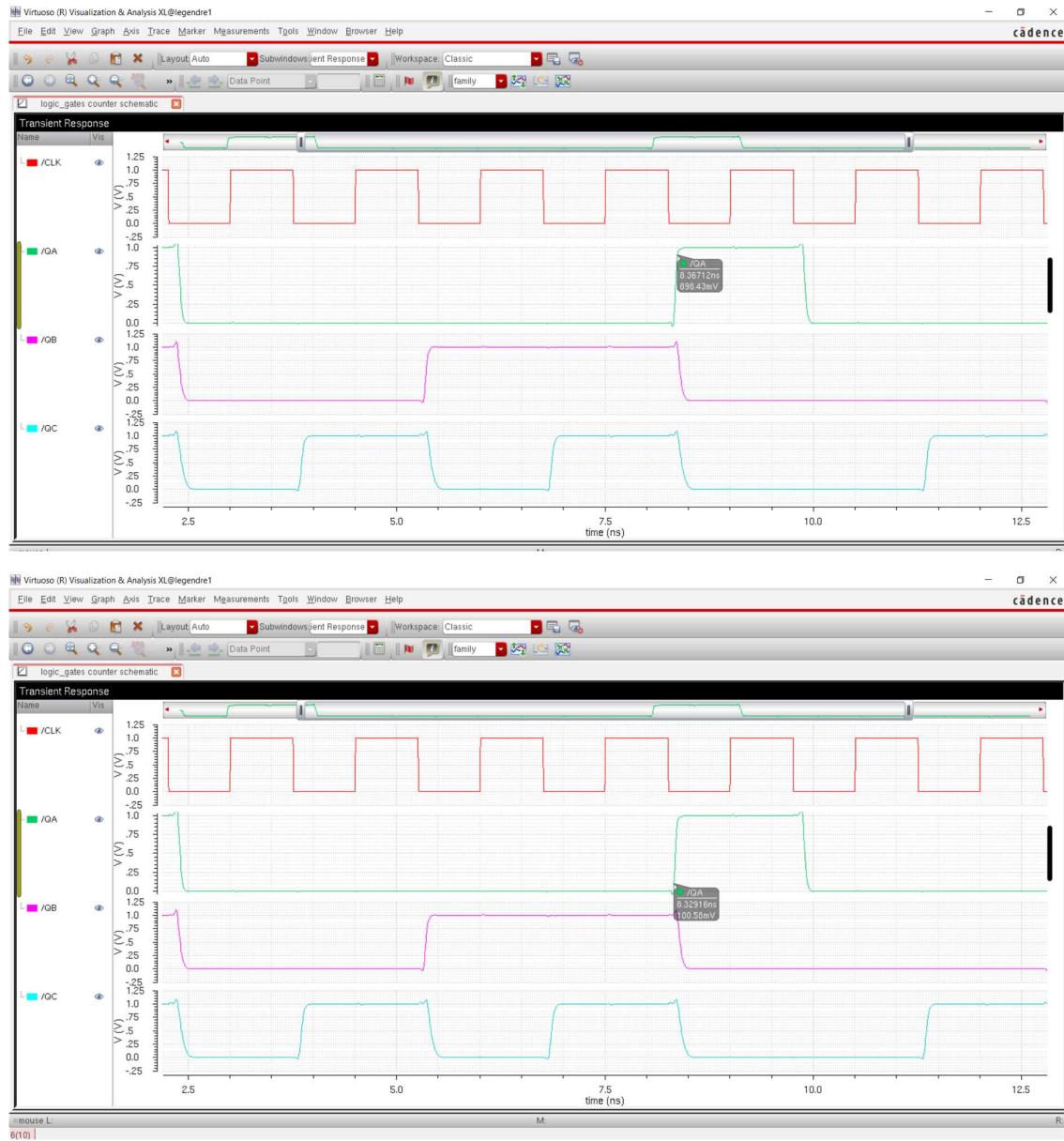


## Calculation of fall time:



$$\text{Fall time} = 9.93405\text{ns} - 9.88052\text{ns} = 0.05353\text{ns}$$

## Calculation of Rise time:



$$\text{Rise Time} = 8.36712\text{ns} - 8.32916\text{ns} = 0.03796\text{ns}$$

(ii) 333MHz



## POST-LAYOUT EXTRACTION ANALYSIS

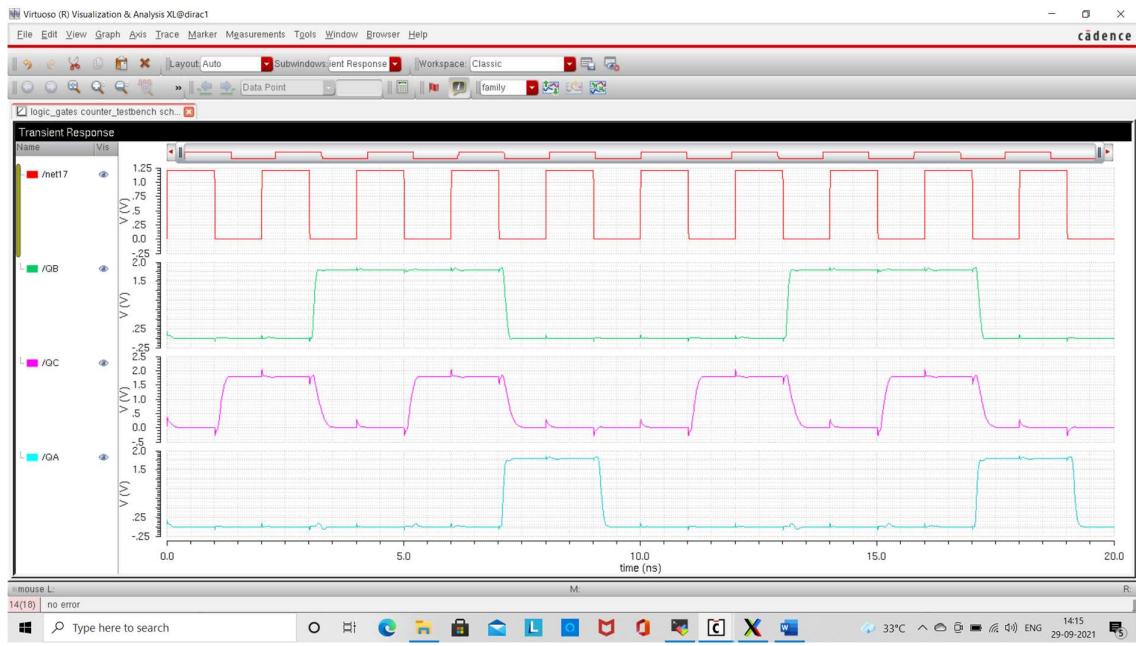


Fig. OUTPUT OF COUNTER AT 500MHz



Fig. OUTPUT OF COUNTER AT 250MHz

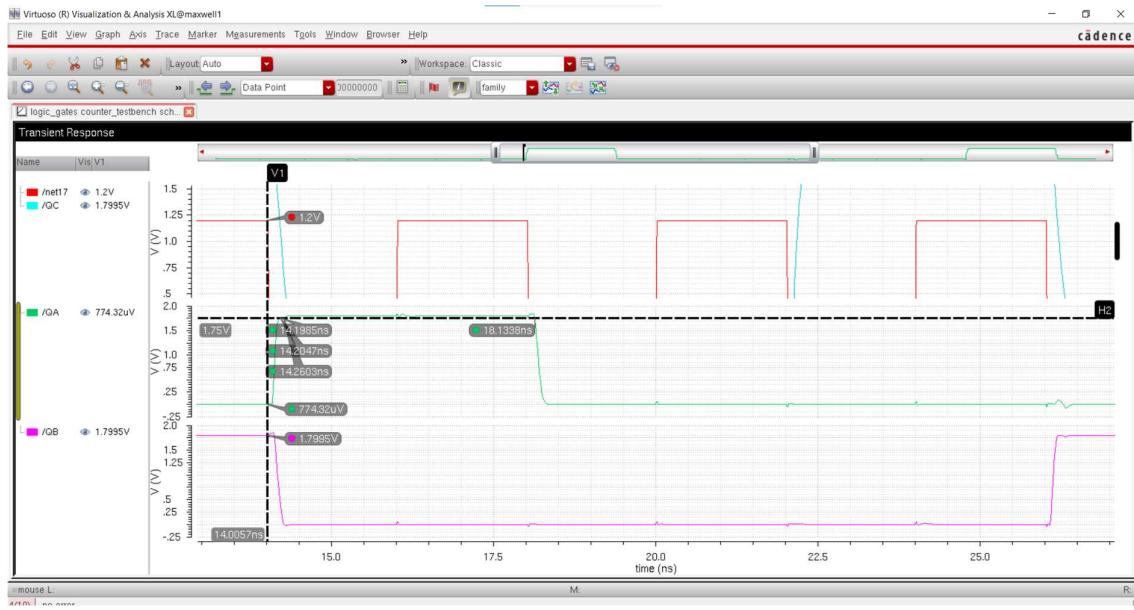
## TIMING ANALYSIS



### SET UP:

Set up time is defined as minimum amount of time required for which an input should be stable just before the clock transition occur.





From the graphical analysis:

$$\text{Hold Time} = 14.1985\text{n} - 14.0057\text{n} = 0.1928\text{ns}$$

#### HOLD TIME:

The hold time is the interval after the clock where the data must be held stable. Hold time can be negative, which means the data can change slightly before the clock edge and still be properly captured.





$$\text{Set Up Time} = 220.646\text{n} - 21.9969\text{n} = 0.0677\text{ns}$$

## COMPONENTS USED TO MAKE THIS COUNTER

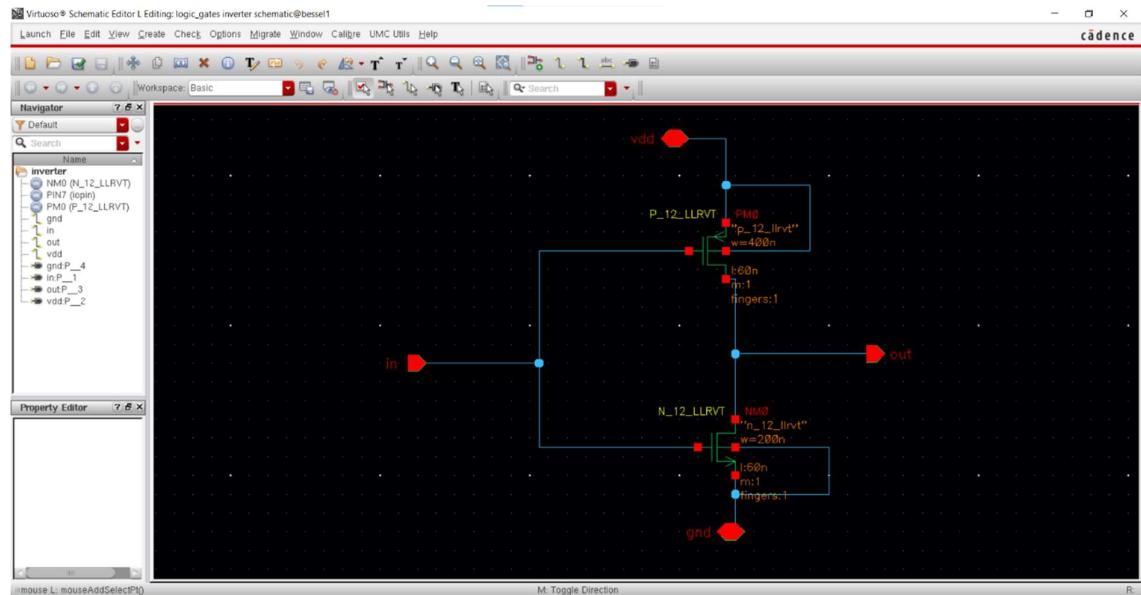
### Inverter

Specifications:

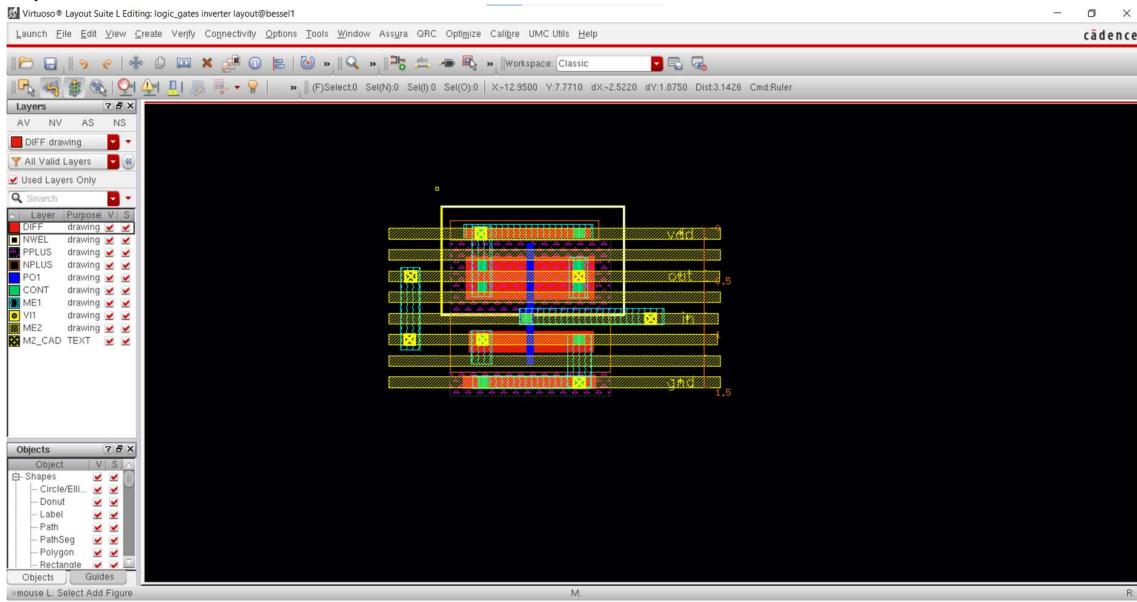
INPUT: Time period =20ns, Pulse Width=10ns, Amplitude=1.2V

Layout: Height=1.4um

### Schematic



## Layout



## Output

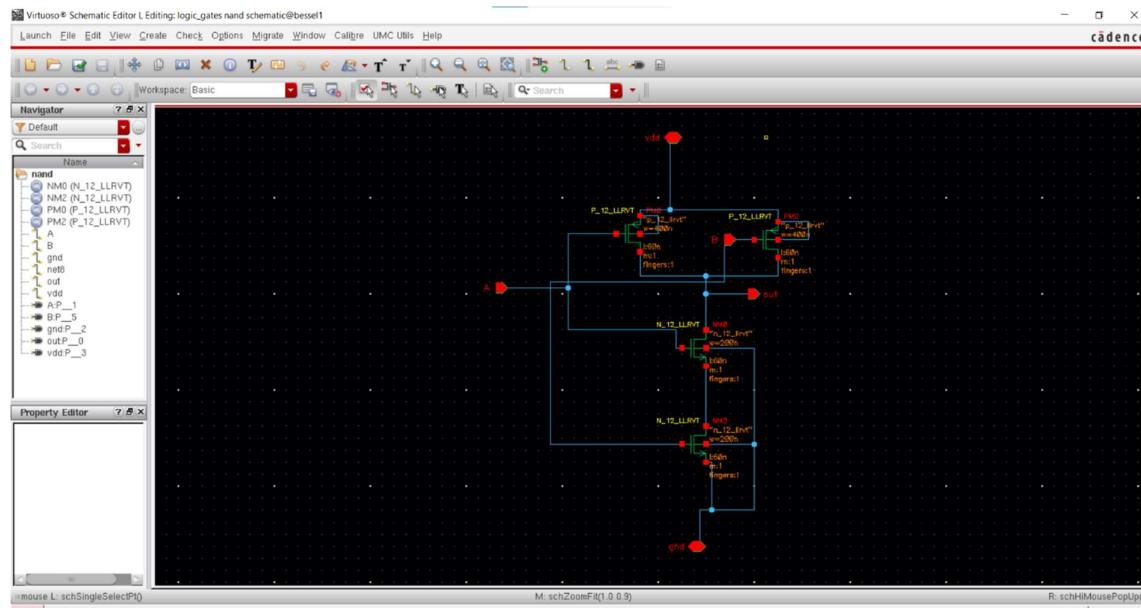


## Two Input Nand Gate

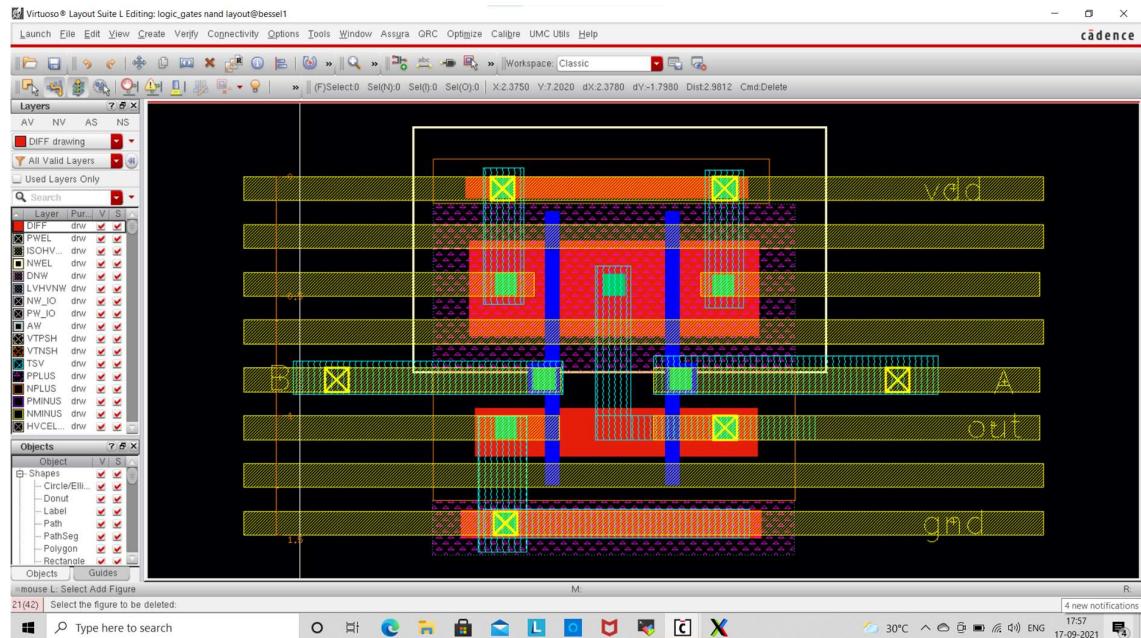
Input Pins: A, B ; Output Pins: out; Power: vdd, gnd

Specifications: Height: 1.4um

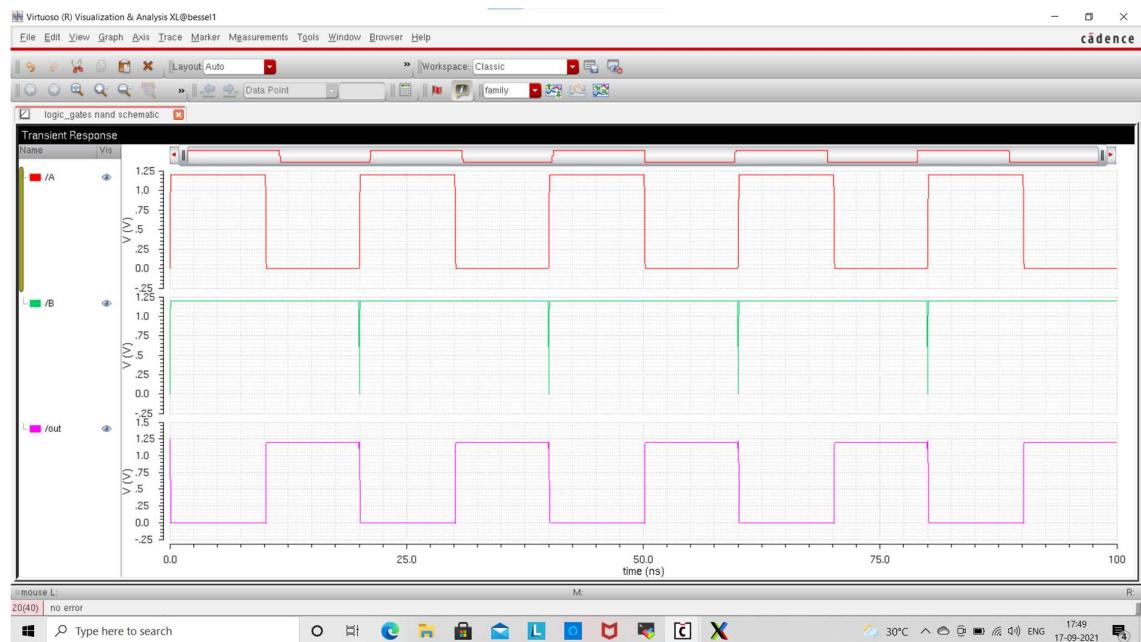
### Schematic



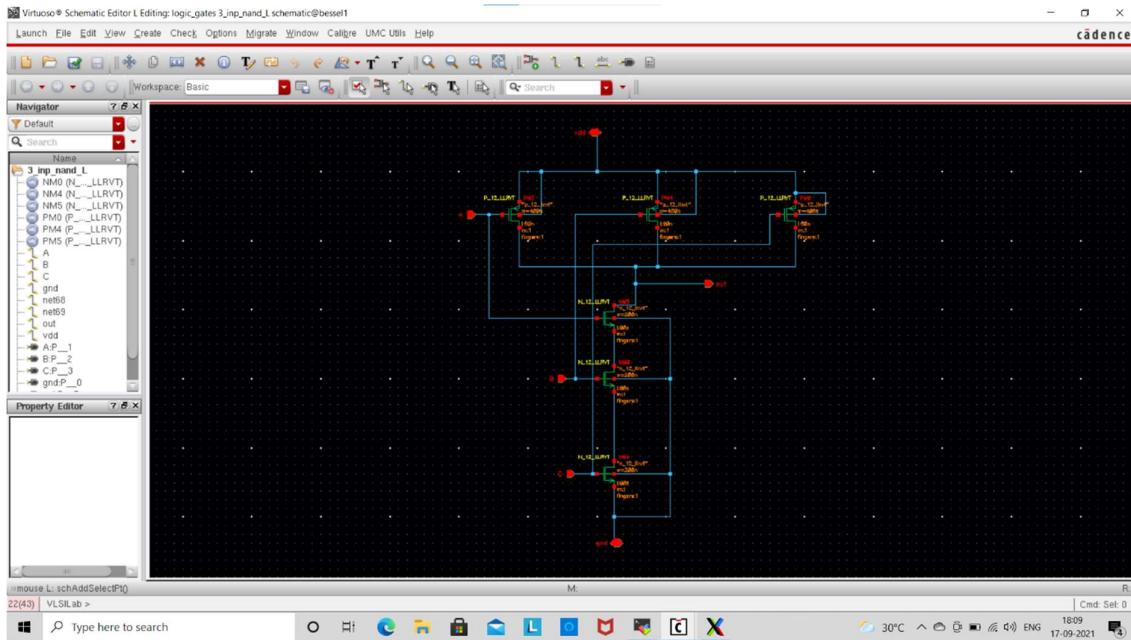
### Layout



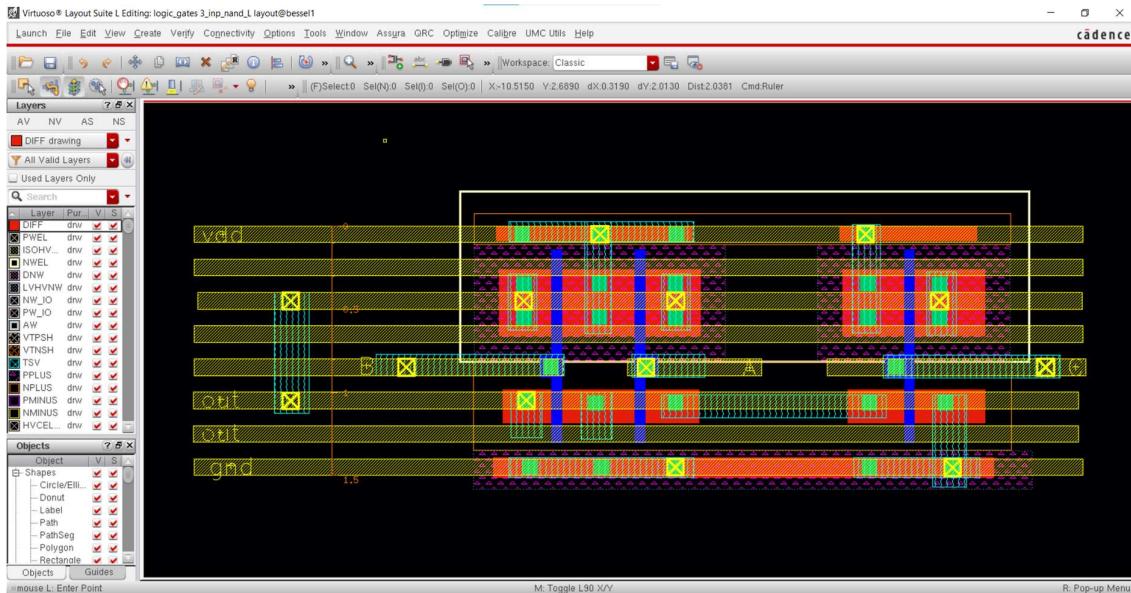
## Output



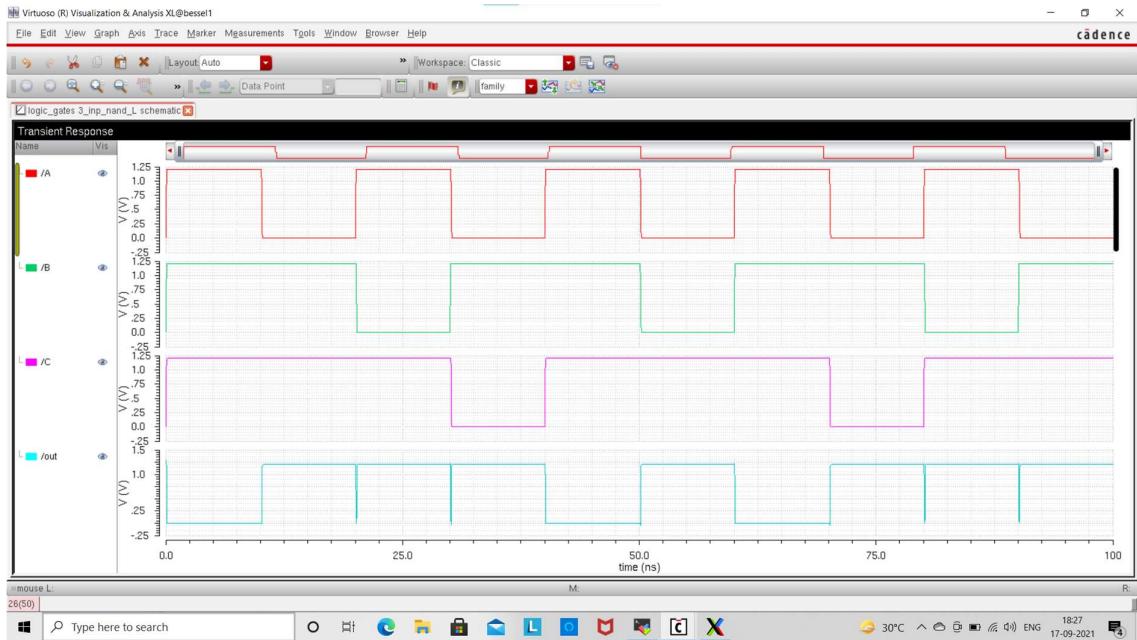
### Three Input Nand Gate



### Layout

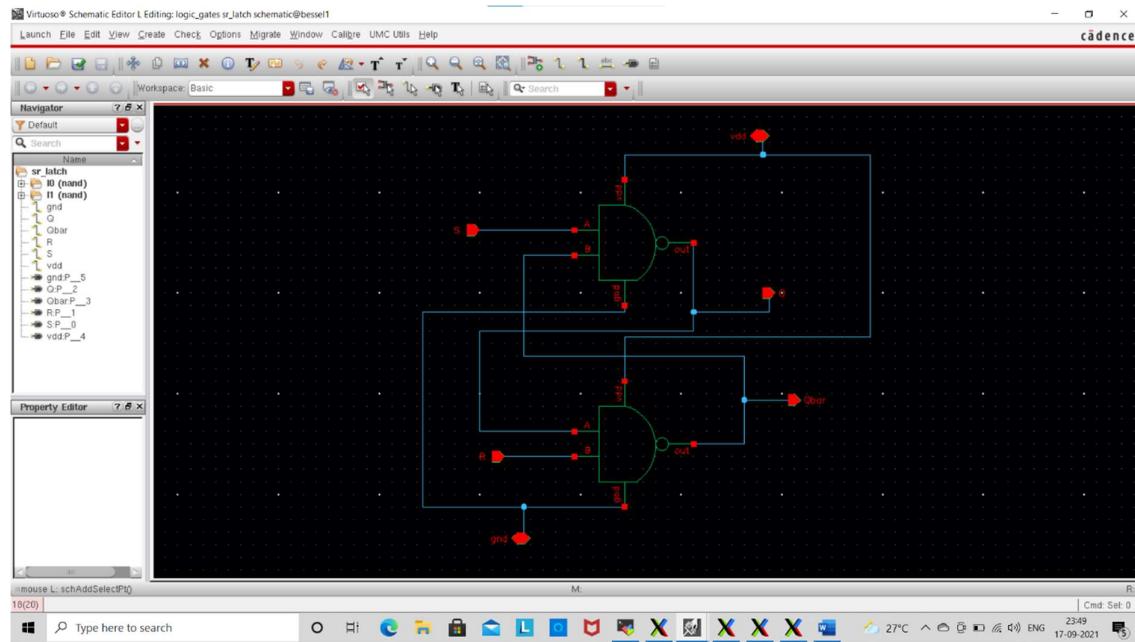


## Output

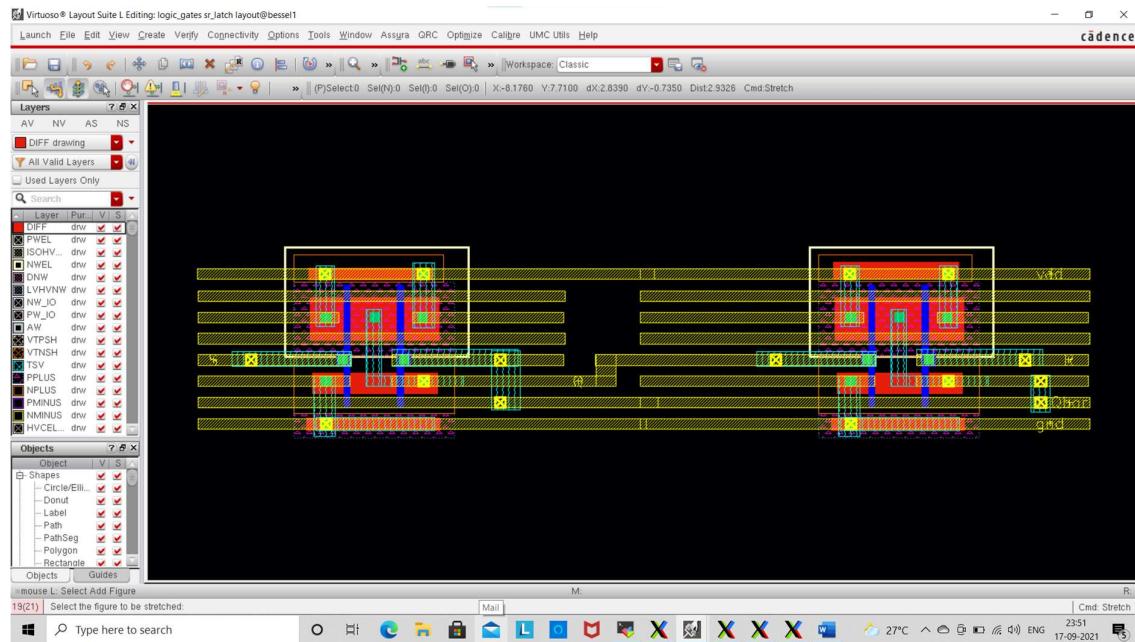


## SR Latch

### Schematic

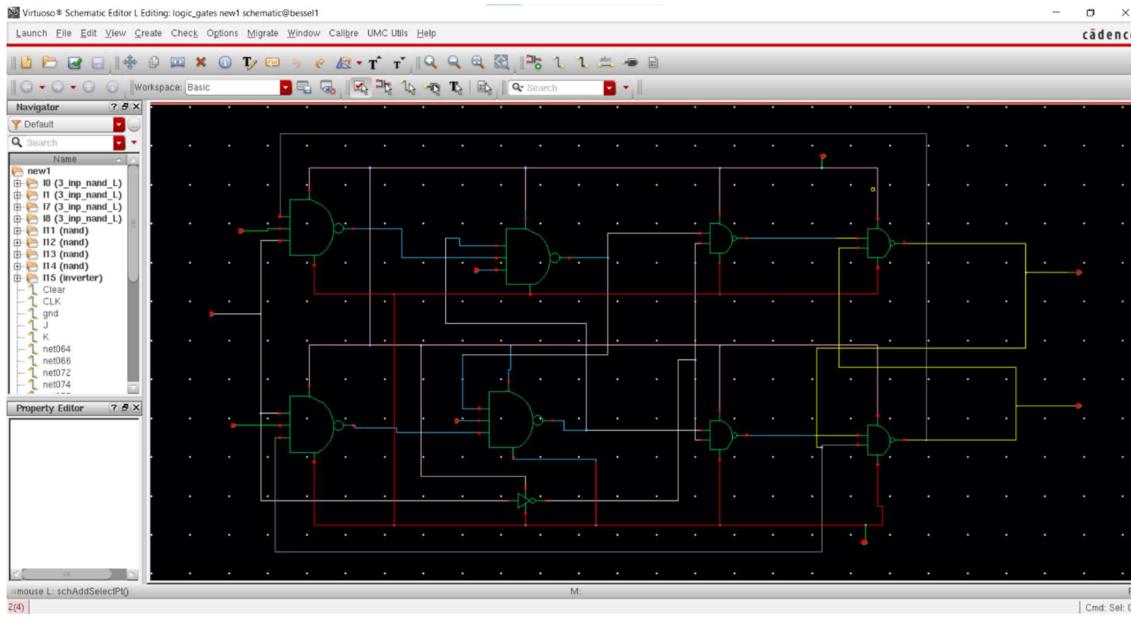


### Layout

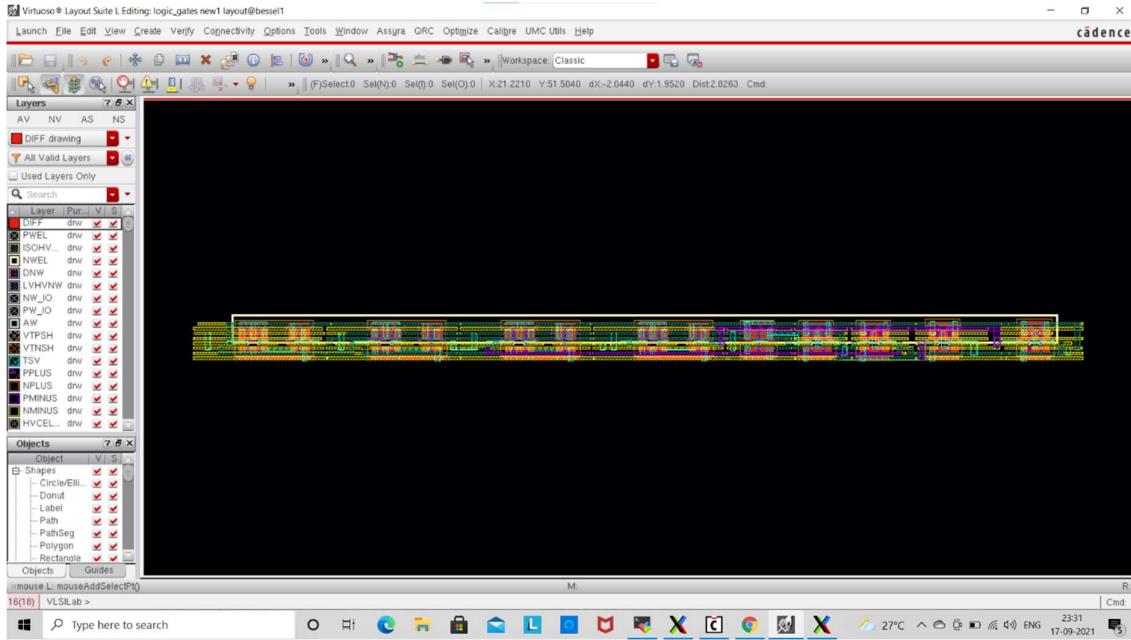


## Master-Slave JK Flip Flop with Preset and Clear Controls

### Schematic



### Layout



## Output (pre layout simulation)



Time period of clock pulse = 4ns

Pulse width = 2ns