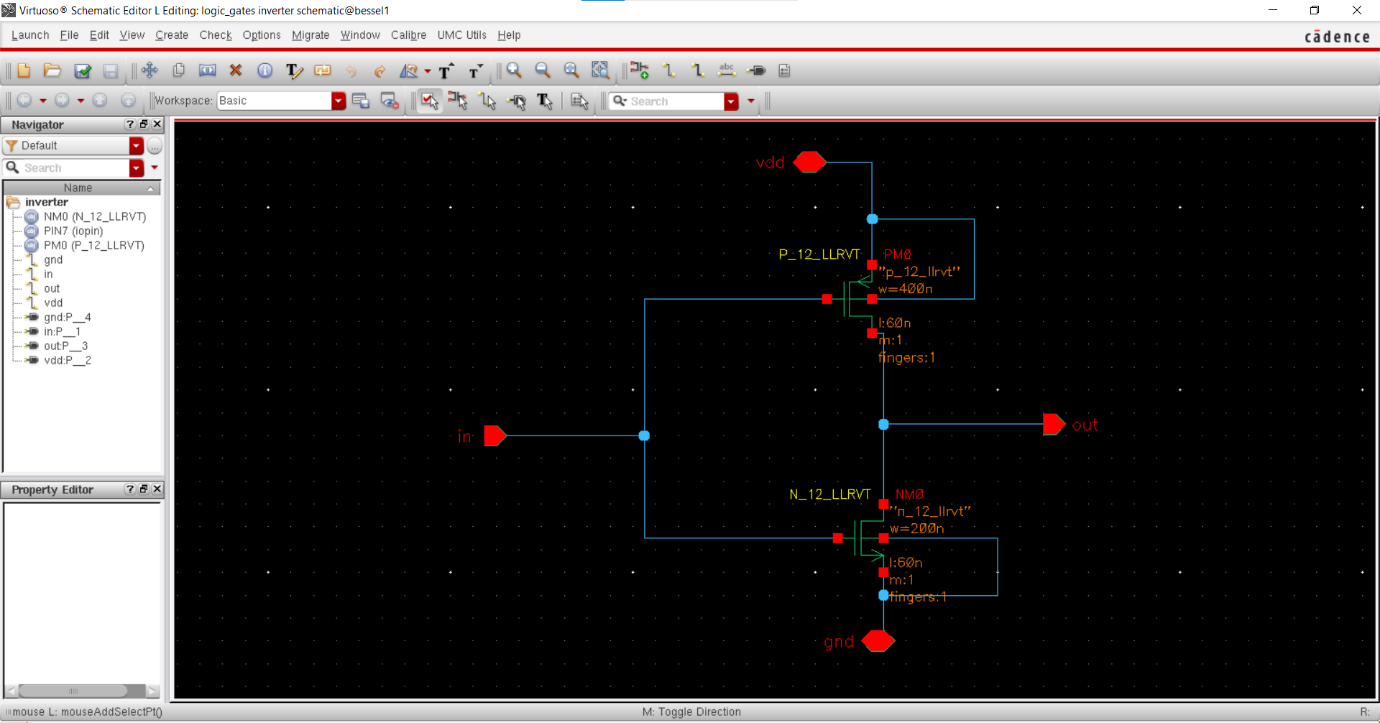
Inverter

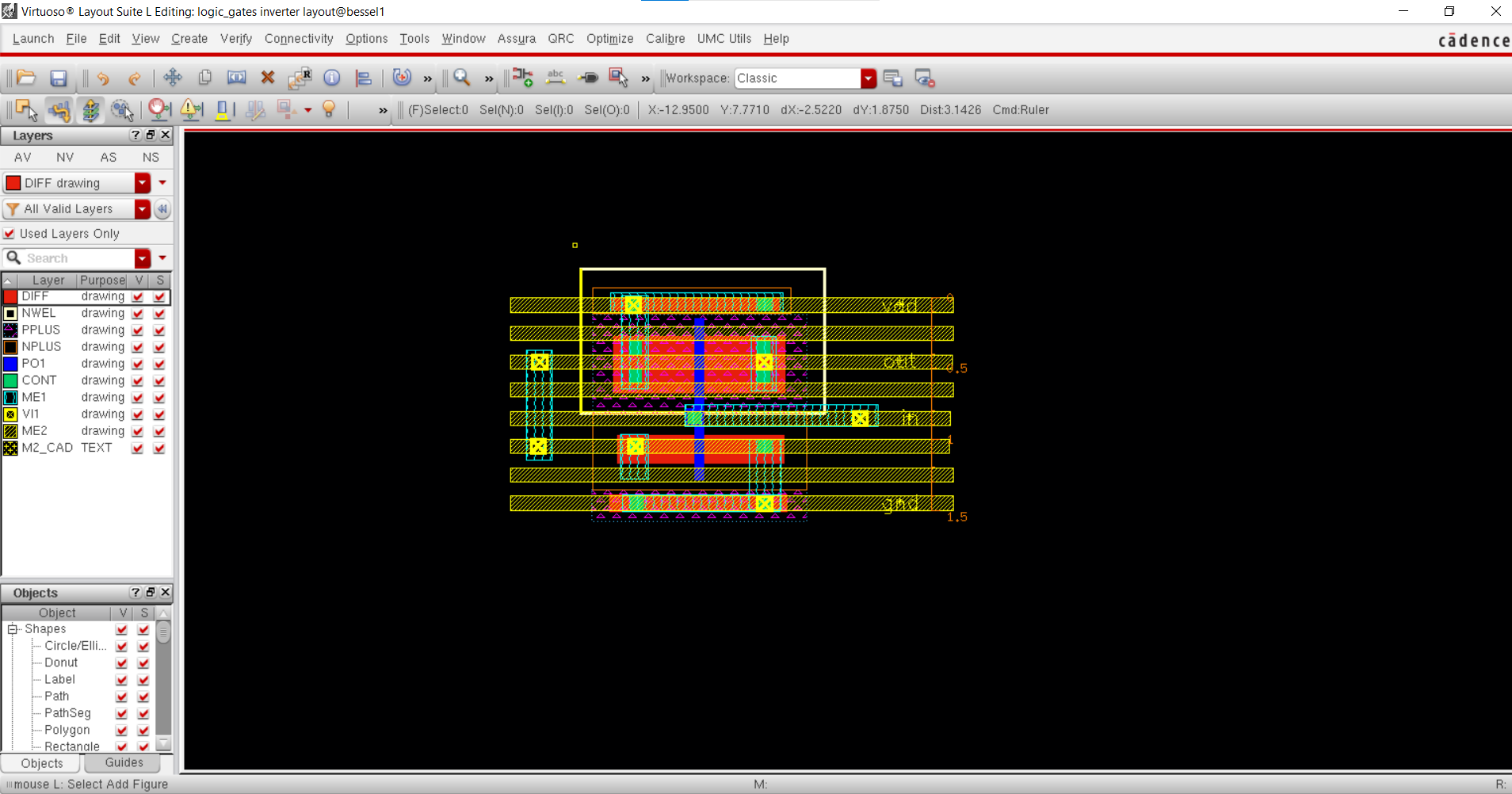
Specifications:

INPUT: Time period =20ns, Pulse Width=10ns,Amplitude=1.2V

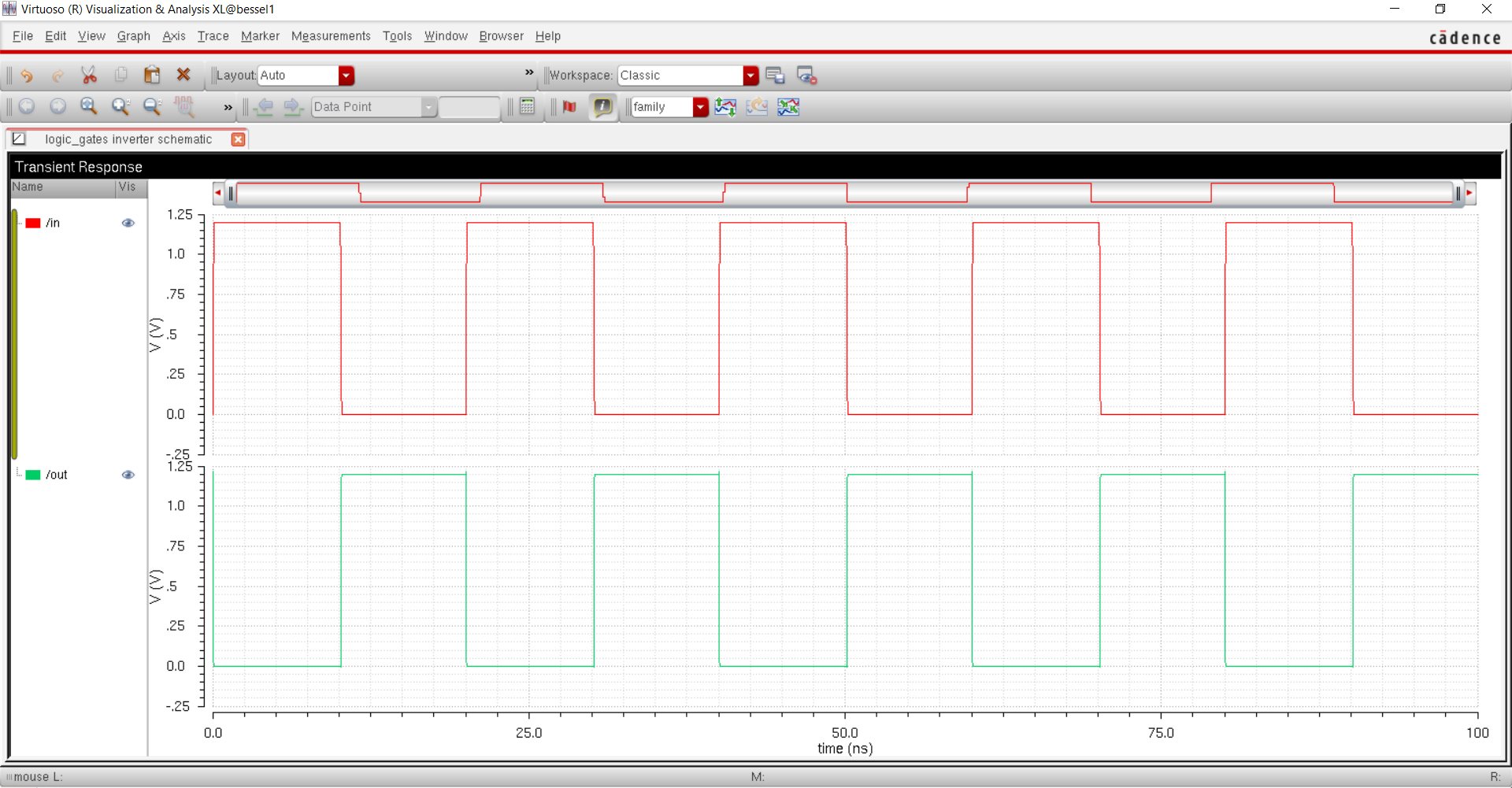
Layout: Height=1.4um

Schematic



Layout

Output

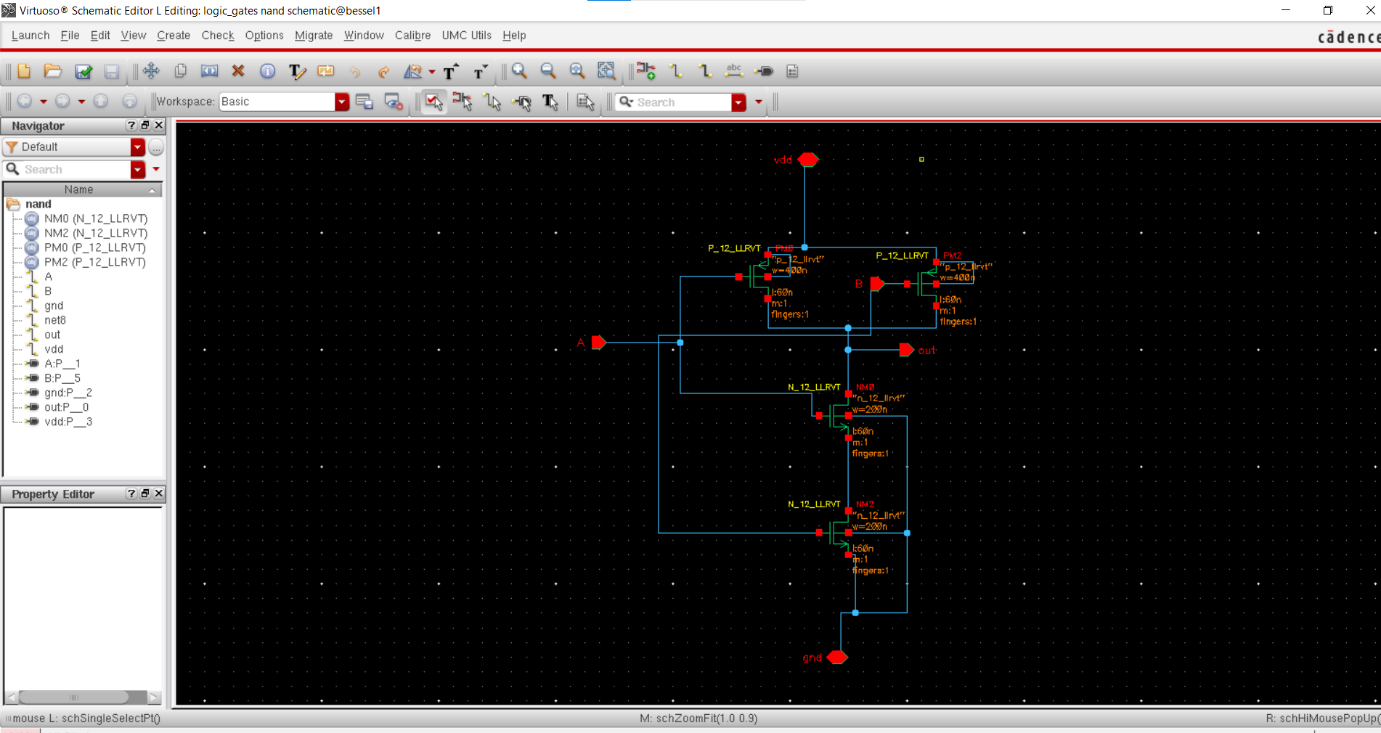


Two Input Nand Gate

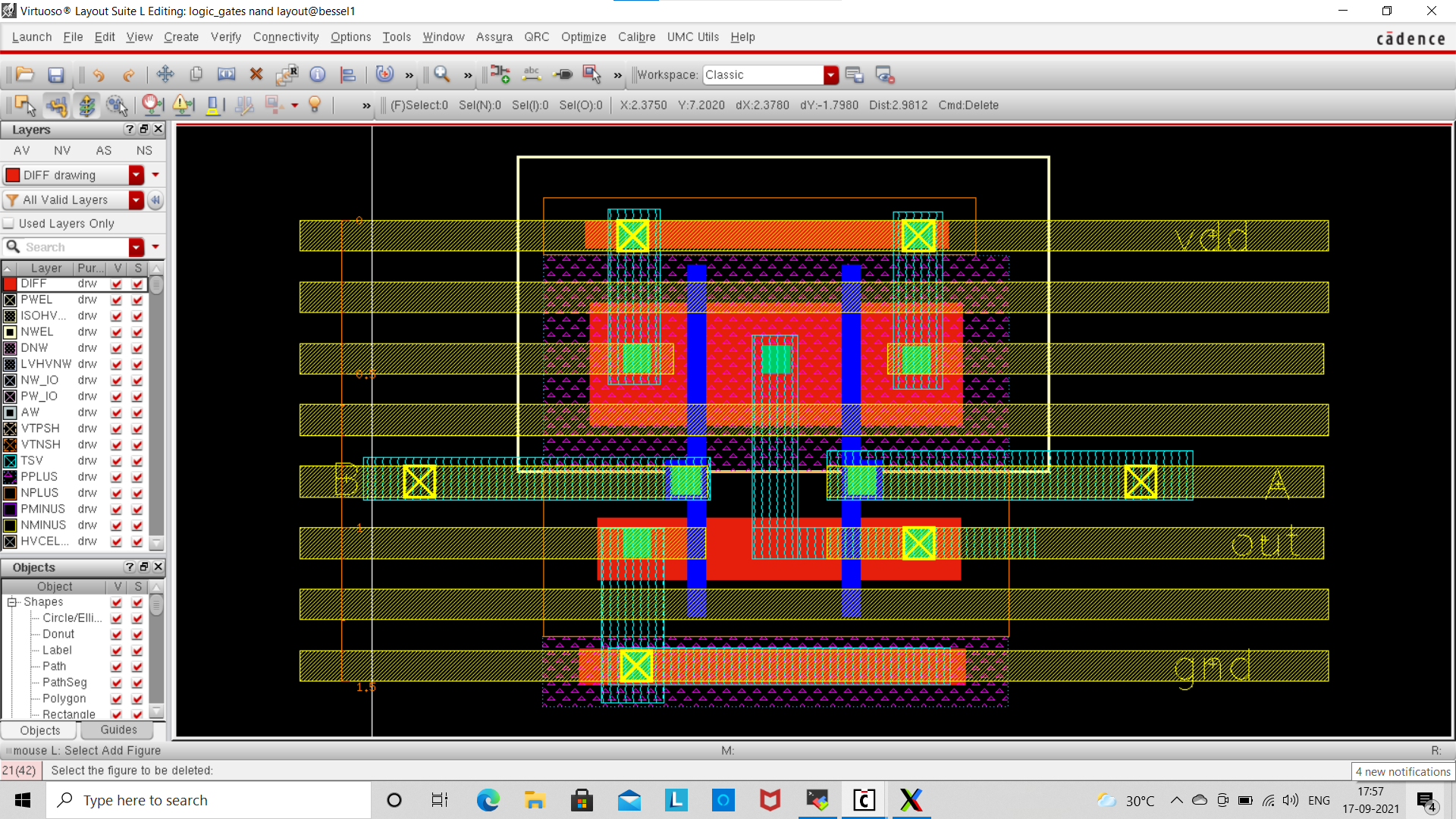
Input Pins: A, B ; Output Pins: out; Power: vdd, gnd

Specifications: Height: 1.4um

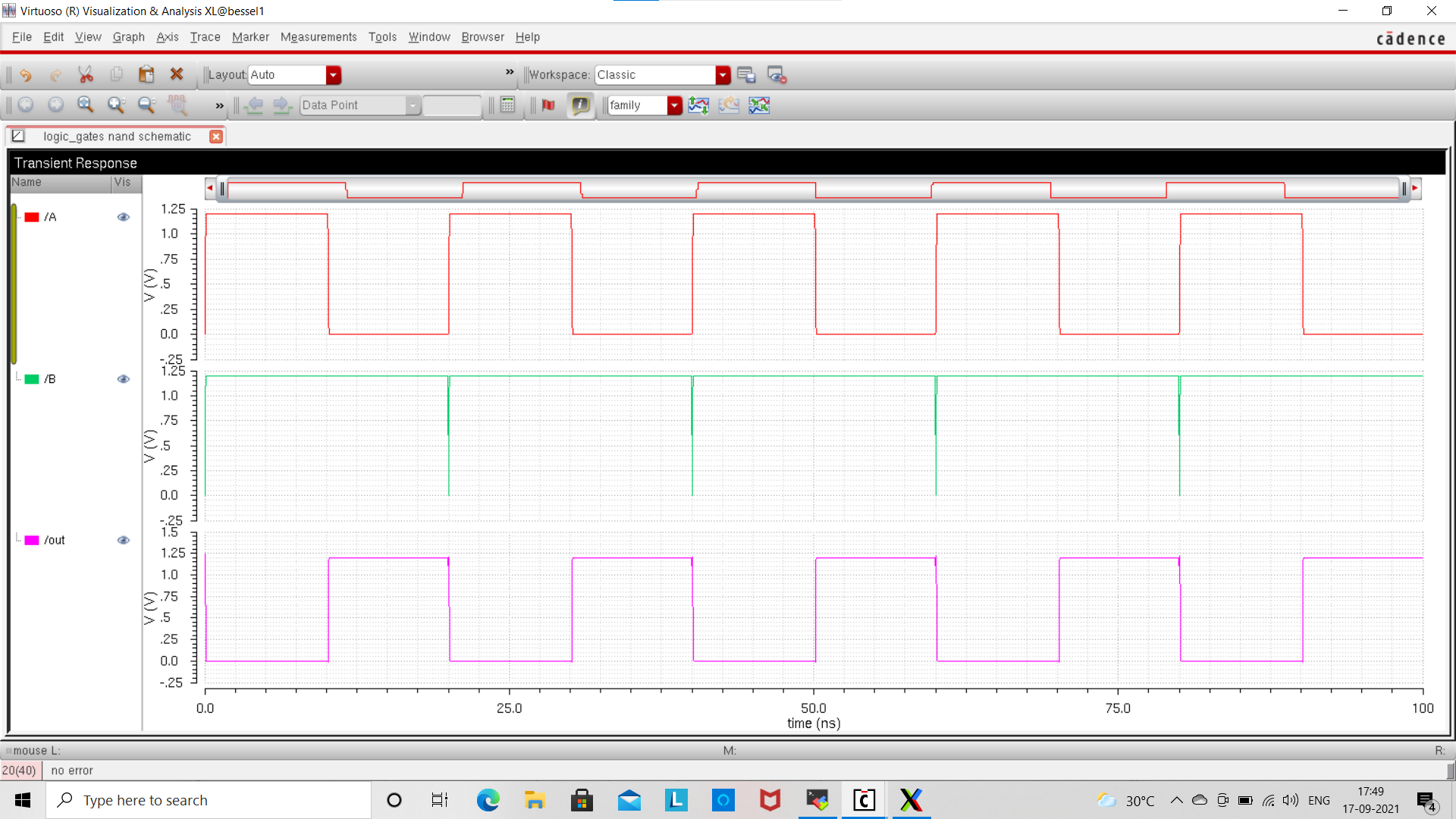
Schematic



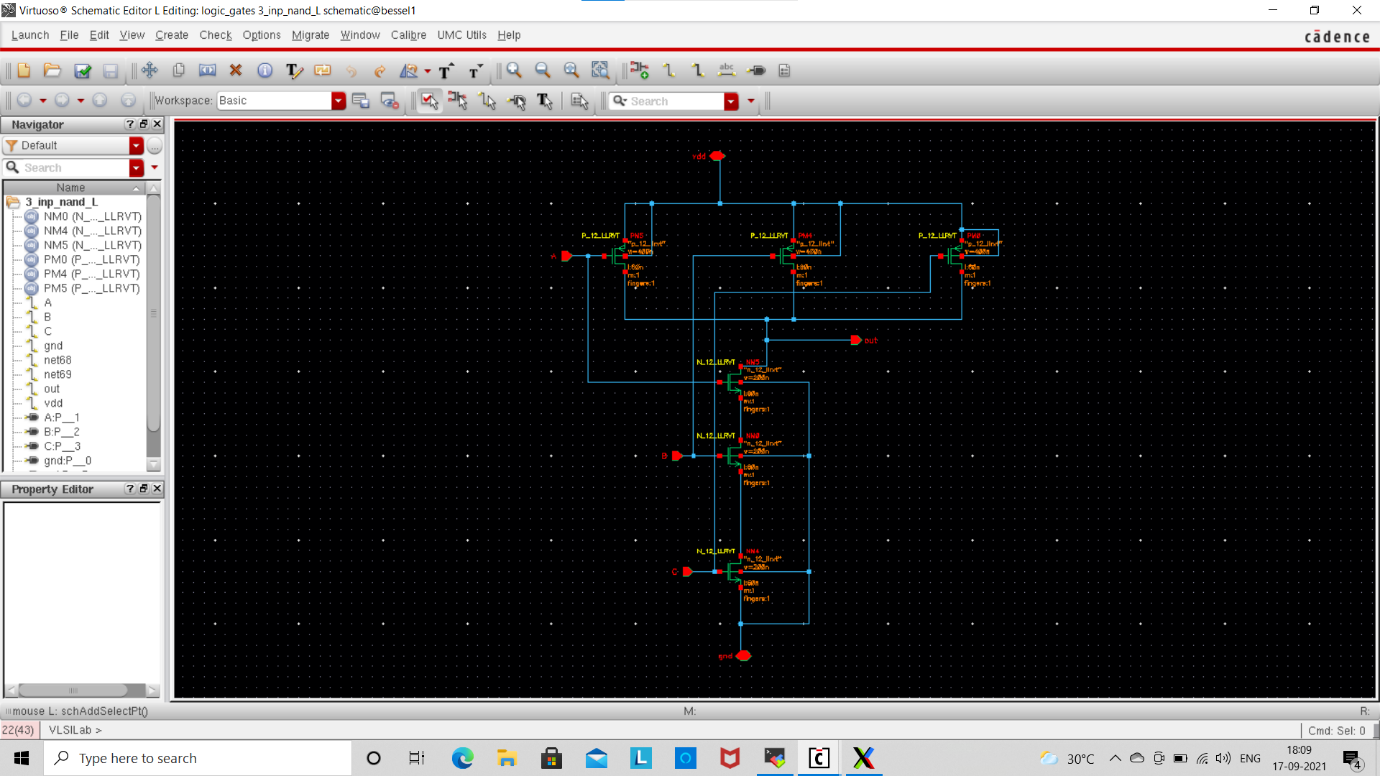
Layout



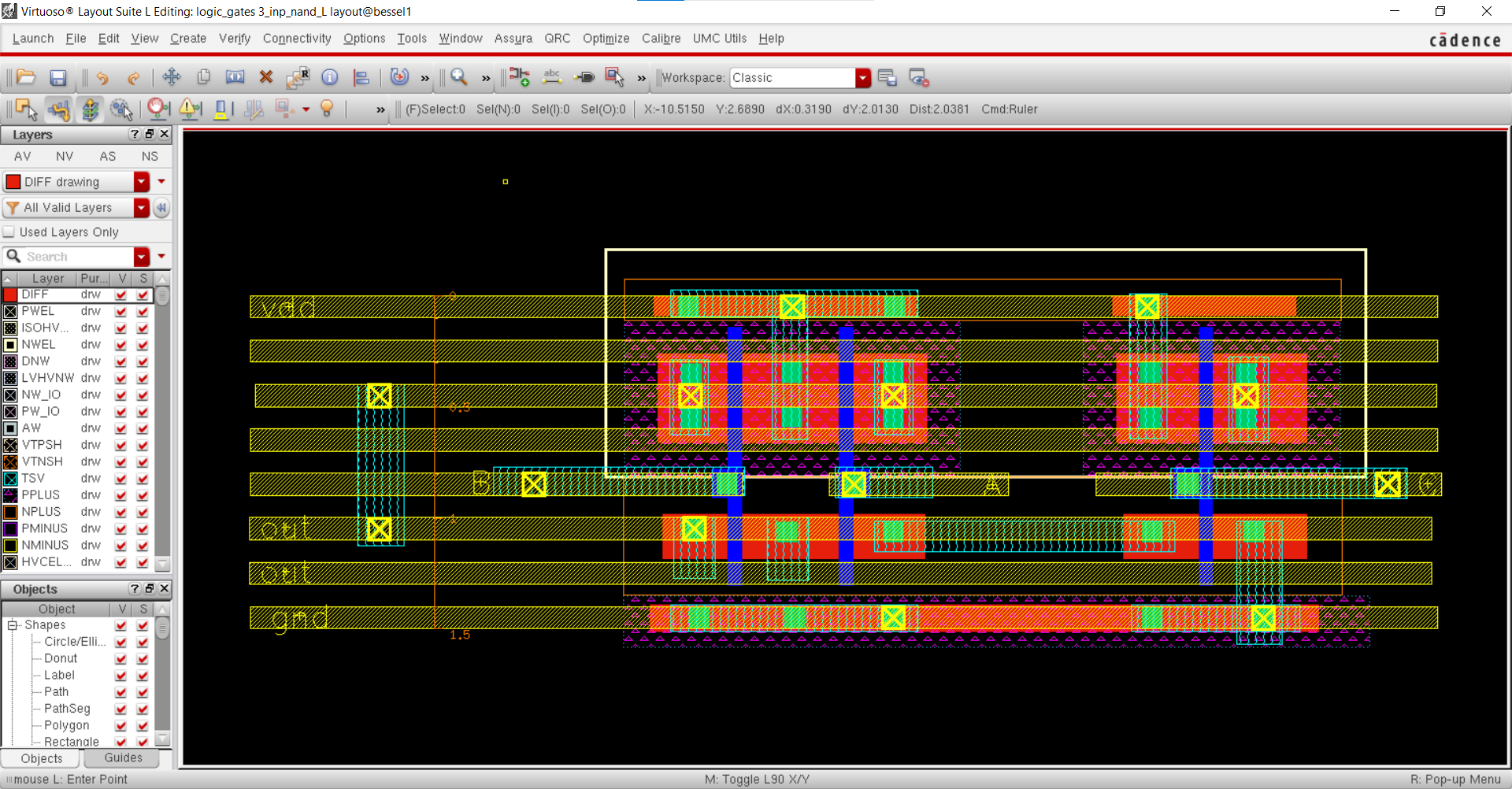
Output



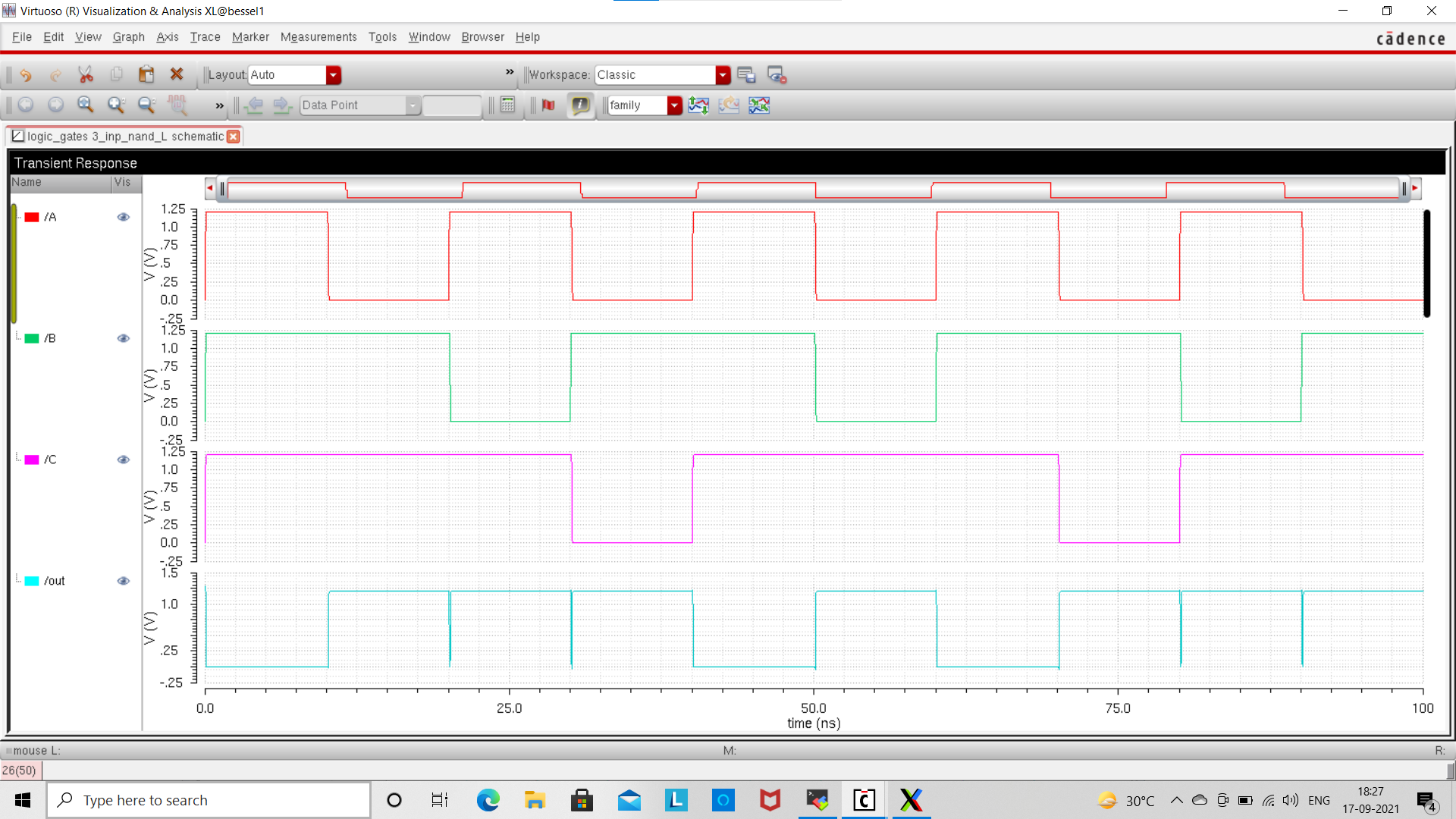
Three Input Nand Gate



Layout

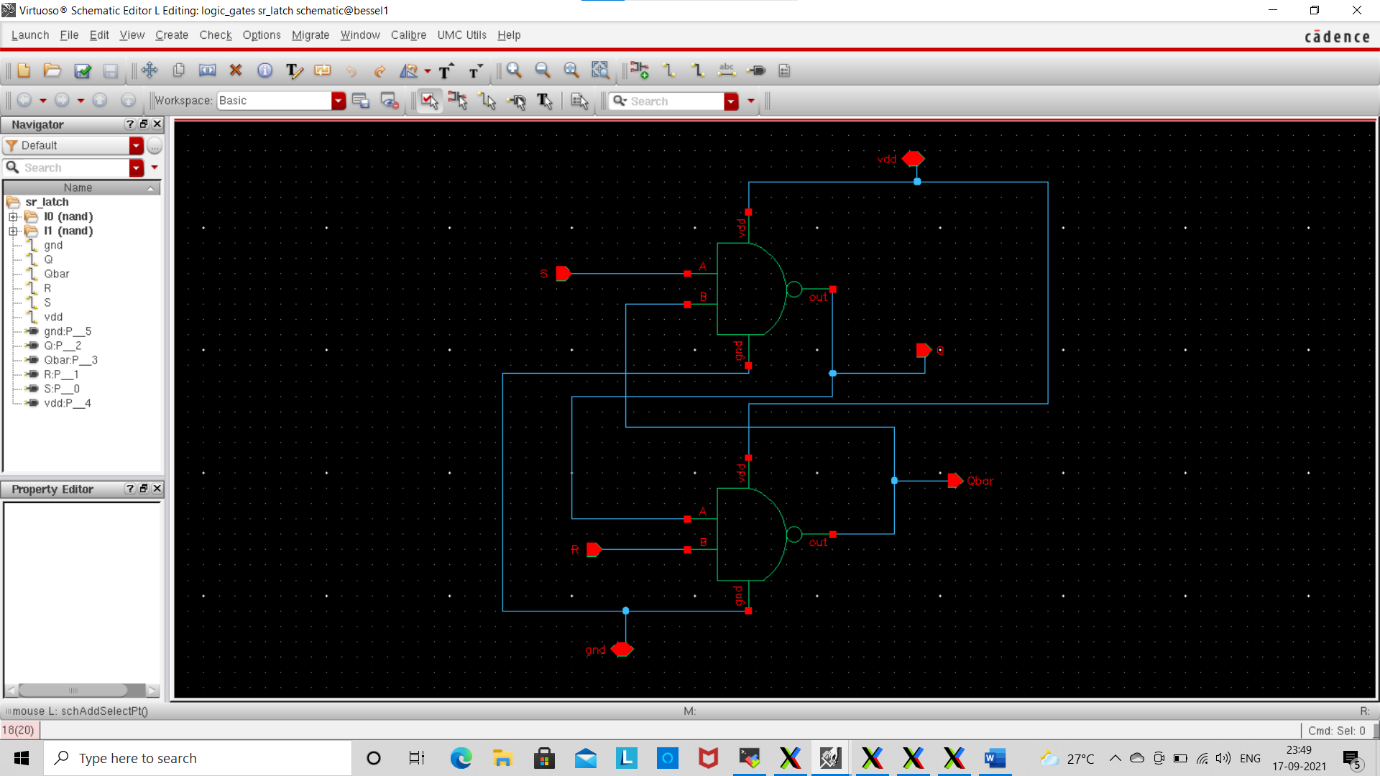


Output

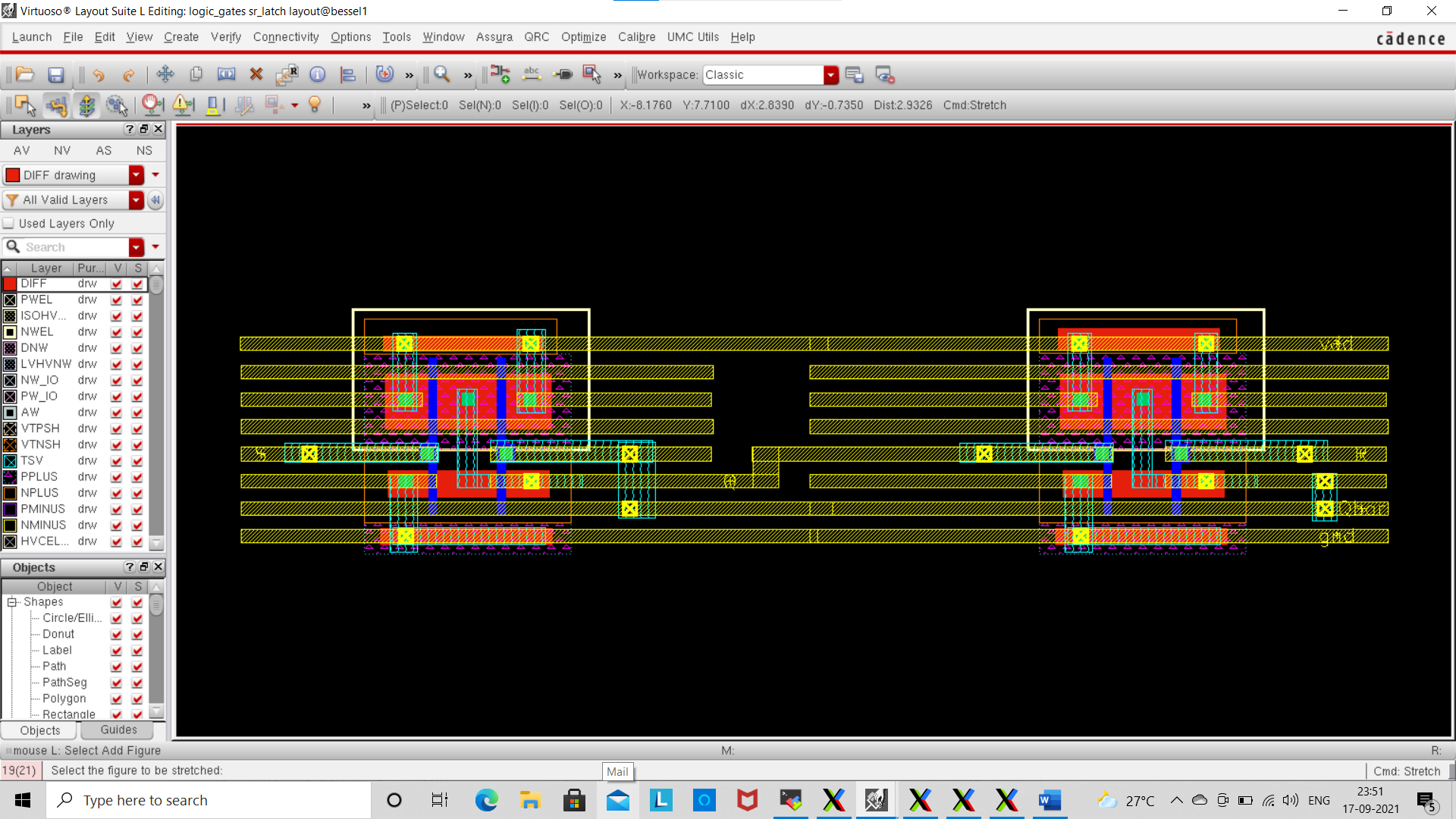


SR Latch

Schematic

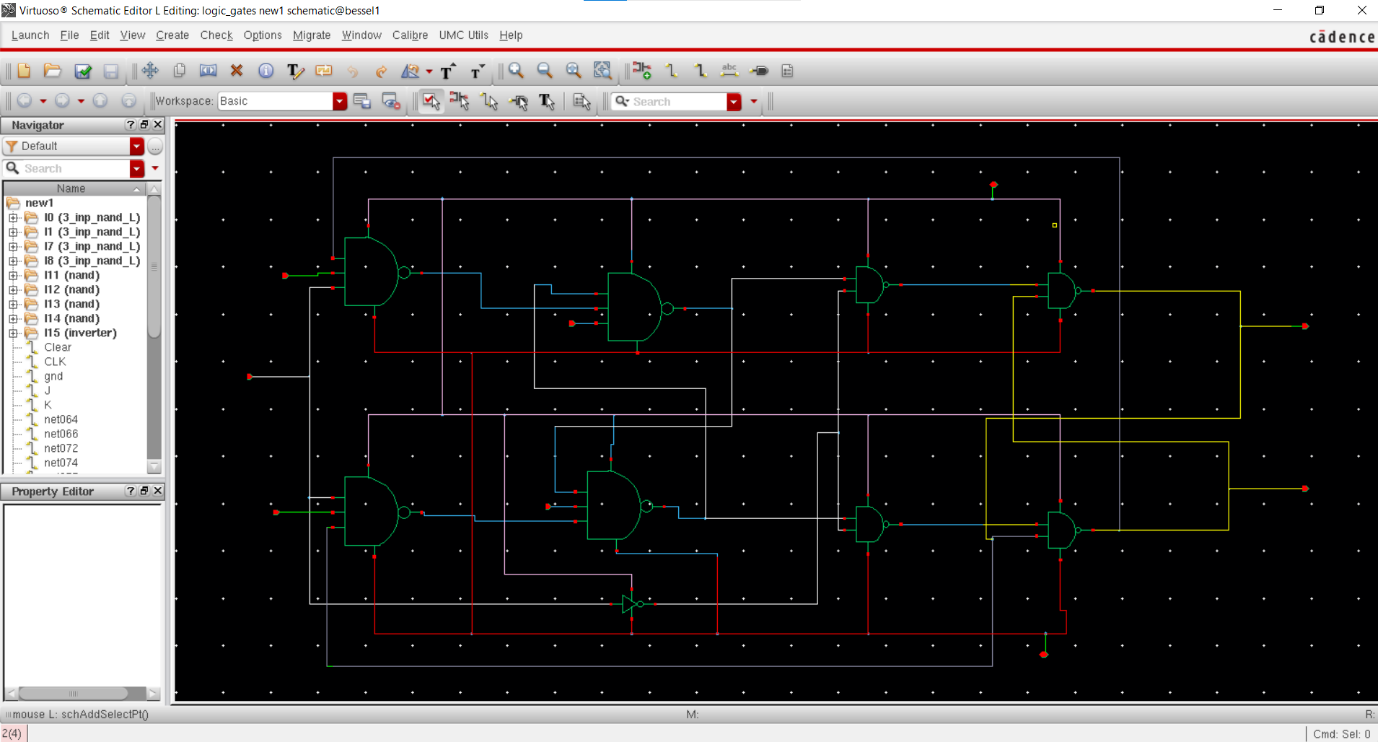


Layout

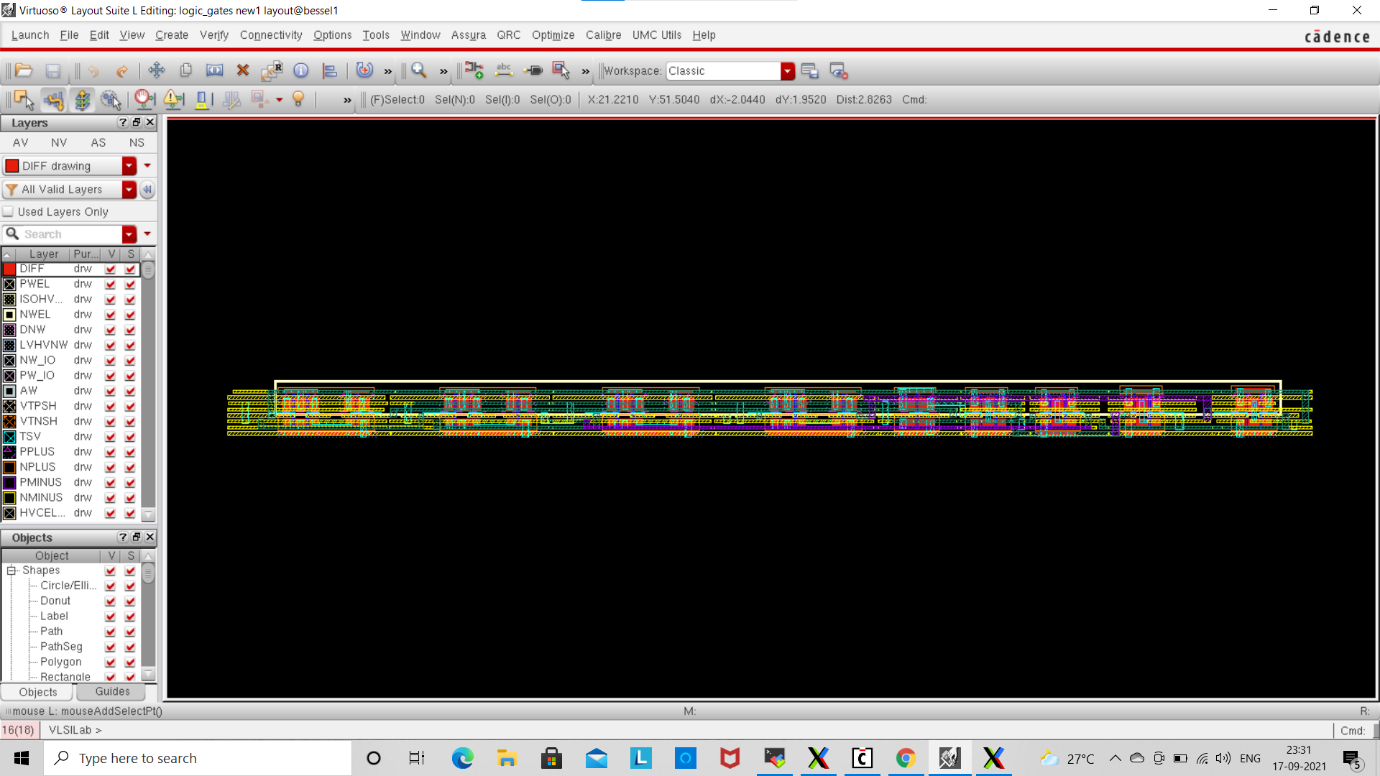


Master-Slave JK Flip Flop with Preset and Clear Controls

Schematic

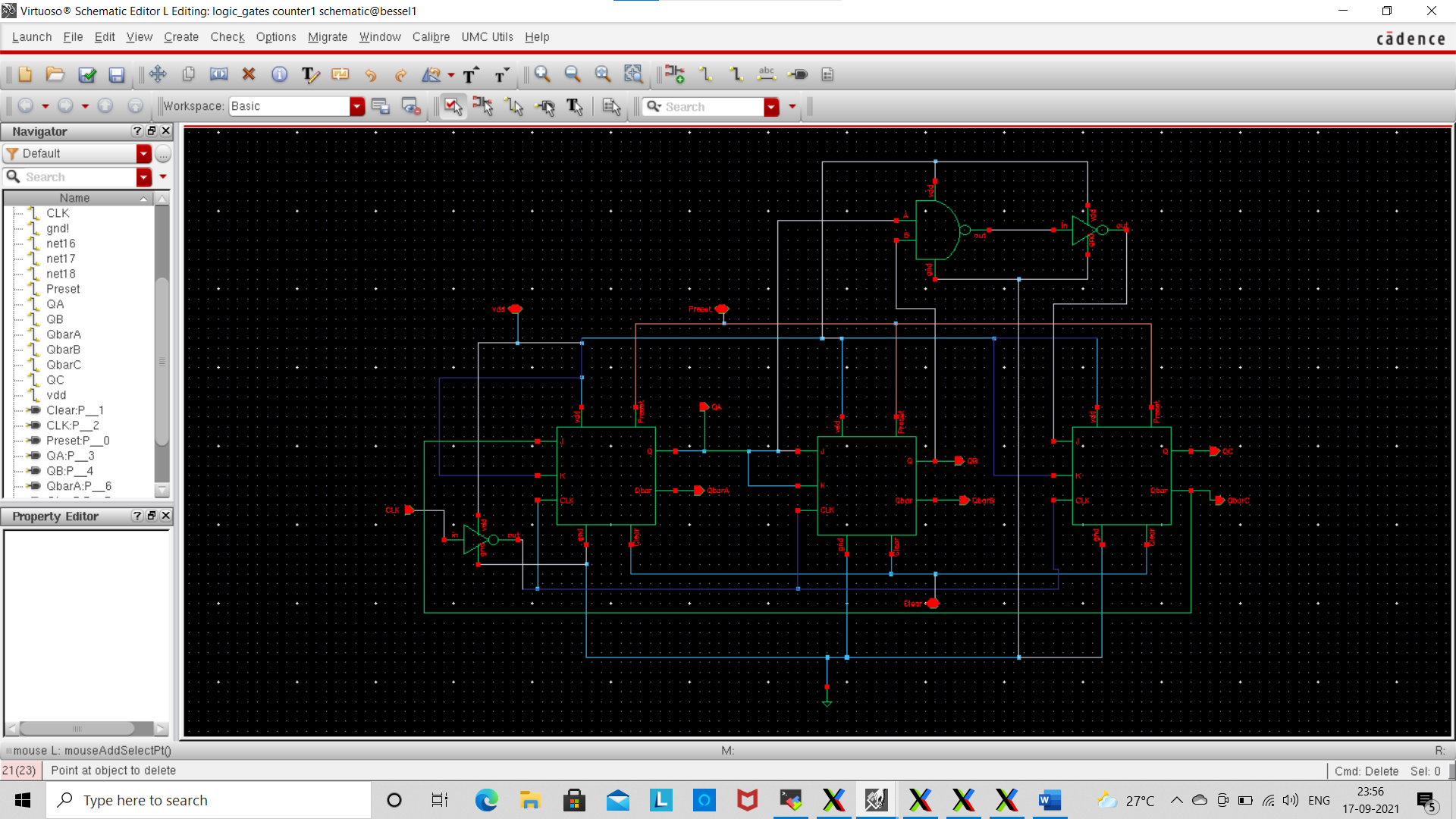


Layout

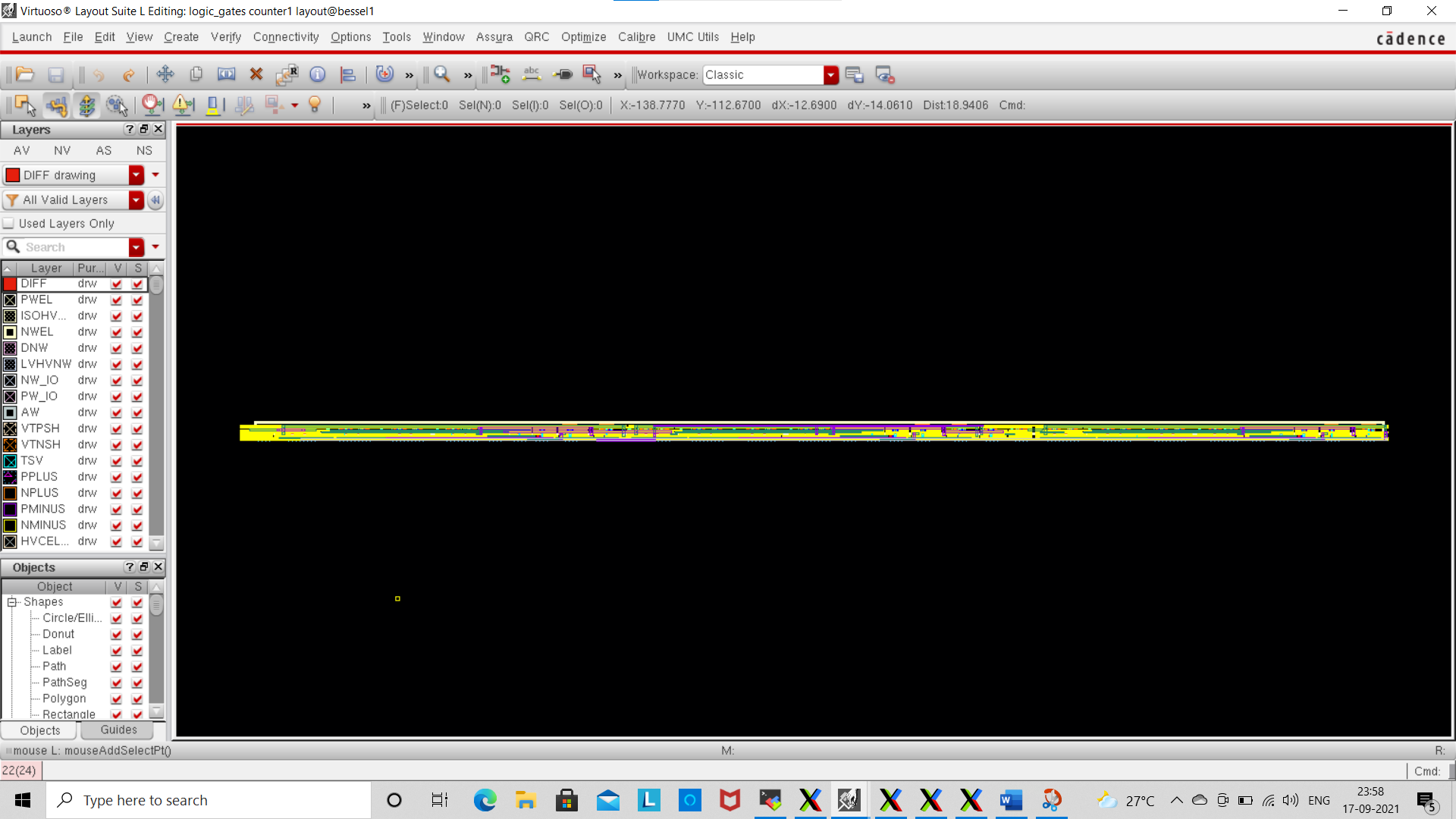


MOD -5 Counter

Schematic



Layout



\*\* All drc and lvs reports are given in another document attached to the repository.