

SEARCH FOR SOMETHING

by

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## SEARCH FOR SOMETHING

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my abstract



## ACKNOWLEDGMENTS

Many people has contributed to make this work possible that it is impossible to name them all.

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## CHAPTER 1

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### **Introduction**

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Talk about particle physics in general and the organization of the documents

## CHAPTER 2

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### The LHC Accelerator and the CMS Experiment

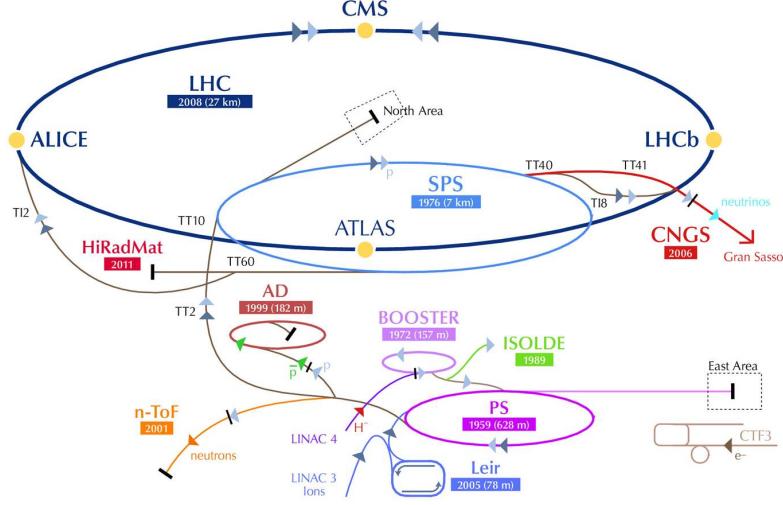
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In the 1960s Peter Higgs and others *need ref* put up the finishing touches on a theory combining three of the four fundamental forces. This theory became to be known as the Standard Model (SM) of particles physics. It predicted the existence of several particles which were discovered in the following decades. However, one particle was proving to be elusive, the so-called Higgs boson. With this in mind the European Organization for Nuclear Research (CERN) started plans to build an accelerator large enough to be able to find this elusive particle. Hence, the Large Hadron Collider (LHC) was born.

## 2.1 The LHC Accelerator

The LHC, the biggest particle accelerator *built* by mankind to date, was built in the french-Swiss border outside of Geneva, Switzerland. A circular ring of 27 km built at the European Council for Nuclear Research (CERN) using the same tunnel as the large electron-positron collider. It accelerates two beams of protons in opposite directions until they reach an energy of 7 Tera electron Volts (TeV), making the center of mass energy 14 TeV.

It began operation in 2010 after two years solving issues that cause a false start



**Figure 2.1:** The CERN acceleration facilities showing the location of the four main experiments as well as the acceleration process[need ref].

in 2008. The LHC prove soon to be a success and in just two years of operations dele

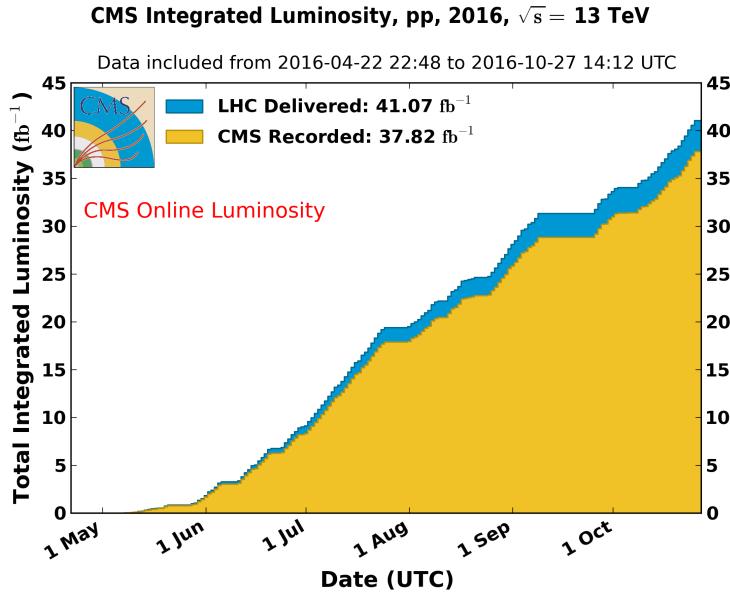
The protons starts from a bottle of hydrogen

Four experiments were designed and built around the LHC 27 km long acceleration ring to test different physics theories and search for undiscovered particles at the LHC. Two of them, A Toroidal Large Aparatus (ATLAS) [1] and the Compact Muon Solenoid (CMS) [2] are large multipurpose experiments. The third experiment is LHCb [3], which is specifically dedicated to study B-meson physics, the last experiment ALICE [4], A Large Ion Collider Experiment, was design to investigate heavy ion collisions.

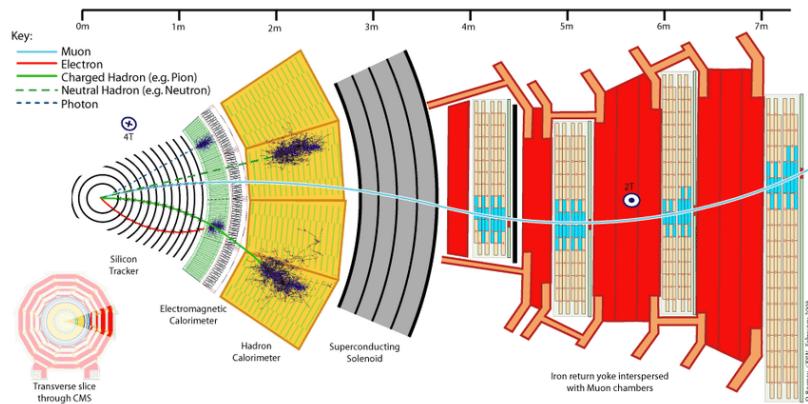
## 2.2 CMS

The compact muon soleinod is one of the two multipurpose experiment at the LHC.

images: run276282->An event where two Z candidates are produced and each decay into two muons, each given by the red lines. This event has 27 reconstructed



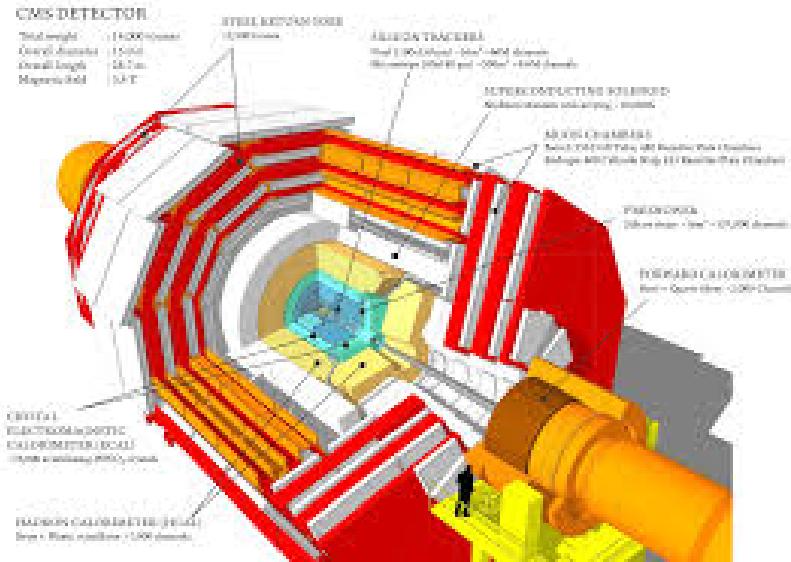
**Figure 2.2:** Total integrated luminosity delivered by the LHC machine to the CMS experiment as of 2016.[find current one](#)



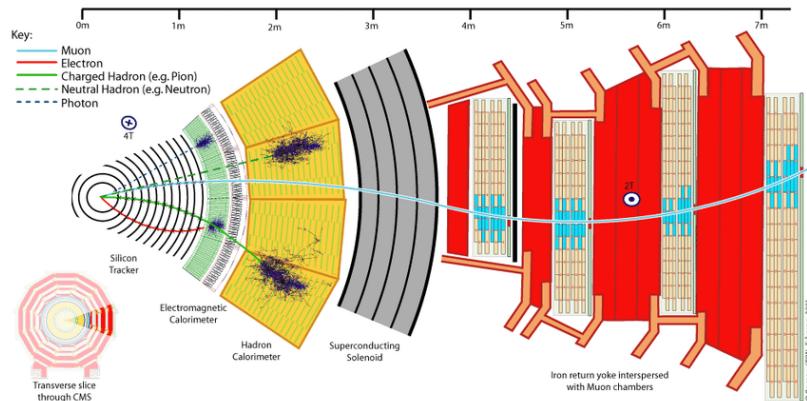
**Figure 2.3:** LHC dipoles.

vertices. (CMS SketchUp model by Tai Sakuma) (Image: CERN) fig1 gammagamma

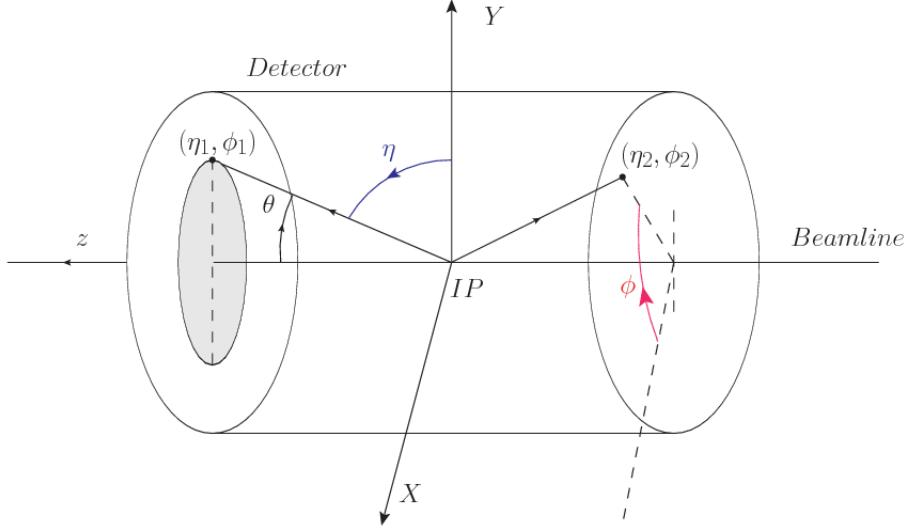
Describe from the outside the CMS experiment subdetector are: the muon chambers, the hadronic calorimeter, the Electromagnetic calorimeter, the superconducting solenoid, and the tracker detector which is composed of the silicon strips and the pixel detector.



**Figure 2.4:** CMS detector.



**Figure 2.5:** CMS cross sectional view.



**Figure 2.6:** CMS detector coordinate system [8].

### 2.2.1 The Muon Chambers

### 2.2.2 The Hadronic Calorimeter

### 2.2.3 The Electromagnetic Calorimeter

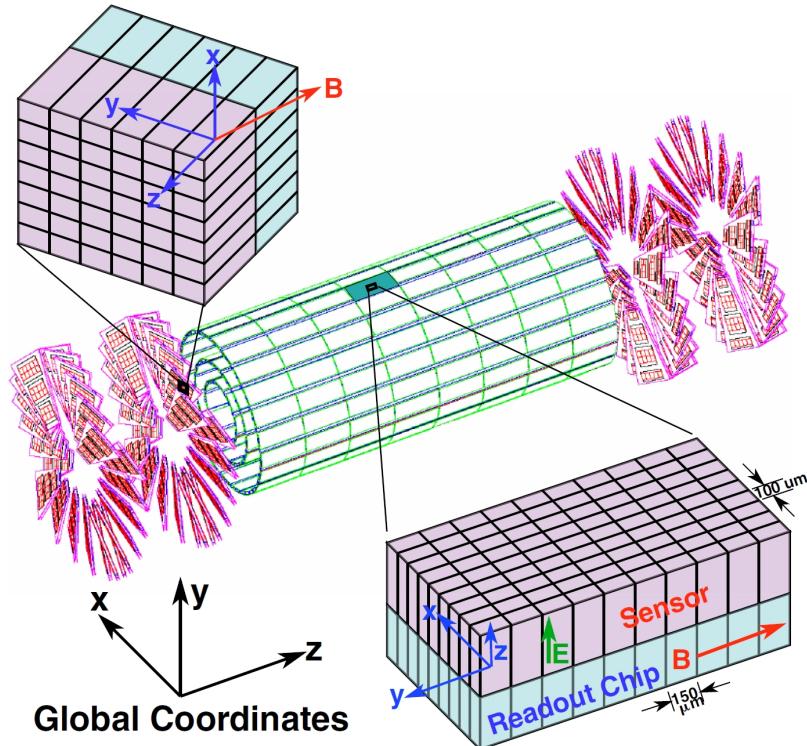
### 2.2.4 The Tracker Detector

#### 2.2.4.1 Silicon Strips

#### 2.2.4.2 Pixel Detector

Being the innermost detector in CMS, the pixel detector works in a high radiation environment but, due to its excellent design and construction, it performed well during the initial CMS run. It provided two or more hits per track, allowing secondary vertex identification of long-lived objects. The pixel detector is composed of two parts, the barrel (BPix) and a disk at each end, denominated Forward pixel detector (FPix), as showing in figure 2.7. The BPix is made of three layers located at 4.3 cm, 7.2 cm, and 11.0 cm from the interaction point respectively. The FPix has two layers, one at

34.5 cm and the other at 46.5 from the interaction point. This thesis will focus on the FPix, the part of the detector where UNL has made major contributions in the last **two** three decades.



**Figure 2.7:** Pixel detector.

The original FPix, also known as phase 0, was populated by 672 modules of 100 by  $100 \mu m$

## CHAPTER 3

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### The SM and BSM Theories

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It is the most succedfull scintific theory ever written. Proposed in the 1960s the standard model of particles physics has been successful in describing many phenomena of the particle world

## CHAPTER 4

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### **Event generation, simulation and reconstruction**

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Description of event generation and simulation

## CHAPTER 5

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### Search for the particle

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Data analysis details

## CHAPTER 6

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### More on the Analysis?

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More?

## CHAPTER 7

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### Module Production for the Phase I CMS Pixel Detector Upgrade

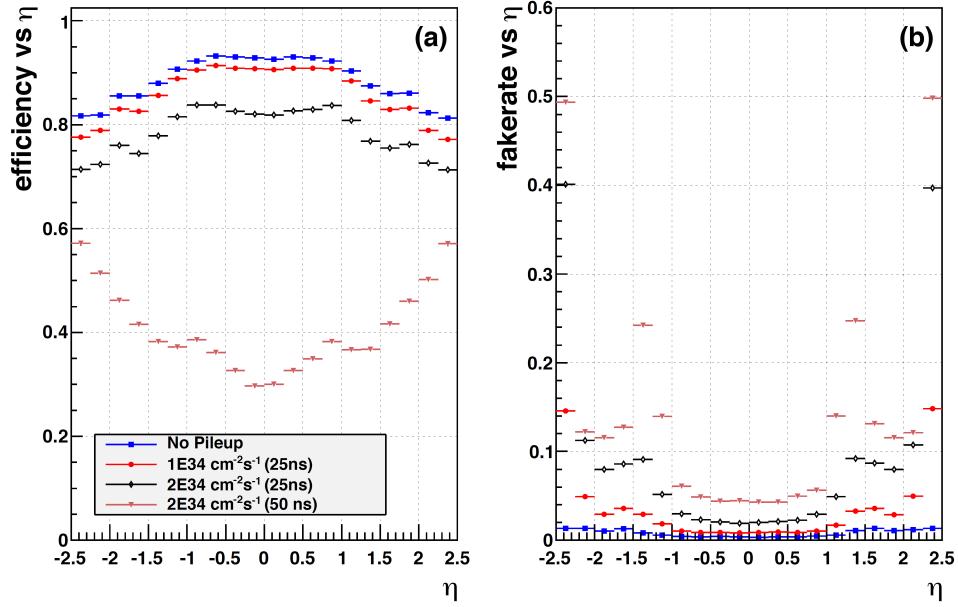
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As discussed in chapter 2 the CMS pixel detector will **suffer** from radiation damage throughout its lifetime hence the need for periodical upgrades. The first version of the detector was known as phase 0, it became fully operational 2010 after solving a setback during the original starting period in 2008. In 2017 the pixel detector was replaced during the so-called phase 1 upgrade, the University of Nebraska, high energy group (UNL-HEP) played a major role in assembling and testing over 500 modules, from 2013 to 2016, which then became part of the forward region of the pixel detector. The next update of this detector, the phase II upgrade, is projected to take place in 2025 when the current detector will be reaching its limits and its performance will be deteriorated. In this chapter we describe why the phase 0 pixel detector needed an upgrade making and **describe** the work done by the UNL-HEP group. Some of these steps will be highlighted and **described** in detail as they were my contributions to this production campaign.

## 7.1 The CMS Forward Pixel Detector Phase I Upgrade

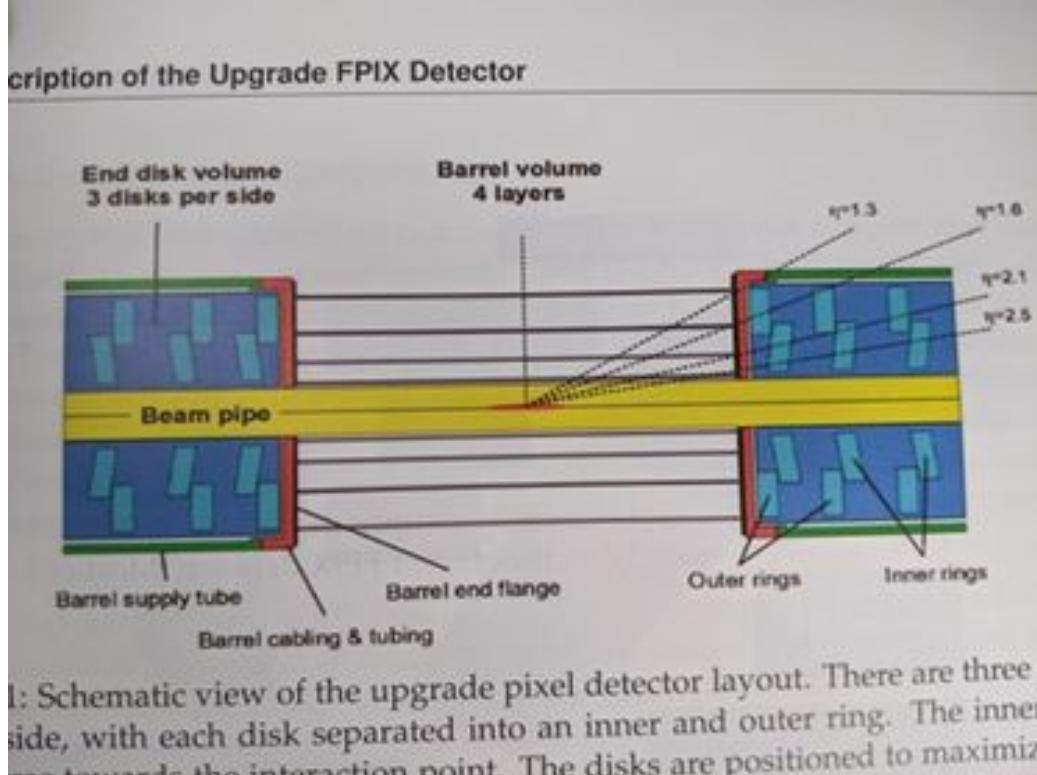
how many modules 768 or 672.

The phase 0 detector performed well during the LHC run I, taking data at an initial luminosity of  $7 \times 10^{33} cm^{-2}s^{-1}$ , which was then used in many analysis including the discovery of the Higgs boson published in 2013. But after a few years of operation the pixel detector started to degrade due to radiation damage, causing an increase of fake rates as well as loose on resolution. Moreover, for run II the LHC planned to double its luminosity with successive increment until it reaches its peak of  $2 \times 10^{35} cm^{-2}s^{-1}$ . A simulation of the performance of the pixel detector under different luminosity conditions can be seen in figure 7.1.



**Figure 7.1:** Expected performance of the original pixel detector under different luminosity conditions: a) track-finding efficiency; b) fake rate. Conventions are the same for both plots, considering zero pileup (blue squares), average pileup of 25 (red dots), average pileup of 50 (black diamonds), and average pileup of 100 (magenta triangles). [6].

The current forward pixel detector have three endcap disks located at 29.1 cm, 39.6 cm, and 51.6 cm from the interaction point. Compared to the old FPix, innermost disk is 4.4 cm closer to the interaction point. This provides a four-hit coverage for tracks ranging up to  $\pm 2.5$  in pseudorapidity, as showing in figure 7.2.



**Figure 7.2:** Schematic view of the pixel detector highlighting the positions of the disks to maximize the 4 hit eta coverage [6].

To reduce the extra material added by the extra layer of the pixel detector a lightweight support was used, a CO<sub>2</sub> cooling system was adopted, and inactive materials were moved from the tracking area. Figure 7.3 shows the amount of material needed for both the old and the current pixel detector as a function of eta.

Overall the geometry of the current FPix is similar to the old detector. The three disks are vertically divided into half-disks, and are composed of inner and outer disks. This allows for easy assembly and disassembly for repairs when necessary. Each of

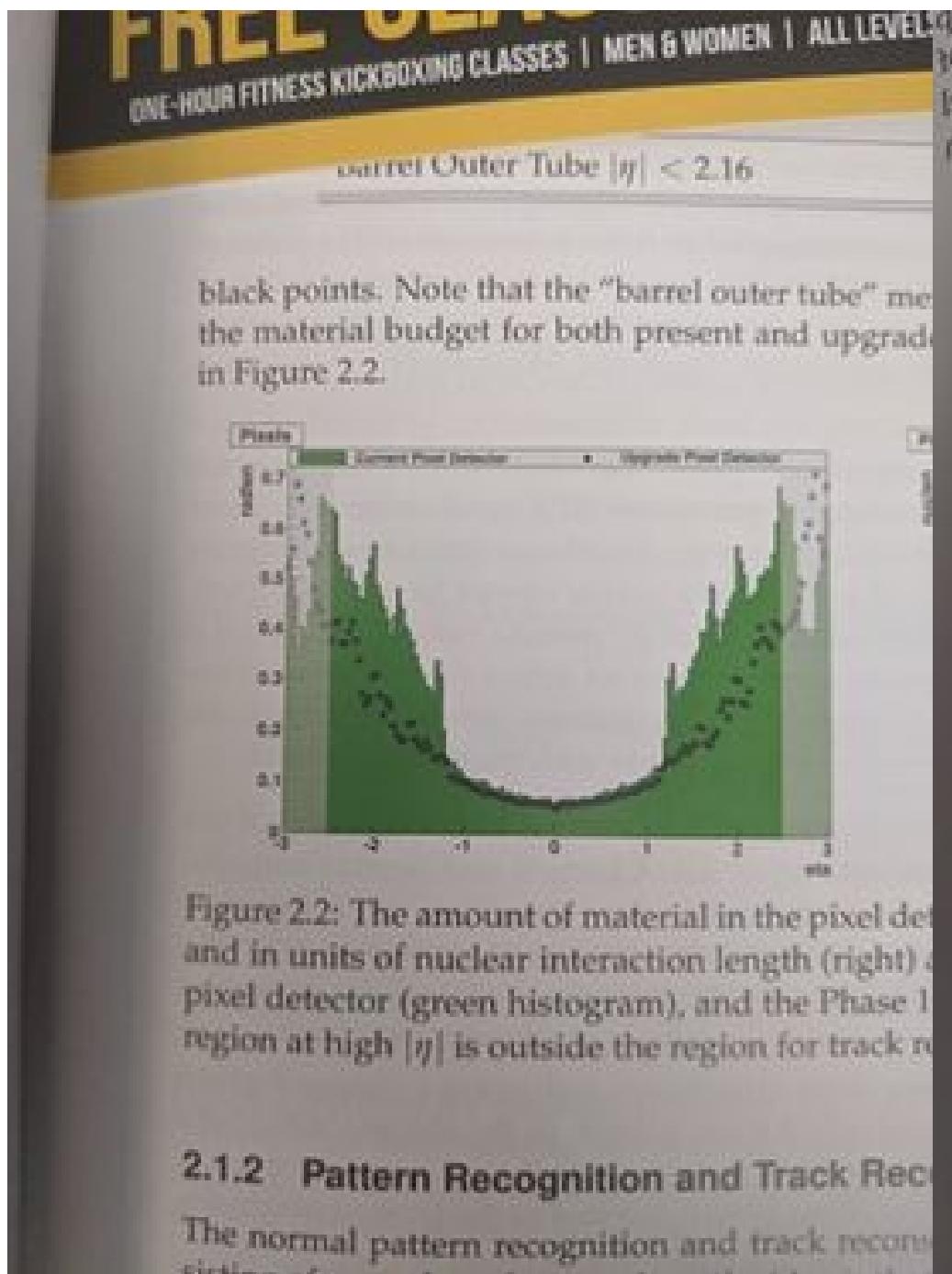


Figure 2.2: The amount of material in the pixel detector (left) and in units of nuclear interaction length (right) for the old pixel detector (green histogram), and the Phase 1 upgrade (black dots). The Phase 1 region at high  $|\eta|$  is outside the region for track reconstruction.

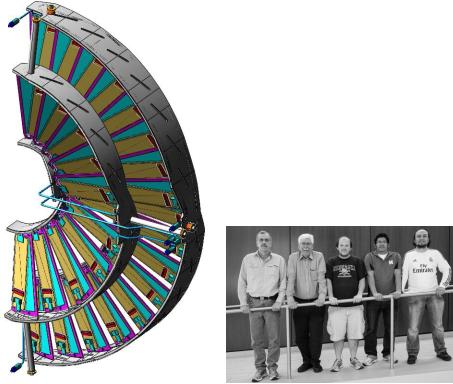
### 2.1.2 Pattern Recognition and Track Reconstruction

The normal pattern recognition and track reconstruction is done by the

**Figure 7.3:** Material used by the old (green histograms) and current (black dots) pixel detector [6].

these three disks are mounted on half cylinders, which also contains the CO<sub>2</sub> cooling tubes and the readout electronics as shown in figure 7.4. Each half disk contains 56

modules bringing the total number of modules for the FPix to 672. One key difference between the old and current detector is the use of one single module type in a 2x8 array. This made easier the installation compared to the old detector.



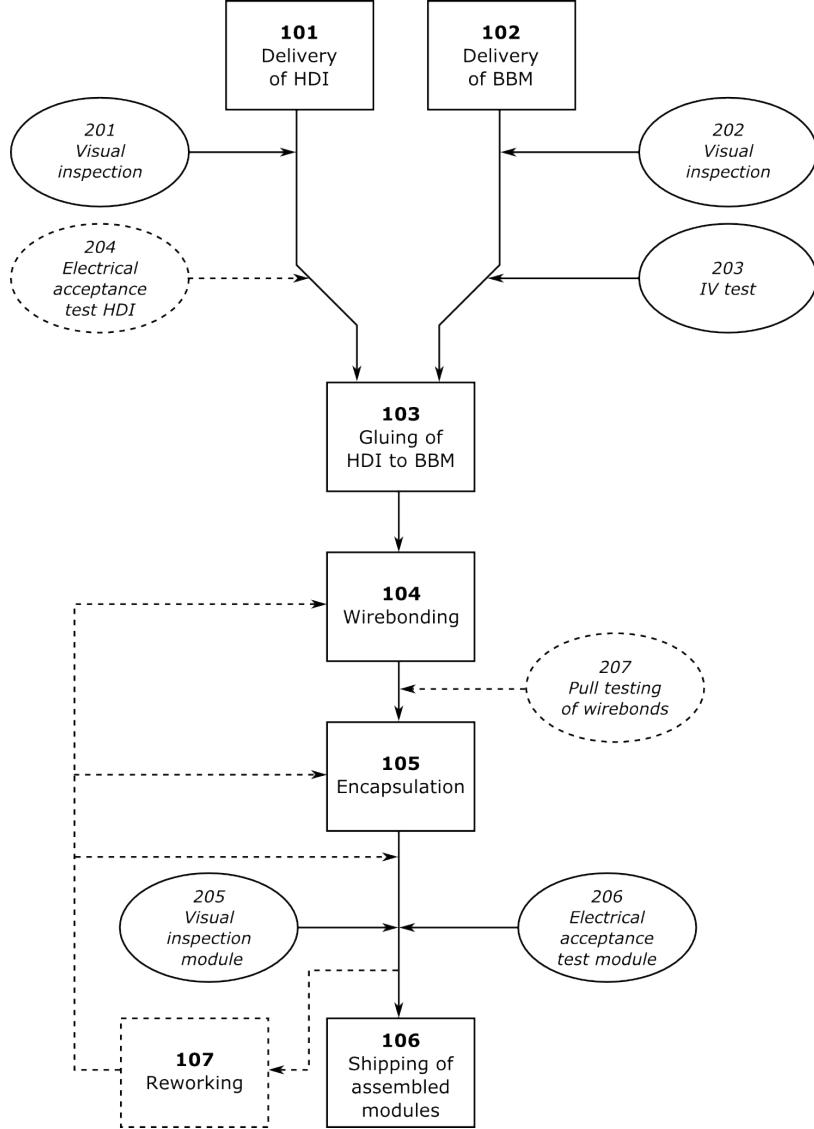
**Figure 7.4:** Half disks and half cylinder for the forward pixel detector [6].

Modules are mounted on the inner and outer half disks and not attached to the half cylinder. This allows damage modules to be replaced without having to disassembly the half cylinder. The modules in the inner ring are rotated by 12 degrees towards the interaction point to improve resolution in both the azimuthal and radial direction.

The size of the pixel is 100 x 150 mm.

## 7.2 Module Production at UNL

The UNL module production workflow was designed to follow a pipeline-like structure as shown in figure 7.5. This allows for different batches of modules to be going through it at different stages without stopping the workflow. Following is a short description of the tests and procedures performed during the production in the UNL silicon Lab. Special emphasis will be made in IV test, visual inspection and electrical test, the stages where the author of this work made a lot of contributions **improve**.



**Figure 7.5:** UNL module assembly workflow. Dashed lines represent occasional quality testing and reworking procedures [7].

### 7.2.1 Visual Inspections

The UNL-HEP group assembly workflow started upon receiving two components: a Bare Bonded Module (BBM) and a High Density Interconnect (HDI), see figure 7.6. The first stage of the module production was a visual inspection on these components to ensure they were in good conditions and able to continue into the production

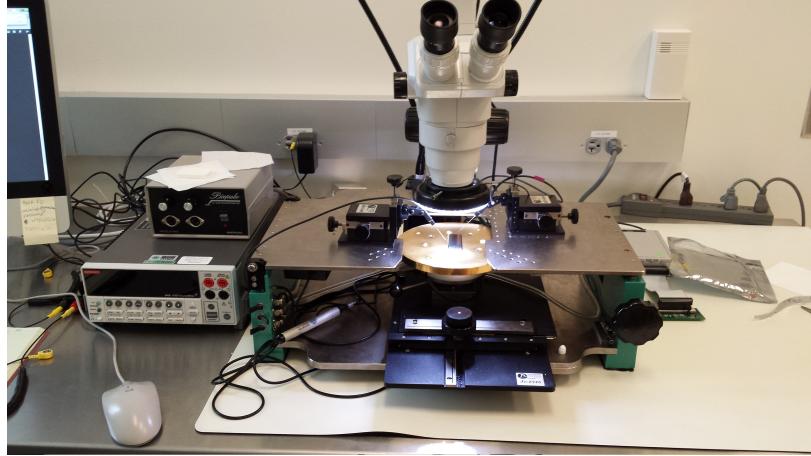
pipeline.



**Figure 7.6:** Photograph of a BBM (left) and HDI (right) as received by the UNL-HEP group.

To get a good view of such a small components a powerful microscope with magnification of [confirm](#), an attached camera, and LED ring illumination was used. A photograph of the set up, also referred to as probe station, is shown in figure 7.7. The entire set up was connected to a vacuum line to secure these component in place and

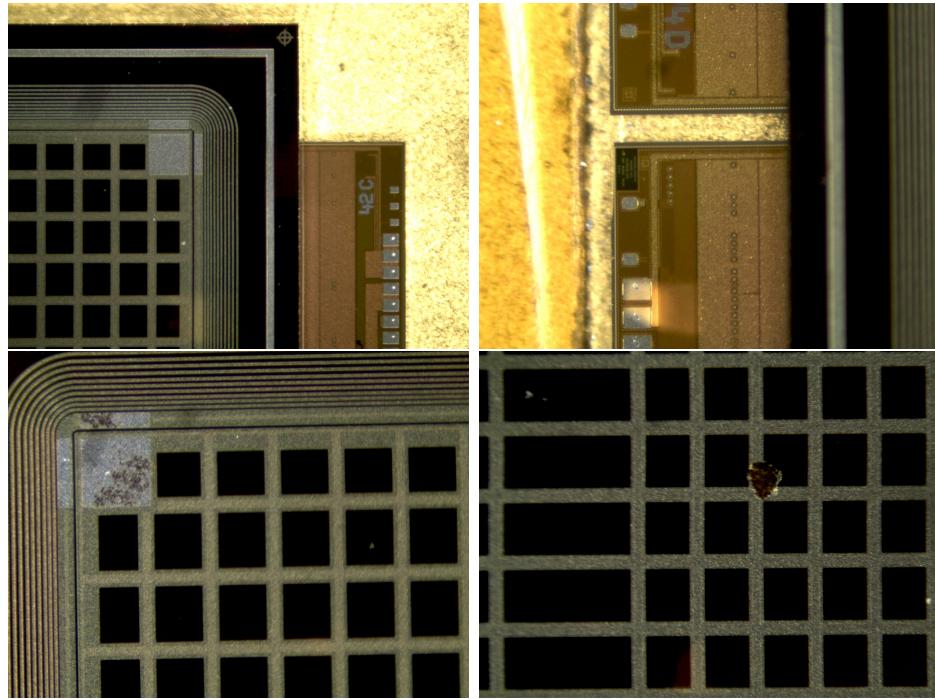
avoid any damage during the visual inspection. BBMs were received in a gel pack while HDIs were usually received in their modules carriers. BBMs and HDIs were then moved into the probe station using a vacuum pen and taking the appropriate safety precaution: ESD wristband, gloves, face mask, etc.



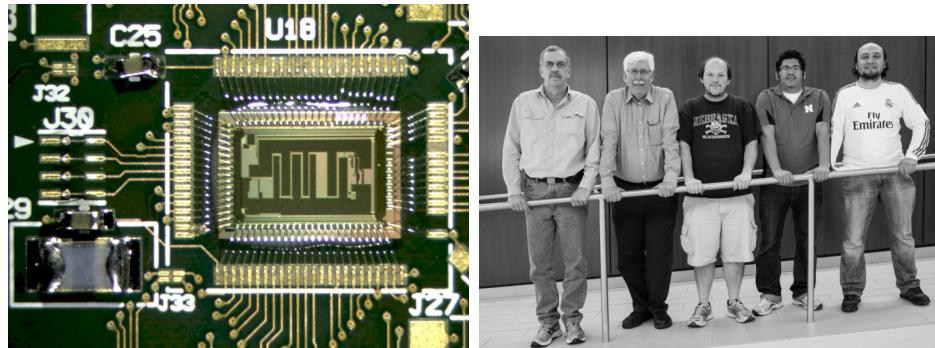
**Figure 7.7:** Photograph showing a BBM under the microscope during a visual inspection. This station also served as IV test stand.

During visual inspection BBMs were scanned for unusual features or sign of damage, special attention was given to the high voltage connection and bond pads. Figure 7.8 shows different parts of four different modules where defects on three of them could be observed. Some of these defects, bottom right figure, caused the module to be rejected immediately while others, bottom figures, will still undergo an IV test. While for the HDI the bond pads of the 16 ROCs, the wirebonds of the tbm, and the address pads were carefully checked. Figure 7.9 shows the TBM wirebonds as well as the bondpads of a ROC in a HDI.

Figures 7.8 and Fig. 7.9 also show a trend that was observed throughout the entire production phase. In general more unusual features and damage were observed in BBMs than on HDI. This was because BBM were delivered directly from the production company to our lab while HDIs were first delivered to the Fermi National



**Figure 7.8:** Photograph of the visual inspection of a BBM showing few of the things observed during a visual inspection: A good module (top left), chipped ROC (top right), scratches on the high voltage connection pad (bottom left), and scratch on the middle of a ROC (bottom right)

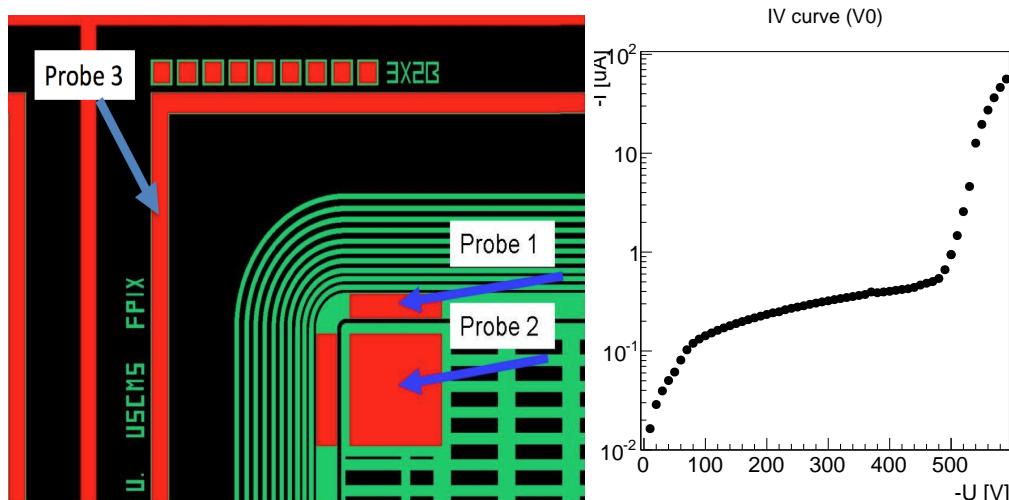


**Figure 7.9:** Photograph of the visual inspection of a HDI shwing the wirebonds of the TBM (left) and the bondpads of a ROC (right). [right fig](#)

Laboratory (FermiLab) where they were preliminary tested and inspected before they arrive at our testing facilities.

### 7.2.2 IV Test

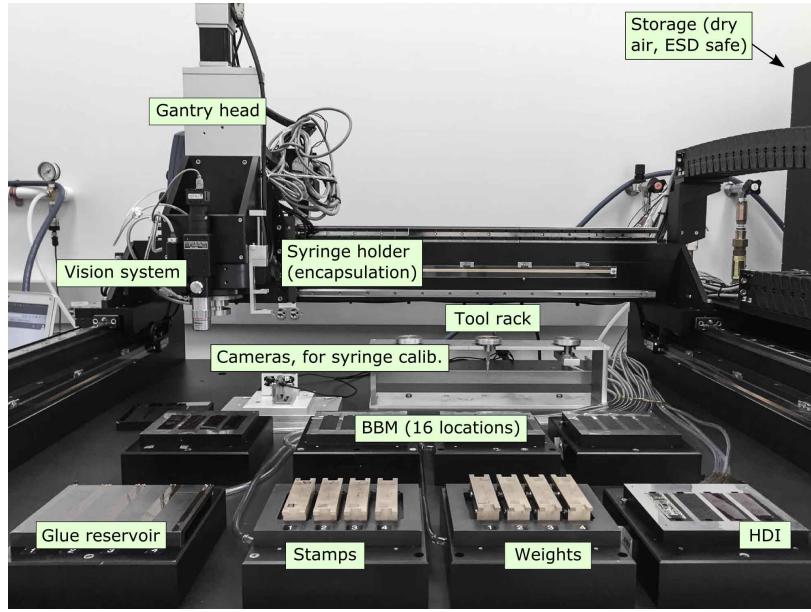
After both BBM and HDI have successfully passed the visual inspection the BBM continues to the probe station for a current vs voltage (IV) test. The test uses the fact that the sensor behaves like a diode. During operation a potential difference is applied to the sensor to draw the electrons created by a charge particle passing through the sensor towards the bump bond to be collected. If this potential difference is too small not all electron will be collected in time and if it is large the sensor could break. This potential difference is known as a depletion voltage. The IV test is meant to find the operating range, a voltage where all the electron could be collected and the sensor will not break, for a given module (sensor). Figure 7.10 (left) shows the position of the probes to perform an IV on a BBM and figure 7.10 (right) shows IV results for a BBM in good operating condition.



**Figure 7.10:** Left: Probe position for an IV test on a BBM. Probe 2 is high voltage, probe 3 is ground, and probe 1 was not used [7]. Right: IV test results for a good BBM. The depletion voltage for this module is around [confirm with right picture](#).

### 7.2.3 Gluing

The gluing routine was carefully designed to perfectly match the HDI and BBM bond-pads, in preparation for the wirebonding. This stage of the production was done using a custom made gantry, *AGS15000 Series Gantry*, fabricated by Aerotech [10]. It offered translational motion in 3D as well as rotation in x-y (gantry table) plane. A camera was attached to the gantry head allowing the user to monitor the entire process. This camera was of particular importance during the development and improvement of the gluing and encapsulation routine. A video showing the gluing routine in action can be watched at [9] and a full description of the gluing routine and procedure can be found in [8]. Figure 7.11 shows the gantry with the different tools used to glue a HDI on a BBM. The final product after the process is completed can be seen in Fig. 7.12.



**Figure 7.11:** Photograph of a gantry used for gluing and encapsulation showing different parts of the set up and tools.



**Figure 7.12:** HDI glued on top of a BBM. For a batch of four modules (top) and zoom in view to note the almost perfect alignment between the HDI and BBM bondpads.

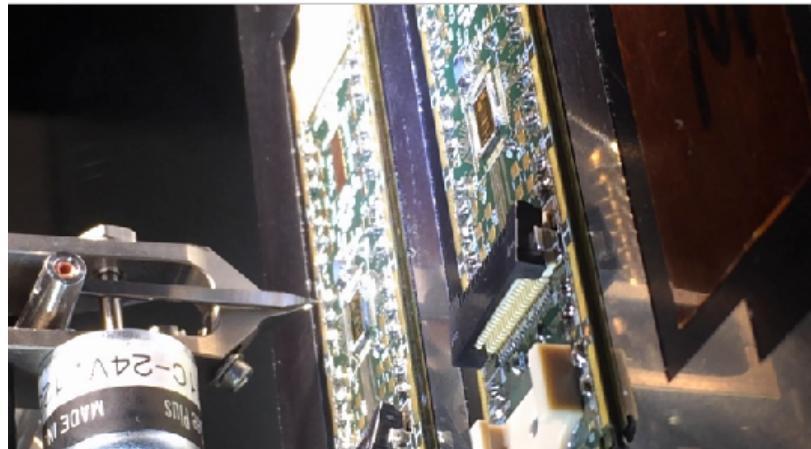
#### 7.2.4 Wirebonding

After an HDI is glued to a BBM the next step in the assembly process is to make electrical connection between them. To this end, a wirebonder machine, Delvotec 56XX, and aluminium wires of  $25\text{ }\mu\text{m}$  diameter were used. [need more](#)

Figures 7.13, 7.14 and 7.15 show the set up the process and the final product respectively



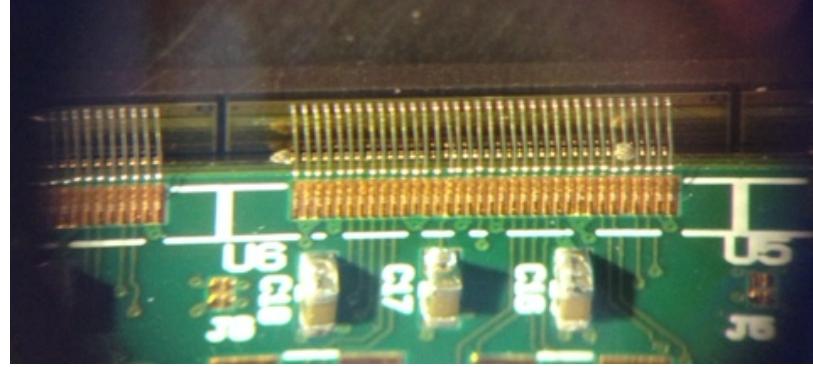
**Figure 7.13:** Wirebonding set up [find good picture of the wirebonder](#).



**Figure 7.14:** Wirebonder in action with a batch of two modules [?].

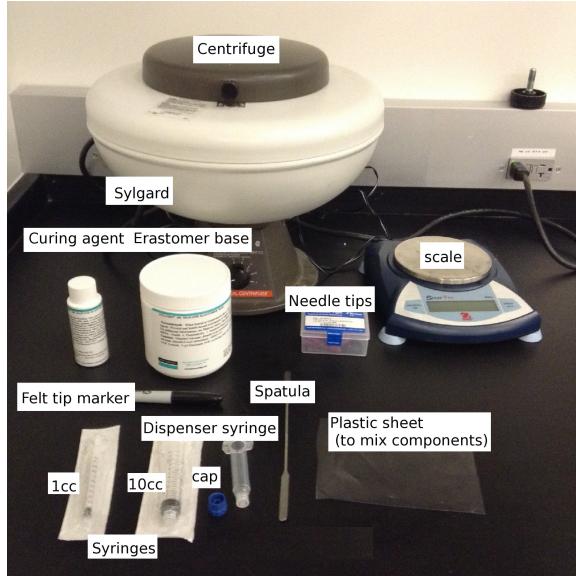
### 7.2.5 Encapsulation

The final step in manufacturing a module is to protect (cover) the wirebonds with an encapsulant, wirebond encapsulation. This procedure is necessary to ensure that the wirebonds are secure at both HDI and BBM ends. The set up and the equipment used is the same as for gluing showed in figure 7.11. Additional materials needed for



**Figure 7.15:** Close up view of the wirebonds for a single ROC on a wirebonded module.

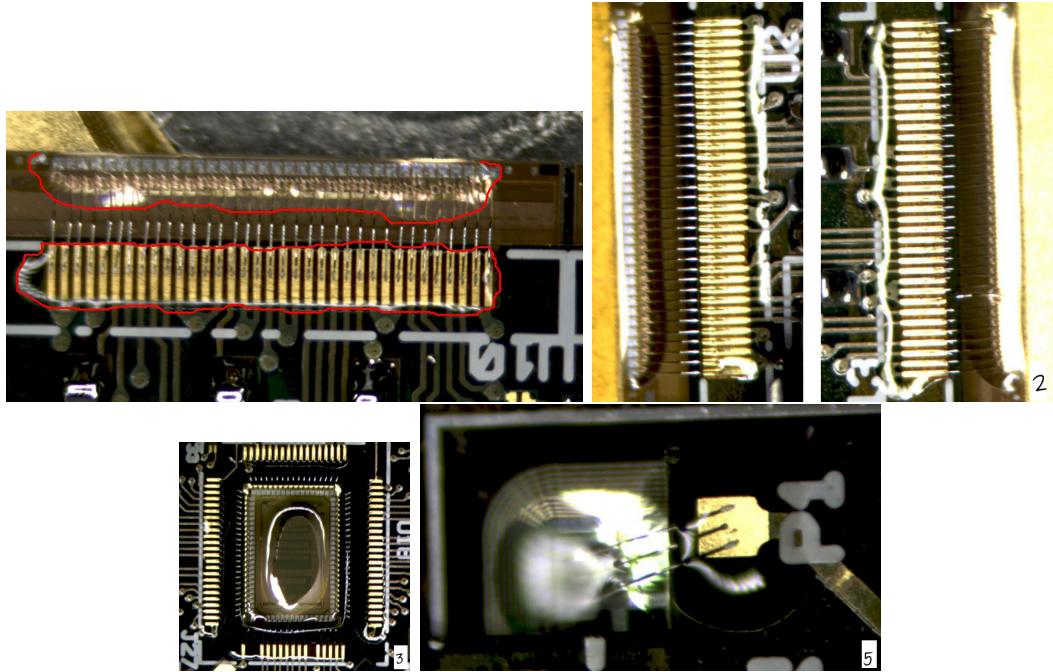
this step are shown in figure 7.16.



**Figure 7.16:** Wirebonds encapsulation materials [7].

A material suitable for this task must be radiation hard and lightweight among other properties. After testing different material and alloys we settle on *Silgard 186*, a mixture of two-component encapsulant. Erastomer (10 cc) and elastomer (1 cc) base and curing agent respectively. The components then, were mix together using a centrifuge and place in a syringe for dispensing. There are three components that need encapsulation, HDI and BBM bond pads, TBM wirebonds, and high votage pads.

Figure 7.17 shows a module after its different components have been encapsulated. Note how all bond foots and pads are fully covered as needed [8].

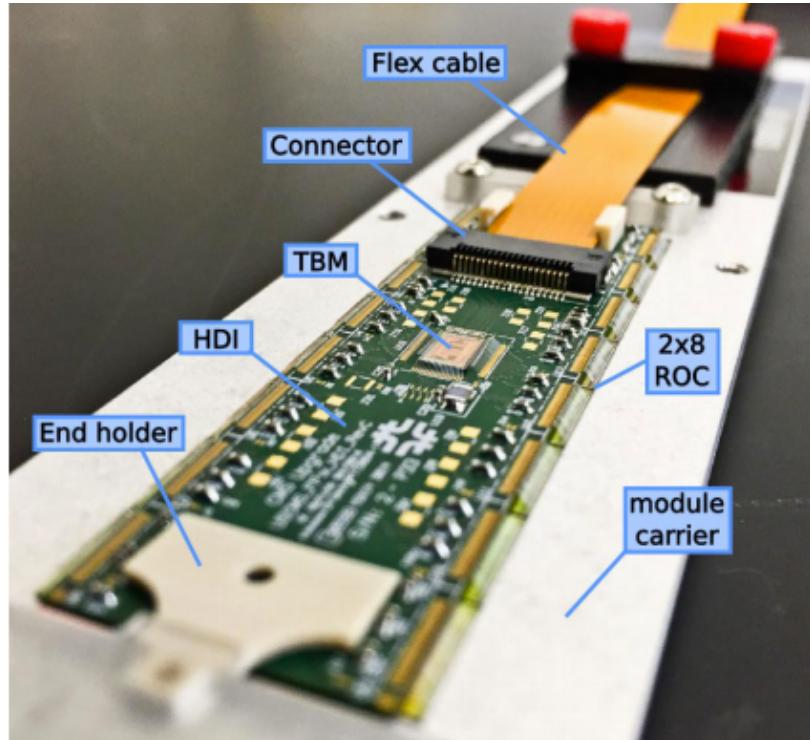


**Figure 7.17:** Wirebonds encapsulation of the components of a module. Top left, roc used as reference, the boundaries of the encapsulant are enhanced with red lines for better visibility. Top right, two ROCs on two different modules side by side, b) encapsulation of TBM, c) encapsulation of the high voltage pad.

## 7.2.6 Electrical Test of a Fully assembly Module

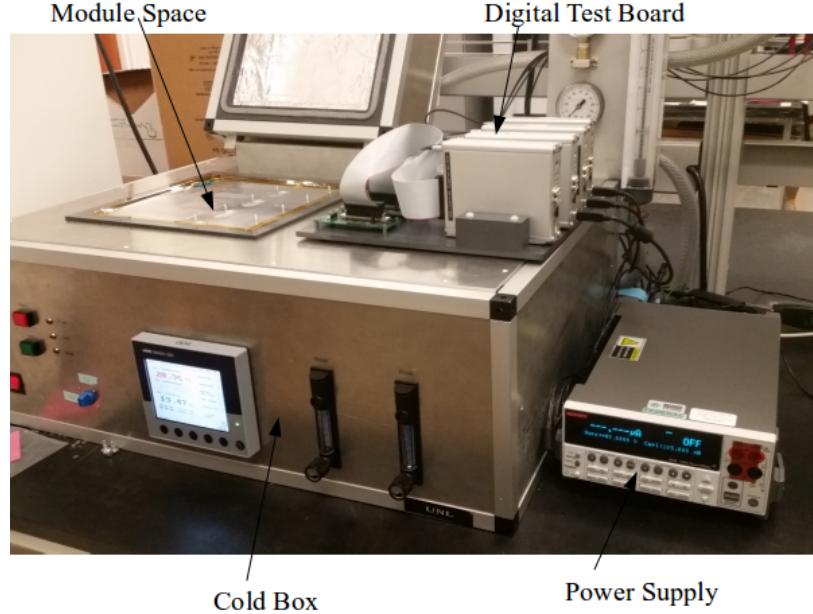
A manufactured module can be seen in Figure 7.18, it is then visually inspected and mark as ready for electrical test [at the end of previous session?](#). The electrical test, hereon fulltest, of fully assembly modules is done using the *pXar* software framework, written by the CMS FPix collaboration. More information on *pXar* can be found in [12]. The objective of the *Fulltest* is to ensure that all 16 ROCs were functional and have good performance. For this purpose a suit of several tests were designed and developed, the software is flexible in the sense that we could execute a single test

just by calling its name or we could execute them all with a single command *Fulltest* with the exception of the IV test. The *Fulltest* at UNL was done using the set up showing in figure 7.19 at a temperature of  $17^{\circ} C$  and using a depletion voltage of  $-150 V$ . The set up allowed us to test up to 4 modules in parallel using a software called *ElComandante* [?] written specifically for this purpose. The modules are connected via flex cables to adapter cards which convert the data into SCSI format. Each adapter card is connected to a digital test board and the data is finally transferred to a computer via an USB cable. The temperature inside the colbox was controlled by a chiller.



**Figure 7.18:** Fully assembly Module

The following section [subsections?](#) give a short description of the most *important* tests a module has to surpass as well as the output of these test. A full list of the tests, a comprehensive description of them, and a [description](#) of their purpose can



**Figure 7.19:** Fully assembly module testing set up

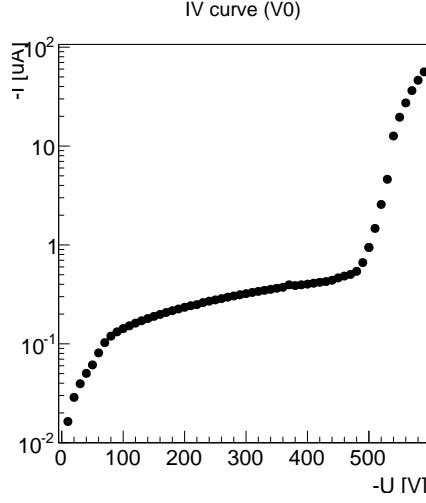
be found in [13] and references therein. After the *Fulltest* of modules was completed some were shipped to Kansas university for X-ray testing and the rest were shipped to FermiLab for testing at  $-10^{\circ} C$

#### 7.2.6.1 IV Test

A fully assembled module also undergoes an IV test as described in 7.2.2. The primary purpose of this test is to ensure that no damage was caused to the circuitry during the assembly process and the module could be operated at high voltages. The IV result for a sample module is shown in figure 7.20. The operational range for this particular module is between -100 V and -400 V.

#### 7.2.6.2 Pretest

It is composed of several subtests and its purpose is to check the basic functionalities of the ROCs and to calibrate some of the DAC [list of DAC here or in ch 2?](#) settings. A

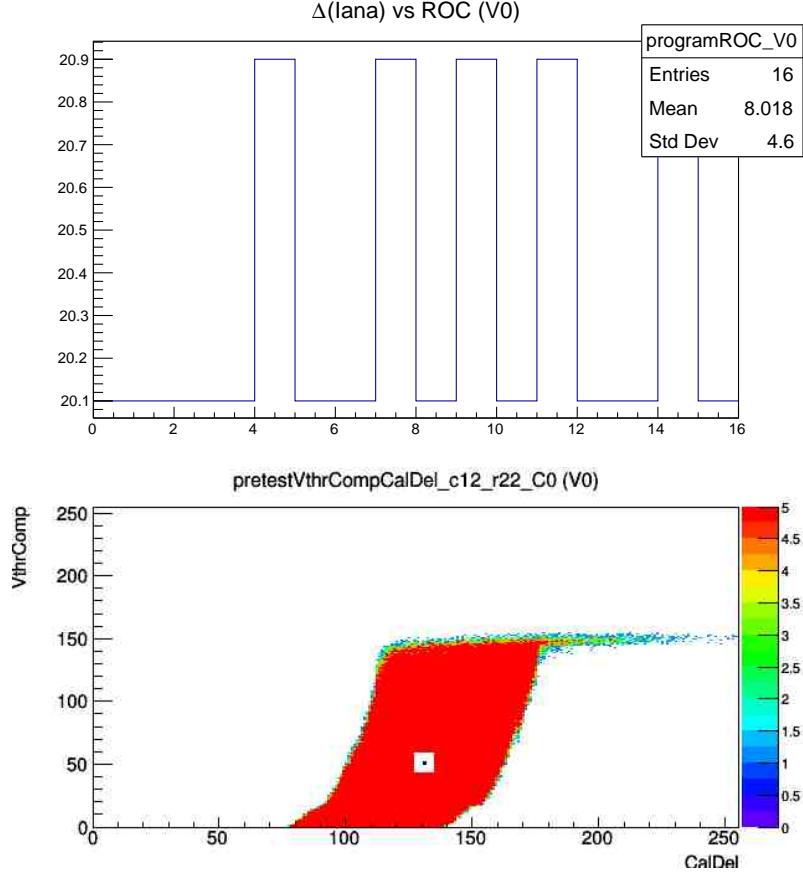


**Figure 7.20:** IV test for a fully assembly module.

couple of these subtests are *ProgramRoc* and *SetVthrCompCalDel*. The *ProgramRoc* measures the difference in current ( $I_{ana}$ ) drawn by the amplifiers when a voltage ( $V_{ana}$ ) is applied and remove. If the difference between these two measurements is non-zero it implies that we are able to change DAC values by sending a command, the ROC is programmable. This test is done for all 16 modules in a ROC. The *SetVthrCompCalDel* subtest is done to optimize the value of the *VthrComp* and *CalDel* DACs. It chooses a pixel from within a ROC and sends 5 calibration pulses to the PUC of this pixel. This process is repeated for the  $256 \times 256$  parameter space of these DACs and the response of the pixel is read to make an efficiency plot. Then *VthrComp* is set to the lower plateau plus 50 units and *CalDel* is set to half of the left and right edges. This is known as the *VthrComp* and *CalDel* working point of the pixel. Figure 7.21 shows the output of these subtests for a sample module

### 7.2.6.3 Pixel Alive

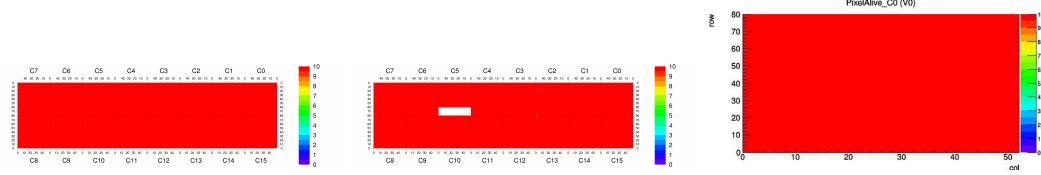
In the pixel alive test three subtests are performed: *Alive test* checks for the response of a pixel by sending 10 calibration pulses (hits) to it and recording how many the



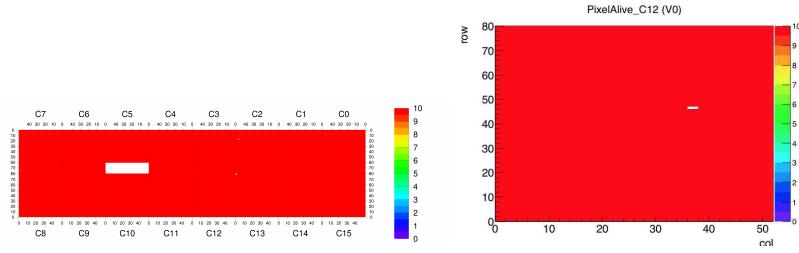
**Figure 7.21:** Output of the ProgramRoc (left) and finding working pixel (right) subtests.

pixel reports back. Pixel with 10 hits are marked as good, those with less than 10 hits are flagged as faulty, and those with zero hits are called dead. In the *Mask test* all pixels are disable and the same efficiency measurement is done. Pixels with zero efficiency are marked as good while those with efficiency grater than zero are bad. The *AddressDecoding* test checks the specific address of the pixel within the ROC. If the response of the pixel does not match the address to which it was sent the pixel is marked as bad. repeats the same procedure but checks that the order of the resulting data. If the address of a given pixel is out of order, the recorded hit is given a negative pulse height value. Pixels with negative hits are flagged as faulty. Figure 7.22 shows the result of the pixel alive test for a fully working module and Figure 7.23 shows a

module with faulty ROC and a ROC with faulty pixels.



**Figure 7.22:** Pixel alive test for a fully assembled module. a) Alive test, b) Mask test, and c) AddressDecoding test.

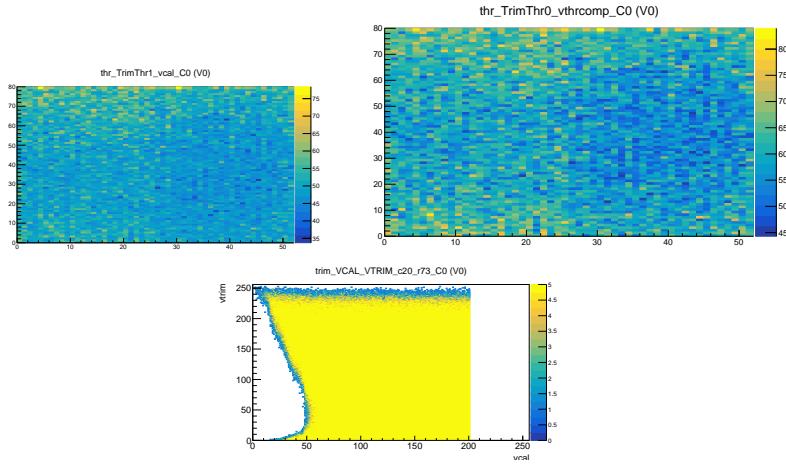


**Figure 7.23:** Pixel alive for a fully assembled module. a) a module with a faulty ROC and b) a ROC with faulty/dead pixels

#### 7.2.6.4 Trimming Test

The aim of the the trimming test is to (calibrate) set the threshold of all pixel on a ROC as uniform as possible. It attempts to do this by varying the VthrComp, Vtrim, and Trim bits DACs. The Trimming test sets VthrComp and Vtrim for the entire ROC and then uses trim bits to further refined the threshold of individual pixels. After the trimming test is finished all pixels within the ROC **will have a threshold value as low as possible but still higher than the electrical noise**. Furthermore, a TrimBits subtest verifies that all trim bits are working by sequentially enabling each bit and observing its effect on the pixel threshold distribution. The trimming test works as follows: first, with Vcal set to a target value, it finds the VthrComp turn-on value by producing S-Curves for all pixels with respect to VthrComp. Then, VthrComp is set to the value of the pixel with the lowest turn-on value. A ROC map distribution of

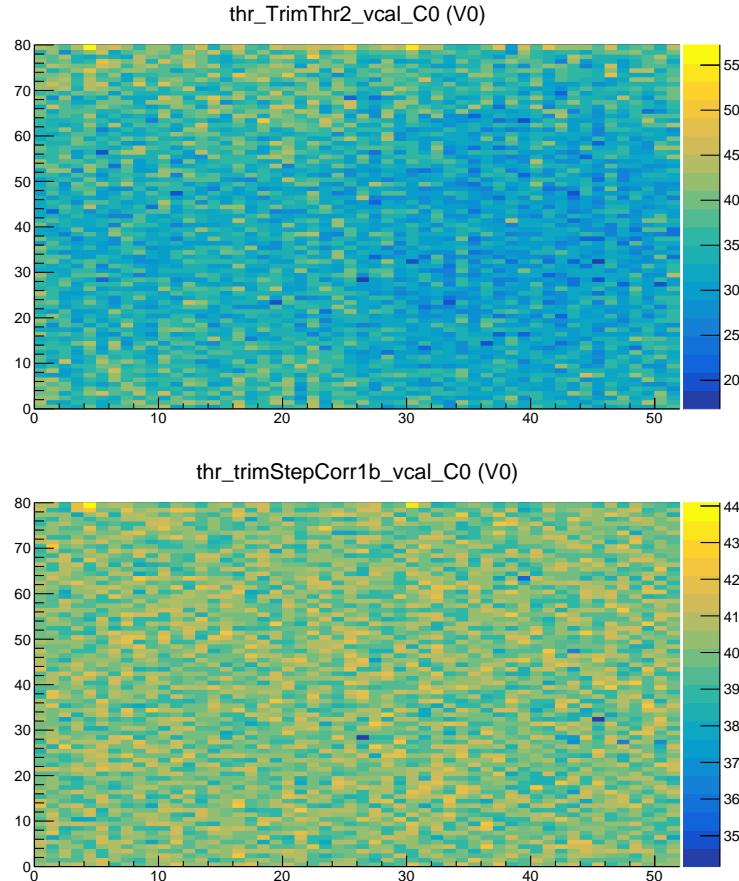
turn on values for a ROC can be seen in figure 7.24. Then, with the VthrComp set to its lowest value, the test tries to minimize the Vtrim value by repeating the previous process and finding the pixel with the highest Vcal turn-on value, see Fig 7.24. This is the pixel that requires the most trimming to have its Vcal threshold reduced to the target value. Following, with all trim bits enabled, the test performs an efficiency scan over Vtrim and Vcal DACs 7.24 to find the value of Vtrim that corresponds to a turn-on at the target Vcal.



**Figure 7.24:** Trim test optimization for. left: Vcal turn on, center: Vthr turn on, right: efficiency in the Vtrim-Vcal plane.

Next, starting from a high Vtrim, its value is iteratively lowered until the Vcal turn-on surpasses the target Vcal, which corresponds to the minimum value that can trim this pixel. This is the final value of the Vtrim DAC for the the ROC. Finally, with the values of the VthrCaomp and Vtrim set, the test refine the threshold on each pixel by modifying the 4 Trim bits. Starting with the Trim bits set to 7 [0111], scurves are used to find the Vcal turn-on value. If the pixel **reports a hit** fires below (above) the target Vcal value, the Trim bits value is increased (decreased) by 4, so that the amount of trimming is decreased (increased). This process is repeated three more time increasing or decreasing the Trim bits values by 2, 1, and 1 unit respectively,

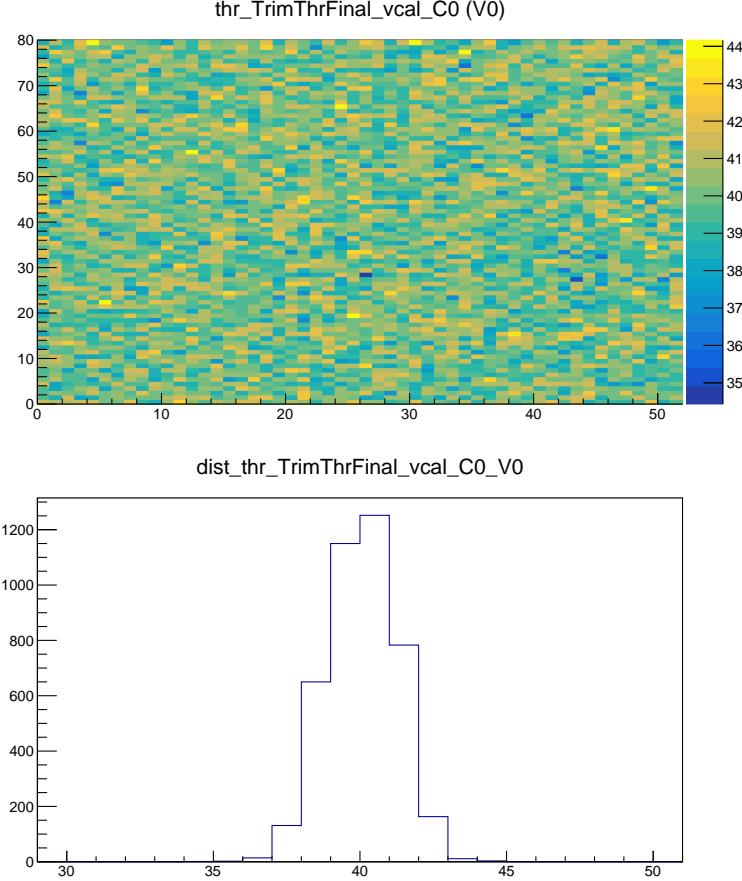
covering the full range, 0-15, of the Trim bits. Figure 7.25 shows a ROC map of Vcal for Trim bits = 7 and after 4 corrections are made and the final Vcal map and distribution could be seen in figure 7.26.



**Figure 7.25:** Trim bits map distributions for the Vcal turn-on values for the initial and final Trim bits values.

### 7.2.6.5 PH Optimization

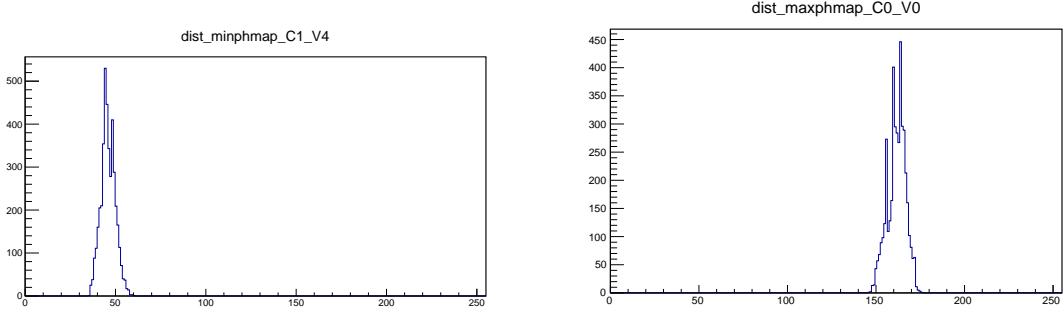
The PHOptimization test is responsible for setting the dynamic range of the output pulse height (PH) as calculated by the ADC serializer. It accomplishes this by optimizing the *PHOFFSET* and *PHSCALE* DACs, which adds a constant offset to the pulse height measurement and sets the gain of the ADC. *PHOptimization* works in the fo-



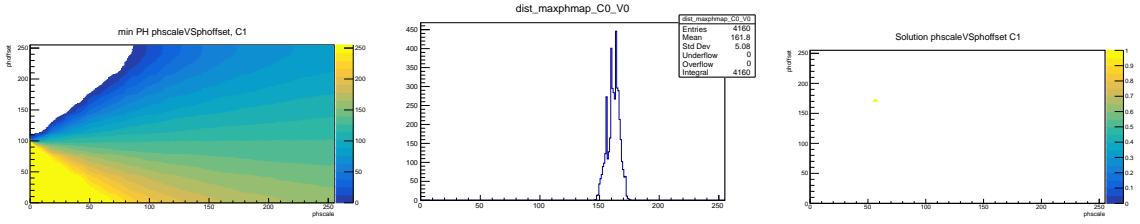
**Figure 7.26:** Final map and distribution of Vcal threshold after the Trim test have finished.

llowing way: First it identifies a low gain and a high gain ensuring it is working (good in pixel alive) and as far as possible from the edges of the sensor. Then, two Vcal signals, low = 60 and high = 255, are sent to each pixel in a ROC and 1D distribution of the PH is created for each vcal value, see figure 7.27. A pixel close to the center in each of these distribution is selected as the low and high gain pixel for that ROC.

After both pixels have been identified the test optimizes *PHScale* and *PHOffset* by performing a 2D scan over these two DACs plane. The output of these scan is showing if figure 7.28. The final value of the DACs are chosen from the interception of these two plots as showing in figure 7.28c.



**Figure 7.27:** Distribution of PH as a function of Vcal used to indentify low (top or left) and high (bottom or right) gain pixels.

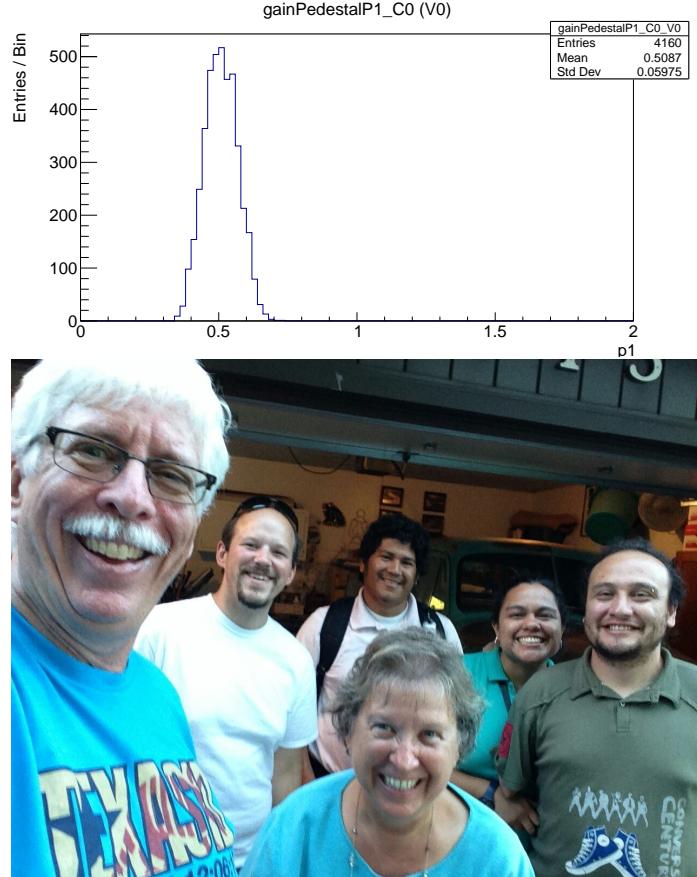


**Figure 7.28:** Scan on the PHOffset-PHScale plane used to optimize these DACs. a) for a low gain pixel, b) for a high gain pixel, c) interception of a) and b) showing the values of PHOffset and PHScale.

#### 7.2.6.6 Gain Pedestal

The *Gainpedestal* test measures and records the variation in gain for each pixel in a ROC. Since each pixel will have a different gain these values are needed to calibrate the PH to an input signal. It produces a PH vs. Vcal curve and fits it with an error function recording the its 4 parameters. Parameter 0 corresponds to the Vcal value at the center of the error function. Parameter 1 is proportional to the width of the turn-on and is therefore inversely related to the gain of the pixel. Parameter 2 shifts the error function upwards, with a value of unity moving the floor of the function to zero. Parameter 3 corresponds to half the height of the function, and should be near 127.5 ( $255/2$ ). *include equation?* The test also measures the linearity of the pixel response by comparing the integral of the fitted error function in the vcal range to a linear approximation. The results of the test for parameter zero and its linearity are

shown in figure 7.29.

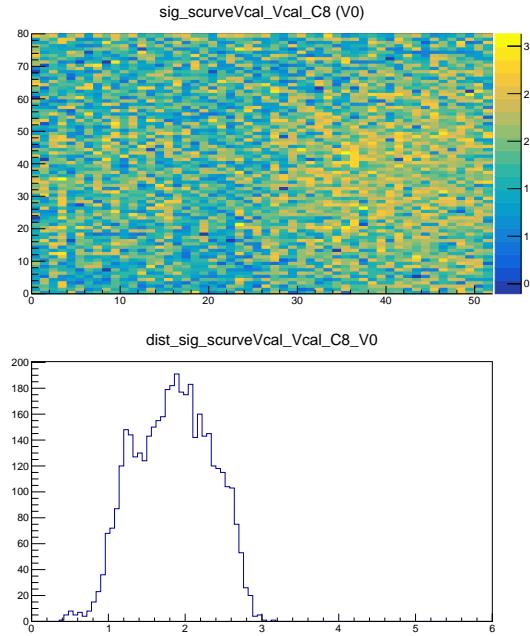


**Figure 7.29:** Results of the *GainPedestal* test. a) parameter 0 and b) linearity test [find figure](#)

#### 7.2.6.7 Scurve Test

The SCurve test measures the efficiency of a pixel as a function of Vcal. It is based on the assumption that a pixel will not respond to lower values of Vcal but it will always respond for higher values. In the absence of noise this curve will be just a step function which changes from zero efficiency below the threshold to a region of 100% efficiency above. The effect of the noise is to smear out the step function giving it a *S* shape. As the noise is assumed to follow a Gaussian distribution, the SCurve if fitted with an error function and its width is a measure of the noise level in the pixel. Since

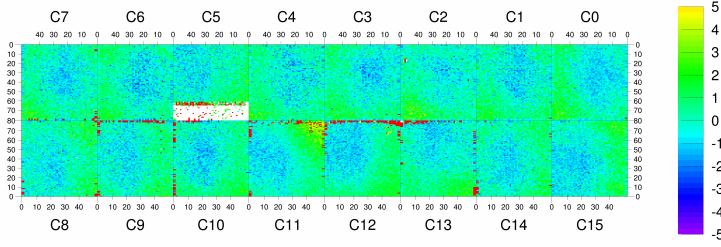
the Vcal is known at this point in the testing procedure the SCurve is done around this Vcal value. In order to extract an accurate estimate of the width the number of triggers used for the test is 200. The output of this test can seen in figure ??



**Figure 7.30:** Left: ROC map of the Vcal s-curve turn-on widths. Right: 1D distribution of the vcal scurve width.

### 7.2.6.8 Bond Bonding Test

could be better, include the ROC-Sensor air gap? The primary purpose of the *Bump-Bonding test* is to identify problems with the bumps connecting the sensor to the ROC. The test works by a calibration signal to the sensor via the alternatively path labeled 'sensor calib' 7.34. The signal then reaches the sensor and makes its way to the ROC via the bump bond where it can be normally read. The strength of the signal is measure and compare to the one sent. In the *pXar* software usually 5 signal of 250 Vcal units are sent to each pixel during a *BumpBonding* test. The *output* of the test is shown if figure 7.31



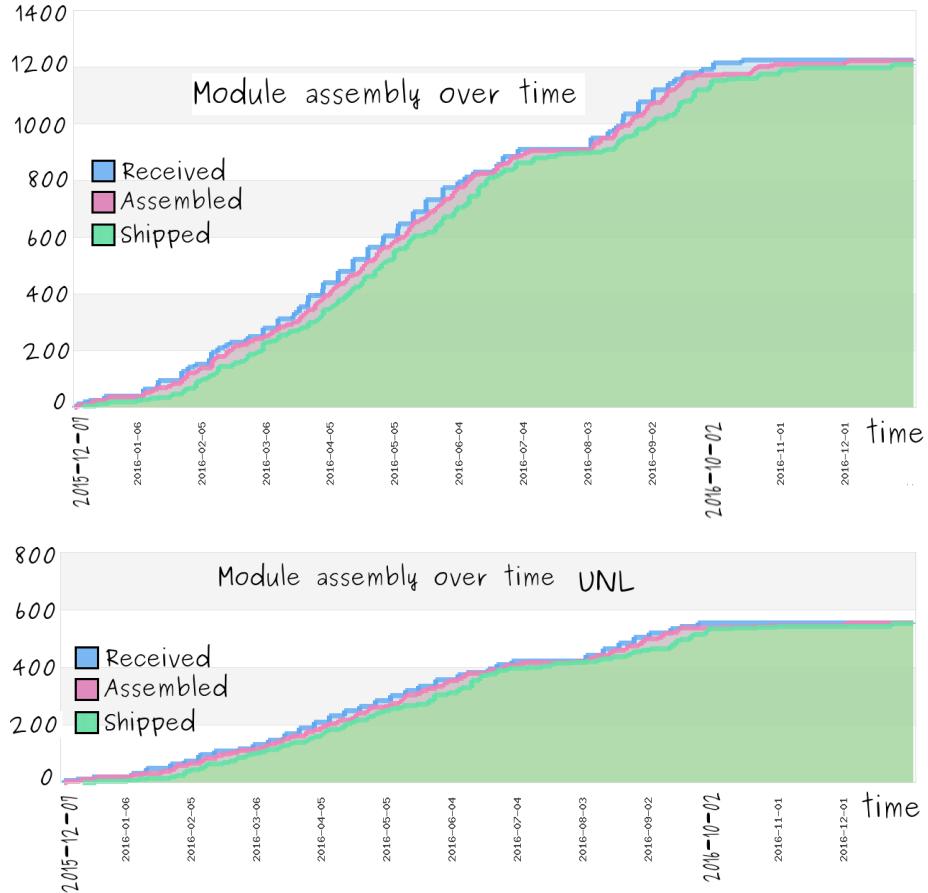
**Figure 7.31:** Bond bonding test.

#### 7.2.6.9 Summary

The UNL-HEP module production was a successful project that culminated with the production and testing of over 500 modules. Figure 7.32 shows the module production over time for both assembly sites, UNL and Purdue University. Production started slow for the first two months but ramped up after fixing some issues with the parts. Besides that the other time when production almost stopped was around July of 2016 when the BBM provider had difficulties and could not supply BBMs on time. [include purdue database](#)

Following the production and testing these of modules a grading scheme was adopted. The grade of a module was given based on the amount of current drawn by it at nominal operating voltages and the number of pixel defects. UNL graded modules at  $17\text{ }^{\circ}\text{C}$  but the final grade of the modules was given at FermiLab, where the *Fulltest* was done at  $-10\text{ }^{\circ}\text{C}$ . Table 7.1 shows the grade names and the requirements a module needs to meet to obtain this grade. Since there are 672 modules needed to populate the forward part of the pixel detector and there were not enough grade A modules, some parts of the outer most cylinder was populated with grade B modules.

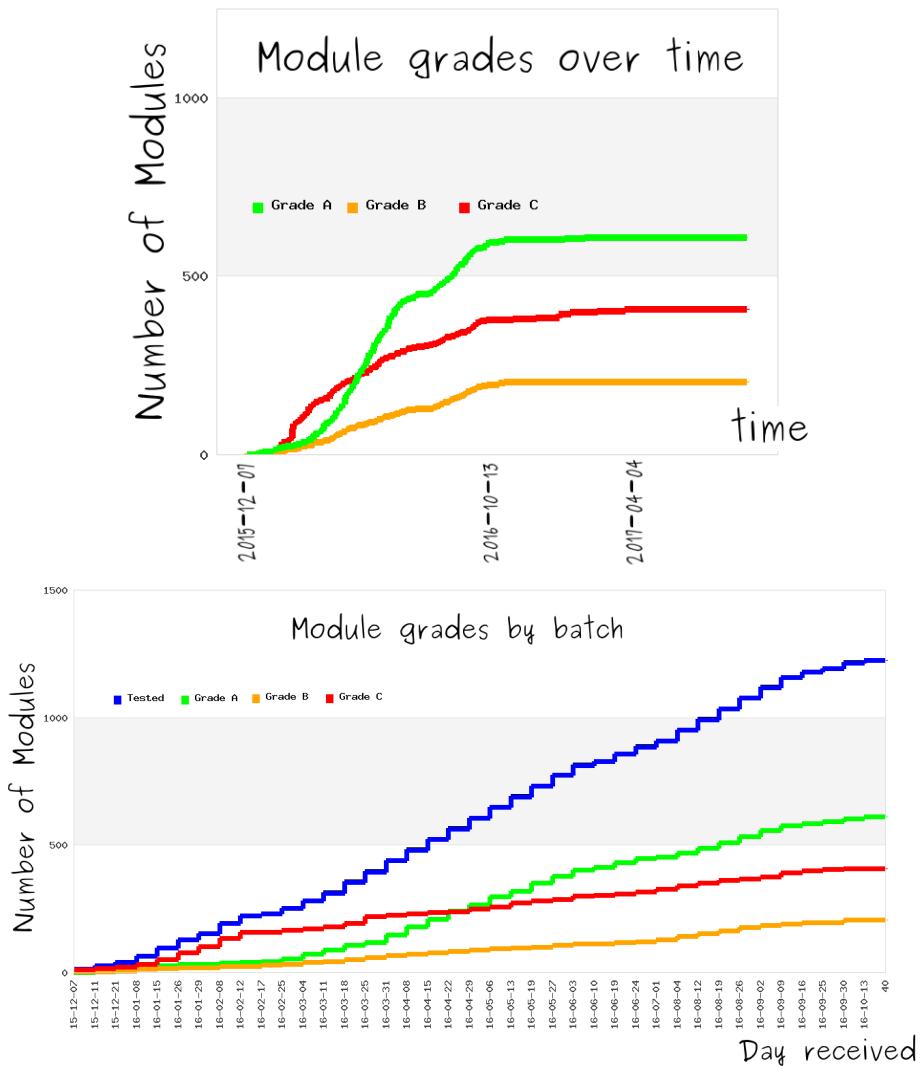
Figure 7.33 shows graded modules over time as well as the module grading by batch received and tested at FermiLab. The integration of the modules into the half cylinders was done at FermiLab, they were later transported to Switzerland and installed into the CMS detector.



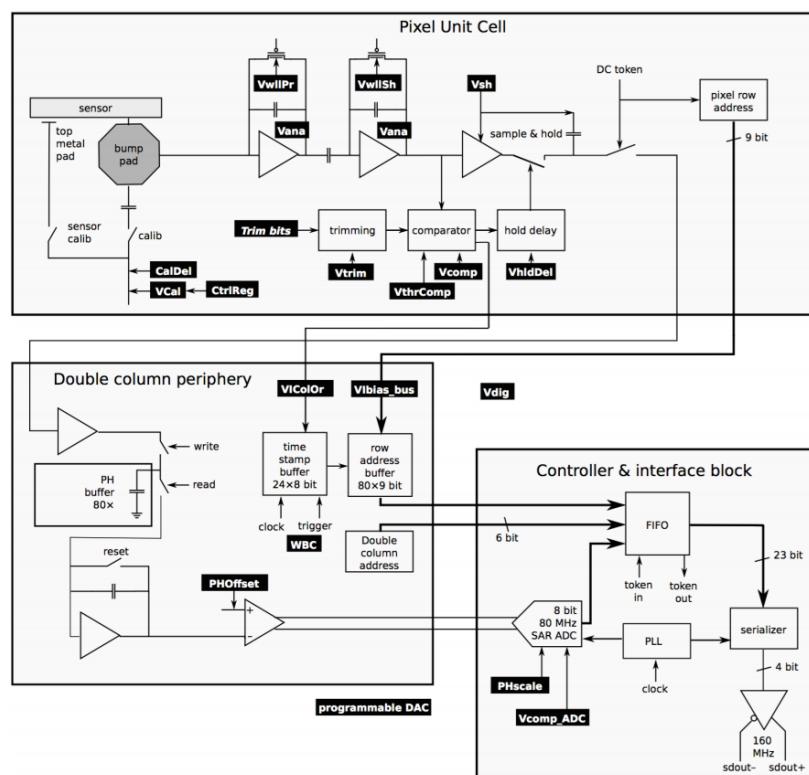
**Figure 7.32:** Module assembly over time for both assembly sites (top) and for UNL (bottom).

Grade	$I(V=-150V)$	$I(V=-150V)/I(V=-100V)$	Pixel defects
A	$< 2\mu A$	$< 2$	$< 1\%$
B	$< 10\mu A$	$< 2$	$< 4\%$
C	$> 10\mu A$	$> 2$	$> 4\%$

**Table 7.1:** Module grades for the Fpix phase I module production.



**Figure 7.33:** Module grade over time (top) and per received batch at the integration site(bottom).



**Figure 7.34:** A schematic view of a pixel circuit showing the PUC, CIB, DCP, and some of the relevant DACs.

## CHAPTER 8

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### **Beam Test of the RD53 chip for CMS Pixel Detector Upgrade Phase 2**

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#### **8.1 Introduction**

#### **8.2 The RD53 Chip**

#### **8.3 Purpose of Test Beam**

#### **8.4 Test Beam Set Up**

#### **8.5 Results**

## CHAPTER 9

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### Conclusions

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#### **9.1 Analysis**

#### **9.2 Phase 1**

#### **9.3 Beam Test**

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