Lab 05

ECE 171L

Lab Section - Thurs. 5:30p - 7:30p

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March 2, 2022

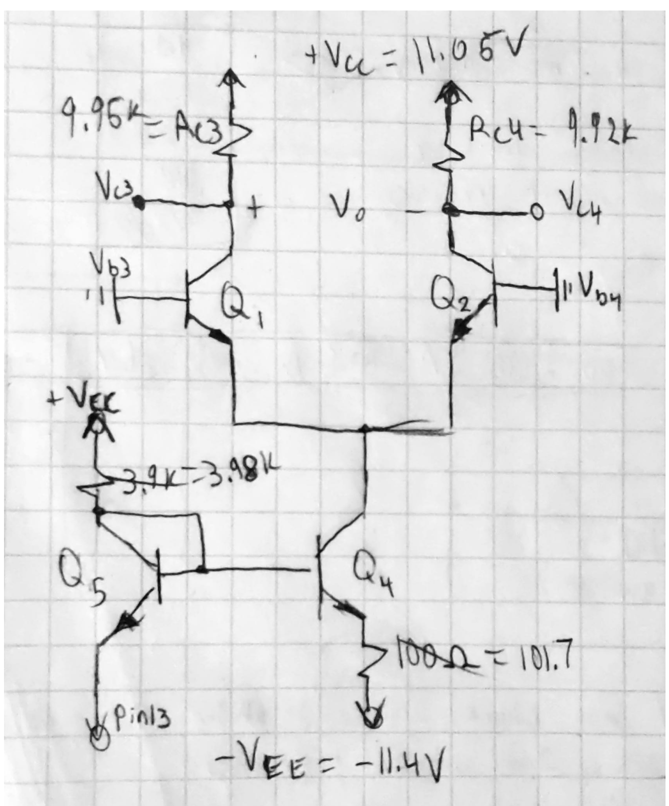
1 Introduction and Overview

The general purpose of this lab was mostly implement a differential amplifier using the BJT IC using a circuit named the "Widlar currentmirror". This circuit is a basic building block in many designs. We were tasked with examining both the Common-mode and differential-mode behaviors of this circuit. We were also tasked with investigating A_d, A_{cm}, CMRR, single-ended and differential inputs and outputs as well as common-mode range and output impedance.

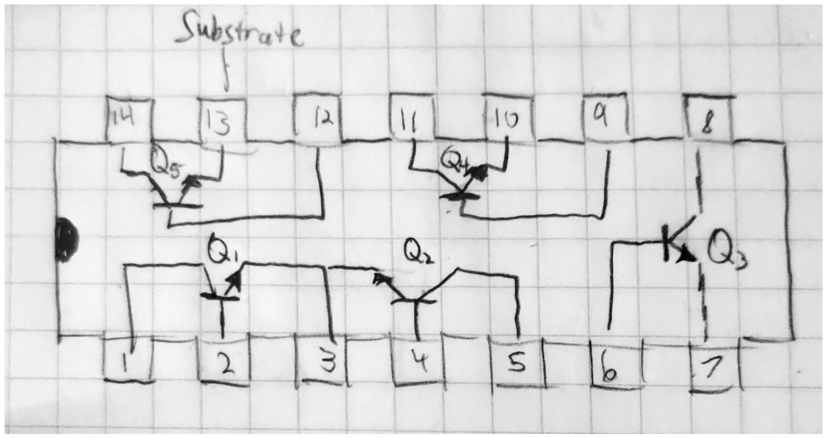
2 Methodology and Results

Circuit 1

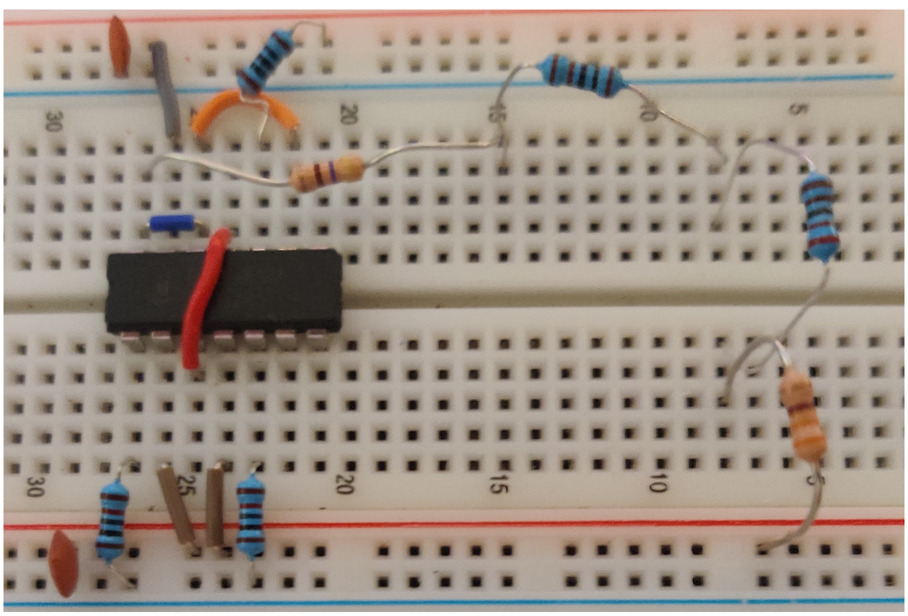
For parts 1 through 4, all the data we were asked to collect was to be done with the first circuit diagram in the lab manual. The following circuit was creating:



This circuit was implemented using the following diagram of the CA3046N BJT integrated circuit:



This was the resulting breadboard:



1. Measure I_{REF}, I_O, I_{C3}, and I_{C4} using Ohm's Law.

For the first part of the lab, after having built the first circuit, we were tasked with acquiring the stated measurements. The values I_{REF}, I_{C3}, and I_{C4} were each found using the Ohm's law equation:

$$I = \frac{V}{R}$$

For the values, the voltage drop was taken across the $R_{REF} = 3.98k\Omega$, $R_{C3} = 9.95k\Omega$, $R_{C4} = 9.92k\Omega$ resistors respectively. Finding I_O required another equation to find. I_O could be found by solving for the current flowing out of the Q_4 BJT emitter using the equation:

$$I_C = I_O = \frac{\beta}{\beta+1} I_E$$

In the equation, β is an inherent value of the BJT known as the Forward Current Transfer Ratio. This was found in the CA3046N as $h_{FE} = \beta = 100$ when $I_C \approx 0.856mA$. Using these equations, the following data table was collected:

	A	B	C	D
1	V_3.98KΩ **(V)**	V_101.7Ω **(V)**	V_9.95kΩ **(V)**	V_9.92kΩ **(V)**
2	22.75	0.088	3.869	3.881
3				
4				β
5				100
6				
7	I_REF **(mA)**	I_O **(mA)**	I_C3 **(mA)**	I_C4 **(mA)**
8	5.716080402	0.8567228404	0.3888442211	0.3912298387
9				
10		I_101.7Ω **(mA)**		
11		0.8652900688		

In this table, the columns with a green header were the values measured. The columns with the blue header had the desired calculated values using the equations previously stated.

2. Determine the quiescent collector voltages V_{C3} and V_{C4}, and DC output offset voltage. Determine whether the offset is due to load resistor mismatches, transistor mismatches, either or both.

For this part, using the same circuit and ensuring V_{b3} and V_{b4} are grounded, we were tasked with measuring V_{C3} and V_{C4}. That is the voltage difference between these points marked on the circuit diagram and ground. We then were asked to find the DC difference between these two points. This was to be done by measuring the voltage difference between the two directly rather than computing $V_{C4} - V_{C3}$ to ensure a more accurate result. The following was measured:

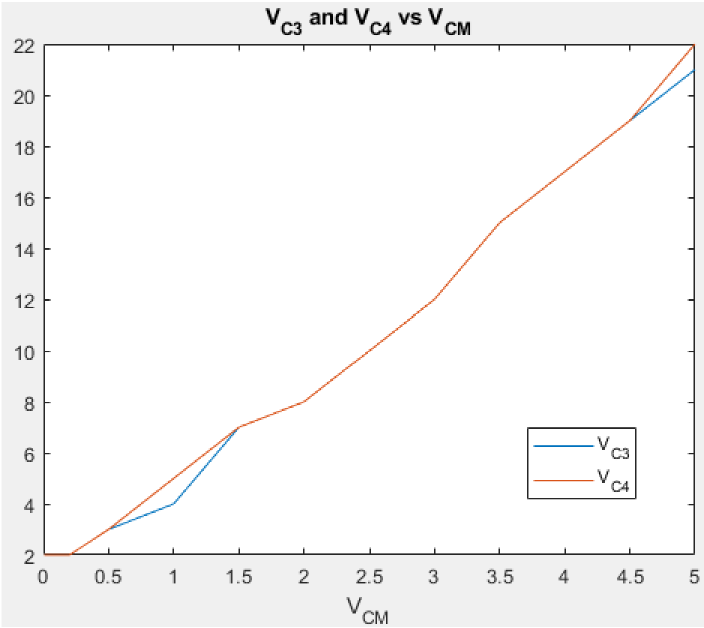
V_C3 **(V)**	V_C4 **(V)**	V_diff **(V)**
7.933	7.943	0.016
		|V_C4 - V_C3|
		0.01

3. Measure A_{CM}, common-mode gain.

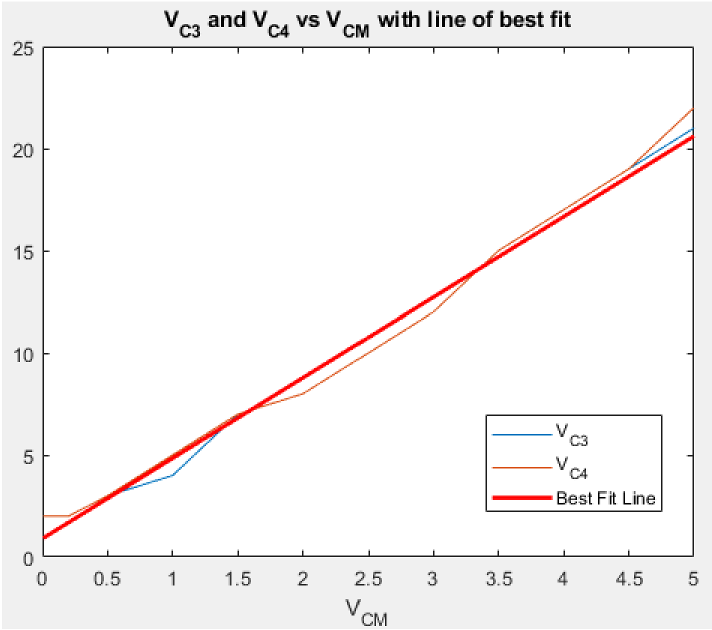
For this part, we were now asked to apply a 1kHz AC signal at the V_{b3} and V_{b4} points. We then take the AC rms voltage measurements of V_{C3} and V_{C4} vs. V_{CM} and use this to plot A_{CM} vs. V_{CM}. I used the wave generator on the Analog Discovery 2 to supply the V_{CM} and varied the voltage, while keeping the frequency at 1kHz. I got the following results:

V_CM **(Amplitude V)**	V_C3 **(AC RMS mV)**	V_C4 **(AC RMS mV)**
0.006	2	2
0.2	2	2
0.5	3	3
1	4	5
1.5	7	7
2	8	8
2.5	10	10
3	12	12
3.5	15	15
4	17	17
4.5	19	19
5	21	22

This resulted in the following graph:



And now with the line of best fit added:



The resulting slope for both V_{C3} and V_{C4} vs. V_{CM} were both about $A_{CM} = 3.94V/V$

4. Using a DC input for V_{CM}, observe how V_{C2}, V_{BE3}, V_{BE4}, V_{C3}, and V_{C4} vary.

This part was done by changing the DC input, V_{CM} and observing the outputs with the AD2. We already know that the V_{C3} and V_{C4} values should not be changing when we vary the base voltage of their BJTs. This is because there should be no flowing of current that way. The primary thing to be changing would be the emitter voltage when the V_{CM} rises.V_{BE3} and V_{BE4} change proportionally to V_{CM} so there is no visible change. After measuring these values, I got the following table as a result:

V_CM **(V)**	V_C2 **(V)**	V_C3 **(V)**	V_C4 **(V)**	V_BE3 **(V)**	V_BE4 **(V)**
0.006	-0.722	7.982	7.978	0.728	0.728
0.2	-0.525	7.978	7.977	0.725	0.725
0.5	-0.222	7.977	7.975	0.722	0.722
1	0.279	7.974	7.972	0.721	0.721
1.5	0.779	7.972	7.97	0.721	0.721
2	1.277	7.967	7.966	0.723	0.723
2.5	1.775	7.964	7.963	0.725	0.725
3	2.276	7.959	7.959	0.724	0.724
3.5	2.777	7.956	7.955	0.723	0.723
4	3.277	7.951	7.952	0.723	0.723
4.5	3.776	7.949	9.51	0.724	0.724
5	4.278	7.947	7.948	0.722	0.722

5. Measure A_d, differential-mode voltage gain, using the special op-amp circuit in Fig. 2 to provide a true small-signal differential input, V_d, to the amplifier at v_{b1} and v_{b2}. Determine the region of linear and non-linear amplification and produce and plot the amplifier's transfer characteristics.

I was not at all sure how the two circuits ended up being put together and I'm sure I could have figured it out if I didn't leave myself so little time to finish this. I am turning it in, hopefully without losing too much credit on this section, so I can continue working on more pressing assignments for other classes.

3 Conclusion

This lab required making two circuits which made it take a decent amount of time. Using BJTs was not new, but we now built a differential amplifier with them and compared it to one built with Op-Amps.