Lab 06

ECE 171L

Lab Section - Thurs. 5:30p - 7:30p

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1 Introduction and Overview

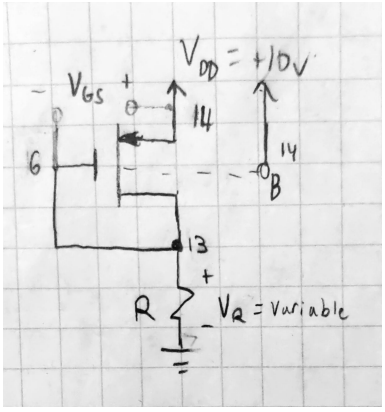
The general purpose of this lab was to investigate and observe experimentally some important properties of CMOS circuits. We started by experimentally characterizing parameters for each of the series connected transistors separately. These parameters included their threshold voltages and conductivity parameters. We then observed the classic transfer characteristic of the CMOS circuit.

2 Methodology and Results

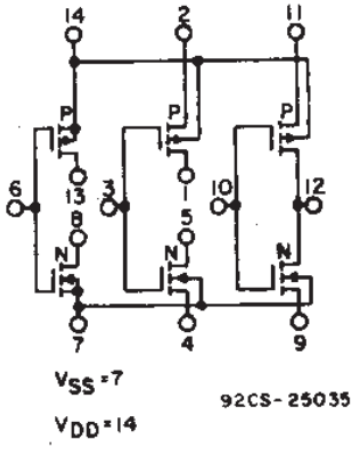
II. DC Device Characterization

2.0.1 PMOS

For this section, we were tasked with experimentally determining the PMOS transistor's threshold voltage, V_t, and conductivity parameter k. This was accomplished by using the CD4007UBE chip to implement the first circuit diagram in the lab manual, the enhancement NMOS basic circuit:



(a) Circuit Diagram



(b) CD4007UBE Internal Diagram

In the internal integrated circuit diagram, the top MOSFETs are PMOS and the bottom ones, NMOS. For this first part, we are utilizing the PMOS pins. We were to use a series of different R resistor values in the circuit diagram to determine the saturation drain current from measured voltage drops across R. We then measured

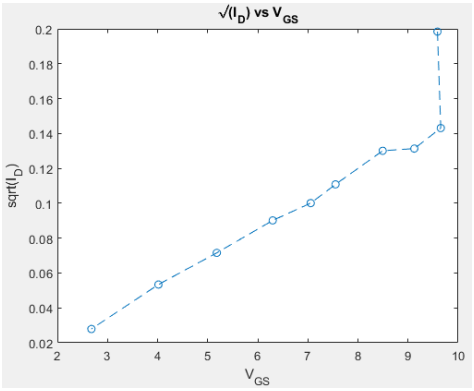
V_{GS} and used V_R with Ohm's law to calculate I_D. We then used that to calculate the voltage threshold V_T using the equation:

$$I_D = k(V_{GS} - V_t)^2 \rightarrow \sqrt{I_D} = \sqrt{k}(V_{GS}) - \sqrt{k}(V_t)$$

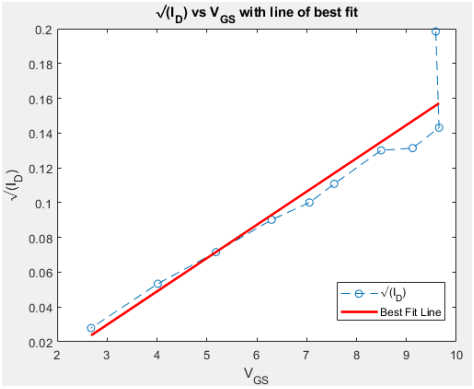
This means, once we graph multiple points of $\sqrt{I_D}$ vs. V_{GS}, the slope of the line will be $\sqrt{k}$ which we us to find the k value. This we can plug into the formula $V_t = V_{GS} - \sqrt{\frac{I_D}{k}}$ to solve for V_t. Plugging in different R values and measuring the desired points gave the following table:

R value **(Ω)**	V_R **(V)**	I_D **(mA)**	V_GS **(V)**	√I_D **(mA)**
10.9	0.429	39.35779817	9.587	6.273579374
21	0.43	20.47619048	9.653	4.525062483
47.7	0.823	17.25366876	9.125	4.153753575
100	1.692	16.92	8.493	4.11339276
225	2.763	33.56444444	7.552	5.793482929
333	3.335	21.18918919	7.056	4.603171645
469	3.812	8.12793177	6.299	2.850952783
1000	5.121	5.121	5.182	2.26296266
2220	6.329	2.850900901	4.017	1.688461104
9995	7.777	0.7780890445	2.679	0.8820935577

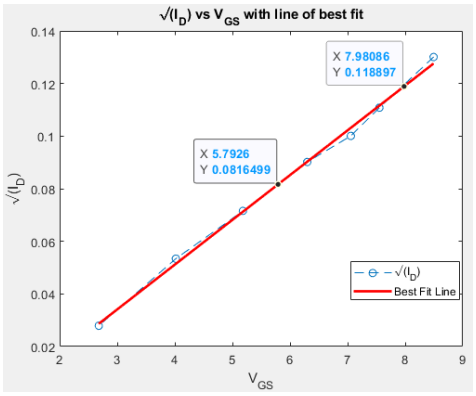
This resulted in the following graphs:



(c) $\sqrt{I_D}$ vs. V_{GS} Graph



(d) Graph with LSR Line Applied



(e) Graph Without Outliers

The slope of the line, throwing out the outliers was calculated to be

$$\text{slope} = \sqrt{k} = 0.01702$$

so it follows that

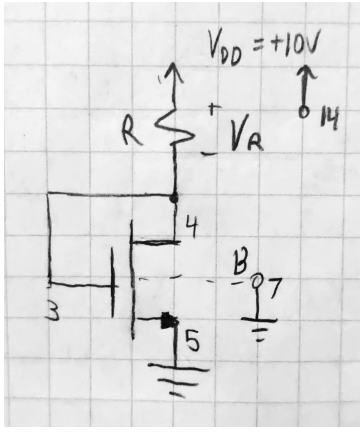
$$k = (\sqrt{k})^2 = (0.01702)^2 = 0.000289726$$

Using the previous equation with the one of points that wasn't an outlier, $(6.299, 0.090155)$.

$$V_t = V_{GS} - \sqrt{\frac{I_D}{k}} = (6.299) - \sqrt{\frac{(0.090155)^2}{(0.000289726)}} = 1.00241\text{V}$$

2.0.2 NMOS

For this section, we were now tasked with completing the exact same experiment, except now we are searching for the V_t and k values of the NMOS transistor. This required the following circuit diagram to be implemented instead:

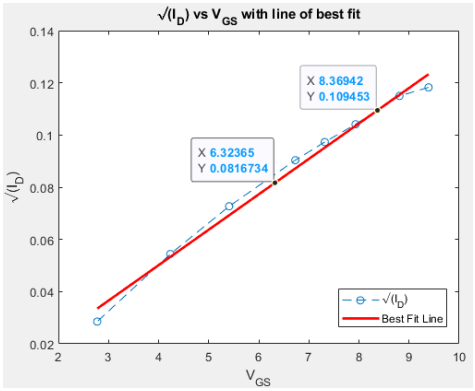


(f) Circuit Diagram 2

After performing the same procedure previously outlined, I got the following data:

NMOS					
R value (Ω)	V_R (V)	I_D (mA)		V_GS (V)	√I_D (mA)
10.9	0.142	13.02752294		9.474	3.609366002
21	0.351	16.71428571		9.529	4.088310863
47.7	0.667	13.98322851		9.389	3.739415531
100	1.322	13.22		8.809	3.635931793
225	2.439	35.25333333		7.932	5.937451754
333	3.153	21.97297297		7.317	4.687533784
469	3.829	8.164179104		6.729	2.857302767
1000	5.284	5.284		5.409	2.298695282
2220	6.57	2.959459459		4.235	1.720307955
9995	8.133	0.8137068534		2.775	0.9020570123

(g) $\sqrt{I_D}$ vs. V_{GS} Graph



(h) Graph with LSR Line Applied

In order to get the graph, I once again needed to throw out some outlier points. I think I got some bad data because my small resistor values were too close together, and my multi-meter might not be accurate enough to measure their resistances. Now the slope of the line, throwing out the outliers was calculated to be

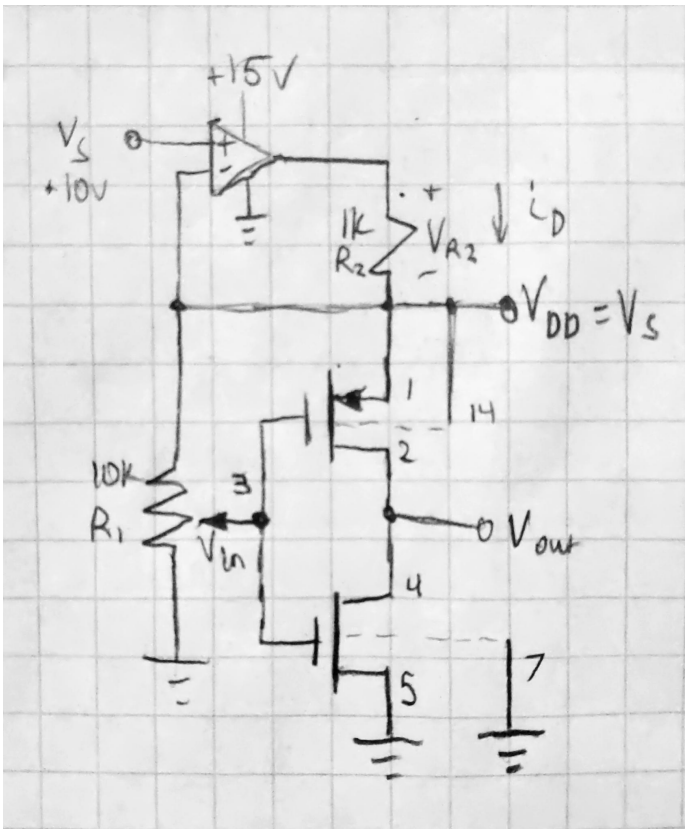
$$\text{slope} = \sqrt{k} = 0.01358$$
$$\text{so it follows that}$$
$$k = (\sqrt{k})^2 = (0.01358)^2 = 0.0001844$$

Using the previous equation with the one of points that wasn't an outlier, $(8.809, 0.114978)$.

$$V_t = V_{GS} - \sqrt{\frac{I_D}{k}} = (8.809) - \sqrt{\frac{(0.114978)^2}{(0.0001844)}} = 0.34167\text{V}$$

2.0.3 CMOS

For this final part, we were tasked with building the following circuit:

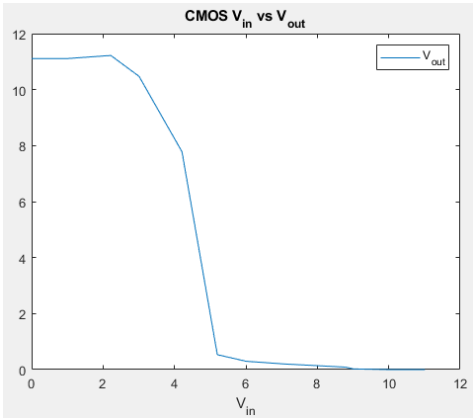


(i) Circuit Diagram 3

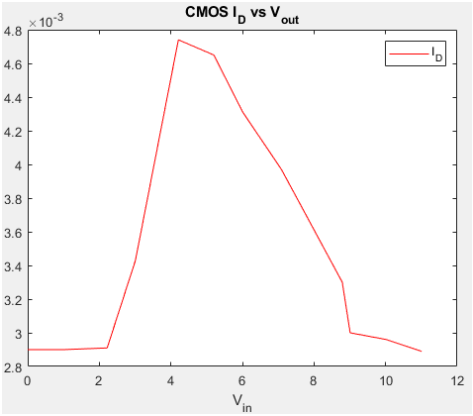
We then used this circuit and varying the potentiometer, R_1 from $0V \rightarrow V_{dd}$ and plotted the V_{out} vs V_{in} along with I_d vs V_{in}. We also had to locate the points where the slopes of V_{out} vs $V_{in} = -1$. I got the following table and graph of data:

CMOS			
V_in **(V)**	V_out **(V)**	V_R2 **(V)**	I_D **(mA)**
0	11.11	2.9	2.9
1	11.11	2.9	2.9
2.22	11.22	2.92	2.91
3.01	10.47	3.47	3.43
4.21	7.78	4.74	4.74
5.2	0.533	4.66	4.65
6.01	0.296	4.31	4.31
7.09	0.2	3.97	3.97
8.79	0.087	3.5	3.3
9.01	0.023	3.01	3
10.02	0	2.96	2.96
11.01	0	2.86	2.89

(j) Data Table



(k) Graph of V_{out} vs V_{in}

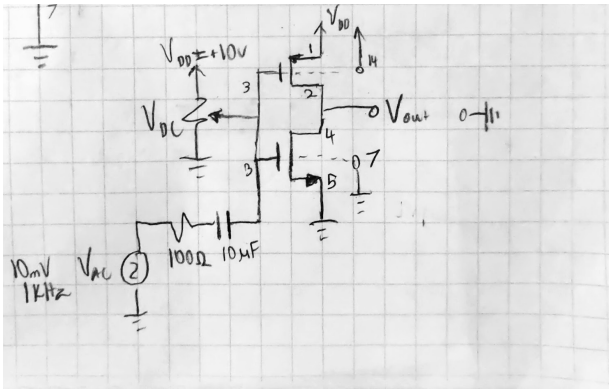


(l) Graph of I_D vs V_{in}

In the V_{out} vs V_{in} graph, the slope is ≈ -1 @ $V_{in} = 2.5$V and 5.2V. V_T for the PMOS should define the region that guarantees V_{out} =HIGH and V_T for the NMOS should define the region that guarantees V_{out} =LOW. This is what these two margin points, where the slope = -1 should represent.

III. AC Device Characterization

This part of the lab was asking us to use the CMOS circuit, bias it in the center of its transfer characteristic, couple in an AC signal, and then determine the small-signal gain voltage gain at a suitable frequency. This was done first by implementing the following circuit diagram:



(m) Circuit Diagram 4

With this, I set the V_{in} DC component to be in the saturation zone. The gain was then found using

$$\text{Gain} = A_v = \frac{V_{out}}{V_{in}}$$

where $V_{in} = V_{DC} + V_{AC}$ and $V_{out} = V_{DC} + V_{AC}$, and the AC components measured in RMS, so

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_{DC}+V_{AC}}{V_{DC}+V_{AC}} = \frac{(8.164V)+(24mV)}{(4.48V)+(11mV)} = 1.8232\text{V/V}$$

I found that the higher I went with the AC frequency and the smaller the AC RMS component was for the input, the same with the output. The output of the AC component scaled evenly with the input so the gain never really changed.

3 Conclusion

This lab required making four separate circuits and taking a lot of measurements. Thankfully by now, I have become quite proficient in building circuits and taking measurements. As always, it is hard to have good data and I still find places where my data collection went wrong and end up retaking measurements again and again. In this lab, I realized in my PMOS and NMOS V_t calculations I had accidentally graphed $\sqrt{I_D}$ in milli-amps rather than in amps so I had to go back and fix that. This wasn't even a large problem because I didn't have to remake any circuits. I just had to re-graph and calculate data. Because this lab required making 4 totally different circuits, every time I did make a mistake that required going back, I would have to remake the circuit and retake measurements. This was made particularly annoying by doing it online. I wish I went into the lab more but the last two times I did, there was no one there. I hope my data turned out as expected, and thank you for a lovely quarter!