# Jean Simatic

*Asynchronous microelectronics PhD candidate*

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## Education

2014 — 2017 **PhD Thesis**, *TIMA Laboratory*, Grenoble, France.
Design flow for ultra-low power: non-uniform sampling and asynchronous circuits

2013 — 2014 **Master**, *ENSTA*, Robotics and Embedded Systems.
Multiprocessors on chip, embedded software, robotics, mecatronics

2013 — 2014 **Master**, *UPMC*, Electronic Systems and Computer Systems.
Mixed and analog circuit design, noise, design for test, MEMS

2010 — 2013 **Engineering**, *École polytechnique*, Electrical Engineering major.
Digital circuit design, processor architecture, semi-conductors, optoelectronics, network (Internet), statistics

## Experience

2017 — Auj. **Startup incubation and executive direction**, *Hawai.tech*, Grenoble, France.
- Design of a modular architecture for low-power probabilistic circuits.
- Commercial and financial development.

2014 (6 months) **Intern**, *Tiempo*, Montbonnot Saint Martin, France.
- Design of a verification tool for standard cells Verilog modules
- Evaluation of a commercial fault simulator on QDI circuits

2013 (4 months) **Intern**, *Asynchronous Research Center*, Portland (Oregon), USA.
- Design of asynchronous IP for merge sort
- Contribution to the development of a CAD tool (ARCWelder)

2012 (1 months) **Intern**, *EADS Astrium, Digital electronic department*, Élancourt, France.
- Development of a test environment for a spatial CAN bus

2011 — 2012 (1 year) **Electronic designer and treasurer**, *Robotic club at École polytechnique*.
Participation to French Robotic Cup
- Design and fabrication of the electronic boards of the robot
- Financial management of the project

## Skills

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| EDA Tools | ModelSim, Design Compiler, Quartus |
| Programming | VHDL, Verilog, SystemC, Spice, Python, Java, GNU Make, C/C++, PHP, Caml |
| OS | Linux (Ubuntu, ArchLinux), Windows, RTEMS |
| Misc | Git, Subversion, LaTeX, Scilab, Matlab, Eclipse |

## Languages

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| French | Native language | German | Conversational |
| English | Fluent | Portuguese | Conversational |

## Interests

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| Music | Viola and trumpet player in orchestras and marching bands. Classical and Jazz amateur. |
| Sports | Badminton, hiking and cross-country skiing. |
| Pyrotechnics | C4/T2 trained firework firer. |

## PhD Thesis

Title Design flow for ultra-low power: Non-uniform sampling and asynchronous circuits

Advisor Laurent Fesquet

Co-advisor Rodrigo Possamai Bastos

Abstract The Internet of Things requires developing ultra-low power platforms embedding actuators, sensors, and signal processors. Event-driven sampling and circuitry allow reducing the amount of sampled data, the system activity, and therefore the power consumption. For helping designers in rapidly developing event-driven ultra-low power platforms, we have devised a complete framework named ALPS: Architectural tools for ultra-Low Power (event-driven) Systems. ALPS framework will allow to choose and simulate a signal-specific sampling scheme, and to synthesize a dedicated event-driven circuit for processing the non-uniformly sampled data. The estimated power reduction factor for a the event-driven version of a filter systems is from 3 to 30 depending on the input signal activity.

## Publications

J. Simatic, A. Cherkaoui, F. Bertrand, R. P. Bastos, and L. Fesquet, "A practical framework for specification, verification, and design of self-timed pipelines," in *2017 23rd IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, May 2017, pp. 65–72.

A. Skaf, J. Simatic, and L. Fesquet, "Seeking low-power synchronous/asynchronous systems: A FIR implementation case study," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017, pp. 1–4.

S. M. Qaisar, J. Simatic, and L. Fesquet, "High-level synthesis of an event-driven windowing process," in *3rd International Conference on Event-based Control, Communication and Signal Processing (EBCCSP)*, May 2017, pp. 1–8.

A. El-Hadbi, A. Cherkaoui, O. Elissati, J. Simatic, and L. Fesquet, "On-the-fly and sub-gate-delay resolution TDC based on self-timed ring: A proof of concept," in *15th IEEE International New Circuits and Systems Conference (NEWCAS)*, June 2017, pp. 305–308.

J. Simatic, R. P. Bastos, and L. Fesquet, "High-level synthesis for event-based systems," in *2nd International Conference on Event-based Control, Communication, and Signal Processing (EBCCSP)*, June 2016, pp. 1–7.

J. Simatic, A. Cherkaoui, R. P. Bastos, and L. Fesquet, "New asynchronous protocols for enhancing area and throughput in bundled-data pipelines," in *29th Symposium on Integrated Circuits and Systems Design (SBCCI)*, Aug 2016, pp. 1–6.

J. Simatic, L. Fesquet, and B. Bidegaray-Fesquet, "Correctly sizing FIR filter architecture in the framework of non-uniform sampling," in *International Conference on Sampling Theory and Applications (SampTA)*, 2015, pp. 269–273.