

Education

UNIV GRENOBLE ALPES

PHD IN CIRCUIT DESIGN/HLS

📅 2014 – 2017 📍 Grenoble, FR

Design flow for ultra-low power:
Non-uniform sampling and
asynchronous circuits

ENSTA PARISTECH

ENG. ROBOTICS AND EMBEDDED
SYSTEMS📅 2013 – 2014 📍 Palaiseau, FR
Multiprocessors on chip, embedded
software, robotics, mecatronics

UNIV. PIERRE & MARIE CURIE

MSc. ELECTRONIC SYSTEMS AND
COMPUTER SYSTEMS📅 2013 – 2014 📍 Paris, FR
Mixed and analog circuit design,
noise, design for test, MEMS

ÉCOLE POLYTECHNIQUE

ENG. ELECTRICAL ENGINEERING

📅 2010 – 2013 📍 Palaiseau, FR
Digital circuit design, processor
architecture, semi-conductors,
optoelectronics, network (Internet),
statistics. French Robotics Cup.

Skills

Development

• Python • Pytest • Pandas • Conda
• C/C++ • Rust • Make • Shell • Tcl
• Git • Subversion • VS Code • Emacs
• Docker • Vagrant • Kubernetes

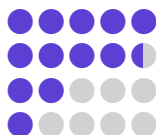
🔧 Digital electronic

• Vivado • Vitis HLS • Vitis • Quartus
• SystemVerilog • Verilog • VHDL •
SystemC • VHDL-AMS • Spice
• DesignCompiler • PrimeTime •
ModelSim • Innovus

💻 Software

• Ubuntu • ArchLinux • CentOS • Win
• OVH cloud • AWS • SSH • Nginx
• Jira • Confluence • \LaTeX • Office

🗣 Languages

French
English
Portuguese
German

Work Experience

DEEPTech STARTUP CHIEF TECHNOLOGY OFFICER

🏢 HAWAI.TECH

📅 Feb 2019 – Ongoing 📍 Grenoble, FR

- Manage 10-person technical team (Scrum master then Product Owner).
- Design of a modular architecture for low-power probabilistic circuits.
- Implementation in software, FPGA (AWS F1) and ACAP (Xilinx Versal) using RTL and HLS.
- Install and maintain the company's web services on cloud servers.

ELECTRONICS R&D ENGINEER • STRATUP INCUBATION

🏢 PROBAYES

📅 Jan 2018 – Feb 2019 📍 Grenoble, FR

- Design highly efficient Bayesian sensor fusion and Bayesian filters using stochastic computing. Benchmark on Intel Cyclone V.
- Lead legal, financial and business structuration for the spin-off

ASYNCHRONOUS CIRCUITS PHD CANDIDATE

🏢 TIMA LABORATORY

📅 Nov 2014 – Nov 2017 📍 Grenoble, FR

- Parse synchronous FSM (from AUGH HLS) and generate asynchronous bundle data controllers using new synchronization protocol.
- Design and test circuits for non-uniform sampling and filters.

ASYNCHRONOUS CIRCUITS VERIFICATION INTERN

🏢 TIEMPO SECURE

📅 April 2014 – Oct 2014 📍 Saint-Martin d'Hères, FR

- Design of a verification tool for standard cells Verilog modules
- Evaluation of a commercial fault simulator on QDI circuits

ASYNCHRONOUS CIRCUITS DESIGN INTERN

🏢 ASYNC RESEARCH CENTER

📅 April 2013 – Aug 2013 📍 Portland, OR, USA

- Design of asynchronous IP for merge sort
- Contribution to the development of a CAD tool (ARCWelder)

Recent Projects

TEST AND GENERATION OF PARAMETRIZED IP BLOCKS

🏢 HAWAI.TECH

📅 Aug 2022 – Feb 2023 📍 Grenoble, FR

Python set of utilities to handle in-house developed IP blocks. Used Jinja templates to generate IP based on YAML config. Pytest fixtures and parameterization to run parallelized regression tests.

RUST TRAINING

🏢 SIDE-PROJECT

📅 Sep 2022 – Nov 2022 📍 Grenoble, FR

Learn Rust by the book, and solving puzzles. Small webscraping and data plotting project. Share learnt concepts with a tutorial for Hawai.tech's team.

BAYESIAN GRAMMAR FOR AN EFFICIENT OCR PIPELINE

🏢 HAWAI.TECH

📅 June 2021 – Dec 2021 📍 Grenoble, FR

Integrate industrial client existing knowledge in Bayesian model (beam search based) to correct errors of a PP OCR reader. Results post-processing and visualization with pandas and matplotlib. Pipeline delivered in Docker.

FPGA ACCELERATION OF BAYESIAN MATRIX FACTORIZATION

🏢 HAWAI.TECH

📅 Nov 2020 – Oct 2021 📍 Grenoble, FR

Specify architecture in particular AXI and AXI-L interface with AWS F1 shell. Develop AXI-Stream vector processing core. Co-develop Python API to generate modularly handle each computation steps and manage the FPGA execution from a Jupyter notebook. Demonstrated 5x speed/W on MovieLens.