Jean Simatic

Last Updated on 12th March 2023

@ jean@simatic.org +33 (0)6 28 13 12 jsimatic jean-simatic scholar CodingGame

Education

UNIV GRENOBLE ALPES
PhD in circuit design/HLS
2014 – 2017 Grenoble, FR
Design flow for ultra-low power: Non-uniform sampling and asynchronous circuits

ENSTA PARISTECH
Eng. Robotics and embedded systems
2013 – 2014 Palaiseau, FR
Multiprocessors on chip, embedded software, robotics, mecatronics

UNIV. PIERRE & MARIE CURIE
MSc. Electronic systems and Computer systems
2013 – 2014 Paris, FR
Mixed and analog circuit design, noise, design for test, MEMS

ÉCOLE POLYTECHNIQUE
Eng. Electrical Engineering
2010 – 2013 Palaiseau, FR
Digital circuit design, processor architecture, semi-conductors, optoelectronics, network (Internet), statistics. French Robotics Cup.

Skills

Development
- Python • Pytest • Pandas • Conda
- C/C++ • Rust • Make • Shell • Tcl
- Git • Subversion • VS Code • Emacs
- Docker • Vagrant • Kubernetes

Digital electronic
- Vivado • Vitis HLS • Vitis • Quartus
- SystemVerilog • Verilog • VHDL • SystemC • VHDL-AMS • Spice
- DesignCompiler • PrimeTime • ModelSim • Innovus
- I2C • SPI • AMBA • CAN

Software
- Ubuntu • ArchLinux • CentOS • Win
- OVH cloud • AWS • SSH • Nginx
- Jira • Confluence • LaTeX • MS Office

Languages

French	●●●●●
English	●●●●◐
Portuguese	●●○○○
German	●○○○○

Work Experience

DEEPTECH STARTUP CHIEF TECHNOLOGY OFFICER
HawAI.tech Feb 2019 – Ongoing Grenoble, FR
- Manage 10-person technical team (Scrum master then Product Owner).
- Design of a modular architecture for low-power probabilistic circuits.
- Implementation in software, FPGA (AWS F1) and ACAP (Xilinx Versal) using RTL and HLS. Develop test fixtures (Python) and host code (Python/C++).
- Install and maintain the company's web services on cloud servers.

ELECTRONICS R&D ENGINEER • STRATUP INCUBATION
Probayes Jan 2018 – Feb 2019 Grenoble, FR
- Design highly efficient Bayesian sensor fusion and Bayesian filters using stochastic computing. Benchmark on Intel Cyclone V.
- Lead legal, financial and business structuration for the spin-off

ASYNCHRONOUS CIRCUITS PHD CANDIDATE
TIMA Laboratory Nov 2014 – Nov 2017 Grenoble, FR
- Parse synchrounous FSM (from AUGH HLS) and generate asynchronous bundle data controllers using new synchronization protocol.
- Design and test circuits for non-uniform sampling and filters.

ASYNCHRONOUS CIRCUITS VERIFICATION INTERN
Tiempo Secure April 2014 – Oct 2014 Saint-Martin d'Hères, FR
- Design of a verification tool for standard cells Verilog modules
- Evaluation of a commercial fault simulator on QDI circuits

ASYNCHRONOUS CIRCUITS DESIGN INTERN
Async Research Center April 2013 – Aug 2013 Porland, OR, USA
- Design of asynchronous IP for merge sort
- Contribution to the development of a CAD tool (ARCWelder)

Recent Projects

TEST AND GENERATION OF PARAMETRIZED IP BLOCKS
HawAI.tech Aug 2022 – Feb 2023 Grenoble, FR
Python set of utilities to handle in-house developped IP blocks. Used Jinja templates to generate IP based on YAML config. Pytest fixtures and parameterization to run parallelized regression tests.

RUST TRAINING
Side-project Sep 2022 – Nov 2022 Grenoble, FR
Learn Rust by the book, and solving puzzles. Small webscrapping and data plotting project. Share leant concepts with a tutorial for HawAI.tech's team.

BAYESIAN GRAMMAR FOR AN EFFICIENT OCR PIPELINE
HawAI.tech June 2021 – Dec 2021 Grenoble, FR
Integrate industrial client existing knowledge in Bayesian model (beam search based) to correct errors of a PP OCR reader. Results post-processing and visualization with pandas and matplotlib. Pipeline delivered in Docker.

FPGA ACCELERATION OF BAYESIAN MATRIX FACTORIZATION
HawAI.tech Nov 2020 – Oct 2021 Grenoble, FR
Specify architecture in particular AXI and AXI-L interface with AWS F1 shell. Develop AXI-Stream vector processing core. Co-develop Python API to generate modularely handle each computation steps and manage the FPGA execution from a Jupyter notebook. Demonstrated 5x speed/W on MovieLens.