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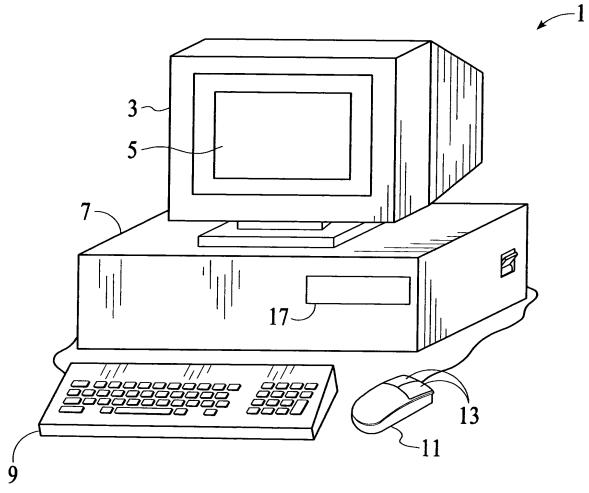


FIG.1A

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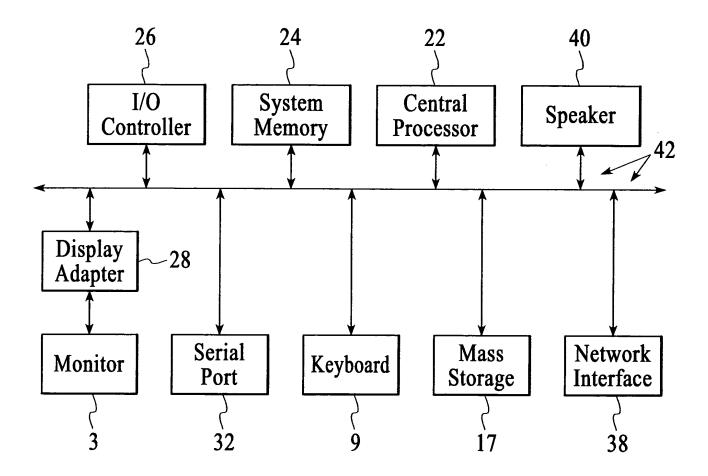


FIG.1B

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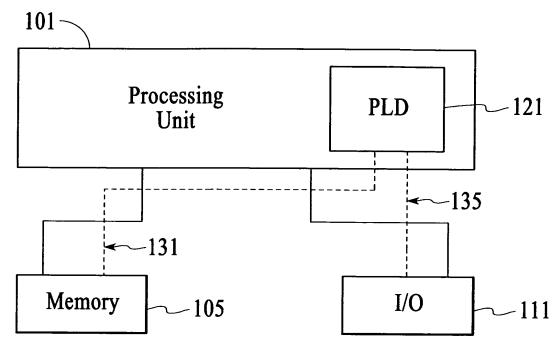
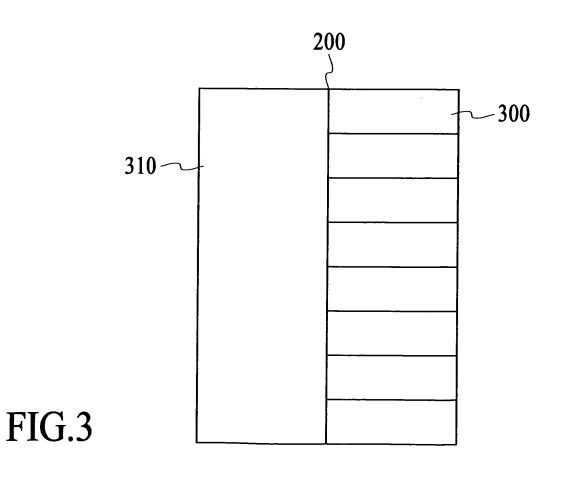


FIG.1C



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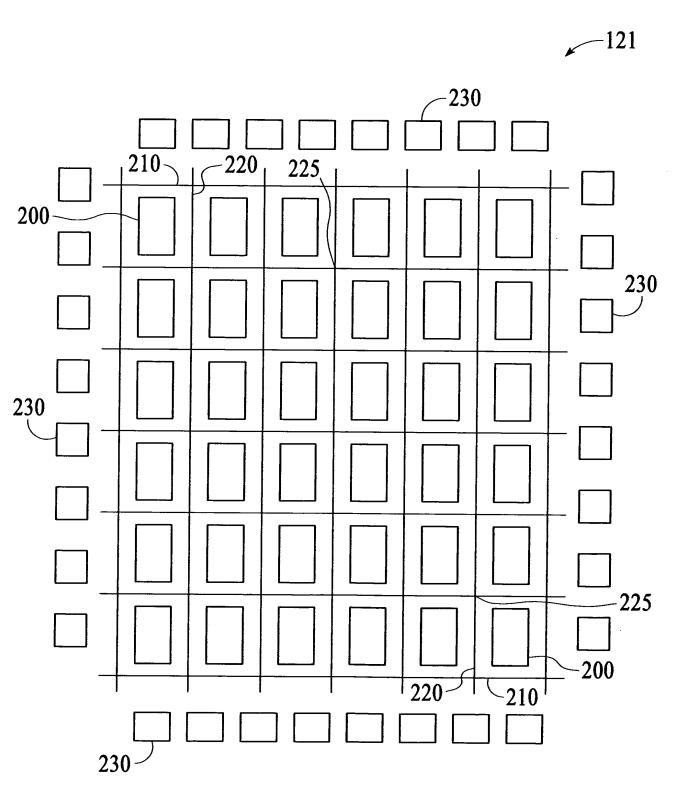
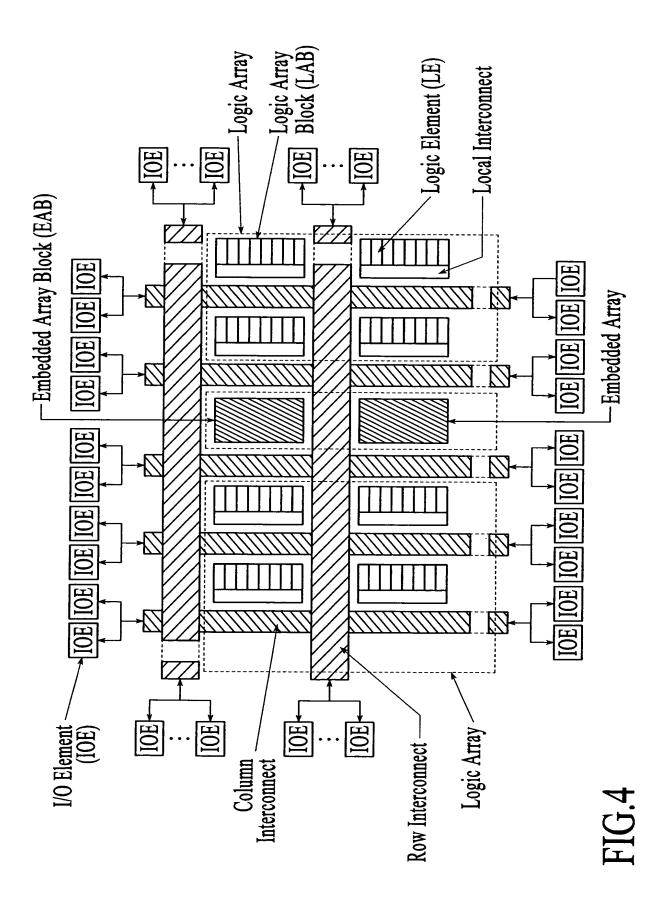


FIG.2

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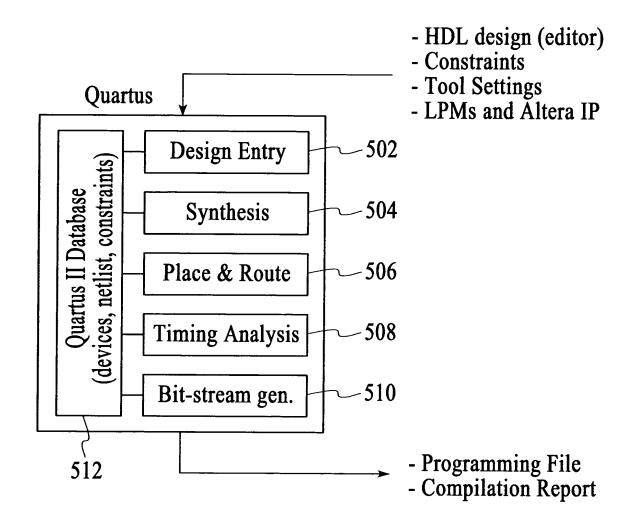


FIG.5A

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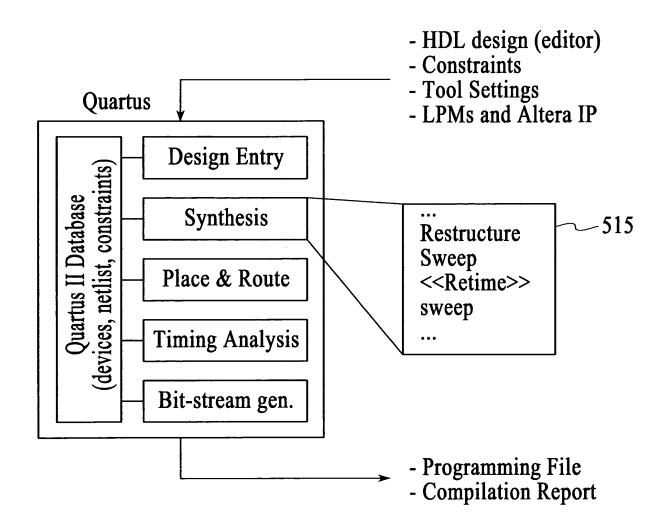


FIG.5B

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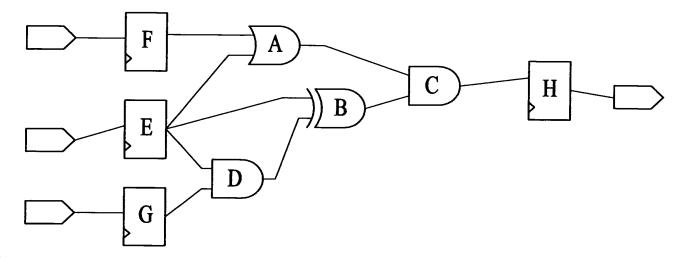


FIG.6A

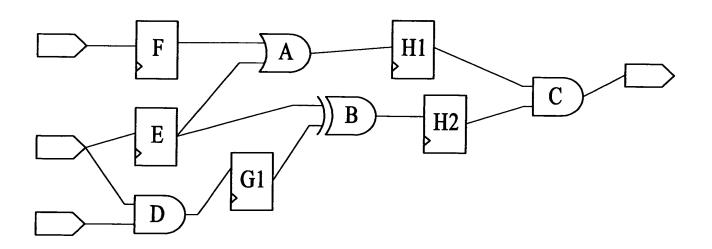


FIG.6B

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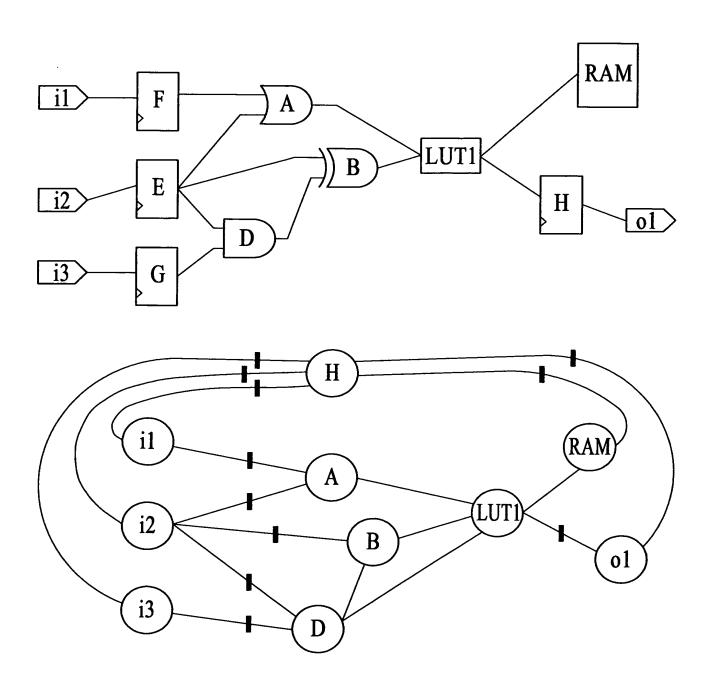


FIG.7

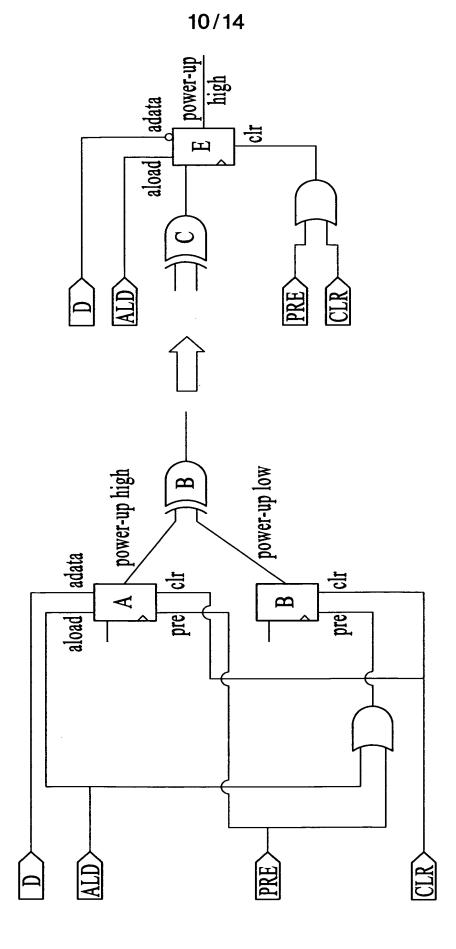
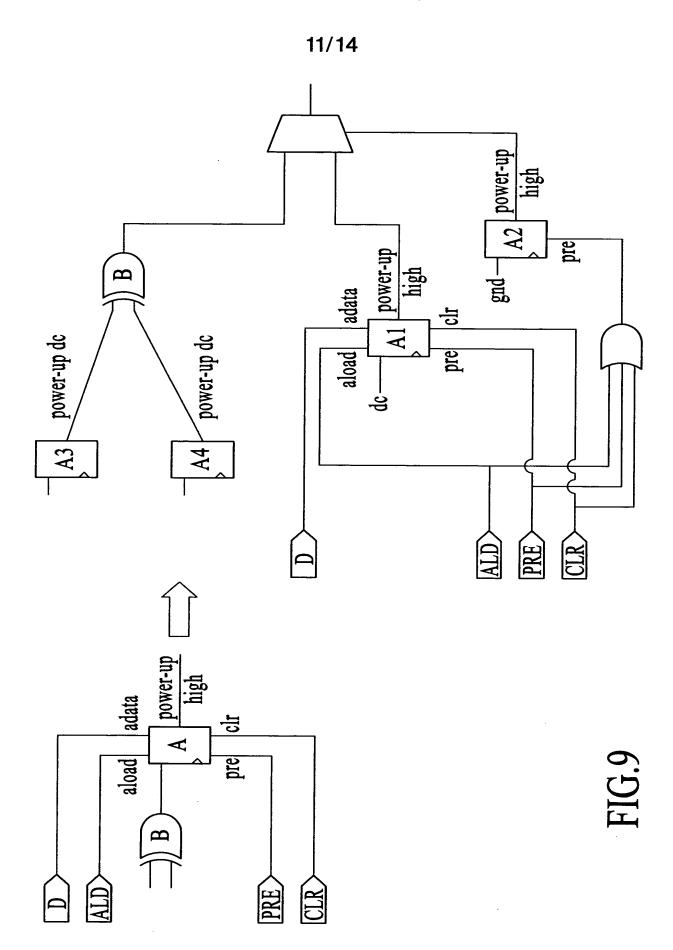


FIG.X



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Settings  Category:	
Category:	Netlist Optimizations  Specify options for performing netlist optimizations during synthesis or fitting.  Note: The availability of these options depends on the current device family.  Changes apply to Compiler settings 'mike_decoder'  Synthesis optimizations  Perform gate-level register retiming  Allow register retiming to trade off Tsu/Tco with Fmax
Nettist Optimizations Simulator Settings Software Build Settings Stratix GX Registration HardCopy Settings	OK Cancel

**FIG.10** 

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