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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/513,450	08/30/2006	Babette van Antwerpen	015114-063920US	2433

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/513,450	VAN ANTWERPEN ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *77-86* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *79* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the Patent Application 11/513,450 filed on 8/30/06.

Claims 77-86 are pending.

Claim Objection

The status identifier "(not entered)" of claims 53-76 is improper and should be changed to "(canceled)". Correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 77-78, 80-86 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Suaris (US pub. US 2005/0132316)

(Claim 77)

A method for designing logic circuitry implemented by a programmable logic device PLD (*PLD in one or more of par. 6-7, fig 4-5, 8, 16-17, 19*), the method comprising:

Providing a design file incorporating the logic design circuitry in computer readable format (*Fig. 22 shows computer readable format design file being sent/loaded (blocks 450/452) from/to computer systems in fig. 22*);

Generating from the design file a retiming graph *(block 454 in fig 22 (more details of retiming graph shown in one or more of fig. 6-7, 12-15, etc)*) for each of a plurality of clock domains (par. 55, 84) associated with the logic design circuitry;

Applying constraints to the retiming graph (*fig 12 discloses constraints applied to retiming*) to determine which registers of the retiming graph (*i.e., by considering, sorting, selecting, reconfiguring and finding the best retimable registers)* are capable of being moved forward or backward across a combinational logic element of the logic design circuitry (*moving (relocation/reposition) of registers forward or backward based on retiming graph is disclosed in fig 14-15, i.e. REGISTER FORWARD/BACKWARD RETIMABLE CUTS, REGISTER FORWARD/BACKWARD RETIMABLE TRACES and corresponding text. More register forward/backward retimable move/reposition are disclosed in numerous locations in the prior art, i.e., one or more of par. 15-16, 19-20, 27-33, 44-45, 78-84 etc);* and

Retiming the logic design circuitry by moving compatible registers on the retiming graph backward or forward across the combinational logic elements until the difference between gate-to-gate delays for the logic design is minimized (*i.e., fig 12, 14 show iteration of retiming by register moving until there is no more registers to consider (at decision blocks*) and *DELAY/SLACK is optimized and minimized*).

(Claim 78) wherein applying the constraints comprises determining which of the registers are compatible (*fig. 12 shows which of the registers are compatible by considering, sorting, selecting, reconfiguring and finding the best retimable registers*)

(Claim 80) wherein retiming comprises iteratively retiming the logic design circuitry to find a minimal difference between the gate-to-gate delays (fig 12, 14).

(Claim 81) wherein retiming comprises determining delays associated with a netlist and determining a required cycle time (par 3).

(Claim 82) wherein retiming the logic design circuitry comprises forming a host node (fig 21-22) to store the constraints.

(Claim 83) Applying constraints for asynchronous signals by setting upper and lower boundaries on edges in the retiming graph (fig 6-7).

(Claim 84) Applying the retiming graph to a netlist based on user selectable criteria (par 3).

(Claim 86) Applying the retiming comprises modifying power-up signals, or reset signals, or asynchronous logic signals on the registers retimed (par 46).

Removing registers of the retiming graph that are not capable of being moved forward or backward across logic elements of the logic design circuitry (one or more of par 41, 69, 5, 84).

Allowable Subject Matter

Claim 79 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/
Primary Examiner, Art Unit 2825