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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/018,205	01/23/2008	Kuan-Hua Chao	MTKP0517USA	7729

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EXAMINER	
TRAN, JANY	

ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
01/23/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
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Office Action Summary	Application No.	Applicant(s)	
	12/018,205	CHAO ET AL.	
	Examiner	Art Unit	
	JANY TRAN	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/23/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki (US 6,452,422).

With respect to **claim 1**,

Figure 8 of Suzuki discloses a driving circuit, comprising:

a pair of input ports (where the first input port is coupled to the output of 111 [hereinafter 'IN1'] and the second input port is coupled to the output of 112 [hereinafter 'IN2']);

a pair of differential output ports (XD_O and R_O);

a first differential pair (P_1 and P_2), directly connected to a first voltage level (V_{DD}), having a first input terminal coupled to one of the input ports (gate of P_1 is coupled to IN1), a second input terminal coupled to the other of the input ports (gate of P_2 is coupled to IN2), a first output terminal coupled to one of the differential output ports (drain of P_1 is coupled to XD_O), and a second output terminal coupled to the other of the differential output ports (drain of P_2 is coupled to R_O);

a second differential pair (N_1 and N_2), having a first input terminal coupled to one of the input ports (gate of N_1 is coupled to IN1), a second input terminal coupled to the

other of the input ports (gate of N_2 is coupled to IN2), a first output terminal coupled to one of the differential output ports (drain of N_1 is coupled to XD_O), and a second output terminal coupled to the other of the differential output ports (drain of N_2 is coupled to R_O);

a load unit (R_L), coupled to the pair of differential output ports (XD_O and R_O); and

a current source (N_{C1}), coupled between the second differential pair (N_1 and N_2) and a second voltage level (ground).

With respect to **claim 2,**

Suzuki further teaches wherein the first differential pair comprises:

a first transistor (P_1) having a source terminal directly connected to the first voltage level (V_{DD}), a drain terminal coupled to one of the differential output ports (XD_O), and a gate terminal coupled to one of the input ports (IN1); and

a second transistor (P_2) having a source terminal directly connected to the first voltage level (V_{DD}), a drain terminal coupled to the other of the differential output ports (R_O), and a gate terminal coupled to the other of the input ports (IN2).

With respect to **claim 3,**

Suzuki further teaches wherein the second differential pair comprises:

a third transistor (N_1) having a drain terminal coupled to one of the differential output ports (XD_O), and a gate terminal coupled to one of the input ports (IN1); and

a fourth transistor (N_2) having a drain terminal coupled to the other of the differential output ports (R_O), and a gate terminal coupled to the other of the input ports (IN2).

With respect to **claim 4,**

Suzuki further teaches wherein the first voltage level is higher than the second voltage level (wherein V_{DD} is higher than ground).

With respect to **claim 5,**

Suzuki further teaches wherein the first transistor (P_1) and the second transistor (P_1) are PMOS transistors (see Figure 8), and the third transistor (N_1) and the fourth transistor (N_2) are NMOS transistors (see Figure 8).

With respect to **claim 6,**

Suzuki further teaches wherein the second voltage level is higher than the first voltage level (see the complementary circuit of Figure 8 that is shown in Figure 6 – where the second voltage level (V_{DD}) is higher than the first voltage level (ground)).

With respect to **claim 7,**

Suzuki further teaches wherein the first transistor and the second transistor are NMOS transistors (see Figure 6 where in this case N_1 and N_2 are the first and second transistors), and the third transistor and the fourth transistor are PMOS transistors (see Figure 6 where in this case P_1 and P_2 are the third and fourth transistors).

With respect to **claim 8,**

Suzuki further teaches wherein the load unit is a resistance element (R_L, see Figure 8).

With respect to **claim 9,**

Figure 8 of Suzuki discloses a driving circuit, comprising:

a pair of input ports (where the first input port is coupled to the output of 111 [hereinafter 'IN1'] and the second input port is coupled to the output of 112 [hereinafter 'IN2']);

a pair of differential output ports (XD_O and R_O);

a first transistor (P_1) having a source terminal directly connected to a first voltage level (V_{DD}), a drain terminal coupled to one of the differential output ports (XD_O), and a gate terminal coupled to one of the input ports (IN1);

a second transistor (P_2) having a source terminal directly connected to the first voltage level (V_{DD}), a drain terminal coupled to the other of the differential output ports (R_O), and a gate terminal coupled to the other of the input ports (IN2);

a third transistor (N_1) having a drain terminal coupled to one of the differential output ports (XD_O), and a gate terminal coupled to one of the input ports (IN1);

a fourth transistor (N_2) having a drain terminal coupled to the other of the differential output ports (R_O), and a gate terminal coupled to the other of the input ports (IN2);

a load unit (R_L), coupled to the pair of differential output ports (XD_O and R_O); and

a current source (N_{C1}), coupled between a second voltage level (ground) and the sources of the third and fourth transistors (sources of N_1 and N_2).

With respect to **claim 10,**

Suzuki further teaches wherein the first voltage level is higher than the second voltage level (wherein V_{DD} is higher than ground).

With respect to **claim 11,**

Suzuki further teaches wherein the first transistor (P_1) and the second transistor (P_1) are PMOS transistors (see Figure 8), and the third transistor (N_1) and the fourth transistor (N_2) are NMOS transistors (see Figure 8).

With respect to **claim 12,**

Suzuki further teaches wherein the second voltage level is higher than the first voltage level (see the complementary circuit of Figure 8 that is shown in Figure 6 – where the second voltage level (V_{DD}) is higher than the first voltage level (ground)).

With respect to **claim 13,**

Suzuki further teaches wherein the first transistor and the second transistor are NMOS transistors (see Figure 6 where in this case N_1 and N_2 are the first and second transistors), and the third transistor and the fourth transistor are PMOS transistors (see Figure 6 where in this case P_1 and P_2 are the third and fourth transistors).

With respect to **claim 14,**

Suzuki further teaches wherein the load unit is a resistance element (R_L, see Figure 8).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JANY TRAN whose telephone number is (571) 270-5074. The examiner can normally be reached on Monday - Friday, 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jany Tran/
Examiner, Art Unit 2819
/Rexford N BARNIE/
Supervisory Patent Examiner, Art Unit 2819