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Description

The present invention relates to a PLL-system, specifically to a charge pump circuit within such system.

The document US-A-4,745,372 discloses in its Figs. 1 and 8, and in the related description, a charge pump circuit within a PLL-system, said circuit comprising:

- a series connection of a first transistor and a second transistor of the type complementary to the type of said first transistor, between a power source voltage terminal and ground;
- a third transistor being connected to said second transistor to form a mirror circuit together with said second transistor; and
- a transistor means being connected to said first transistor and being connected in series with said third transistor between said power voltage terminal and ground.

In this prior art charge pump circuit, the transistor means comprises only a single transistor acting as a diode, to form a mirror circuit with the first transistor. The diode-transistors in both mirror circuits are connected to each other via a resistor which may be shortcut by a switch. Depending on whether the switch is permanently open or whether it is pulsed, the charge pump circuit operates in one of two different modes. When the switch is pulsed, the circuit is in a synchronized mode having a narrow noise band, whereas, when the switch is open, the circuit provides fast response speed in a pull-in transition. This prior art charge pump circuit has the disadvantage that, when it is used in a PLL-system, the cut-off frequency of the loop filter cannot be adjusted independently from the loop gain of the system, and vice versa.

It is therefore the object of the present invention to provide a charge pump circuit within a PLL-system, for charging a loop filter, wherein the cut-off frequency of the loop filter is independent of the loop gain of the PLL-system, and vice versa.

The circuit of the present invention is defined by the teaching of the enclosed claim.

The present invention will be explained in more detail based on embodiments which are illustrated by the accompanying drawings.

Fig. 1 is a partially schematic circuit diagram illustrating a first embodiment of a charge pump circuit and PLL-system in accordance with the present invention;

Fig. 2 is a graph of certain operational characteristics of the PLL-system of the present invention; and

Fig. 3 is a partially schematic circuit diagram illustrating a second embodiment of a charge pump circuit and PLL-system in accordance with the present invention.

Fig. 1 illustrates a phase locked loop system in accordance with a first embodiment of the present invention.

In a charge pump circuit 21 of the Fig. 1 embodiment, the source-drain paths of p-channel FETs Q_3 and Q_4 are connected in series between a positive voltage power source terminal T_3 and an output terminal T_2 of the charge pump circuit 21. Charge pump circuit 21 also includes n-channel FETs Q_5 and Q_6 whose drain-source paths are connected in series between the output terminal T_2 and circuit ground. The FET Q_3 is a current source transistor which supplies a charging current i_3 of constant magnitude in a first direction toward the output terminal T_2 for charging a loop filter 22 described in greater detail hereinbelow. The FET Q_6 is a current sink transistor which draws a discharging current i_6 of constant magnitude in a second direction from the output terminal T_2 to circuit ground for discharging the loop filter 22. The FET Q_4 acts as a first switching transistor for controlling the application of the charging current i_3 supplied by the current source transistor Q_3, while the FET_5 Q_5 serves as a second switching transistor for controlling the flow of the discharging current i_6 from the output terminal T_2 to ground through the current sink transistor Q_6.

A current mirror circuit 11 includes a p-channel FET Q_1 at an input side thereof, the FET Q_1 having a source electrode connected with terminal T_3 and drain and gate electrodes both connected to a control terminal T_1 of the charge pump circuit 21. The FET Q_3 is arranged at an output side of the current mirror circuit 11 such that its gate electrode is coupled with that of the FET Q_1. A further p-channel FET Q_2 is also connected at the output side of the current mirror circuit 11 such that its gate electrode is coupled with that of the FET Q_1 and its source electrode is connected with that of FET Q_1 to the terminal T_3.

A second current mirror circuit 12 includes an n-channel FET Q_7 whose source electrode is connected to circuit ground and whose drain and gate electrodes are connected with the drain electrode of the FET Q_2. The current sink transistor Q_6 forms the output side of the current mirror circuit 12 such that its gate electrode is connected with that of the FET Q_7.

The output terminal U′ of the digital phase comparison circuit 4 is connected to the gate electrode of the first switching transistor Q_4 and the output terminal D′ of the digital phase comparison circuit 4 is coupled through an inverter Q_8 to the gate electrode of the second switching transistor Q_5. The digital phase comparison.circuit 4 and the charge pump circuit 21 together with the frequency-dividing circuits 2 and 3, are fabricated as an integrated circuit 23, as indicated in Fig. 1.

A resistor R_2 is connected between the control terminal T_1 and circuit ground. A resistor R_1 has a first terminal connected to the control terminal T_1 and a second terminal connected with the collector of an

npn transistor Q_9 whose emitter is connected to circuit ground.

The loop filter 22 includes a capacitor C_1 connected between the output terminal T_2 and circuit ground. The loop filter 22 further includes a resistor R_3 having a first terminal connected with the output terminal T_2 of the charge pump circuit 21, and a capacitor C_2 having a first terminal connected with a second terminal of the resistor R_3 and a second terminal connected with the circuit ground. The loop filter 22 produces a voltage E_6 at the terminal T_2 which the loop filter 22 supplies to the control terminal of the VCO 7.

The digital phase comparison circuit 4 receives the first and second phase comparison signals R and V as inputs and produces the first and second phase difference signals U and D as outputs, as known e.g. from US-A- 4,745,372. Accordingly, the relationship of the first and second phase difference signals U and D produced by the phase comparison circuit 4 to the phase difference between the first and second phase comparison signals R and V provided as inputs thereto is expressed essentially by the discontinuous line A of Fig. 2.

In operation, the current i_1 flowing in the FET Q_1 has a constant magnitude depending on a signal level applied to the base of the transistor Q_9, as discussed more fully hereinbelow. Since the FETs Q_1 and Q_3 form respective input and output portions of the current mirror circuit 11, the magnitude of the current i_3 flowing in the source-drain path of the FET Q_3 will be equal to that of the current i_1 of the FET Q_1. Since the FETs Q_1 and Q_2 likewise form respective input and output portions of the current mirror circuit 11, the current flowing in the source-drain path of the FET Q_2 is also equal in magnitude to that of the current i_1 and, therefore, to that of the current i_3. Since the FETs Q_7 and Q_6 constitute input and output portions, respectively, of the current mirror circuit 12, the current i_6 flowing in the source-drain path of the FET Q_6 is equal to the current flowing in the source-drain path of the FET Q_7. Since the current flowing in the source-drain path of the FET Q_7 is equal to that flowing in the source-drain path of the FET Q_2 and, therefore, is also equal to that of i_3, it is apparent that the magnitudes of the currents i_3 and i_6, when permitted to flow through the switching transistors Q_4 and Q_5, respectively, will have the same magnitude. Accordingly, the charge pump circuit 21 forces the magnitudes of the currents i_3 and i_6 to equal that of the reference current i_1 whenever the respective switching transistors Q_4 and Q_5 are turned ON.

In operation, where the phase comparison signal V is phase delayed with respect to the phase comparison signal R such that the phase difference signal U is in a logic "0" state and the phase difference signal D is in a logic "1" state, the switching transistor Q_4 is turned ON and the switching transistor Q_5 is turned OFF. Accordingly, the constant current i_3 is then provided to the loop filter 22 to charge the capacitors C_1 and C_2 to increase the level of the output voltage E_6 of the loop filter 22. Consequently, the phase (that is, the oscillation frequency) of the oscillation signal produced by the VCO 7 is advanced. Since the capacitors C_1 and C_2 are charged by a current i_3 having a constant magnitude, the voltage level E_6 is linearly increased thereby.

When the second phase comparison signal V is phase advanced with respect to the first phase comparison signal R so that the first phase difference signal U is in a logic "1" state while the second phase difference signal D is in a logic "0" state, the first switching transistor Q_4 is then turned OFF while the second switching transistor Q_5 is turned ON such that the capacitors C_1 and C_2 are thereby discharged by the constant current i_6. Consequently, this simultaneously decreases the level of the output voltage E_6 of the loop filter 22 in a linear fashion, such that the phase of the oscillation signal produced by the VCO 7 is delayed.

Furthermore, at such times that the first and second phase comparison signals R and V are in phase such that the first and second phase difference signals U and D are in a logic "1" state, the first and second switching transistors Q_4 and Q_5 are both turned OFF, so that neither the current i_3 nor the current i_6 is permitted to flow to the output terminal T_2. Consequently, the capacitors C_1 and C_2 are neither charged or discharged and the output voltage level E_6 is maintained at a constant value such that the phase of the oscillation signal produced by the VCO 7 is likewise unchanged.

As noted above, where the phase comparison signals R and V are in phase, during a short period of time commencing from the trailing edges of the phase comparison signals R and V, both of the first and second phase difference signals U and D switch to a logic "0" state before returning to a logic "1" state at the end of the short time period. Since, however, the magnitudes of the charging and discharging currents i_3 and i_6, respectively, are equal, they add to zero when both of the first and second switching transistors Q_4 and Q_5 are turned ON by the logic "0" levels of the first and second phase difference signals U and D. Accordingly, the capacitors C_1 and C_2 of the loop filter 22 are neither charged nor discharged at such time and the level of the output voltage E_6 is maintained at a constant value so that the phase of the oscillation signal produced by the VCO 7 is unchanged.

With reference again to Fig. 2, the continuous line C indicates the relationship of the phase difference $\Delta\theta$ between the phase comparison signals V and R input to the phase comparison circuit 4 and the charging and discharging periods produced in response thereto by the charge pump circuit 21. It will be seen therefrom that a linear relationship exists between the

phase difference $\Delta\theta$ and the resulting charging and discharging periods. Since the charge pump circuit 21 supplies charging and discharging currents i_3 and i_6, respectively, which have a constant magnitude, it will be appreciated that the Fig. 1 embodiment provides a linear relationship between the phase difference $\Delta\theta$ and the control voltage E_6 even at arbitrarily small phase differences. Accordingly, the phase of the oscillation signal produced by the VCO 7 varies linearly with the phase difference $\Delta\theta$ between the first and second phase comparison signals R and V.

When the transistor Q_9 is turned OFF, the reference current i_1 flows through the resistor R_2 only, such that the reference current i_1 is maintained at a relatively low value by the relatively high impedance presented by the resistor R_2 alone. When however, the transistor Q_9 is turned ON, the current i_1 is able to flow through the parallel combination of resistors R_1 and R_2, such that the magnitude of the current i_1 flowing through the FET Q_1 is increased. Since the currents i_3 and i_6 are equal in magnitude to the reference current i_1, it will be seen that a means is provided for adjusting the magnitudes of the constant currents i_3 and i_6 by controlling the ON-OFF states of the transistor Q_9. Since the output voltage E_6 of the loop filter 22 varies linearly with the magnitudes of the currents i_3 and i_6, it will be seen that, by adjusting the magnitudes of the constant currents i_3 and i_6 by selecting the ON-OFF states of the transistor Q_9, the loop gain of the phase locked loop is thereby adjusted. It will also be appreciated that the lock-up time of the phase locked loop can be selectably reduced by increasing the loop gain in the foregoing manner. Since the cut-off frequency of the loop filter 22 is determined only by the capacitors C_1 and C_2 and the resistor R_3, whose values are unaffected by the magnitudes of the charging and the discharging currents i_3 and i_6, the cut-off frequency of the loop filter 22 is unaffected by adjusting the loop gain in the foregoing manner. It will also be apparent that the loop gain can be made independent of the cut-off frequency.

With reference now to Fig. 3, a second embodiment of a phase locked loop system in accordance with the present invention is illustrated therein. Elements of the Fig. 3 embodiment corresponding to elements shown in Fig. 1 bear the same reference numerals.

In the Fig. 3 embodiment, the first and second current source transistors Q_3 and Q_6 are coupled directly to the output terminal T_2, while the source-drain path of the current source transistor Q_3 is coupled to the positive voltage power source terminal T_3 through a resistor R_6, while the source-drain path of the current sink transistor Q_6 is coupled to circuit ground through a resistor R_8. The source of the FET Q_1 is coupled to the positive voltage power supply terminal T_3 through a resistor R_4, while the source of the FET Q_2 is coupled to the positive voltage power source T_3 through a resistor R_5. The source of the FET Q_7 is coupled to circuit ground through a resistor R_7. A p-channel bypass switching FET Q_{10} has its source-drain path coupled in series with the resistor R_6 between the terminal T_3 and circuit ground and has its gate electrode coupled with the output terminal U' of the phase comparison circuit 4 through an inverter Q_{12}. Accordingly, the bypass switching transistor Q_{10} is operative to control the flow of the constant current i_3 supplied by the current source transistor Q_3 by bypassing the current i_3 whenever the first phase difference signal U is high.

An n-channel bypass switching FET Q_{11} has its source-drain path connected in series through the resistor R_8 between the terminal T_3 and circuit ground and its gate electrode connected with the output terminal D' of the phase comparison circuit 4. Accordingly, the FET Q_{11} acts as a second bypass switching transistor for controlling the flow of the constant current i_6 supplied by the current sink transistor Q_6 such that whenever the second phase difference signal supplied at the output terminal D' of the phase comparison circuit 4 is in a logic "1" state, the second bypass switching transistor Q_{11} is turned ON to bypass the current i_6 which otherwise would flow through the current sink transistor Q_6. In all other respects, the operation of the Fig. 3 embodiment is identical to that of the Fig. 1 embodiment.

It will be readily appreciated by those skilled in the art that the embodiments of Figs. 1 and 3 may be similarly constructed with the use of bipolar transistors in place of the field effect transistors (FETs) specifically disclosed herein.

Although specific embodiments of the invention have been described in detail herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various changes and modifications may be effected therein by one skilled in the art without departing from the scope of the invention as defined in the appended claims.

Claims

1. Charge pump circuit in a PLL-system with a digital phase comparison circuit, comprising:
   - a series connection of a first transistor (Q_3) and a second transistor (Q_6) of the type complementary to the type of said first transistor, between a power source voltage terminal and ground;
   - a third transistor (Q_7) being connected to said second transistor to form a mirror circuit together with said second transistor; and
   - a transistor means (Q_1, Q_2) being connected to said first transistor (Q_3) and being

connected in series with said third transistor (Q_7) between said power voltage terminal and ground;

characterized in that

- an input circuit is provided, having a parallel connection between a terminal (T_1) and ground of a first resistor (R_2), and a series connection of a transistor (Q_9) and a second resistor (R_1), the control terminal of said transistor receiving a voltage for controlling its ON-OFF state; and
- said transistor means comprises the following features:
  -- it is composed of a fourth transistor (Q_1) in a mirror circuit together with said first transistor (Q_3), and a fifth transistor (Q_2), which transistors are of complementary types and have their control terminals connected to each other;
  -- the fifth transistor (Q_2) being connected in series with said third transistor (Q_7) between said power source voltage terminal and ground; and
  -- the control terminals of said first, fourth and fifth transistors are connected to the terminal of said input circuit.

Patentansprüche

1. Ladungspumpschaltung in einem PLL-System mit einer digitalen Phasenvergleichsschaltung, mit:
   - einer Reihenschaltung aus einem ersten Transistor (Q_3) und einem zweiten Transistor (Q_6) vom Typ, der zum Typ des ersten Transistors komplementär ist, zwischen einem Spannungsquelleanschluß und Masse;
   - einem dritten Transistor (Q_7), der so mit dem zweiten Transistor verbunden ist, daß er zusammen mit diesem eine Spiegelschaltung bildet; und
   - einer Transistoreinrichtung (Q_1, Q_2), die mit dem ersten Transistor (Q_3) verbunden ist und in Reihe zum dritten Transistor (Q_7) zwischen den Spannungsquelleanschluß und Masse geschaltet ist;

   dadurch gekennzeichnet, daß
   - eine Eingangsschaltung vorhanden ist, mit einer Parallelschaltung zwischen einem Anschluß (T_1) eines ersten Widerstands (R_2) und Masse und einer Reihenschaltung aus einem Transistor (Q_9) und einem zweiten Widerstand (R_1), wobei der Steueranschluß des Transistors eine Spannung zum Steuern seines EIN/AUS-Zustands erhält; und
   - die Transistoreinrichtung die folgenden Merkmale aufweist:
     -- sie besteht aus einem vierten Transistor (Q_1) in einer Spiegelschaltung zusammen mit dem ersten Transistor (Q_3) und einem fünften Transistor (Q_2), wobei die Transistoren von komplementärem Typ sind und ihre Steueranschlüsse miteinander verbunden sind;
     -- der fünfte Transistor (Q_2) ist in Reihe zum dritten Transistor (Q_7) zwischen den Spannungsquelleanschluß und Masse geschaltet und
     -- die Steueranschlüsse des ersten, vierten und fünften Transistors sind mit dem Anschluß der Eingangsschaltung verbunden.

Revendications

1. Circuit à pompe à charge dans un oscillateur à phase asservie (PLL) avec un circuit numérique de comparaison de phase, comprenant:
   - un montage en série d'un premier transistor (Q3) et d'un deuxième transistor (Q6) du type complémentaire du type dudit premier transistor, entre une borne à tension de source d'énergie et la masse;
   - un troisième transistor (Q7) connecté audit deuxième transistor pour former un circuit à miroir de courant avec ledit deuxième transistor; et
   - des moyens formant transistor (Q1, Q2) connectés audit premier transistor (Q3) et montés en série avec ledit troisième transistor (Q7) entre ladite borne à tension de source d'énergie et la masse,

     caractérisé en ce que:
   - un circuit d'entrée est prévu, ayant un montage en parallèle, entre une borne (T1) et la masse, d'une première résistance (R2), et un montage en série d'un transistor (Q9) et d'une deuxième résistance (R1), la borne de commande dudit transistor recevant une tension pour commander son état bloqué ou débloqué; et
   - lesdits moyens formant transistor comprennent les particularités suivantes:
   - ils sont constitués par un quatrième transistor (Q1) dans un circuit à miroir de courant avec ledit premier transistor (Q3), et un cinquième transistor (Q2), lesquels transistors sont de types complémentaires et ont leurs bornes de commande connectées l'une à l'autre;
   - le cinquième transistor (Q2) étant monté en série avec ledit troisième transistor (Q7) en-

tre ladite borne à tension de source d'énergie et la masse; et

- les bornes de commande desdits premier, quatrième et cinquième transistors sont connectées à la borne dudit circuit d'entrée.

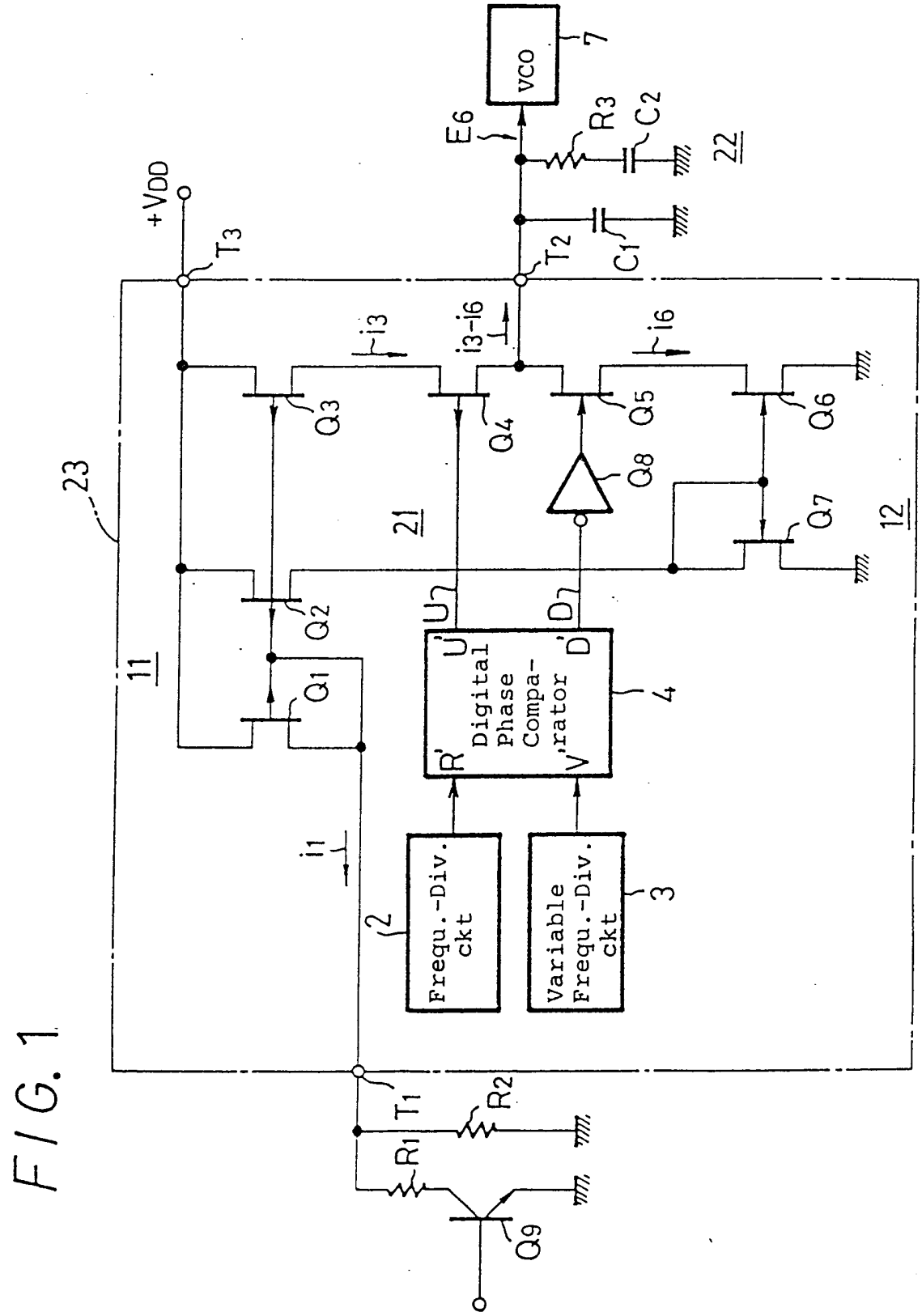

VCO
7
E6
R3
C2
22
+VDD
T3
T2
C1
i3
i3-i6
i6
Q3
Q4
Q5
Q6
Q8
Q7
23
21
12
11
Q2
Q1
U
D
U'
D'
R'
V'
Digital Phase Compa-rator
4
i1
Frequ.-Div. ckt
2
Variable Frequ.-Div. ckt
3
T1
R2
R1
Q9

FIG. 1

FIG. 2

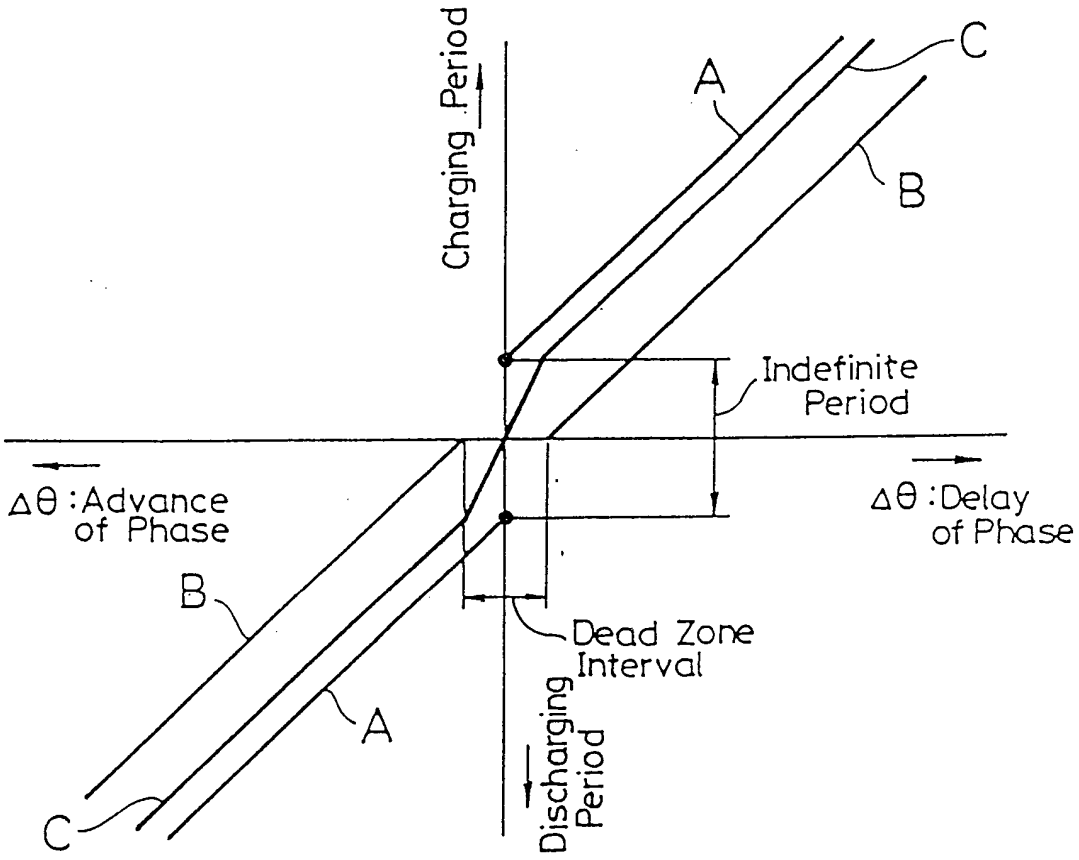
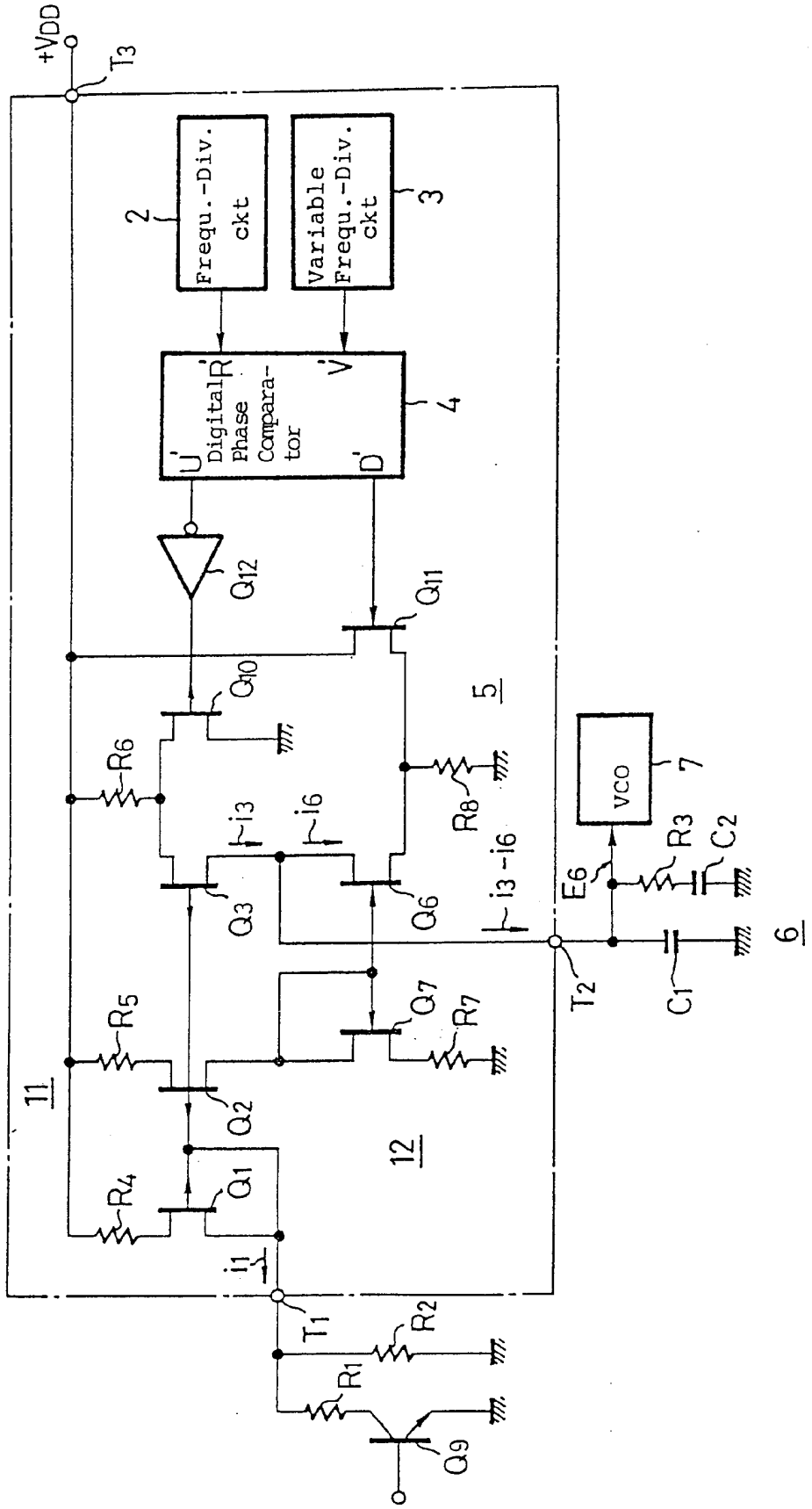

Charging Period
A
C
B
Indefinite Period
Δθ :Advance of Phase
Δθ :Delay of Phase
B
Dead Zone Interval
A
C
Discharging Period

FIG. 3


+VDD
T3
2
Frequ.-Div. ckt
3
Variable Frequ.-Div. ckt
4
U'
Digital Phase Comparator
R'
V'
D'
Q12
Q11
Q10
5
R6
R8
i3
i6
i3 -i6
Q3
Q6
VCO
7
E6
R3
C2
C1
T2
6
R5
Q7
R7
11
Q2
12
R4
Q1
i1
T1
R2
R1
Q9