3. The circuit of claim 1, further comprising a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal.

4. The circuit of claim 3, further comprising a charge/discharge control logic for determining the amount of phase correction to be made based on the determination of said difference of phase.

5. The circuit of claim 1, wherein said analog image data and said time reference signal are received on two separate signal paths.

6. The circuit of claim 5, wherein said reference clock comprises a binary signal.

7. The circuit of claim 1, wherein said digital circuit distributes phase error between said feedback signal and said reference signal during a comparison cycle by changing the phase of individual clock pulses in said sampling clock.

8. The circuit of claim 1, wherein said frequency correction logic generates a multi-bit number, wherein said multi-bit number is representative of the amount of phase advance of said sampling clock generated by said DTO during a DTO clock period, and wherein said multi-bit representation enables said PLL to reach said sampling frequency within a short duration.

9. The circuit of claim 1, wherein said frequency correction logic comprises:

a first multiplexor accepting as input Pnom and Fdp values, wherein Pnom represents an expected frequency of said sampling clock and Fdp represents the correction due to the long-term frequency drifts;

a flip-flop for storing a value representative of the phase correction corresponding to the frequency correction logic;

an adder for adding or subtracting the output of said first multiplexor from the value stored in said flip-flop, wherein the output of said adder is stored in said flip-flop; and

a frequency correction control coupled to said flip-flop and said adder, wherein said frequency correction control causes said flip-flop to be set to Pnom at the beginning of a phase acquisition phase, and wherein said frequency correction control causes said adder to add or subtract Fdp depending on whether the sampling clock is early or late in comparison to said time reference.

10. The circuit of claim 1, further comprising:

a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal, wherein said phase and frequency detector asserts an EARLY signal a number of clock pulses proportionate to the difference of phase by which said feedback signal is earlier than said time reference signal and a or a LATE signal a number of pulses proportionate to the difference of phase by which said feedback signal is later than said time reference signal; and

a charge/discharge control logic implemented using digital components, said charge/discharge control logic including a phase integrator, said charge/discharge control logic charging said phase integrator according to the number of pulses said EARLY signal or said LATE signal is asserted, said charge/discharge logic discharging over a longer period of time than the charging period so as to spread the difference in phase over a comparison cycle, wherein the phase of said sampling clock is corrected during the discharging period.

11. The circuit of claim 10, further comprising a sign and zero crossing detector for correcting any over-correction performed by said charge/discharge logic during said discharging period.