Claims

What is claimed is:

1. A driving circuit, comprising:

a pair of input ports;

a pair of differential output ports;

a first differential pair, directly connected to a first voltage level, having a first input terminal coupled to one of the input ports, a second input terminal coupled to the other of the input ports, a first output terminal coupled to one of the differential output ports, and a second output terminal coupled to the other of the differential output ports;

a second differential pair, having a first input terminal coupled to one of the input ports, a second input terminal coupled to the other of the input ports, a first output terminal coupled to one of the differential output ports, and a second output terminal coupled to the other of the differential output ports;

a load unit, coupled to the pair of differential output ports; and

a current source, coupled between the second differential pair and a second voltage level.

2. The driving circuit of claim 1, wherein the first differential pair comprises:

a first transistor having a source terminal directly connected to the first voltage level, a drain terminal coupled to one of the differential output ports, and a gate terminal coupled to one of the input ports; and

a second transistor having a source terminal directly connected to the first voltage level, a drain terminal coupled to the other of the differential output ports, and a gate terminal coupled to the other of the input ports.

3. The driving circuit of claim 2, wherein the second differential pair comprises:

a third transistor having a drain terminal coupled to one of the differential output ports, and a gate terminal coupled to one of the input ports; and

a fourth transistor having a drain terminal coupled to the other of the differential output ports, and a gate terminal coupled to the

other of the input ports.

4. The driving circuit of claim 3, wherein the first voltage level is higher than the second voltage level.

5. The driving circuit of claim 4, wherein the first transistor and the second transistor are PMOS transistors, and the third transistor and the fourth transistor are NMOS transistors.

6. The driving circuit of claim 3, wherein the second voltage level is higher than the first voltage level.

7. The driving circuit of claim 6, wherein the first transistor and the second transistor are NMOS transistors, and the third transistor and the fourth transistor are PMOS transistors.

8. The driving circuit of claim 1, wherein the load unit is a resistance element.

9. A driving circuit, comprising:

a pair of input ports;

a pair of differential output ports;

a first transistor having a source terminal directly connected to a first voltage level, a drain terminal coupled to one of the differential output ports, and a gate terminal coupled to one of the input ports;

a second transistor having a source terminal directly connected to the first voltage level, a drain terminal coupled to the other of the differential output ports, and a gate terminal coupled to the other of the input ports;

a third transistor having a drain terminal coupled to one of the differential output ports, and a gate terminal coupled to one of the input ports;

a fourth transistor having a drain terminal coupled to the other of the differential output ports, and a gate terminal coupled to the other of the input ports;

a load unit, coupled to the pair of differential output ports; and

a current source, coupled between a second voltage level and the

sources of the third and fourth transistors.

10. The driving circuit of claim 9, wherein the first voltage level is higher than the second voltage level.

11. The driving circuit of claim 10, wherein the first transistor and the second transistor are PMOS transistors, and the third transistor and the fourth transistor are NMOS transistors.

12. The driving circuit of claim 9, wherein the second voltage level is higher than the first voltage level.

13. The driving circuit of claim 12, wherein the first transistor and the second transistor are NMOS transistors, and the third transistor and the fourth transistor are PMOS transistors.

14. The driving circuit of claim 9, wherein the load unit is a resistance element.