PATENT ABSTRACTS OF JAPAN

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(54) SYNCHRONIZING CIRCUIT

(57)Abstract:

PURPOSE: To obtain the synchronizing circuit quickening the operating speed of a relevant circuit.

CONSTITUTION: A time difference detection pulse 23 is obtained by resetting a D flip-flop 9 with a detection pulse via a NAND gate 5, an AND gate 7 and triggering the flip-flop 9 with a reference pulse via an AND gate 6 in order to detect a time difference between a detection pulse resulting from a synchronization pattern of an input data at a synchronization pattern detection circuit 1 and the reference pulse from a frame counter 4. The pulse 23 is fed to an AND gate 11 via a pulse width limit circuit 10 to inhibit the clock input to the frame counter 4. In this case, a limit in the loop delay is avoided and the operating speed is quickened.