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(54) **Method to synchronize video modulation using a constant time base**

Verfahren zur Synchronisierung von Videomodulation mit konstanter Zeitbasis

Procédé de synchronisation de modulation vidéo utilisant une base de temps constante

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(56) References cited:
EP-A- 0 096 628
US-A- 5 027 212

EP 0 615 222 B1

Description

This invention relates to apparatus for synchronizing incoming video data in the form of pixels in successive lines in a raster scan to coincide with successive system clock signals at a particular frequency. The invention is especially adapted to be used in a graphics system.

Video data in the form of successive pixels in each line of a raster scan is often provided for use in a graphics system. For example, graphics data may be displayed on the face of a video monitor and the video may be displayed on a window on the face of this video monitor. The pixels are often presented from an external source such as from a tape at a frequency different from the clock in the graphics system in which the video data is to be displayed. Furthermore, the frequency of the video data sometimes varies somewhat. This results from the fact that the lengths of the successive lines of the pixels tend to vary somewhat.

From EP-A2-096 628 it is known to use a signal display for overlaying or separately displaying computer generated graphics/text and video data. It is described to lock the synchronisation of an apparatus for combining a video signal with graphics and text from a computer to the timing of the video image source when video data is displayed.

US 5 027 212 relates to a system for combining video signals and graphic signals on a common display. Both signals are combined using the synchronisation from the computer graphics generator. To achieve conversion of the video input signal to a signal synchronised to the computer graphics generator, field/frame stores are used which have different video data input and output rates wherein the input rate corresponds to the video clock rate and the read-out of the video data corresponds to the clock rate generated by the computer.

Conventionally, the frequency of the system clock signals has been varied to attempt to have this frequency conform to the frequency at which the pixels in the'video data are presented. This has presented complications. For example, since the frequency of the video data is not constant, the frequency of the system clock signals tends to vary with time. Furthermore, since the operation of the system is tied to the frequency of the system clock signals, variations in the frequency of the system clock signals tends to produce complications in the operation of the system.

In addition to the horizontal sync signal at the beginning of each line, there is also a burst of sinusoidal signals at a sub-carrier frequency. In the NTSC system used in the United States, this frequency is at approximately 3.56 megahertz. In a system developed by Fujitsu and disclosed in "SINGLE-CHIP DIGITAL PLL LSI FOR TELEVISION IMAGE-PROCESSING SYSTEMS" published in FIND, Vol. 10, No. 1, February 1991, the pixels of video data are synchronized in time with the signals at the sub-carrier frequency. Although this system constitutes an improvement over the conventional system discussed in the previous paragraph, it still has significant limitations. It does not synchronize the video data with the system clock signal, thereby still producing complications in the operation of the system. Furthermore, the Fujitsu system provides only one adjustment per line. This causes deviations to occur in the successive pixels in each line from the sub-carrier frequency as a reference.

Video data in the form of successive pixels in a raster scan have been provided for display on the face of a video monitor for many years. In that period of time, the limitations in the systems of the prior art have been known and consideration has been given in all of that period to providing a system which will surmount these limitations.

This system provides a system which surmounts the limitations specified above. The system synchronizes the video data with the system clock signals. Furthermore, the system of this invention provides progressive corrections in the timing of progressive pixels in each line of video data in accordance with the timing of the successive system clock signals in that line.

This is achieved by the features of claim 1.

In one embodiment of the invention, successive pixels representing video data in each of successive lines in a raster scan are buffered. Each of the lines has a sync pulse defining the beginning of the line. System clock signals are provided at a particular frequency. A phase adjustment is determined between the sync pulse, preferably at a particular level in the sync pulse, and the adjacent system clock signal. The actual or expected phase adjustment between the pixels at the end of each line are also determined.

The difference between the phase adjustments at the beginning and end of each line is then determined. Progressive adjustments are made in the phase of each successive pixel in the line relative to the system clock signals in accordance with the number of the system clock signals in the line and the determined difference in the phase adjustment between the beginning and end of the line. In this way, the pixels of video data are synchronized with the system clock signals.

When the actual phase adjustment relative to the system clock signals is determined at the end of each line, the difference in the phase adjustments between the beginning and the end of such line is determined from the phase adjustment for such line and the phase adjustment stored for the previous line. When the expected phase adjustment is provided for the end of each line, this estimated value is altered for each line by an amount equal to the actual phase adjustment at the beginning of such line and the estimated phase adjustment at the end of such line.

In the drawings:

Figure 1 is a circuit diagram in simplified block form of one embodiment of the invention;

Figure 2 is a circuit diagram in simplified block form and shows in additional detail a first embodiment of a particular one of the stages shown in Figure 1,

Figure 3 is a circuit diagram in simplified block form and shows in additional detail another embodiment of the particular one of the stages shown in Figure 1;

Figure 4 is a circuit diagram in simplified block form and shows in additional detail another of the stages shown in Figure 1;

Figure 5 shows a modification in simplified block form of the embodiment shown in Figure 1;

Figure 6 is a chart showing the combinations of the different types of stages which can be included in the blocks designated as "1", "2" and "3" in the embodiments shown in Figures 1 and 5; and

Figure 7 is a schematic representation of one of the lines of video data provided to the embodiments shown in the previous Figures.

In the embodiment of the invention shown in Figure 1, a system generally indicated at 10 is provided as on an integrated circuit chip for synchronizing video data with a system clock signal which is introduced on a line 12 with a substantially constant frequency. For example, the system clock frequency may be generated as by a crystal. The system clock signal synchronizes the operation of a graphics system 14 which operates in conjunction with this invention. For example, the graphics system 14 may receive the video data after processing of the data by the embodiment shown in Figure 1 and may combine the processed video data with graphics data from the graphics system 14. As one illustration, the graphics data may be visually presented on the face of a video monitor (not shown) and the video data may be visually presented in a window on the face of the video monitor.

The video data may be in the form conventionally presented as in broadcast video or in a video tape recorder or in S- video. S- video provides two (2) channels of information such as shown in Figure 5 and described in detail subsequently. The video data may be presented in successive lines in a conventional raster scan. One of these lines is generally indicated at 16 in Figure 7. It includes a horizontal sync signal 18 which defines the beginning of the line. It also includes a plurality of burst signals at a particular frequency such as approximately 3.56 megahertz schematically illustrated at 20 in Figure 7. It further includes video data schematically illustrated at 21 in Figure 7. The video data may be in the form of successive pixels for presentation on the face of a video monitor (not shown).

The video data is introduced in analog form on a line 22 in Figure 1 and is converted to a digital form in a stage 24. The information in digital form is then introduced to a stage 26 designated in Figure 1 as "1". This stage may have several different forms as indicated in a chart shown in Figure 6 and as will be discussed in detail subsequently. The information from the stage 26 may then be introduced to a buffer 28 which may be constructed in a conventional manner. The buffer 28 stores the digital information for the successive pixels and releases the pixels in sequence from the buffer in the order in which the pixels are introduced to the buffer. In effect, the buffer 28 constitutes a first-in first-out (FIFO) shift register. The buffer 28 may store the visual data for a whole line or a part of a line.

The digital signals from the converter 24 are introduced to a low pass filter 30 which passes signals in a relatively low range of frequencies such as approximately zero to five megahertz (0-5 Mhz). The low pass signals from the filter 30 then pass to a threshold stage 32 which produces a signal when the low pass signals pass through a particular voltage level. The threshold stage 32 also receives the system clock signals on a line 12 and produces a phase adjustment signal representing the difference in phase between the threshold level of the low pass signals and a particular portion, such as the rising edge, of the adjacent system clock signal. The phase adjustment signal represents the phase adjustment at the beginning of each line of pixels representing the video data.

A phase adjustment determinator 34 receives the phase adjustment at the beginning of each line of pixels and the phase adjustment at the end of the line and determines the difference between these phase adjustments. This difference represents the change in the phase adjustment through the line. The phase adjustment at the end of each line of pixels may be either an actual phase adjustment or an estimated phase adjustment at the end of the line.

The circuitry for determining the actual phase adjustment through each line on the basis of the difference between the actual phase adjustment at the beginning and end of each line is shown in Figure 2. It includes the threshold stage 32 and a register 40. The phase adjustment signal from the threshold stage for each line of pixels is introduced to a register 40 which stores the phase adjustment signal and introduces the stored signal to an arithmetic stage 42. The arithmetic stage 42 also receives the phase adjustment signal from the threshold stage 32. In this way, the arithmetic signal determines the difference between the phase adjustment signals at the beginning of successive pairs of lines. The difference signal from the arithmetic stage 42 is introduced to a line 44.

The circuitry for determining the estimated phase adjustment through each line on the basis of the difference between the estimated phase adjustment at the end of each line and the actual phase adjustment at the beginning of each line is shown in Figure 3. The system shown in Figure 3 includes the threshold stage 32 and a stage 50 indicating the estimated phase adjustment at the end of each line. The phase adjustments from the threshold stage 32 and the phase adjustment estimator 50 are introduced to an arithmetic stage 52 which determines the difference between such phase adjust-

ments. The signal from the arithmetic stage 52 for each line of pixels represents the expected phase adjustment through such line of pixels.

The signal from the arithmetic stage 52 for each line of pixels is introduced to a low pass filter 53 which introduces signals at relatively low frequencies such as zero to five megahertz (0-5 Mhz) to a line 54. The signals on the line 54 pass to an arithmetic stage 56. The arithmetic stage 56 also receives the output from the phase adjustment estimator 50 and adjusts the estimated phase adjustment in accordance with the signal on the line 54. In this way, the phase adjustment estimator 50 adjusts the estimated phase adjustment for each line of pixels in accordance with the adjustments made on the line 54 for the previous line of pixels.

The signal on the line 44 in Figure 2 in representation of the actual phase adjustment through a line of pixels or the signal on the line 54 in representation of the estimated phase adjustment through a line of pixels is introduced to an interpolation phase generator 60 in Figure 1. The interpolation phase generator 60 also receives the system clock signals in each line of pixels and determines the number of the system clock signals in such line. The interpolation phase generator 60 then determines the phase adjustment for each system clock signal in each line. In effect, the interpolation phase generator 60 divides the actual or estimated phase adjustment per line by the number of the system clock signals in the line. Thus, the interpolation phase generator 60 may be considered as a multiplier which multiplies the actual or expected phase adjustment per line by 1/N where N is the number of system clock signals per line. The results of the division are provided on a line 62 in Figures 1, 4 and 5.

The signals from the interpolation phase generator 60 in Figure 1 are introduced to an interpolator 70 in Figure 1. The interpolator 70 also receives the output from a stage 78 which is designated as "2" in Figure 1. The input of the stage 78 is connected to the output of the line buffer 28 in Figure 1. The stage 78 may take a number of different forms as shown in Figure 6 and as described in detail subsequently.

The interpolator 70 accumulates the phase adjustment per system clock signal on the line 62 in Figure 1 for the successive clock signals in each line of pixels and adjusts the phases of the successive pixels from the line buffer 28 in accordance with the accumulated phase adjustments for the successive system clock signals in that line. The interpolator 70 is shown in additional detail in Figure 4.

The interpolator 70 includes an arithmetic stage 72 and an accumulator 74 of the stored interpolation phase in Figure 4. The arithmetic stage 72 receives the output on the line 62 (also shown in Figure 1) in representation of the phase adjustment per system clock signal in each line of pixels. The arithmetic stage 72 also receives the output from the accumulator 74 and adds this output to the phase adjustment per system clock signal every time that a system clock signal appears on the line 12. In this way, the accumulator 74 progressively accumulates the phase adjustment per system clock signal as the system clock signals progressively occur throughout each line of pixels. This phase adjustment is then introduced to a phase shifter 80. The pixel data is shifted accordingly in phase.

The signals from the interpolator 70 are introduced to a stage 76 designated as "3" in Figure 1. The stage 76 has various possibilities of forms as shown in Figure 6 and discussed in detail subsequently. The signals from the stage 76 pass to the graphics system 14 the operation of which is synchronized with the system clock signals on the line 12. The graphics system 14 may illustratively provide graphics information from a display memory (not shown) at the frequency of the system clock signals. The information in the display memory may be displayed on the face of a video monitor (not shown). The visual data represented by the pixels in each line may be displayed in a window on the video monitor.

Figure 6 illustrates some of the various forms in which the stages 26, 76 and 78 may operate. Three columns are shown in Figure 6. The first column indicates the form in which the stage 26 may operate. This column is designated as "1" to conform to the designation for the stage 26 in Figure 1. The second column is designated as "2" to correspond to the designation "2" for the stage 78 in Figure 1. The indications in column 2 in Figure 6 indicate the different forms in which the stage 78 may operate. The third column in Figure 6 indicates the form in which the stage 76 may operate. The third column in Figure 6 has the designation "3" to correspond to the designation "3" for the stage 76 in Figure 1.

As will be seen, the indications in the three (3) different columns in Figure 6 have the designations "a", "b", "c", "d". Below the columns in Figure 6, but included in Figure 6, are descriptions of the forms identified by the designations "a", "b", "c" and "d". All of the forms "a", "b", "c" and "d" are well known in the art. A stage such as the stage "1" (the stage 26) may have the designation "a, b, c". This means that the stage "1" (the stage 26) may have either the form "a", the form "b" or the form "c". Alternatively, the designation "a", "b", "c" for the stage "1" (the stage 26) may have a combination of some or all of the stages "a", "b" and "c". The above description for the stage "1" (the stage 26) also applies to the stage "2" (the stage 72) and the stage "3" (the stage 76).

The designation "a" is identified at the bottom of Figure 6 as a "Y/C Separator". As will be appreciated, the designation "Y" indicates the luminance of color pixels and the designation "C" indicates the chrominance of the color pixels. The "Y" and "C" components of color pixels are provided in an S-band video. Figure 5 indicates an S-band video system generally indicated at 80 and corresponding to the system shown in Figure 1. The system 80 has two (2) channels, one (1) for processing

the "Y" component and the other for processing the "C" component. Each of these channels corresponds to the channel including the stages 26, 28, 78, 70 and 76 in Figure 1. The stages in the "Y" channel are accordingly designated as "26a", "28a" "78a", "70a" and "76a" in Figure 5. The stages in the "C" channel are similarly designated as "26b", "78b", "70b" and "76b". The outputs from the stages 76a and 76b are introduced to the graphics system 14 also shown in Figure 1. The system shown in Figure 6 additionally includes the stages 30, 32, 34 and 60 also shown in Figure 1.

The designation "b" in Figure 6 identifies a demodulator for separating the chrominance information "C" for the color pixels into the two (2) quadrature components "I" and "Q". The designation "C" in Figure 6 identifies a color space converter. The color space converter changes the luminance and chrominance components of the color in the pixels in each line into indications of the three (3) primary colors red, green and blue.

The designation "d" identifies a gamma translator. The gamma translator is disclosed and claimed in application Serial No. 07/987,367 filed by James Corona on December 7, 1992 for "Apparatus For, and Methods of, Providing a Universal Format of Pixels and For Scaling Fields in the Pixels" and assigned of record to the assignee of record of this application. The gamma corrector receives binary bits, less than a particular number, of information for each of the primary colors and converts such information to binary bits of a particular number to identify each of such primary colors. For example, the gamma corrector converts six (6) bits of binary indications for each of the primary colors red, green and blue to eight (8) bits of binary indications for each of such primary colors. The gamma corrector provides such conversion with an error less than one half (1/2) of the value of the least significant binary bit for each of the primary colors.

The system constituting this invention has certain important advantages. It provides for the transfer of video data representing successive pixels in each line in a raster scan in synchronism with the system clock signals. Furthermore, the system determines the phase adjustment between the video pixels and the system clock signals at the beginning and the end of each line and then determines the difference between these phase adjustments. The system then uses this difference and the number of system clock signals in each line to provide progressive adjustments for the successive pixels in each line in accordance with the occurrence of the successive system clock signals in such line.

In another embodiment, it is possible to generate data at a sampling resolution different from the system clock which is provided in the integrated circuit chip. By adding or subtracting a (programmable) constant to the output 62 of the interpolation phase generator 60 (Figures 1 and 5), it is possible to vary the effective output rate from the frequency of the system clock signals on the line 12. The data will be aligned to signals at a constant frequency above or below the system clock frequency.

Claims

1. Apparatus for synchronising video data, comprising:

   first means (24) for providing video data in a raster scan having successive lines (16) and having successive pixels in each of the successive lines and having a horizontal sync pulse (18) in each of the successive lines to define the beginning of such line;

   second means (12) for providing system clock signals at a particular frequency;

   characterised by

   third means (32,34) for determining the difference in time between each horizontal sync pulse and the adjacent one of the system clock signals to determine a phase adjustment to be made per line in the video data for providing the video data in synchronism with the system clock signals;

   fourth means (60) for determining the number of system clock signals in each line of the video data; and

   fifth means (70) for providing an adjustment in the phase of the successive pixels in the video data in accordance with the difference in the time between successive horizontal sync pulses and the adjacent ones of the system clock signals and in accordance with the number of system clock signals per line to have such pixels occur in synchronism with the system clock signals.

2. Apparatus according to claim 1
   characterised in that

   the fifth means (70) including a buffer (74) for storing the video data in at least a portion of each line,

   the fifth means being operative to provide an adjustment in time of the successive pixels in the buffer to occur in synchronism with the system clock signals.

3. Apparatus according to claims 1 or 2
   characterised in that
   the third means includes sixth means (32) for deter-

mining the adjustment in phase between the horizontal sync signal in each line and the adjacent one of the system clock signals and seventh means (40) for storing such phase adjustment determination and eighth means (62) for determining the difference between the stored phase adjustment from the seventh means (40) for each line and the phase adjustment determined by the sixth means (32) for each line to determine the phase adjustment to be made per line in the video data for providing the video data in synchronism with the system clock signals.

4. Apparatus according to claims 1 or 2
characterised in that
the third means includes sixth means (32) for determining the adjustment in phase between the horizontal sync signal in each line and the third means includes seventh means (50) for providing an estimated adjustment in phase at the end of each line and the third means includes means (52) for adjusting the estimated phase adjustment at the end of each line in accordance with the difference between the determinations by the sixth means (32) and the estimated adjustment provided by the seventh means (50).

Patentansprüche

1. Vorrichtung zur Synchronisation von Videodaten mit:

einer ersten Einrichtung (24) zur Bereitstellung von Videodaten in einer Rasterabtastung mit aufeinanderfolgenden Zeilen (16) und mit aufeinanderfolgenden Pixeln in jeder der aufeinanderfolgenden Zeilen und mit einem horizontalen Synchronisationsimpuls (18) in jeder der aufeinanderfolgenden Zeilen, um den Anfang dieser Zeile festzulegen;

eine zweite Einrichtung (12) zur Bereitstellung von Systemtaktsignalen mit einer bestimmten Frequenz;

gekennzeichnet durch

eine dritte Einrichtung (32, 34) zur Bestimmung der zeitlichen Differenz zwischen jedem horizontalen Synchronisationsimpuls und dem Benachbarten der Systemtaktsignale, um eine Phasenanpassung festzulegen, die pro Zeile in den Videodaten zur Bereitstellung der Videodaten in Synchronisation mit den Systemtaktsignalen durchgeführt wird;

eine vierte Einrichtung (60) zur Bestimmung der Systemtaktsignale in jeder Zeile der Videodaten und

eine fünfte Einrichtung (70) zur Bereitstellung einer Phasenanpassung der aufeinanderfolgenden Pixel in den Videodaten in Übereinstimmung mit der zeitlichen Differenz zwischen aufeinanderfolgenden horizontalen Synchronisationsimpulsen und den Benachbarten der Systemtaktsignale und in Übereinstimmung mit der Anzahl der Systemtaktsignale pro Zeile, damit die Pixel in Synchronisation mit den Systemtaktsignalen auftreten.

2. Vorrichtung nach Anspruch 1
dadurch gekennzeichnet, daß

die fünfte Einrichtung (70) einen Puffer (74) zur Speicherung der Videodaten zumindest eines Teils jeder Zeile enthält,

die fünfte Einrichtung betrieben wird, um eine zeitliche Anpassung der aufeinanderfolgenden Pixel in dem Puffer zu bewerkstelligen, damit sie in Synchronisation mit den Systemtaktsignalen auftreten.

3. Vorrichtung nach Anspruch 1 oder 2,
dadurch gekennzeichnet, daß
die dritte Einrichtung eine sechste Einrichtung (32) zur Bestimmung der Phasenanpassung zwischen dem horizontalen Synchronisationssignal in jeder Zeile und dem Benachbarten der Systemtaktsignale und eine siebte Einrichtung (40) zur Speicherung dieser Phasenanpassungsbestimmung und eine achte Einrichtung (62) zur Bestimmung der Differenz zwischen der gespeicherten Phasenanpassung von der siebten Einrichtung (40) für jede Zeile und der Phasenanpassung enthält, die von der sechsten Einrichtung (32) für jede Zeile bestimmt wird, um die Phasenanpassung zu bestimmen, die pro Zeile an den Videodaten durchgeführt wird, um Videodaten in Synchronisation mit dem Systemtaktsignal bereitzustellen.

4. Vorrichtung nach Anspruch 1 oder 2,
dadurch gekennzeichnet, daß
die dritte Einrichtung eine sechste Einrichtung (32) zur Bestimmung der Phasenanpassung zwischen dem horizontalen Synchronisationssignal in jeder Zeile enthält und die dritte Einrichtung eine siebente Einrichtung (50) zur Bereitstellung einer geschätzten Phasenanpassung am Ende jeder Zeile enthält, und die dritte Einrichtung enthält eine Einrichtung (52) zur Einstellung der geschätzten Phasenanpassung am Ende jeder Zeile in Übereinstimmung mit der Differenz zwischen den Bestimmungen durch die sechste Einrichtung (32) und die geschätzte An-

passung, die von der siebten Einrichtung (50) bereitgestellt wird, enthält.

Revendications

1. Dispositif pour synchroniser des données vidéo, comprenant :

des premiers moyens (24) pour délivrer des données vidéo en un balayage de trame ayant des lignes successives (16) et ayant des pixels successifs dans chacune des lignes successives, et ayant une impulsion de synchronisation horizontale (18) dans chacune des lignes successives pour définir le commencement de cette ligne ;
des seconds moyens (12) pour délivrer des signaux d'horloge de système à une fréquence pariculière ;

caractérisé par

des troisièmes moyens (32, 34) pour déterminer la différence de temps entre chaque impulsion de synchronisation horizontale et celui adjacent des signaux d'horloge de système pour déterminer un ajustement de phase à apporter, par ligne, aux données vidéo de manière à délivrer les données vidéo de façon synchrone avec les signaux d'horloge de système ; et
des quatrièmes moyens (60) pour déterminer le nombre de signaux d'horloge de système dans chaque ligne des données vidéo ; et
des cinquièmes moyens (70) pour réaliser un ajustement de phase des pixels successifs dans les données vidéo en fonction de la différence de temps entre des impulsions de synchronisation horizontales successives et ceux adjacents des signaux d'horloge de système et en fonction du nombre de signaux d'horloge de système par ligne pour que ces pixels surviennent de façon synchrone avec les signaux d'horloge de système.

2. Dispositif selon la revendication 1
caractérisé en ce que

les cinquièmes moyens (70) incluent une mémoire tampon (74) pour mémoriser les données vidéo dans au moins une partie de chaque ligne,
les cinquièmes moyens sont opérants pour délivrer un ajustement de temps des pixels successifs dans la mémoire tampon pour qu'ils surviennent de façon synchrone avec les signaux d'horloge de système.

3. Dispositif selon la revendication 1 ou 2
caractérisé en ce que
les troisièmes moyens incluent des sixièmes moyens (32) pour déterminer l'ajustement de phase entre le signal de synchronisation horizontale de chaque ligne et celui adjacent des signaux d'horloge de système, et des septièmes moyens (40) pour mémoriser cette détermination de l'ajustement de phase et des huitièmes moyens (62) pour déterminer la différence entre l'ajustement de phase mémorisé à partir des septièmes moyens (40) pour chaque ligne et l'ajustement de phase déterminé par les sixièmes moyens (32) pour chaque ligne, afin de déterminer l'ajustement de phase à apporter, par ligne, aux données vidéo de manière à délivrer les données vidéo de façon synchrone avec les signaux d'horloge de système.

4. Dispositif selon la revendication 1 ou 2
caractérisé en ce que
les troisièmes moyens incluent des sixièmes moyens (32) pour déterminer l'ajustement de phase entre le signal de synchronisation horizontale de chaque ligne et les troisièmes moyens incluent des septièmes moyens (50) pour délivrer un ajustement de phase estimé à la fin de chaque ligne et les troisièmes moyens incluent des moyens (52) pour ajuster l'ajustement de phase estimé à la fin de chaque ligne en fonction de la différence entre les déterminations par les sixièmes moyens (32) et l'ajustement estimé de phase délivré par les septièmes moyens (50).

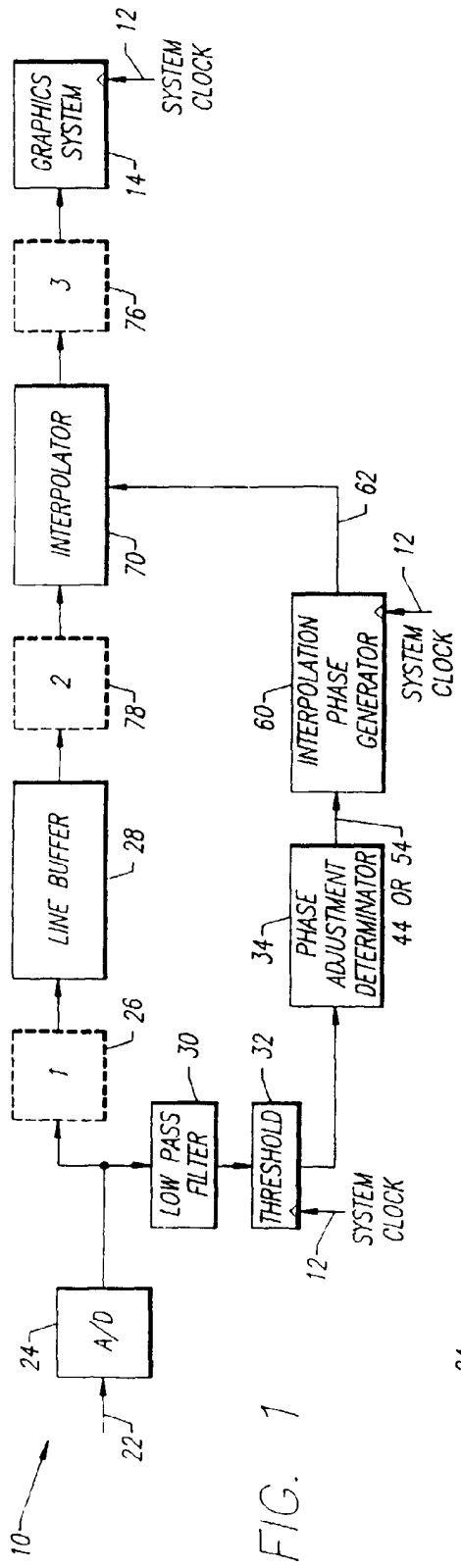

10
22
24
A/D
1
26
LINE BUFFER
28
2
78
INTERPOLATOR
70
3
76
GRAPHICS SYSTEM
14
12
SYSTEM CLOCK
LOW PASS FILTER
30
THRESHOLD
32
PHASE ADJUSTMENT DETERMINATOR
34
44 OR 54
INTERPOLATION PHASE GENERATOR
60
62
SYSTEM CLOCK

FIG. 1

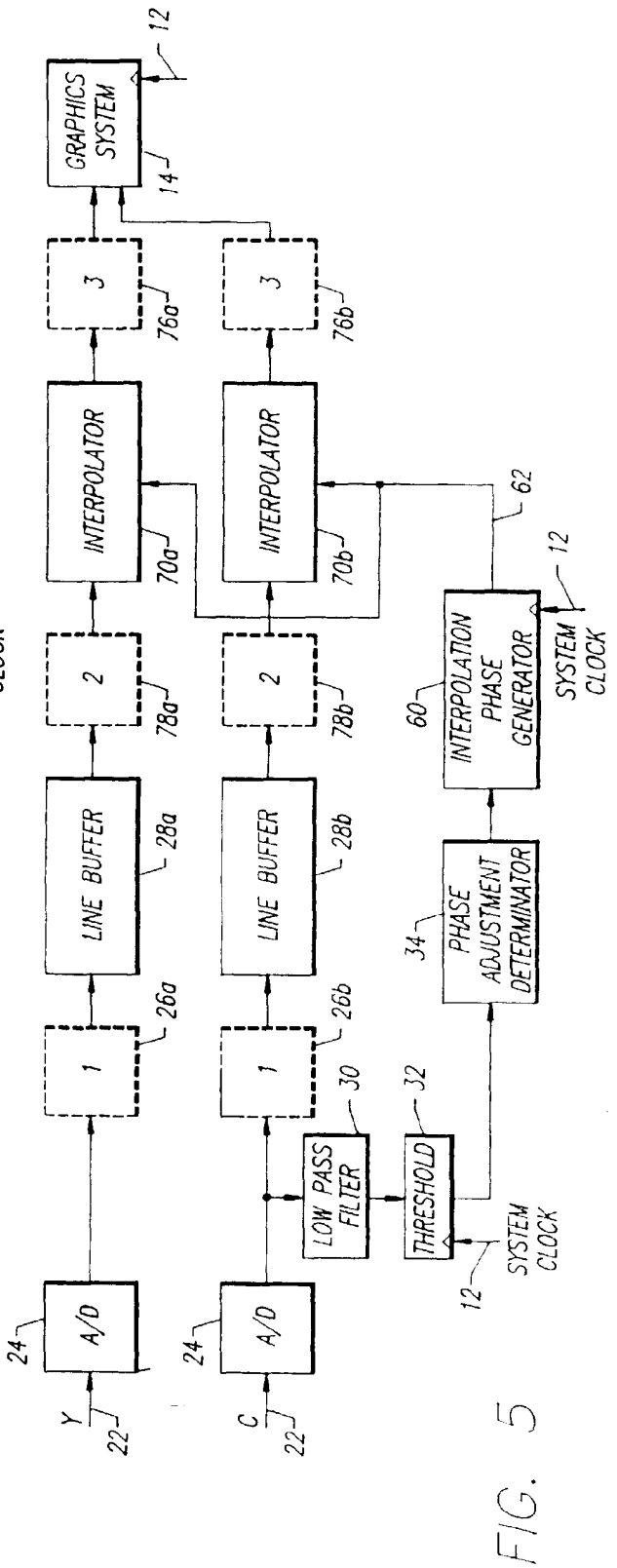

Y
C
22
24
A/D
1
26a
26b
LINE BUFFER
28a
28b
2
78a
78b
INTERPOLATOR
70a
70b
3
76a
76b
GRAPHICS SYSTEM
14
12
LOW PASS FILTER
30
THRESHOLD
32
PHASE ADJUSTMENT DETERMINATOR
34
INTERPOLATION PHASE GENERATOR
60
62
SYSTEM CLOCK

FIG. 5

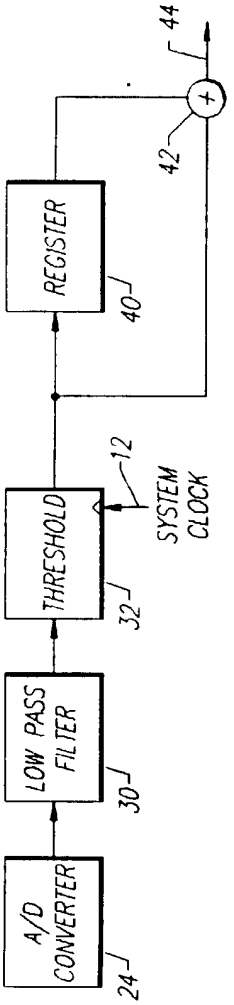

A/D CONVERTER
24
LOW PASS FILTER
30
THRESHOLD
32
12
SYSTEM CLOCK
REGISTER
40
42
44

FIG. 2

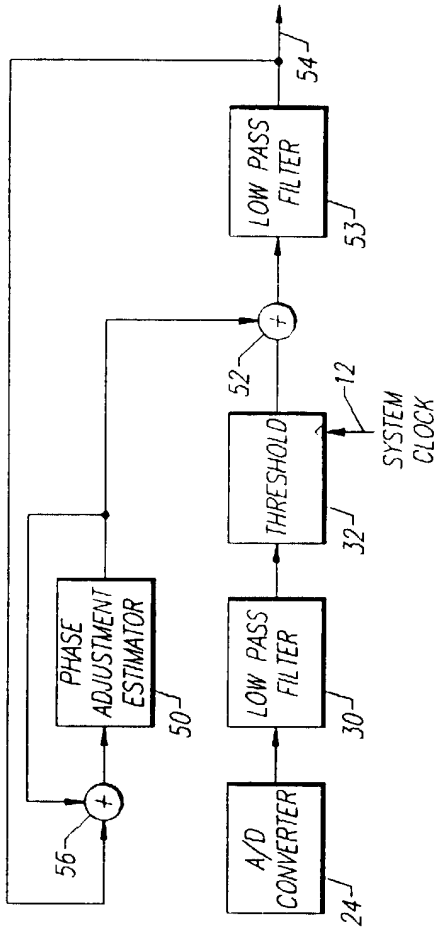
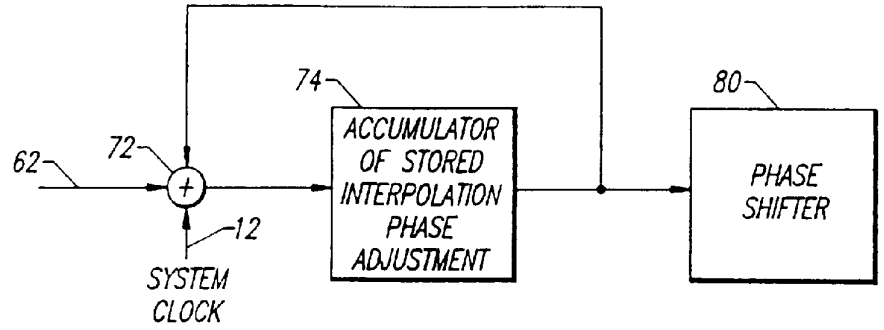

A/D CONVERTER
24
LOW PASS FILTER
30
THRESHOLD
32
12
SYSTEM CLOCK
52
LOW PASS FILTER
53
54
PHASE ADJUSTMENT ESTIMATOR
50
56

FIG. 3

FIG. 4

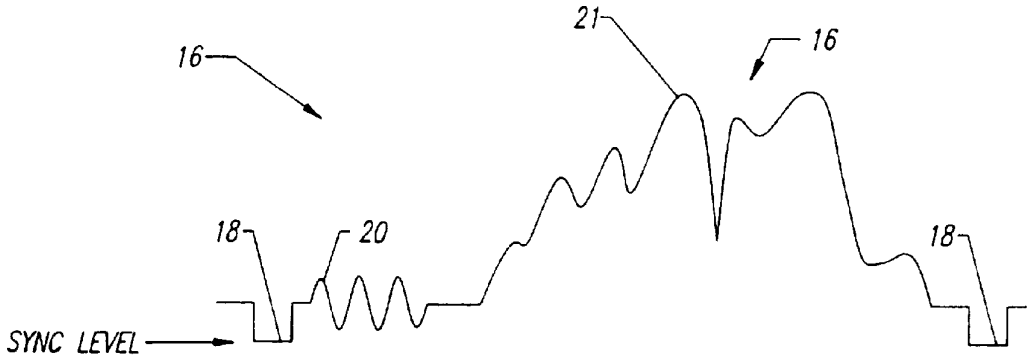


COLUMN 1	COLUMN 2	COLUMN 3
a, b, c		d
a, b	c, d	
a, b	c	d
a, b		c, d
a	c, b, d	
a	c, b	d
a	c	b, d
a		c, b, d
	a, c, b, d	
		a, b, c, d

a) Y/C SEPARATOR
b) DEMODULATOR
c) COLOR SPACE CONVERTER
d) GAMMA TRANSLATOR

FIG. 6

FIG. 7



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