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11/735,583	04/16/2007	Kiyoharu Takano	TI-62395	2263

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EXAMINER	
SOLLENBERGER, STEPHEN J	
ART UNIT	PAPER NUMBER
1791	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	11/735,583	TAKANO ET AL.	
	Examiner	Art Unit	
	STEPHEN SOLLENBERGER	1791	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-18, 20, 21, and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al. (US 5,218,759) in view of Miyajima (US 6,344,162).

Regarding claim 15 Juskey et al. teach a method for manufacturing a semiconductor device (Column 1, Line 61); comprising: providing a substrate that includes a first principal surface and a second principal surface opposite the first principal surface (Fig. 1 shows a substrate **12** with two principle surfaces); placing semiconductor elements on the first principal surface (a semiconductor device on a substrate; Column 1, Lines 14-15); placing the substrate on an insulating region of a lower die ("The temporary support substrate may be selected from a wide variety of materials, but is preferably a thin material such as a printed circuit board, flexible film"; Column 2, Lines 35-38). Note, the examiner considers the "wide variety of materials" to encompass insulators); pressing an upper die having multiple shape-forming parts are formed against the lower die; and supplying a liquid resin for molding the semiconductor elements ("A plastic material is then transfer-molded about the semiconductor device to form a completed package"; Column 1, Lines 18-20). Juskey et al.

does not teach that the upper die is lined with a polymer film. In the same field of endeavor of encapsulating semiconductor elements, Miyajima further teach pressing an upper die having the multiple shape-forming parts lined with a polymer film against the lower die the polymer film contacting a first conductive region on the first principle surface ("the release film 40 may be made from PTFE, ETFE, PET, FEP, etc. The release film 40 should have enough flexibility and extensibility so as to easily deform along inner faces of the molding sections, e.g., the cavities 26a"; Column 6, Lines 56-60; Figure 21; Note, the film lines a die, contacts a first surface of the substrate), and contacts the semiconductor surface when the package is inverted. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to line an upper die to apply the polymer film to the resin without inversion.)

Regarding claim 16, Juskey et al. in view of Miyajima teach the manufacturing method of claim 15. Juskey et al. does not explicitly teach wherein the lower die includes a ceramic member, and the second principal surface of the substrate is mounted on the ceramic member. However, Juskey et al. teach the support can be a wide variety of materials (Column 2, Lines 35-36). Note, it would have been obvious to one of ordinary skill in the art at the time of the invention that the film could be ceramic.

Regarding claim 17, Juskey et al. in view of Miyajima teach the manufacturing method described in claim 15. Juskey et al. further teach wherein the lower die includes an insulating film (Note, the temporary support substrate **18** of Fig. 1 is considered a film could be of a variety of materials

including insulators; Column 2, Lines 35-38), and the second principal surface of the substrate is mounted on the insulating film (Figure 1).

Regarding claim 18, Juskey et al. in view of Miyajima teach the manufacturing method described in claim 15. Juskey et al. further teach wherein the insulating region is larger than the second principal surface of the substrate (See Figure 1; the insulating region **18** is larger than the substrate **19**).

Regarding claim 20, Juskey et al. in view of Miyajima teach the manufacturing method described in claim 15. Juskey et al. further teach wherein the first conductive region on the first principal surface is electrically connected to semiconductor elements ("A semiconductor device is electrically and mechanically connected to one side of a circuit carrying substrate"; Column 1, Lines 61-63).

Regarding claim 21, Juskey et al. in view of Miyajima teach the semiconductor manufacturing method described in claim 20. Jusky et al. further teach wherein the first conductive region is uncovered by the molded resin ("transfer molding a plastic material about the semiconductor device and substantially all of the first major face of the circuit carrying substrate in order to form a second assembly; removing the second assembly from the mold cavity"; Column 6, Lines 31-35).

Regarding claim 26, Juskey et al. teach a method for manufacturing a semiconductor device; comprising: providing a substrate that includes a first principal surface and a second principal surface opposite the first principal surface; placing semiconductor elements on the first principal surface (Column

1, Lines 14-15); placing the substrate on a ceramic region enclosed by an o-ring in a lower die; pressing an upper die against the o-ring; and supplying a liquid resin for molding the semiconductor elements (Column 1, Lines 18-20). Juskey et al. does not teach pressing an upper die against an O-ring. In the same field of endeavor of pressing semiconductor packages, Miyajima teach placing the substrate on a ceramic region enclosed by an o-ring in a lower die; pressing an upper die against the o-ring ("A seal ring 101 is provided so as to suck the air through air suckingholes opened in an inner bottom face of the lower die 21"; Column 13, Lines 42-45; Note, it would have been obvious to one of ordinary skill in the art to include the o-ring on either the upper or lower die and is considered a design choice).

Regarding claim 27, Juskey et al. in view of Miyajima teach the method of claim 26. Juskey et al. further teach comprising covering a conductive land on the first principal surface with the upper die (Column 1, Lines 61-63; Figure 3).

Regarding claim 28, Juskey et al. in view of Miyajima teach the method of claim 27. Miyajima further teach comprising insulating the conductive land from the upper die with a insulative film ("The release film 40 has enough heat-resistibility against heat generated from the dies"; Column 4, Lines 54-56).

Regarding claim 29, Juskey et al. in view of Miyajima teach the method of claim 26. Juskey et al. or Miyajima do not explicitly teach in which the lower die comprises a conductive material having a thermal expansion coefficient of the same order of the thermal expansion coefficient of the ceramic. However, Juskey et al. mentions it is well known in the the art to match the expansion of

the semiconduction with the substrate (Column 1, Lines 29-31). Note, it is well known and would have been obvious to one of ordinary skill in the art at the time of the invention to have similar thermal expansion coefficients between a substrate and a die to prevent damage to the substrate or die.

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. with Miyajimai for the benefit of covering a formed semiconductor package with a film to electrically insulate and further protect the package from damage. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Juskey et al. with Miyajima for the benefit of encapsulating multiple parts of various dimensions.

Claims 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al. (US 5,218,759) in view of Miyajima (US 6,344,162) and in further view of Yamaji (US 5,394,303).

Regarding claim 22, Juskey et al. in view of Miyajima teach the manufacturing method described in claim 15. Juskey et al. in view of Miyajima do not teach the first and second surfaces of the substrate are electrically connected. In the same field of endeavor of forming semiconductor packages, Yamaji teach wherein the substrate includes a second conductive region on the second principal surface, and the second conductive region is electrically connected to the first conductive region or semiconductor elements ("To connect substrate wires 11_1 -11_n of the mounting substrate 10 to the device having the external electrode pads"; Column 3, Lines 12-25).

Regarding claim 25, Juskey et al. in view of Miyajima teach the manufacturing method described in claim 20. Juskey et al. in view of Miyajima do not teach the first and second surfaces of the substrate are electrically connected. In the same field of endeavor of forming semiconductor packages, Yamaji teach further comprising a step of stacking terminals of a second semiconductor device onto the first conductive region on the first principal surface of the substrate (Fig. 8 shows multiple semiconductor chips and terminals stacked on a substrate).

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. in view of Miyajima with Yamaji for the benefit of stacking multiple semiconductor terminals on a substrate and electrically connecting them for the benefit of greater efficiency and capacity.

Claims 19, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al. (5,218,759) in view of Miyajima (US 6,344,162) and in further view of Ujiie et al. (US 7,371,606 B2).

Regarding claim 19, Juskey et al. in view of Miyayama teach the manufacturing method described in claim 15. Juskey et al. fails to teach a polymer film held by suction by air intake on the upper die. In the same field of endeavor of making semiconductor packages, Ujiie et al. teach wherein the polymer film is held by suction in the multiple shape-forming parts by air intake from air intake holes formed in the upper die (“Vacuum suction holes 17b9 are formed in the upper die 17b. The laminate film 17c is vacuum-sucked through

the vacuum suction holes 17b9 and are brought into close contact with the molding surface of the upper die 17b"; Column 15, Lines 40-44).

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. in view of Miyajima with Ujiie et al. for the benefit of efficiency covering the package with a film and preventing damage to the film.

Regarding claim 23, Juskey et al. in view of Miyajima teach the manufacturing method described in claims 15. Ujiie et al. further teach wherein the substrate is a multilayer circuit board ("A semiconductor substrate 1S which constitutes the wafer 1W is formed of a single crystal of silicon (Si) for example and elements for forming a memory circuit such as, for example, SRAM (Static Random Access Memory), as well as a multi-layer interconnection, are formed on a main surface of the semiconductor substrate 1S"; Column 5, Lines 66-67 through Column 6, Lines 1-5).

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. in view of Miyajima with Ujiie et al. for the benefit of forming more complicated circuits including multi-layers.

Regarding claim 24, Juskey et al. in view of Miyajima teach the manufacturing method described in claim 15. Ujiie et al. further teach comprising a step of cutting the substrate into individual semiconductor elements ("covered all together with a sealing resin, and are then cut out into individual semiconductor chips"; Column 1, Lines 36-38).

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. in view of Miyajima with Ujiie et al. for the benefit of forming many individual packages.

Response to Arguments

Applicant's arguments filed 5/01/2009 have been fully considered but they are not persuasive. The applicant argues that the support of Jusky et al. is not an insulating region of a lower die. However, Juskey et al. discloses that the support is incorporated into the lower mold and is selected from a wide variety of materials. It is thus would have been obvious to one of ordinary skill in the art at the time of the invention that this layer can be chosen as an insulating region of a lower die. Additionally, any such material would provide some degree of insulation.

The applicant argues that the insulating film of Yamaji is not combinable with Juskey et al. However, an insulating film such as disclosed in Yamaji for semiconductor packages would be obvious to adapt to the device of Juskey et al. to one of ordinary skill in the art at the time of the invention.

The applicant argues that the lower of Juskey et al. is not ceramic. However, Juskey et al. states that this material could be selected from a wide variety of materials and it would have been obvious to one of ordinary skill in the art at the time of the invention that ceramic is included in “a wide variety of materials" as a very broad class of materials with insulative properties.

Applicant's remaining arguments with respect to amended claims 15-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN SOLLENBERGER whose telephone number is (571) 270-1922. The examiner can normally be reached from 9 am to 5 pm ET, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Del Sole can be reached at 571-272-1130. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

S.J.S.

/Joseph S. Del Sole/

Supervisory Patent Examiner, Art Unit 1791