The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 11 (Cancelled)

12. (New) A memory efficient display controller for upscaling a source image at a first resolution to a destination image at a second resolution, comprising:

an interface arranged to receive source image pixel data in accordance with a first clock;

a line buffer having a size in accordance with a first resolution scan line length arranged to receive the source image pixel data at a second clock and store the received source image pixel data therein; and

an interpolator coupled to the line buffer and arranged to form the destination image using selected stored source image pixel data read from said line buffer in accordance with the second clock.

13. (New) A display controller as recited in claim 12, wherein said interpolator comprises:

a vertical interpolator unit arranged convert a first resolution number of scan lines to a second resolution number of scan lines; and

a horizontal interpolator unit coupled to the vertical interpolator unit arranged to convert each of the second resolution number of scan lines each having the first resolution scan line length to a second resolution scan line length.

14. (New) A display controller as recited in claim 13, wherein the interpolator further comprises:

a second line buffer coupled to the vertical interpolator and the line buffer for storing only a previous scan line.

15. (New) A display controller as recited in claim 14, further comprising:

a third line buffer for storing a current scan line used with the previous scan line by the vertical interpolator to convert the first resolution number of scan lines to the second resolution number of scan lines.

16. (New) A display controller as recited in claim 13, wherein the line buffer is a single port memory type line buffer or wherein the line buffer is a dual ported memory type line buffer.

17. (New) A display controller as recited in claim 16, wherein when the line buffer is the single port SDRAM, then the line buffer further comprises a first bank and a second bank each having a size in accordance with the first resolution scan line length.

18. (New) A display controller as recited in claim 17, wherein when pixel data corresponding to a source image scan line is received in the first bank, then pixel data corresponding to another source image scan line can be concurrently read from the second bank as many times as required.

19. (New) A display controller as recited in claim 16, wherein when said line buffer comprises the dual-ported memory, the data is read from a port that is different from a port that receives the source image pixel data.

20. (New) A display controller as recited in claim 12, wherein the second clock is locked to said first clock in a proportion.

21. (New) A display controller as recited in claim 20, wherein the proportion is equal to (Htotal.sub.-- src.times.Vtotal.sub.-- src)/(Htotal.sub.-- dst.times.Vtotal.sub.-- dst), wherein Htotal.sub.-- src and Htotal.sub.-- dst represent the total number of pixels in each source scan line and each destination scan line respectively, and Vtotal.sub.-- src and Vtotal.sub.-- dst represent the total number of lines in the source image and the destination image, respectively.

22. (New) The display controller of claim 21, wherein the source image pixel data is received using an externally generated first clock that is locked to said first clock.

23. (New) The display controller of claim 12, wherein said source image has a source image aspect ratio and said destination image has a destination image aspect ratio that can be not equal to said source aspect ratio.

24. (New) The display controller of claim 12, wherein when said source image is an analog source image then the first clock is provided to a sampling circuit coupled to the interface that samples the analog source image at a sampling frequency such that each scan line in said source image is sampled a number of times equal to a number of pixels in each scan line in the destination image.

25. (New) A display controller as recited in claim 12, wherein an overrun condition in the line buffer is avoided by commencing writing the source image pixel data in a particular portion of the line buffer after the reading of the stored pixel data has commenced in that same portion of the line buffer.

26. (New) A display controller as recited in claim 12 further comprising:

an incomplete interpolated scan line suppressor unit coupled to the interpolator unit arranged to suppress a last incomplete scan line after the horizontal interpolation based upon a truncated vertical scaling factor (VSF).

27. (New) A display controller as recited in claim 26, wherein the truncated VSF is derived by truncating a fractional portion of VSF where VSF is equal to the ratio Vsize.sub.--src/Vsize.sub.—dst.

28. (New) The display controller of claim 12, wherein said display controller is coupled to a display unit.

29. (New) A display controller as recited in claim 28, wherein said display unit comprises an fixed array monitor selected from a group comprising: an LCD monitor and a plasma monitor.

30. (New) A display controller as recited in claim 29, wherein display unit is part of a television system.

31. (New) A display controller as recited in claim 12, wherein the first resolution corresponds to VGA and wherein the second resolution corresponds to a resolution selected from a group comprising: XGA, SXGA, UXGA, WQSXGA, and QSXGA.

32. (New) A display controller as recited in claim 12, wherein the display controller is formed as a single integrated circuit.

33. (New) A memory efficient method for upscaling a source image at a first resolution to a destination image at a second resolution, comprising:

receiving source image pixel data in accordance with a first clock;

receiving the source image pixel data a line buffer having a size in accordance with the first resolution at a second clock;

storing the received source image pixel data in the line buffer;

reading selected stored image pixel data from the line buffer at the second clock; and

forming the destination image using the selected stored source image pixel data.

34. (New) A method as recited in claim 33, wherein the forming the destination image comprises:

converting a first resolution number of scan lines to a second resolution number of scan lines; and

converting each of the second resolution number of scan lines each having a first resolution scan line length to a second resolution scan line length.

35. (New) A method as recited in claim 34, wherein the converting the first resolution number of scan lines to the second resolution number of scan line is based upon using a current scan line and a previous scan line.

36. (New) A method as recited in claim 33, wherein the line buffer is a single port memory type line buffer or wherein the line buffer is a dual ported memory type line buffer.

37. (New) A method as recited in claim 36, wherein when the line buffer is the single port SDRAM, then the line buffer further comprises a first bank and a second bank each having a size in accordance with the first resolution scan line length.

38. (New) A method as recited in claim 37, wherein when pixel data corresponding to a source image scan line is received in the first bank, then pixel data corresponding to another source image scan line can be concurrently read from the second bank as many times as required.

39. (New) A method as recited in claim 36, wherein when said line buffer comprises the dual-ported memory, the data is read from a port that is different from a port that receives the source image pixel data.

40. (New) A method as recited in claim 33, further comprising:

locking the second clock to the first clock in a proportion.

41. (New) A method as recited in claim 40, wherein the proportion is equal to (Htotal.sub.-- src.times.Vtotal.sub.-- src)/(Htotal.sub.-- dst.times.Vtotal.sub.-- dst), wherein Htotal.sub.-- src and Htotal.sub.-- dst represent the total number of pixels in each source scan line and each destination scan line respectively, and Vtotal.sub.-- src and Vtotal.sub.-- dst represent the total number of lines in the source image and the destination image, respectively.

42. (New) A method as recited in claim 33, wherein the source image pixel data is received using an externally generated first clock.

43. (New) A method as recited in claim 33, wherein said source image has a source image aspect ratio and said destination image has a destination image aspect ratio that can be not equal to said source aspect ratio.

44. (New) A method as recited in claim 33, wherein when said source image is an analog source image then the first clock is provided to a sampling circuit coupled to the interface that samples the analog source image at a sampling frequency such that each scan line in said source image is sampled a number of times equal to a number of pixels in each scan line in the destination image.

45. (New) A method as recited in claim 33, further comprising:

commencing writing the source image pixel data in a particular portion of the line buffer after the reading of the stored pixel data has commenced in that same portion of the line buffer thereby avoiding an overrun condition in the line buffer.

46. (New) A method as recited in claim 34 further comprising:

suppressing a last incomplete scan line based upon a truncated vertical scaling factor (VSF).

47. (New) A method as recited in claim 46, wherein the truncated VSF is derived by truncating a fractional portion of VSF where VSF is equal to the ratio Vsize.sub.-- src/Vsize.sub.—dst.

48. (New) A method as recited in claim 33, wherein said display controller is coupled to a display unit.

49. (New) A method as recited in claim 48, wherein the display unit comprises an fixed array monitor selected from a group comprising: an LCD monitor and a plasma monitor.

50. (New) A method as recited in claim 49, wherein the display unit is part of a television system.

51. (New) A method as recited in claim 33, wherein the first resolution corresponds to VGA and wherein the second resolution corresponds to a resolution selected from a group comprising: XGA, SXGA, UXGA, WQSXGA, and QSXGA.

52. (New) A method as recited in claim 33, wherein the display controller is formed as a single integrated circuit.

53. (New) Computer program product for memory efficient upscaling of a source image at a first resolution to a destination image at a second resolution, comprising:

computer code for receiving source image pixel data in accordance with a first clock;

computer code for receiving the source image pixel data a line buffer having a size in accordance with the first resolution at a second clock;

computer code for storing the received source image pixel data in the line buffer;

computer code for reading selected stored image pixel data from the line buffer at the second clock;

computer code for forming the destination image using the selected stored source image pixel data; and

computer readable medium for storing the computer code.

54. (New) Computer program product as recited in claim 53, wherein the forming the destination image comprises:

computer code for converting a first resolution number of scan lines to a second resolution number of scan lines; and

computer code for converting each of the second resolution number of scan lines each having a first resolution scan line length to a second resolution scan line length.

55. (New) Computer program product as recited in claim 54, wherein the converting the first resolution number of scan lines to the second resolution number of scan line is based upon using a current scan line and a previous scan line.

56. (New) Computer program product as recited in claim 53, wherein the line buffer is a single port memory type line buffer or wherein the line buffer is a dual ported memory type line buffer.

57. (New) Computer program product as recited in claim 56, wherein when the line buffer is the single port SDRAM, then the line buffer further comprises a first bank and a second bank each having a size in accordance with the first resolution scan line length.

58. (New) Computer program product as recited in claim 57, wherein when pixel data corresponding to a source image scan line is received in the first bank, then pixel data corresponding to another source image scan line can be concurrently read from the second bank as many times as required.

59. (New) Computer program product as recited in claim 56, wherein when said line buffer comprises the dual-ported memory, the data is read from a port that is different from a port that receives the source image pixel data.

60. (New) Computer program product as recited in claim 53, further comprising:

computer code for locking the second clock to the first clock in a proportion.

61. (New) Computer program product as recited in claim 60, wherein the proportion is equal to (Htotal.sub.-- src.times.Vtotal.sub.-- src)/(Htotal.sub.-- dst.times.Vtotal.sub.-- dst), wherein Htotal.sub.-- src and Htotal.sub.-- dst represent the total number of pixels in each source scan line and each destination scan line respectively, and Vtotal.sub.-- src and Vtotal.sub.-- dst represent the total number of lines in the source image and the destination image, respectively.

62. (New) Computer program product as recited in claim 53, wherein the source image pixel data is received using an externally generated first clock.

63. (New) Computer program product as recited in claim 53, wherein said source image has a source image aspect ratio and said destination image has a destination image aspect ratio that can be not equal to said source aspect ratio.

64. (New) Computer program product as recited in claim 53, wherein when said source image is an analog source image then the first clock is provided to a sampling circuit coupled to the interface that samples the analog source image at a sampling frequency such that each scan line in said source image is sampled a number of times equal to a number of pixels in each scan line in the destination image.

65. (New) Computer program product as recited in claim 53, further comprising:

computer code for commencing writing the source image pixel data in a particular portion of the line buffer after the reading of the stored pixel data has commenced in that same portion of the line buffer thereby avoiding an overrun condition in the line buffer.

66. (New) Computer program product as recited in claim 54, further comprising:

computer code for suppressing a last incomplete scan line based upon a truncated vertical scaling factor (VSF).

67. (New) Computer program product as recited in claim 66, wherein the truncated VSF is derived by truncating a fractional portion of VSF where VSF is equal to the ratio Vsize.sub.--src/Vsize.sub.—dst.

68. (New) Computer program product as recited in claim 53, wherein said display controller is coupled to a display unit.

69. (New) Computer program product as recited in claim 68, wherein the display unit comprises an fixed array monitor selected from a group comprising: an LCD monitor and a plasma monitor.

70. (New) Computer program product as recited in claim 69, wherein the display unit is part of a television system.

71. (New) Computer program product as recited in claim 53, wherein the first resolution corresponds to VGA and wherein the second resolution corresponds to a resolution selected from a group comprising: XGA, SXGA, UXGA, WQSXGA, and QSXGA.

72. (New) Computer program product as recited in claim 53, wherein the display controller is formed as a single integrated circuit.

73. (Currently Amended) A memory efficient upscaler for upscaling a source image to a destination image having more pixels than the source image, comprising:

a source interface arranged to receive source image pixels;

a line buffer arranged to receive and store pixels from the source interface; and

a display interface arranged to receive pixels from the line buffer and provide the destination image without using a frame buffer.