AMENDMENT TO THE SPECIFICATION

Please replace the title with:

[CIRCUIT AND METHOD FOR GENERATING PIXEL DATA ELEMENTS FROM ANALOG IMAGE DATA AND ASSOCIATED SYNCHRONIZATION SIGNALS]
METHOD AND SYSTEM FOR DISPLAYING AN ANALOG IMAGE BY A DIGITAL DISPLAY DEVICE

Please add the following to page 1:

CROSS REFERENCE TO RELATED APPLICATIONS

More than one reissue application has been filed for the reissue of Patent No. 6,320,574. The reissue applications are application numbers 10/720,001, 11/408,669 (the present application) and 11/408,528, the latter two of which are divisional reissues of Patent No. 6,320,574.

ABSTRACT

[A clock recovery circuit in a digital display unit for recovering a time reference signal associated with analog display data. The clock recovery circuit includes a phase-locked loop (PLL) implemented in digital domain and an analog filter to eliminate any undesirable frequencies from the output signal of the PLL. The PLL includes independent control loops to track long term frequency drifts of the time reference signal and the transient phase differences respectively. By providing such independent control loops, the generated clock can be better synchronized with the time reference signal.]

Scaling a source image formed of a number of source image elements to provide a destination image formed of a number of destination image elements using a line buffer and no frame buffer.