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(54) Apparatus for driving liquid crystal display panel for different size images

Vorrichtung zur Steuerung einer Flüssigkristallanzeigetafel für verschiedene Bildgrössen

Dispositif de commande d'un panneau d'affichage à cristaux liquides pour différentes tailles d'image

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- **PATENT ABSTRACTS OF JAPAN vol. 015, no. 075 (P-1169) 21 February 1991 & JP-A-02 294 688 (SEIKO EPSON) 5 December 1990**
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- **PATENT ABSTRACTS OF JAPAN vol. 015, no. 360 (P-1250) 11 September 1991 & JP-A-03 139 622 (MATSUSHITA ELECTRIC) 13 June 1991**
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Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a liquid crystal display (LCD) system, and more particularly, to an apparatus for driving a multi-synchronization type LCD panel for different size images.

Description of the Related Art

There has been known a multi-synchronization type deflecting apparatus for a cathode-ray tube (CRT) panel which can properly display images having different numbers of scan lines at a center portion of the panel. On the other hand, since LCD panels are thinner in size and lower in power consumption with a lower power supply voltage as compared with CRT panels, the LCD panels have recently been applied to personal computers, word processors, color telereceivers, and the like. However, the multi-synchronization type deflecting system of the CRT panels cannot be applied to the multi-synchronization type driving system of the LCD panels, due to the difference in driving (deflecting) methods therebetween.

In a prior art apparatus for driving an LCD panel having M signal lines, N scan lines and M × N liquid crystal cells connected to the signal lines and the scan lines, the operation of a signal line driving circuit for sequentially driving the signal lines is started by a horizontal start timing signal which is obtained by delaying a horizontal synchronization signal with a constant time period. Similarly, the operation of a scan line driving circuit for sequentially driving the scan lines is started by a vertical start timing signal which is obtained by delaying a vertical synchronization signal with a constant time period. As a result, an image having a size different from M × N dots is ill-balanced at an upper portion or a left portion of the LCD panel. This will be explained later in detail.

Patent Abstracts of Japan, vol. 013, No. 495 (P-956), Nov. 1989, discloses an apparatus to make a display at an optional position even with optional display capacity without increasing a display transfer speed by providing a column or row driving means with an offset means which can set a display start position optionally. When an offset means is provided with the column driving means, input display data which are transferred are fetched in order from the position corresponding to the set value of the initial-stage latch in the column driving means and column electrodes are driven according to the fetched data. Further, when an offset means is provided to a row driving means, row electrodes are driven in order from the electrode corresponding to the set value. When the capacity of the display data is smaller than the display capacity of the dot matrix display device, the display data is displayed on the center of the display panel of the dot matrix display device by selecting the set value properly. Thereby the data can be displayed at an optional position without using the transfer speed of the display data.

Patent Abstracts of Japan, vol. 015, No. 360 (P-1250), Sept. 1991, discloses a means for changing the position of an image displayed on a liquid chrystal panel of an image display device which projects the image displayed on plural liquid chrystal panels to a screen in the horizontal and vertical directions on a display panel. For that purpose a gate timing signal and a source timing signal are inputted in a gate driver and a source driver by changing the positions of the signals by means of a gate timing signal movement and a source timing signal movement circuit. Since scanning start timing in the vertical and horizontal directions it moves in the liquid crystal panel, the displayed image can be moved in the vertical and horizontal directions. Thus, the convergence adjustment of the projection type image display device is facilitated and the adjusting stage is simplified.

WO-A-90/12367 discloses a method for controlling the vertical centering of sequential frames of a raster image on a raster imaging surface. It involves detecting the vertical location of the last line of the raster image in the frame preceding the frame to be controlled; and controlling the beginning of the raster image of the controlled frame on the basis of the location of the detected last line. The method further provides for automatic centering of the image on the imaging surface and for compression of the raster image.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a multi-synchronization type driving apparatus for an LCD panel which can display an image having different size images at a center portion thereof.

This object is met by an apparatus as defined in claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description as set forth below, in comparison with the prior art, with reference to the accompanying drawings, wherein:

Fig. 1 is a block circuit diagram illustrating a prior art apparatus for driving an LCD panel;

Fig. 2 is a detailed block circuit diagram of the signal line driving circuit of Fig. 1;

Fig. 3 is a detailed circuit diagram of the horizontal timing generating circuit of Fig. 1;

Figs. 4A through 4F are timing diagrams showing the operation of the circuits of Figs. 2 and 3;

Figs. 5A and 5B are timing diagrams for explaining an image signal of one horizontal line.

Fig. 6 is a detailed block circuit diagram of the scan

line driving circuit of Fig. 1;
Fig. 7 is a detailed circuit diagram of the vertical timing generating circuit of Fig. 1;
Figs. 8A through 8F are timing diagrams showing the operation of the circuits of Figs. 6 and 7;
Figs. 9A through 9D are timing diagrams for explaining a video signal of one frame in the prior art;
Fig. 9E is a diagram showing an image displayed on the LCD panel of Fig. 1;
Fig. 10 is a detailed circuit diagram of the timing generating circuit of Fig. 1;
Fig. 11 is a block circuit diagram illustrating a first embodiment of the apparatus for driving an LCD panel according to the present invention;
Fig. 12 is a detailed block circuit diagram of the image size determining circuit of Fig. 11;
Fig. 13 is a diagram showing the content of the look-up table of Fig. 12;
Fig. 14A through 14D are timing diagrams for explaining a video signal of one frame according to the present invention;
Fig. 14E is a diagram showing an image displayed on the LCD panel of Fig. 11;
Fig. 15 is a block circuit diagram illustrating a second embodiment of the apparatus for driving an LCD panel according to the present invention;
Fig. 16 is a detailed circuit diagram of the image size determining circuit of Fig. 15;
Fig. 17 is a diagram showing the content of the look-up table of Fig. 15;
Fig. 18 is a detailed circuit diagram of the signal processing circuit of Fig. 15;
Fig. 19 is a circuit diagram of the data compression circuit of Fig. 18;
Figs. 20A, 20B and 20C are timing diagrams showing the operation of the circuit of Fig. 19;
Fig. 21 is a circuit diagram of the layer expansion circuit of Fig. 18; and
Figs. 22A through 22H are timing diagrams showing the operation of the circuit of Fig. 21.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the description of the preferred embodiments, a prior art apparatus for driving an LCD panel will be explained with reference to Figs. 1, 2, 3, 4A through 4F, 5A, 5B, 6, 7, 8A through 8F, and 9A through 9E.

In Fig. 1, which illustrates a prior art apparatus for driving an LCD panel, reference numeral 1 designates an LCD panel having M × N dots where M=1280 and N=1024. That is, the LCD panel 1 has signal lines SG_i (i=0, 1,···, 1279) driven by signal line driving circuits 2-1 and 2-2, 1024 scan lines SL_j (j=0, 1,···, 1023) driven by a scan line driving circuit 3, and pixels each connected to one of the scan lines and one of the signal lines. Also, each of the pixels is formed by a thin film transistor (TFT) Q_{ij} and a liquid crystal cell C_{ij}.

An analog/digital (A/D) converter 4 receives color signals R, G and B of a video signal and performs an A/D conversion thereupon by using a clock signal ACK. The digital output of the A/D converter 4 is supplied to a signal processing circuit 5 clocked by a clock signal TCK. The signal processing circuit 5 includes a layer expansion circuit which will be later explained. Two outputs DA and DB of the signal processing circuit 5 are supplied to two D/A converters 6-1 and 6-2, respectively, clocked by a clock signal DCK, and the converters are also connected to the signal line driving circuits 2-1 and 2-2, respectively.

A timing generating circuit 7, which includes a phase-locked loop (PLL) circuit, receives a horizontal synchronization signal HSYNC to thereby generate various clock signals HCK, VCK, CK in addition to the clock signals ACK, TCK and DCK. In this case, the clock signal HCK is used for sequentially driving the signal line driving circuits 2-1 and 2-2, and the clock signal VCK is used for sequentially driving the scan line driving circuit 3.

A horizontal timing generating circuit 8 generates a horizontal start timing signal HS and transmits it to the signal line driving circuits 2-1 and 2-2, to thereby start the operation thereof. Also, a vertical timing generating circuit 9 generates a vertical start timing signal VS and transmits it to the scan line driving circuit 3, to thereby start the operation thereof.

In Fig. 2, which is a detailed block circuit diagram of the signal line driving circuit 2-1 (2-2) of Fig. 1, shift registers (D flip-flops) 21-0, 21-1, ···, 21-639 are serially-connected. The horizontal start timing signal HS is shifted through the shift registers 21-0, 21-1, ···, 21-639 by the clock signal HCK. The outputs of the shift registers 21-0, 21-1,···, 21-639 control switching circuits 22-0, 22-1, ···, 22-639, respectively, which receive the data signal of the D/A converter 6-1 (6-2). Thus, the switching circuits 22-0, 22-1,···, 22-639 sequentially drive the signal lines SG_0, SG_1,···, SG_{639}, respectively, in accordance with the video signal.

In Fig. 3, which is a detailed circuit diagram of the horizontal start timing circuit 8 of Fig. 1, this circuit 8 includes a counter 801 which counts the clock signal CK and is cleared by the horizontal synchronization signal HSYNC. Also, an exclusive OR circuit 802 and an inverter 803 compare the content of the counter 801 with a constant value HSET. That is, only when the content of the counter 801 coincides with the constant value HSET, is the output of the inverter 803, i.e., the horizontal start timing signal HS, "1".

The operation of the horizontal start timing circuit 8 and the signal line driving circuit 2-1 (2-2) will be explained with reference to Figs. 4A through 4F. That is, the horizontal start timing generating circuit 8 counts the clock signal CK after the horizontal synchronization signal HSYNC is made "0" (low) as shown in Fig. 4A. As a result, after the constant time period HSET has passed,

the horizontal timing generating circuit 8 generates the horizontal start timing signal HS as shown in Fig. 4B. Therefore, the horizontal start timing signal HS is supplied to the first stage of the shift registers, i.e., the shift register 21-0, and the horizontal start timing signal HS is shifted through the shift registers 21-0, 21-1,···, 21-639 by the clock signal HCK as shown in Fig. 4C. As a result, the signal lines SG_0, SG_1, ···, SG_{639} are sequentially driven by the AND logic between the output signals of the shift registers 21-0, 21-1,···, 21-639 and the data of the video signal as shown in Figs. 4D, 4E and 4F.

Thus, in the prior art, the relationship between a horizontal line of the video signal as shown in Fig. 5A and the horizontal start timing signal HS as shown in Fig. 5B is constant.

In Fig. 6, which is a detailed block circuit diagram of the scan line driving circuit 3 of Fig. 1, shift registers (D flip-flops) 31-0, 31-1, ···, 31-1023 are serially-connected for driving the scan lines SL_0, SL_1, ···, SL_{1023}, respectively. The vertical start timing signal VS is shifted through the shift registers 31-0, 31-1,···, 31-1023 by the clock signal VCK.

In Fig. 7, which is a detailed circuit diagram of the vertical start timing circuit 9 of Fig. 1, this circuit 9 includes a counter 901 which counts the horizontal synchronization signal HSYNC and is cleared by a vertical synchronization signal VSYNC. Also, an exclusive OR circuit 902 and an inverter 903 compare the content of the counter 901 with a constant value VSET. That is, only when the content of the counter 901 coincides with the constant value VSET, is the output of the inverter 903, i.e., the vertical start timing signal VS, "1".

The operation of the vertical start timing circuit 9 and the scan line driving circuit 3 will be explained with reference to Figs. 8A through 8F. The vertical start timing generating circuit 9 counts the horizontal start signal HS after the vertical synchronization signal VSYNC is made "0" (low) as shown in Fig. 8A. As a result, after the constant time period VSET has passed, the vertical timing generating circuit 9 generates the vertical start timing signal VS as shown in Fig. 8B. Therefore, the vertical start timing signal VS is supplied to the first stage of the shift registers, i.e., the shift register 31-0, and the vertical start timing signal VS is shifted through the shift registers 31-0, 31-1,···, 31-1023 by the clock signal VCK as shown in Fig. 8C. As a result, the scan lines SL_0, SL_1,···, SL_{1023} are sequentially driven by the output signals of the shift registers 31-0, 31-1, ···, 31-1023 as shown in Figs. 8D, 8E and 8F.

Thus, in the prior art, even if an image having 1152 × 900 dots as shown in Fig. 9B, that is smaller than an image having 1280 × 1024 dots as shown in Fig. 9A, is displayed on the LCD panel 1 having 1280 × 1024 dots, the timing of the horizontal start timing signal HS is constant as shown in Fig. 9C, and the timing of the vertical start timing signal VS is constant as shown in Fig. 9D. As a result, as shown in Fig. 9E, a 1152 × 900 dot image is ill-balanced at an upper-left portion of the LCD panel 1.

In Fig. 10, which is a detailed circuit diagram of the timing generating circuit 7 of Fig. 1, this circuit 7 includes a PLL circuit formed by a phase comparator 701, a low-pass filter 702, a voltage controlled oscillator 703, and a 1/n frequency divider 704. That is, the phase comparator 701 compares the phase of the horizontal synchronization signal HSYNC with that of the output signal of the 1/n frequency divider 704. The low-pass filter 702 includes a capacitor which is charged or discharged by the output of the phase comparator 701. The voltage controlled oscillator 703 generates the clock signal CK whose frequency corresponds to the output of the low-pass filter 702. Thus, the frequency of the clock signal CK is maintained at a definite value determined by the horizontal synchronization signal HSYNC. Note the value n of the frequency divider 704 corresponds to the sampling number of the clock signal CK for one horizontal line of the video signal.

The timing generating circuit 7 also includes a frequency divider circuit formed by a plurality of frequency dividers which generate the clock signals ACK, TCK, DCK, HCK and VCK.

In Fig. 11, which illustrates a first embodiment of the present invention, the value HSET of the horizontal timing circuit 8 and the value VSET of the vertical timing circuit 9 are variable, and the values HSET and VSET are changed by an image size determining circuit 10 which calculates an image size of one frame of the video signal in accordance with the horizontal synchronization signal HSYNC and the vertical synchronization signal VSYNC. The image size determining circuit 10 is formed by a circuit as illustrated in Fig. 12.

In Fig. 12, reference numeral 1001 designates a frequency-to-voltage converter for receiving the horizontal synchronization signal HSYNC to generate a voltage V_H in response to the frequency of the horizontal synchronization signal HSYNC. Also, reference numeral 1002 designates a frequency-to-voltage converter for receiving the vertical synchronization signal VSYNC to generate a voltage V_v in response to the frequency of the vertical synchronization signal VSYNC. The voltages V_H and V_v are converted by analog-to-digital converters 1003 and 1004 into digital values f_H and f_v, respectively. Then, the digital values f_H and f_v are supplied to a look-up table 1005, which in turn generates the values HSET and VSET. The look-up table 1005 is formed by a random access memory (RAM) or a read-only memory (ROM) for storing the values HSET and VSET as shown in Fig. 13.

Thus, according to the first embodiment, even if an image having 1152 × 900 dots as shown in Fig. 14B, that is smaller than an image having 1280 × 1024 dots as shown in Fig. 14A, is displayed on the LCD panel 1 having 1280 × 1024 dots, the timing of the horizontal start timing signal HS is variable as shown in Fig. 14C, and the timing of the vertical start timing signal VS is variable as shown in Fig. 14D. As a result, as shown in

Fig. 14E, a 1152 × 900 dot image is balanced at a center portion of the LCD panel 1.

In Fig. 15, which illustrates a second embodiment of the present invention, the image size determining circuit 10 of Fig. 11 is modified to form an image size determining circuit 10' which generates a compression control signal CONT in addition to the signals HSET and VSET. Also, the signal processing circuit 5 of Fig. 11 is modified to from a signal processing circuit 5' which can perform data compression upon the video signal. That is, when a video signal of an image larger than an image having 1280 × 1024 dots is supplied to the signal processing circuit 5', data compression is performed upon the video signal in accordance with the compression control signal CONT including compression ratio information.

In Fig. 16, which is a detailed circuit diagram of the image size determining circuit 10' of Fig. 15, the look-up memory 1005 of Fig. 12 is modified to from a look-up memory 1005' which generates the compression control signal COUT in addition to the signals HSET and VSET. The look-up memory 1005' is formed by a RAM or ROM for storing the values HSET, VSET and CONT as shown in Fig. 17.

In Fig. 18, which is a detailed circuit diagram of the data processing circuit 5' of Fig. 15, this circuit 5' includes switching circuits 501 and 502, a data compression circuit 503, and a layer expansion circuit 504 which is used for distributing the video signal to the two signal line driving circuits 2-1 and 2-2. For example, if a first bit of the compression control signal CONT is "0", the switching circuits 501 and 502 are positioned on their upper sides as illustrated, so that data from the A/D converter 4 is supplied via the switching circuits 501 and 502 directly to the layer expansion circuit 504. Conversely, if the first bit of the compression control signal CONT is "1", the switching circuits 501 and 502 are positioned on their lower sides, so that data from the A/D converter 4 is supplied via the switching circuit 501 to the data compression circuit 503. Therefore, in the data compression circuit 503, data compression is performed upon the video signal using the compression ratio included in the compression control signal COUT in synchronization with the clock signal TCK. Then, the data compressed by the data compression circuit 503 is supplied via the switching circuit 502 to the layer expansion circuit 504.

In Fig. 19, which is a detailed circuit diagram of the data compression circuit 503 of Fig. 18, this circuit 503 includes a frame memory 5031 for writing data from the switching circuit 501 and outputting data to the switching circuit 502. A write operation is carried out upon the frame memory 5031 by a write address counter 5032 whose write address WA is sequentially counted up by receiving the clock signal TCK. On the other hand, a read operation is carried out upon the frame memory 5031 by a read address counter 5033 and an address transforming look-up table 5034. In this case, a read address RA generated by the read address counter 5033 is sequentially counted up in synchronization with the clock signal TCK as shown in Figs. 20A and 20B. However, as shown in Fig. 20C, a read address RA' generated from the address transforming look-up table 5034 is shifted as compared with the read address RA in accordance with the compression ratio information included in the compression control signal CONT. Note that the compression ratio information is composed of a traverse ratio and/or a longitudinal ratio.

Thus, even when a video signal of an image having more dots than 1280 in the traverse direction or more dots than 1024 in the longitudinal direction is input, the entire video signal is so compressed that it can be displayed on the LCD panel 1.

In Fig. 21, which is a detailed circuit diagram of the layer expansion circuit 504 of Fig. 18, this circuit 504 includes D flip-flops 5041, 5042, 5043, 5044, and 5045, an inverter 5046, and a T flip-flop 5047. That is, the D flip-flops 5041, 5042 and 5043 are clocked by the clock signal DCK or its inverted signal having a period T as shown in Fig. 22A, while the D flip-flops 5044 and 5045 are clocked by a clock signal 2DCK having a period 2T as shown in Fig. 22B. Therefore, the outputs S1, S2 and S3 of the flip-flops 5041, 5042 and 5043 are obtained by delaying the output D of the switching circuit 502, as shown in Figs. 22C, 22D, 22E and 22F. On the other hand, since the flip-flops 5044 and 5045 are clocked by the clock signal 2DCK, the outputs DA and DB of the flip-flops 5044 and 5045 have the period 2T, so that the outputs DA and DB of the flip-flops 5044 and 5045 are as shown in Figs. 22G and 22H.

In the above-mentioned embodiments, although the horizontal synchronization signal HSYNC and the vertical synchronization signal VSYNC are supplied independently of the color signals R, G and B, if the horizontal synchronization signal HSYNC and the vertical synchronization signal VSYNC are included in the color signal G, these synchronization signals can be derived from the color signal G.

As explained hereinbefore, according to the present invention, even an image having a different size than an LCD panel can be displayed at a center portion of the LCD panel.

Claims

1. An apparatus for driving a liquid crystal display panel (1) having M signal lines (SG_0, SG_1,···), N scan lines (SL_0, SL_1,···), and M × N liquid crystal cells (C_{ij}) each connected to one of said signal lines and one of said scan lines, comprising:

   a signal line driving circuit (2-1, 2-2), connected to said signal lines, for sequentially driving said signal lines in response to a horizontal start timing signal (HS);

a scan line driving circuit (3), connected to said scan lines, for sequentially driving said scan lines in response to a vertical start timing signal (VS);
a horizontal timing generating circuit (8), connected to said signal line driving circuit, for receiving a horizontal synchronization signal (HSYNC) and delaying it with a first time period (HSET), to generate the horizontal start timing signal and transmit it to said signal line driving circuit;
a vertical timing generating circuit (9), connected to said scan line driving circuit, for receiving a vertical synchronization signal (VSYNC) and delaying it with a second time period (VSET), to generate the vertical start timing signal and transmit it to said scan line driving circuit; and
an image size determining circuit (10), connected to said horizontal timing circuit and said vertical timing circuit, for receiving the horizontal synchronization signal and the vertical synchronization signal, to calculate the first time period and the second time period in accordance with the size of the frame of a video signal and to transmit them to said horizontal timing generating circuit and said vertical timing generating circuit, respectively,

said image size determining circuit comprising:

means (1001, 1003) for calculating a horizontal frequency (f_H) in accordance with a horizontal synchronization signal (HSYNC);
means (1002, 1004) for calculating a vertical frequency (f_V) in accordance with a vertial synchronization signal (VSYNC);
means, connected to said horizontal frequency calculating means and said vertical frequency calculating means, for generating the horizontal start timing signal and the vertical start timing signal in accordance with the horizontal frequency and the vertical frequency,

said horizontal frequency calculating means comprising:

a frequency-to-voltage converter (1001) for receiving the horizontal synchronization signal; and
an analog-to-digital converter (1003), connected to said frequency-to-voltage converter,

said vertical frequency calculating means comprising:

a frequency-to-voltage converter (1002) for receiving the vertical synchronization signal; and
an analog-to-digital converter (1004) connected to said frequency-to-voltage converter, and
wherein said horizontal start timing signal/vertical start timing signal generating means comprises a look-up table (1005).

2. An apparatus as set forth in claim 1, wherein said image size determining circuit generates a compression control signal (CONT) including a compression ratio in accordance with the horizontal synchronization signal and the vertical synchronization signal,
said apparatus further comprising:

a data compression circuit (503) for receiving a video signal;
switching means (501, 502), connected to said image size determining circuit and said data compression circuit, for supplying the video signal to said data compression circuit in accordance with the compression control signal.

3. An apparatus as set forth in claim 2, wherein said data compression circuit comprises:

a frame memory (5031) for storing the video signal;
a write address counter (5032), connected to said frame memory, for generating a sequential write address (WA) and transmitting it to said frame memory, to thereby perform a write operation thereupon;
a read address counter (5033) for generating a sequential read address (RA);
an address transforming circuit (5034), connected to said read address counter, said frame memory, and said image size determining circuit, for transforming the sequential read address into a read address (RA') in accordance with the compression ratio included in the compression control signal and transmitting the read address to said frame memory, to thereby perform a read operation thereupon.

4. An apparatus as set forth in claim 1, wherein said horizontal timing generating circuit comprises:

a counter (801) for counting a clock signal (CK), said counter being cleared by the horizontal synchronization signal; and
a coincidence circuit (802, 803), connected to said counter and said image size determining circuit, for determining whether or not the content of said counter coincides with the first time period, to thereby generate the horizontal start timing signal when the content of said counter coincides with the first time period.

5. An apparatus as set forth in claim 1, wherein said

vertical timing generating circuit comprises:

a counter (901) for counting the horizontal synchronization signal, said counter being cleared by the vertical synchronization signal; and
a coincidence circuit (902, 903), connected to said counter and said image size determining circuit, for determining whether or not the content of said counter coincides with the second time period, to thereby generate the vertical start timing signal when the content of said counter coincides with the second time period.

Patentansprüche

1. Vorrichtung zur Steuerung einer Flüssigkristallanzeigetafel (1), die M Signalleitungen (SG_0, SG_1 ...), N Abtastleitungen (SL_0, SL_1 ...) und M x N Flüssigkristallzellen (C_{ij}) aufweist, die jeweils mit einer Signalleitung und einer Abtastleitung verbunden sind, und die folgendes aufweist:

eine Signalleitungs-Steuerschaltung (2-1, 2-2), die mit den Signalleitungen verbunden ist, zur sequentiellen Steuerung der Signalleitungen in Reaktion auf ein Horizontal-Start-Zeitsteuerungssignal (HS);
eine Abtastleitungs-Steuerschaltung (3), die mit den Abtastleitungen verbunden ist, zur sequentiellen Steuerung der Abtastleitungen in Reaktion auf ein Vertikal-Start-Zeitsteuerungssignal (VS);
eine Horizontal-Zeitsteuerungs-Erzeugungsschaltung (8), die mit der Signalleitungs-Steuerschaltung verbunden ist, zum Empfangen eines Horizontal-Synchronisationssignals (HSYNC) und zum Verzogern desselben um eine erste Zeitspanne (HSET), um das Horizontal-Start-Zeitsteuerungssignal zu erzeugen und es zur Signalleitungs-Steuerschaltung zu übertragen;
eine Vertikal-Zeitsteuerungs-Erzeugungsschaltung (9), die mit der Abtastleitungs-Steuerschaltung verbunden ist, zum Empfangen eines Vertikal-Synchronisationssignals (VSYNC) und zum Verzögern desselben um eine zweite Zeitspanne (VSET), um das Vertikal-Start-Zeitsteuerungssignal zu erzeugen und es zur Abtastleitungs-Steuerschaltung zu übertragen; und
eine Bildgröße-Ermittlungsschaltung (10), die mit der Horizontal-Zeitsteuerungsschaltung und der Vertikal-Zeitsteuerungsschaltung verbunden ist, zum Empfangen des Horizontal-Synchronisationssignals und des Vertikal-Synchronisationssignals, um die erste Zeitspanne und die zweite Zeitspanne gemäß der Größe des Frames eines Videosignals zu berechnen und sie zur Horizontal-Zeitsteuerungs-Erzeugungsschaltung bzw. zur Vertikal-Zeitsteuerungs-Erzeugungsschaltung zu übertragen,

wobei die Bildgröße-Ermittlungsschaltung folgendes aufweist:

eine Einrichtung (1001, 1003) zum Berechnen einer Horizontalfrequenz (f_H) gemäß einem Horizontal-Synchronisationssignal (HSYNC);
eine Einrichtung (1002, 1004) zum Berechnen einer Vertikalfrequenz (f_V) gemäß einem Vertikal-Synchronisationssignal (VSYNC);
eine Einrichtung, die mit der Horizontalfrequenz-Berechnungseinrichtung und der Vertikalfrequenz-Berechnungseinrichtung verbunden ist, zum Erzeugen des Horizontal-Start-Zeitsteuerungssignals und des Vertikal-Start-Zeitsteuerungssignals gemäß der Horizontalfrequenz und der Vertikalfrequenz,

wobei die Horizontalfrequenz-Berechnungseinrichtung folgendes aufweist:

einen Frequenz-/Spannungs-Wandler (1001) zum Empfangen des Horizontal-Synchronisationssignals; und
einen Analog-/Digital-Wandler (1003), der mit dem Frequenz-/Spannungs-Wandler verbunden ist;

wobei die Vertikalfrequenz-Berechnungseinrichtung folgendes aufweist:

einen Frequenz-/Spannungs-Wandler (1002) zum Empfangen des Vertikal-Synchronisationssignals; und
einen Analog-/Digital-Wandler (1004), der mit dem Frequenz-/Spannungs-Wandler verbunden ist; und
wobei die Horizontal-Start-Zeitsteuerungssignal-/Vertikal-Start-Zeitsteuerungssignal-Erzeugungsschaltung eine Nachschlagetabelle (1005) umfaßt.

2. Vorrichtung nach Anspruch 1, bei der die Bildgröße-Ermittlungsschaltung ein Kompressions-Steuersignal (CONT) erzeugt, das ein Kompressionsverhältnis gemäß dem Horizontal-Synchronisationssignal und dem Vertikal-Synchronisationssignal aufweist,

wobei die Vorrichtung weiterhin folgendes aufweist:

eine Daten-Kompressionsschaltung (503) zum Empfangen eines Videosignals;
eine Schalteinrichtung (501, 502), die mit der Bildgröße-Ermittlungsschaltung und der Daten-Kompressionsschaltung verbunden ist,

zum Anlegen des Videosignals an die Daten-Kompressionsschaltung gemäß dem Kompressions-Steuersignal.

3. Vorrichtung nach Anspruch 2, bei der die Daten-Kompressionsschaltung folgendes umfaßt:

einen Frame-Speicher (5031) zum Speichern des Videosignals;

einen Schreibadressenzähler (5032), der mit dem Frame-Speicher verbunden ist, zum Erzeugen einer sequentiellen Schreibadresse (WA) und zum Übertragen derselben an den Frame-Speicher, um dadurch eine Schreiboperation an ihr durchzuführen;
einen Leseadressenzähler (5033) zum Erzeugen einer sequentiellen Leseadresse (RA);
eine Adressen-Umwandlungsschaltung (5034), die mit dem Leseadressenzähler, dem Frame-Speicher und der Bildgröße-Ermittlungsschaltung verbunden ist, zum Umwandeln der sequentiellen Leseadresse in eine Leseadresse (R') gemäß dem Kompressionsverhältnis, das im Kompressions-Steuersignal enthalten ist, und zum Übertragen der Leseadresse an den Frame-Speicher, um dadurch eine Leseoperation an ihr durchzuführen.

4. Vorrichtung nach Anspruch 1, bei der die Horizontal-Zeitsteuerungs-Erzeugungsschaltung folgendes umfaßt:

einen Zähler (801) zum Zählen eines Taktsignals (CK), wobei der Zähler vom Horizontal-Synchronisationssignal gelöscht wird; und
eine Koinzidenzschaltung (802, 803), die mit dem Zähler und der Bildgröße-Ermittlungsschaltung verbunden ist, um festzustellen, ob der Inhalt des Zählers mit der ersten Zeitspanne übereinstimmt oder nicht, um dadurch das Horizontal-Start-Zeitsteuerungssignal zu erzeugen, wenn der Inhalt des Zählers mit der ersten Zeitspanne übereinstimmt.

5. Vorrichtung nach Anspruch 1, bei der die Vertikal-Zeitsteuerungs-Erzeugungsschaltung folgendes umfaßt:

einen Zähler (901) zum Zählen des Horizontal-Synchronisationssignals, wobei der Zähler vom Vertikal-Synchronisationssignal gelöscht wird; und
eine Koinzidenzschaltung (902, 903), die mit dem Zähler und der Bildgröße-Ermittlungsschaltung verbunden ist, um festzustellen, ob der Inhalt des Zählers mit der zweiten Zeitspanne übereinstimmt oder nicht, um dadurch das Vertikal-Start-Zeitsteuerungssignal zu erzeugen, wenn der Inhalt des Zählers mit der zweiten Zeitspanne übereinstimmt.

Revendications

1. Dispositif de commande d'un panneau d'affichage à cristaux liquides (1) possédant M lignes de signal (SG_0, SG_1, ...), N lignes de balayage (SL_0, SL_1, ...), et M X N cellules à cristaux liquides (C_{ij}) chacune connectée à l'une desdites lignes de signal et à l'une desdites lignes de balayage, comprenant :

un circuit de commande de ligne de signal (2-1, 2-2), connecté auxdites lignes de signal, pour commander, de manière séquentielle, lesdites lignes de signal en réponse à un signal de temporisation horizontale de début (HS) ;
un circuit de commande de ligne de balayage (3), connecté auxdites lignes de balayage, pour commander, de manière séquentielle, lesdites lignes de balayage en réponse à un signal de temporisation verticale de début (VS) ;
un circuit de génération de temporisation horizontale (8), connecté audit circuit de commande de ligne de signal, pour recevoir un signal de synchronisation horizontale (HSYNC) et le retarder d'une première période de temps (HSET), pour générer le signal de temporisation horizontale de début et le transmettre audit circuit de commande de ligne de signal ;
un circuit de génération de temporisation verticale (9) connecté audit circuit de commande de ligne de balayage, pour recevoir un signal de synchronisation verticale (VSYNC) et le retarder d'une seconde période de temps (VSET), pour générer le signal de temporisation verticale de début et le transmettre audit circuit de commande de ligne de balayage ; et
un circuit de détermination de la taille d'image (10), connecté audit circuit de temporisation horizontale et audit circuit de temporisation verticale, pour recevoir le signal de synchronisation horizontale et le signal de synchronisation verticale, pour calculer la première période de temps et la seconde période de temps en fonction de la taille de la trame d'un signal vidéo et les transmettre audit circuit de génération de temporisation horizontale et audit circuit de génération de temporisation verticale, respectivement,

ledit circuit de détermination de la taille d'image comprenant :

des moyens (1001, 1003) pour calculer une fréquence horizontale (F_H) en fonction d'un signal de synchronisation horizontale (HSYNC) ;

des moyens (1002, 1004) pour calculer une fréquence verticale (F_V) en fonction d'un signal de synchronisation verticale (VSYNC) ;
des moyens, connectés auxdits moyens de calcul de fréquence horizontale et auxdits moyens de calcul de fréquence verticale, pour générer le signal de temporisation horizontale de début et le signal de temporisation verticale de début en fonction de la fréquence horizontale et la fréquence verticale,

lesdits moyens de calcul de la fréquence horizontale comprenant :

un convertisseur fréquence-tension (1001) pour recevoir le signal de synchronisation horizontale ; et
un convertisseur analogique-numérique (1003) connecté audit convertisseur fréquence-tension,

lesdits moyens de calcul de fréquence verticale comprenant :

un convertisseur fréquence-tension (1002) pour recevoir le signal de synchronisation verticale ; et
un convertisseur analogique-numérique (1004) connecté audit convertisseur fréquence-tension, et
dans lequel lesdits moyens de génération du signal de temporisation horizontale de début/ signal de temporisation verticale de début comprennent une table à consulter (1005).

2. Dispositif selon la revendication 1, dans lequel ledit circuit de détermination de la taille d'image génère un signal de commande de compression (CONT) comportant un rapport de compression qui est fonction du signal de synchronisation horizontale et du signal de synchronisation verticale,
ledit dispositif comprenant en outre :

un circuit de compression de données (503) pour recevoir un signal vidéo ;
un moyen de commutation (501, 502), connecté audit circuit de détermination de la taille d'image et audit circuit de compression de données, pour fournir le signal vidéo audit circuit de compression de données en fonction du signal de commande de compression.

3. Dispositif selon la revendication 2, dans lequel ledit circuit de compression de données comprend :

une mémoire de trame (5031) pour stocker le signal vidéo ;
un compteur d'adresse d'écriture (5032), connecté à ladite mémoire de trame, pour générer une adresse d'écriture séquentielle (WA) et la transmettre à ladite mémoire de trame, pour ainsi effectuer dans celle-ci une opération d'écriture ;
un compteur d'adresse de lecture (5033) pour générer une adresse de lecture séquentielle (RA) ;
un circuit de transformation d'adresse (5034), connecté audit compteur d'adresse de lecture, à ladite mémoire de trame, et audit circuit de détermination de la taille d'image, pour transformer l'adresse de lecture séquentielle en une adresse de lecture (RA') en fonction du rapport de compression compris dans le signal de commande de compression et transmettre l'adresse de lecture à ladite mémoire de trame, pour effectuer ainsi une opération de lecture sur celle-ci.

4. Dispositif selon la revendication 1, dans lequel ledit circuit de génération de temporisation horizontale comprend :

un compteur (801) pour compter un signal d'horloge (CK), ledit compteur étant remis à zéro par le signal de synchronisation horizontale ; et
un circuit de coïncidence (802, 803), connecté audit compteur et audit circuit de détermination de la taille d'image, pour déterminer si oui ou non le contenu dudit compteur coïncide avec la première période de temps, pour ainsi générer le signal de synchronisation horizontale de début lorsque le contenu dudit compteur coïncide avec la première période de temps.

5. Dispositif selon la revendication 1, dans lequel ledit circuit de génération de temporisation verticale comprend :

un compteur (901) pour compter le signal de synchronisation horizontale, ledit compteur étant remis à zéro par le signal de synchronisation verticale ; et
un circuit de coïncidence (902, 903), connecté audit compteur et audit circuit de détermination de la taille d'image, pour déterminer si oui ou non le contenu dudit compteur coïncide avec la seconde période de temps, pour ainsi générer le signal de synchronisation verticale de début lorsque le contenu dudit compteur coïncide avec la seconde période de temps.

Fig. 1

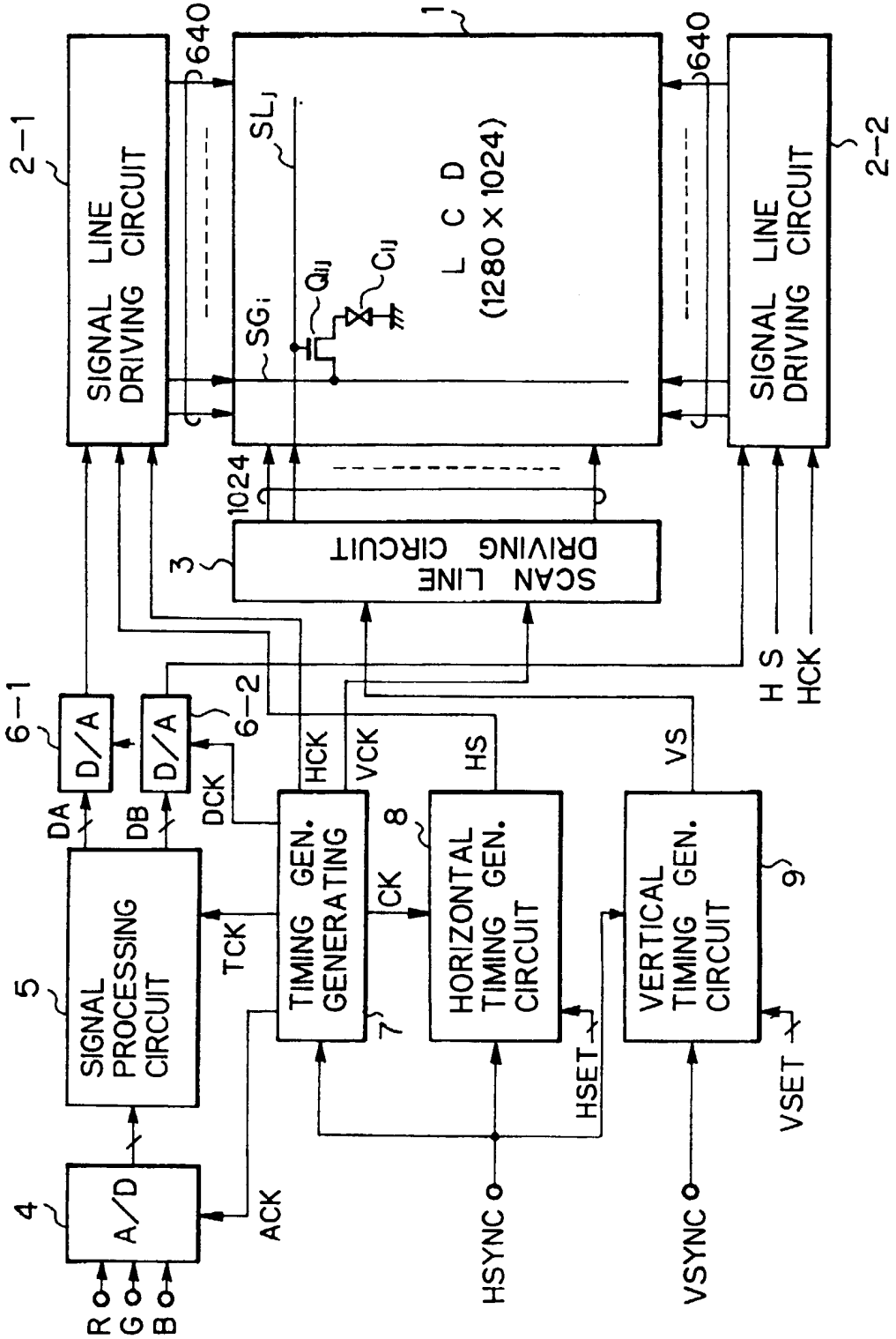

2-1
SIGNAL LINE DRIVING CIRCUIT
640
1
SL_J
SG_i
Q_ij
C_ij
L C D
(1280 X 1024)
640
2-2
SIGNAL LINE DRIVING CIRCUIT
1024
3
SCAN LINE DRIVING CIRCUIT
H S
HCK
6-1
D/A
6-2
D/A
DA
DB
DCK
HCK
VCK
HS
VS
5
SIGNAL PROCESSING CIRCUIT
TCK
TIMING GEN. GENERATING
7
CK
8
HORIZONTAL TIMING GEN. CIRCUIT
HSET
VERTICAL TIMING GEN. CIRCUIT
9
VSET
4
A/D
ACK
R
G
B
HSYNC
VSYNC

Fig. 2 PRIOR ART

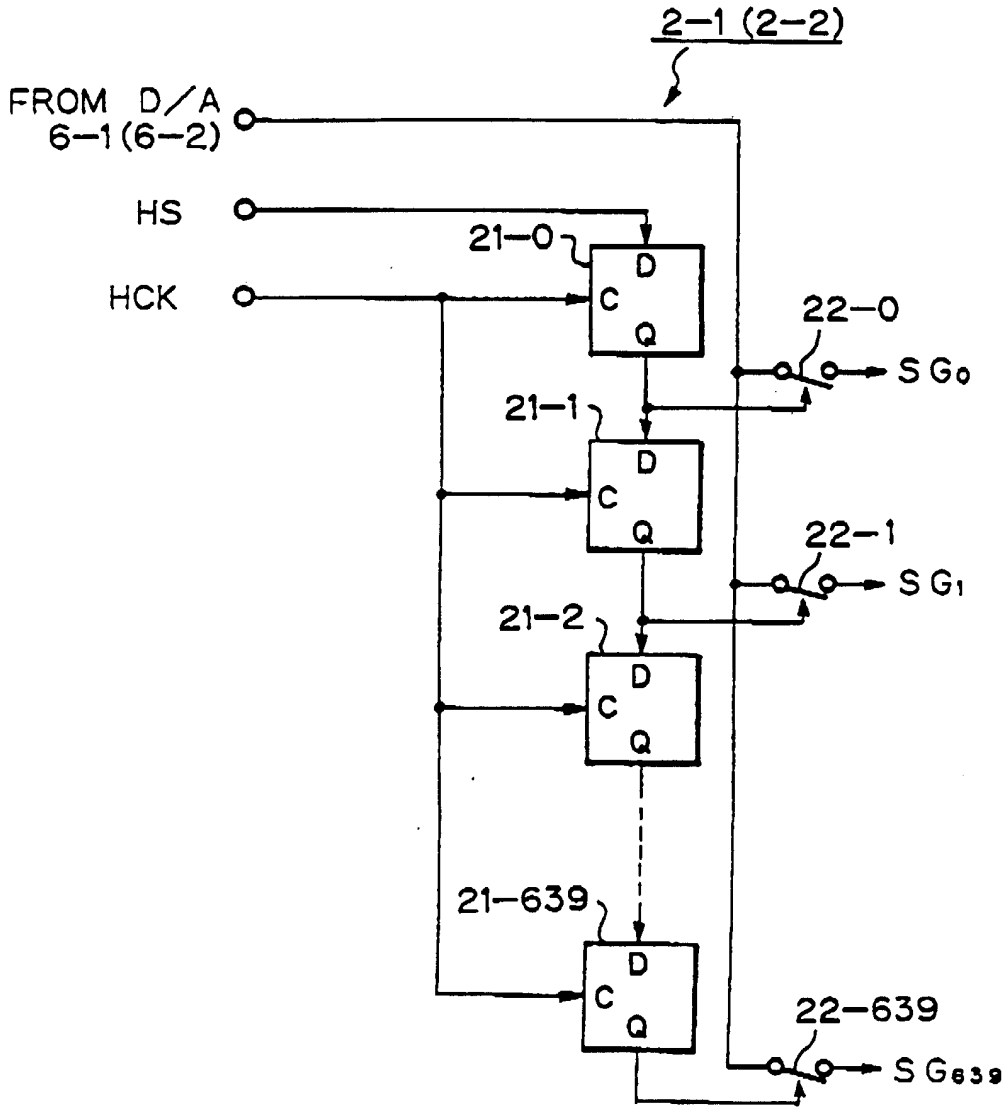
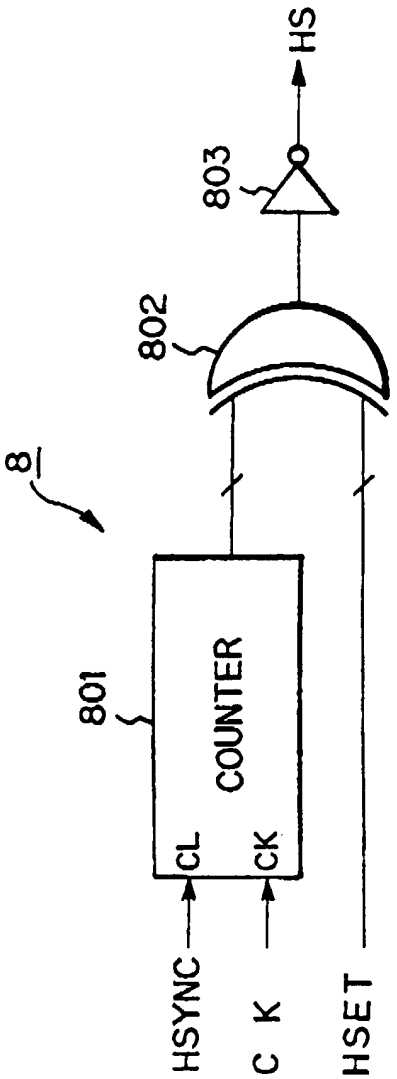


Fig. 3 PRIOR ART



PRIOR ART

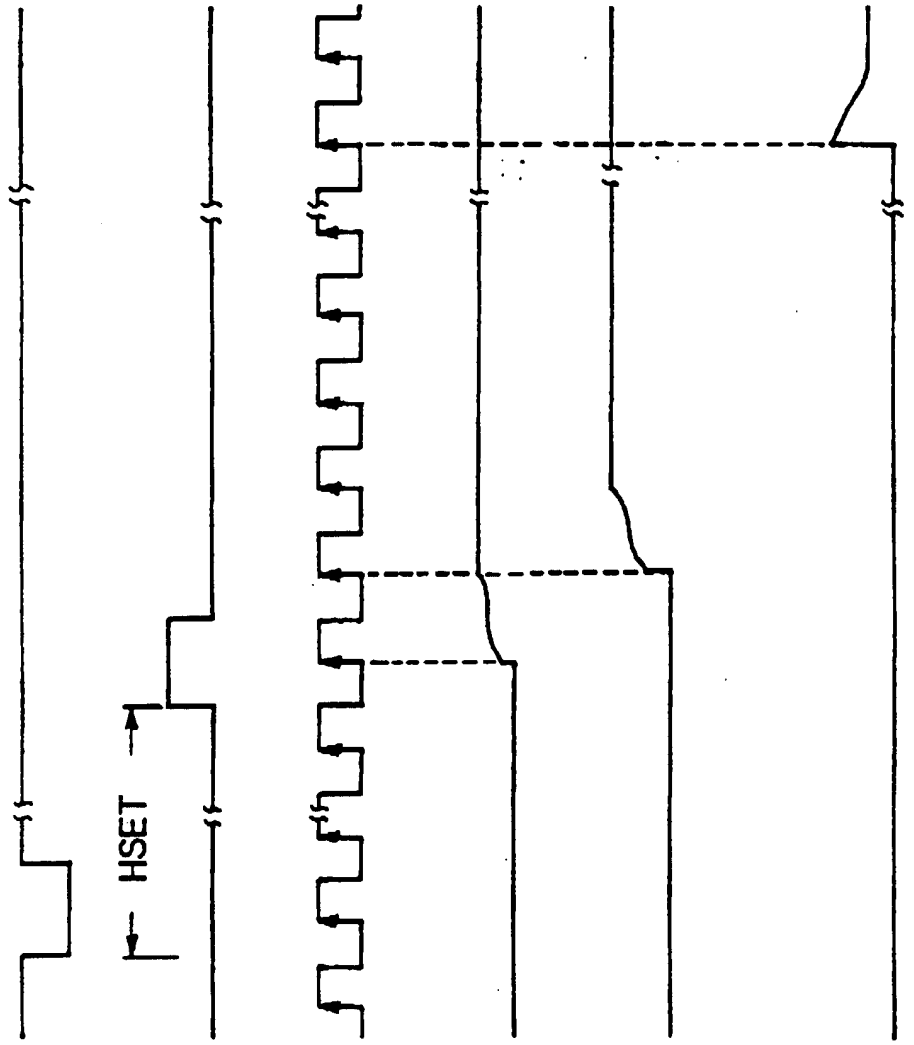


Fig. 4A

Fig. 4B

Fig. 4C

Fig. 4D

Fig. 4E

Fig. 4F

PRIOR ART

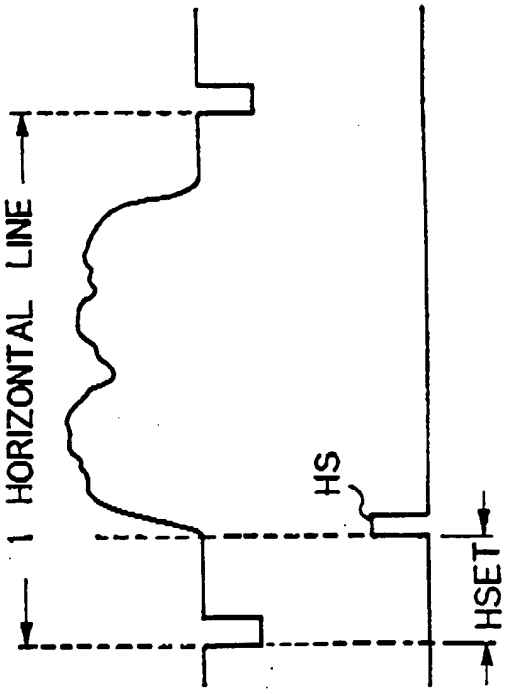


Fig. 5A

Fig. 5B

Fig. 6 PRIOR ART

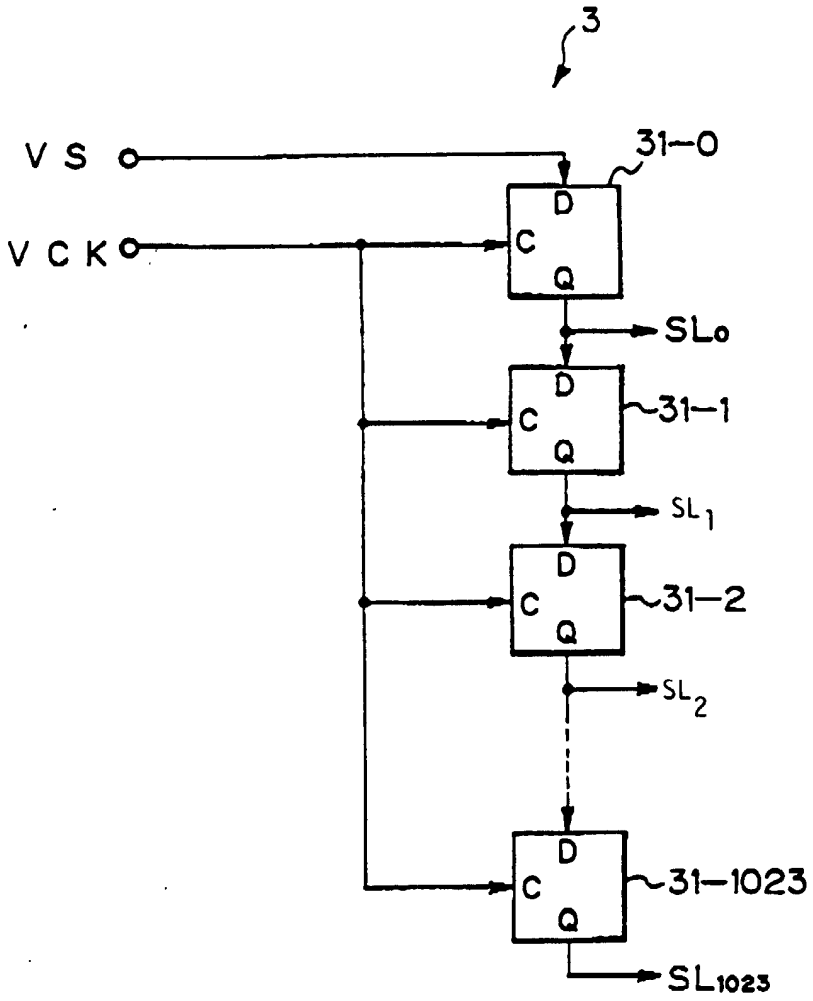
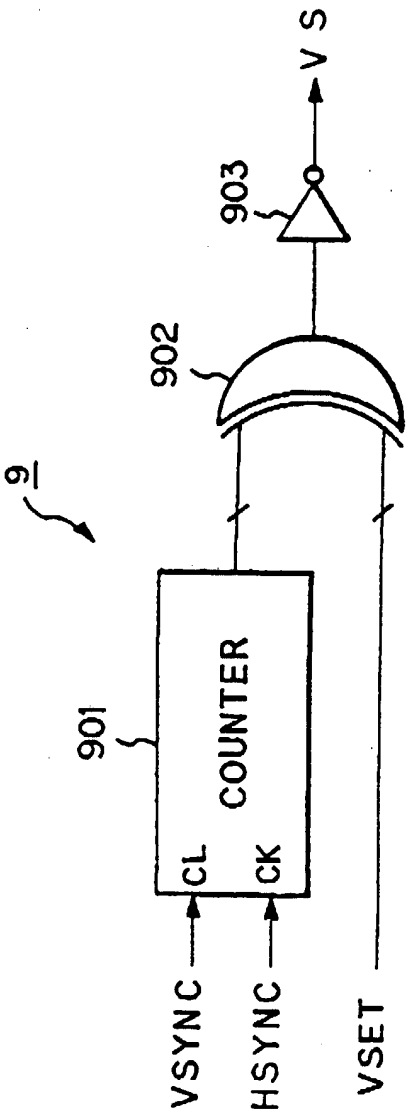


Fig. 7 PRIOR ART



PRIOR ART

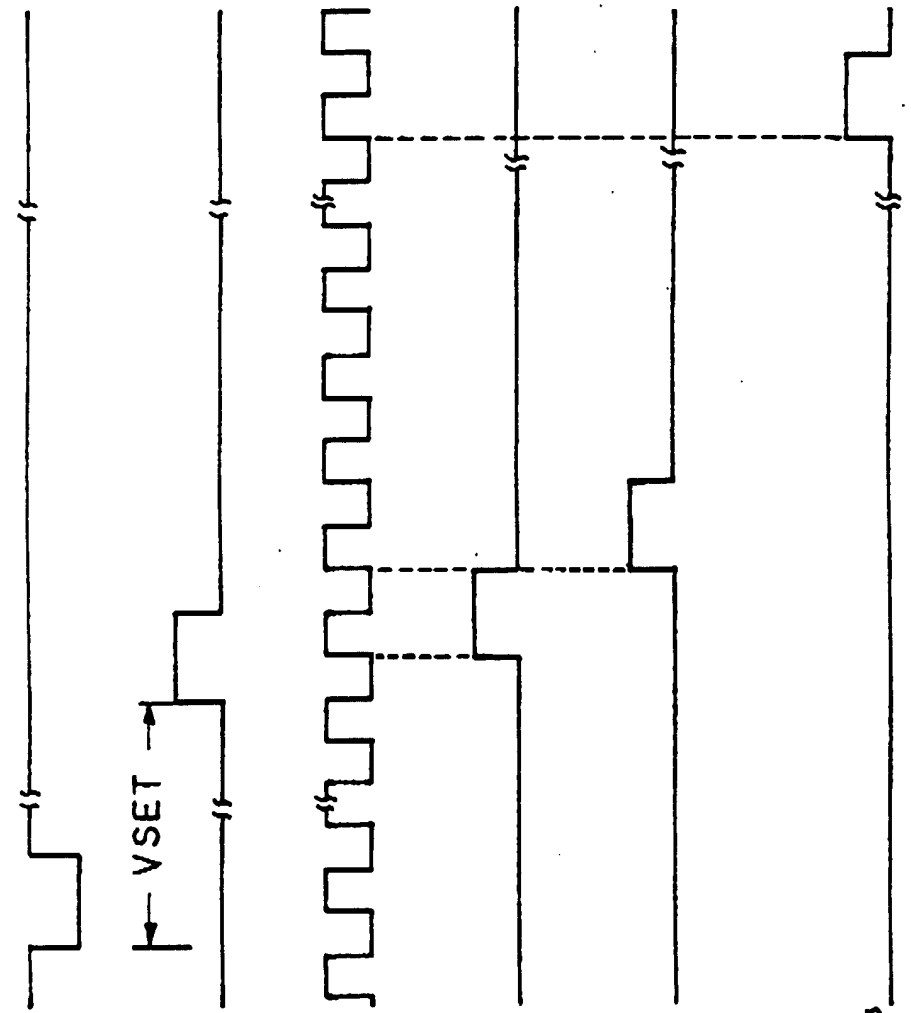


Fig. 8A

Fig. 8B

Fig. 8C

Fig. 8D

Fig. 8E

Fig. 8F

PRIOR ART

Fig. 9A

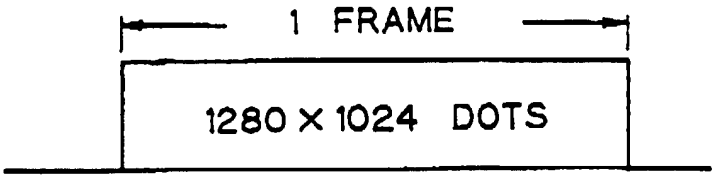


Fig. 9B

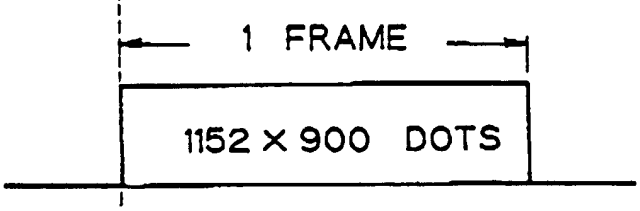


Fig. 9C

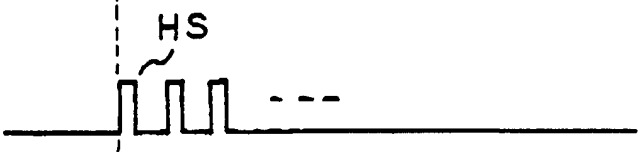


Fig. 9D

Fig. 9E

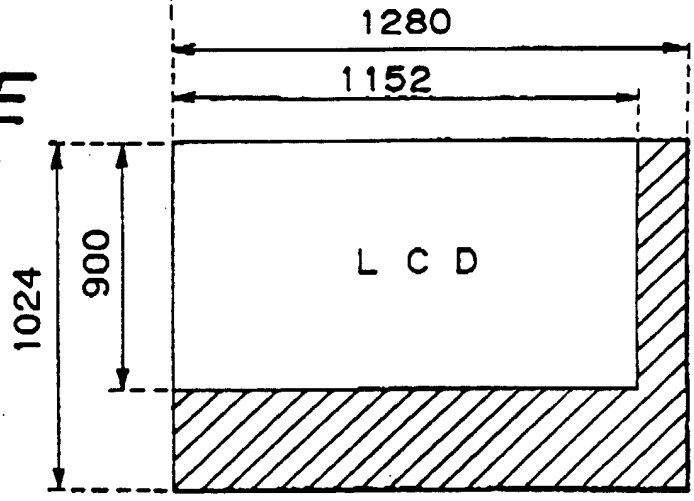


Fig. 10 PRIOR ART

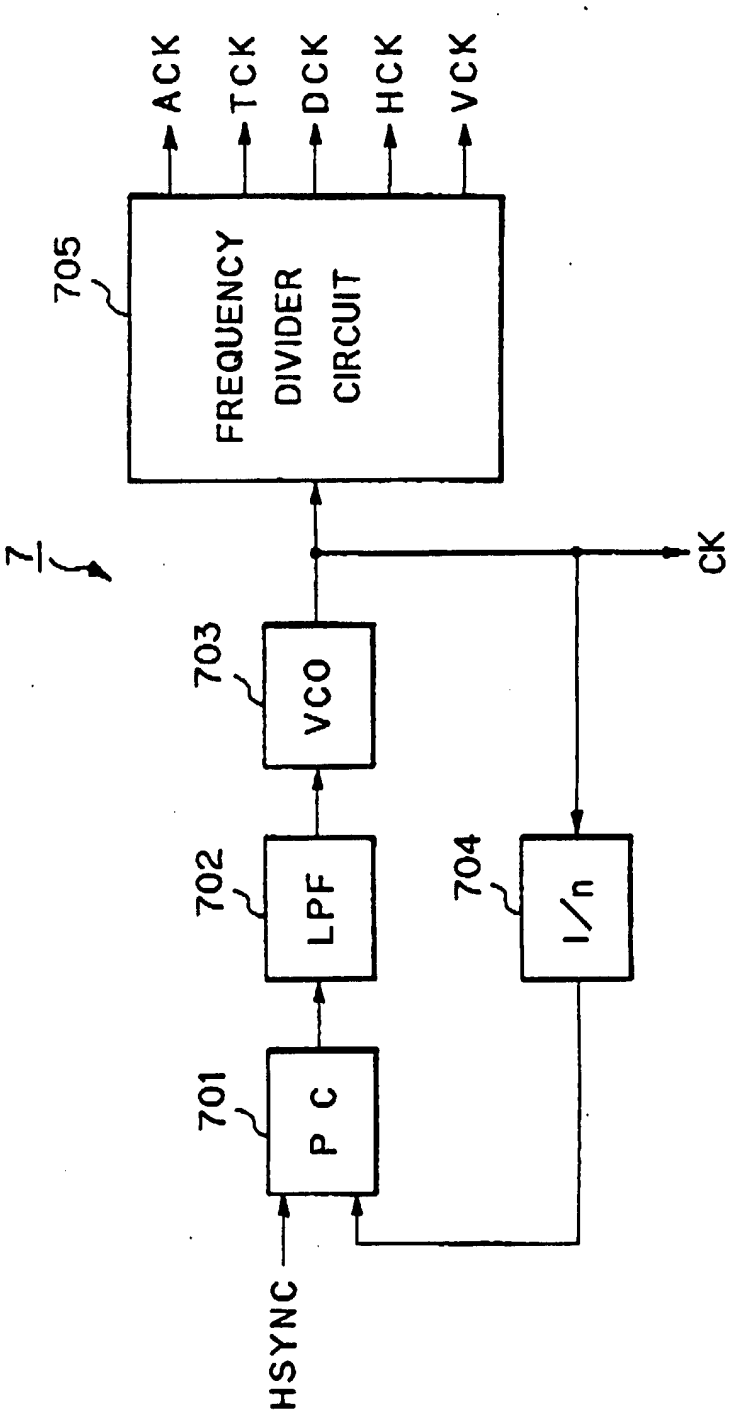


Fig. 11

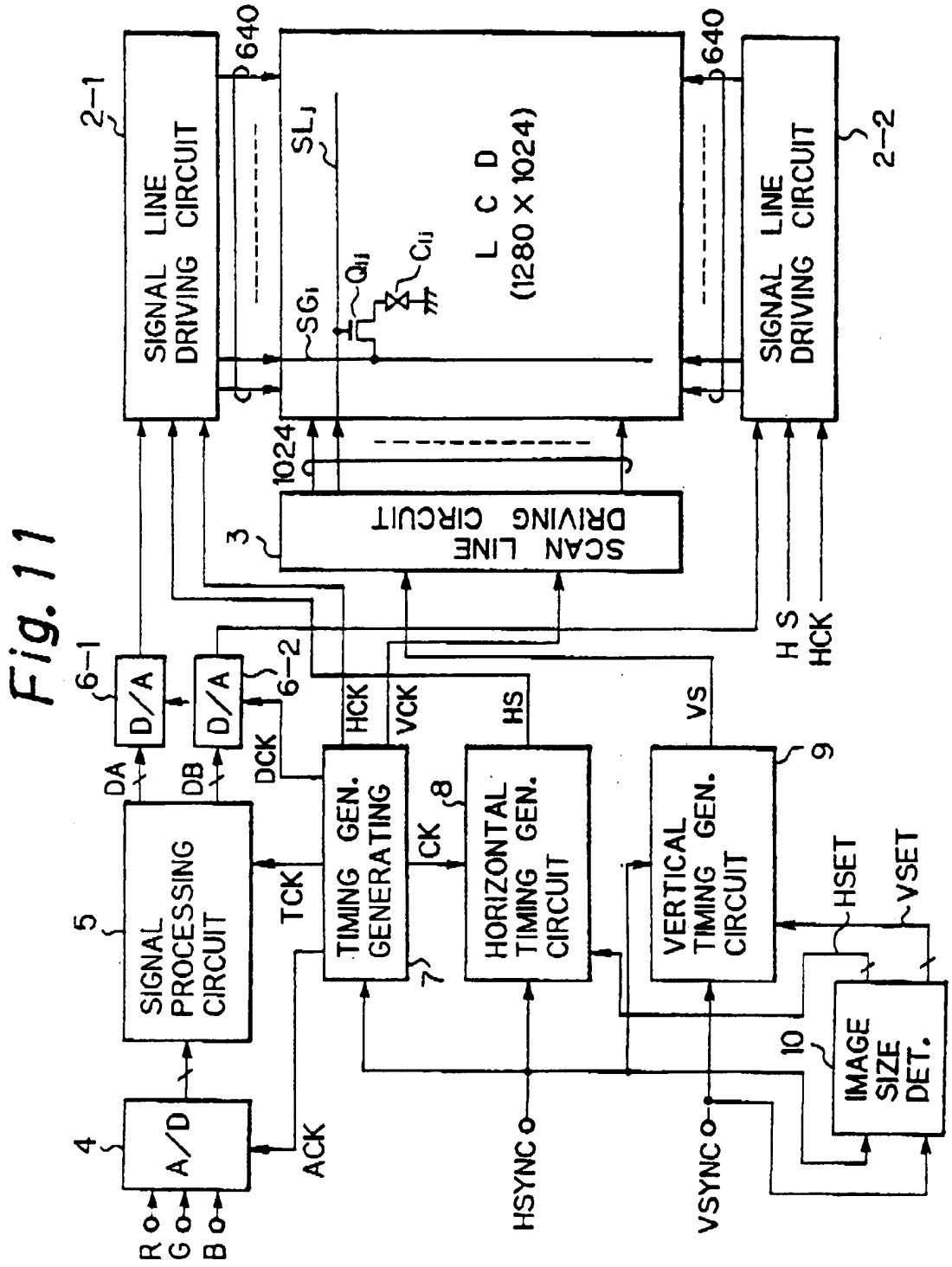

2-1
SIGNAL LINE DRIVING CIRCUIT
640
SLj
SGi
Qij
Cij
L C D
(1280 × 1024)
640
2-2
SIGNAL LINE DRIVING CIRCUIT
1024
3
SCAN LINE DRIVING CIRCUIT
H S
HCK
6-1
D/A
6-2
D/A
DA
DB
DCK
HCK
VCK
HS
VS
9
5
SIGNAL PROCESSING CIRCUIT
TCK
TIMING GEN. GENERATING
CK
8
HORIZONTAL TIMING GEN. CIRCUIT
VERTICAL TIMING GEN. CIRCUIT
HSET
VSET
7
4
A/D
ACK
10
IMAGE SIZE DET.
R
G
B
HSYNC
VSYNC

Fig. 12

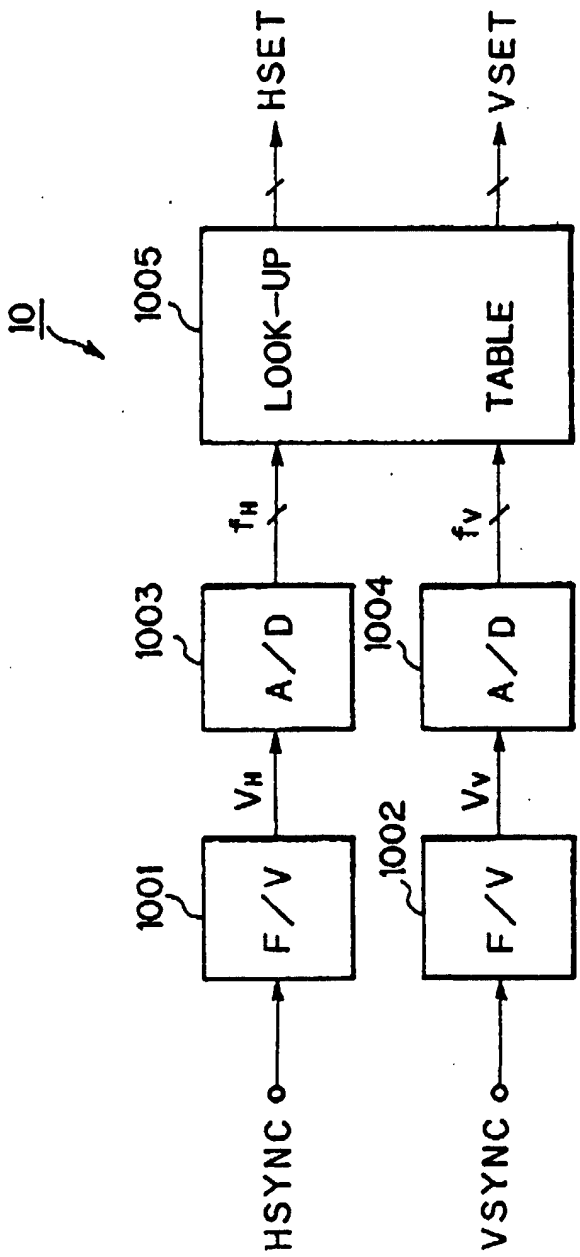
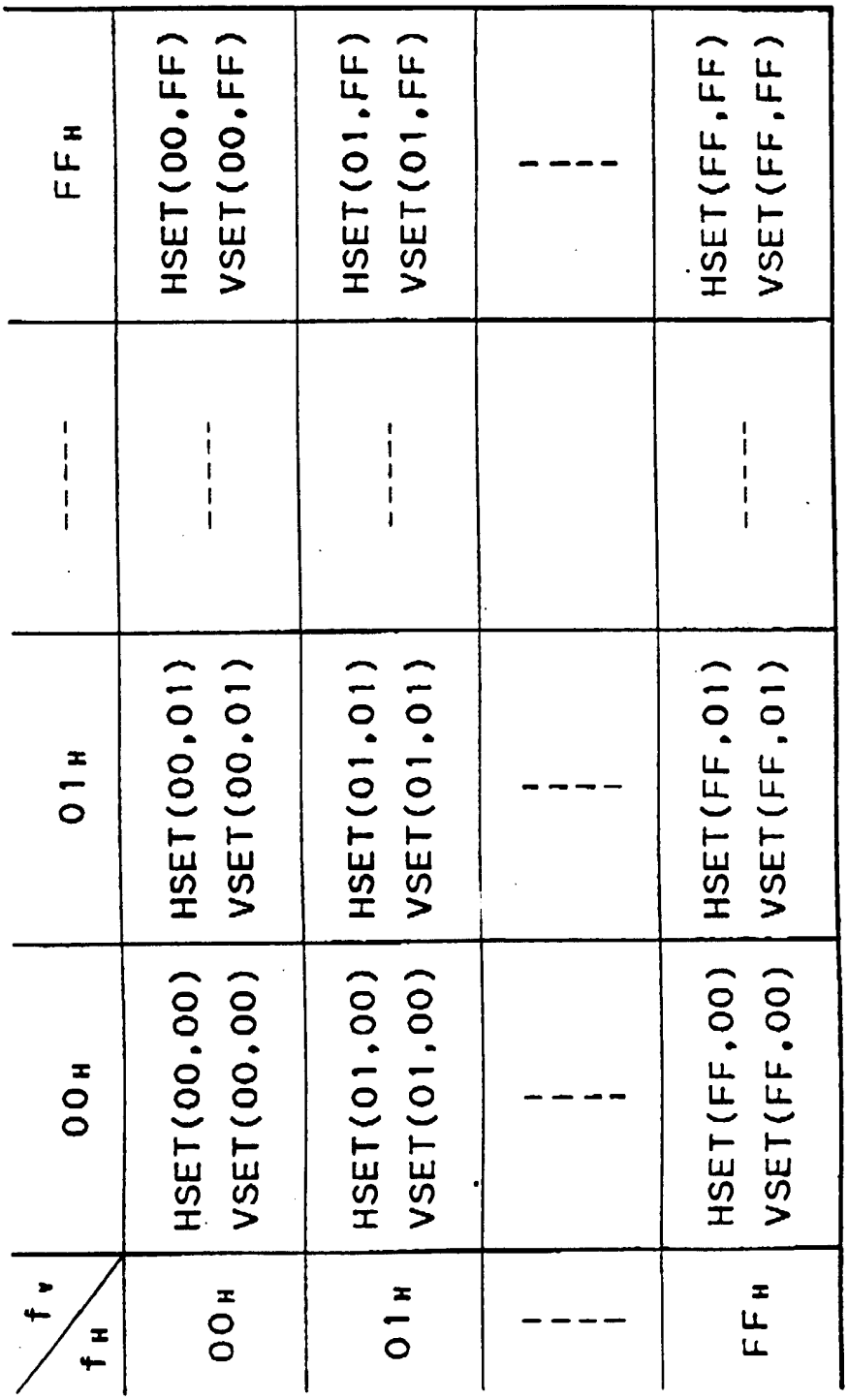

10
1005
LOOK-UP TABLE
HSET
VSET
f_H
f_V
1003
A/D
1004
A/D
V_H
V_V
1001
F/V
1002
F/V
HSYNC
VSYNC

Fig. 13


f_V / f_H
00H
01H

FFH
00H
HSET(00,00)
VSET(00,00)
HSET(00,01)
VSET(00,01)

HSET(00,FF)
VSET(00,FF)
01H
HSET(01,00)
VSET(01,00)
HSET(01,01)
VSET(01,01)

HSET(01,FF)
VSET(01,FF)

FFH
HSET(FF,00)
VSET(FF,00)
HSET(FF,01)
VSET(FF,01)

HSET(FF,FF)
VSET(FF,FF)

Fig. 14A

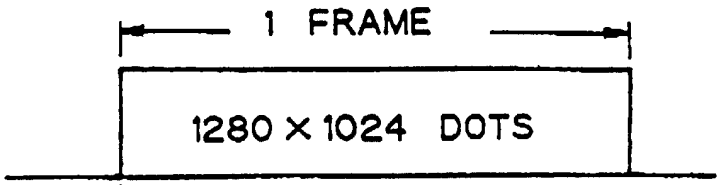


Fig. 14B

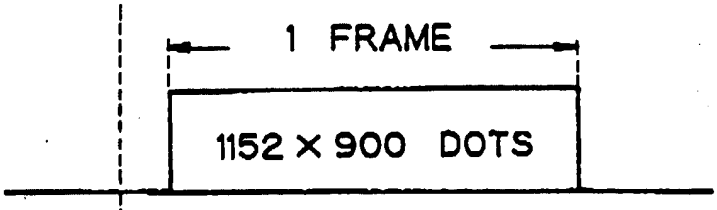


Fig. 14C

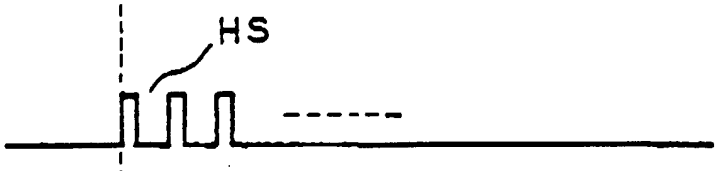


Fig. 14D

Fig. 14E

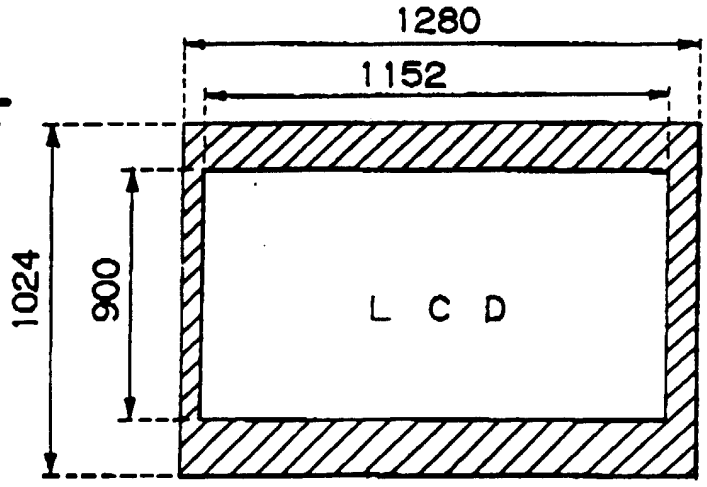


Fig. 15

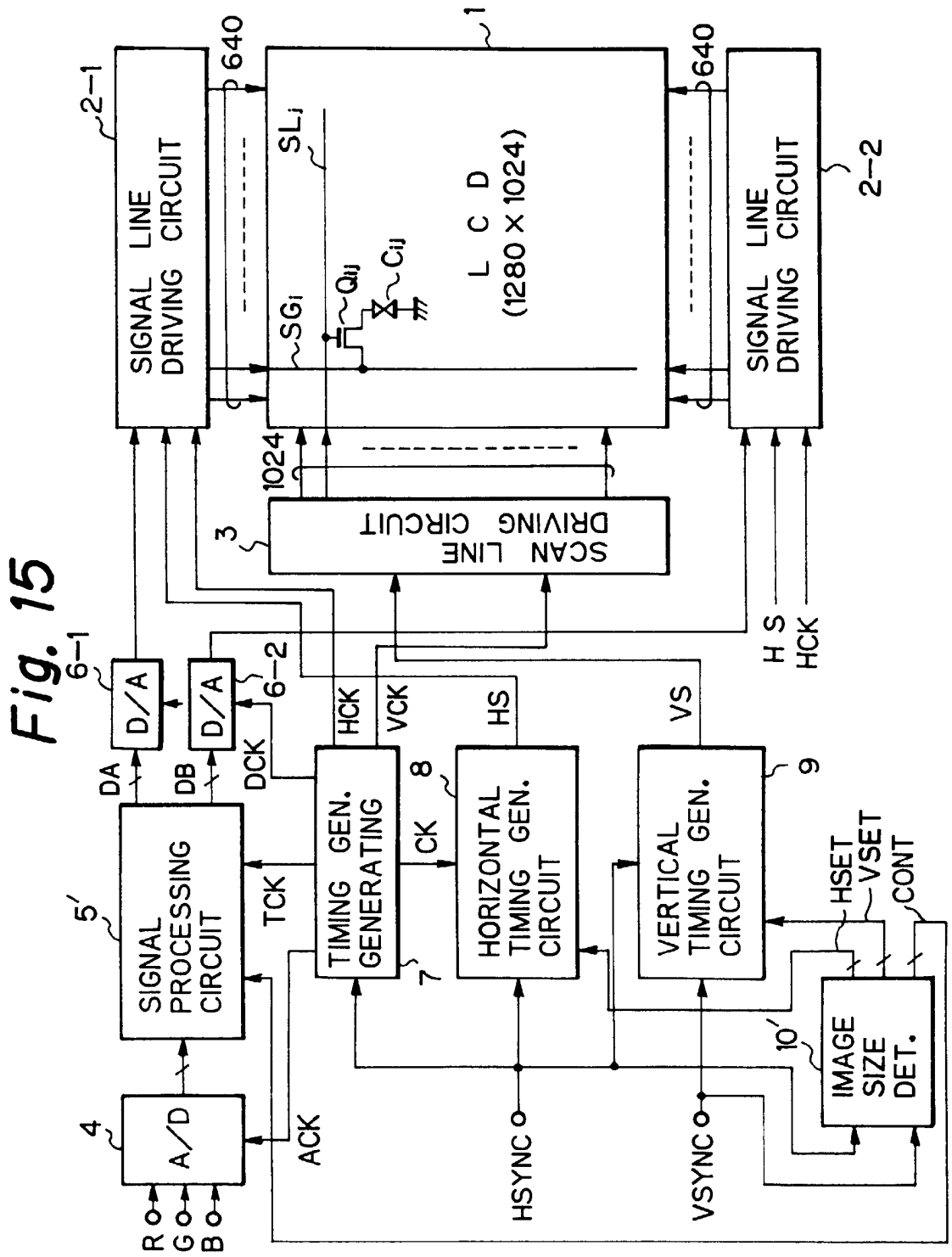

SIGNAL LINE DRIVING CIRCUIT
2-1
640
1
L C D
(1280 × 1024)
SLj
SGi
Qij
Cij
640
SIGNAL LINE DRIVING CIRCUIT
2-2
1024
SCAN LINE DRIVING CIRCUIT
3
H S
HCK
6-1
D/A
6-2
D/A
DA
DB
DCK
HCK
VCK
HS
VS
5'
SIGNAL PROCESSING CIRCUIT
TCK
TIMING GEN. GENERATING
8
CK
7
HORIZONTAL TIMING GEN. CIRCUIT
VERTICAL TIMING GEN. CIRCUIT
9
HSET
VSET
CONT
10'
IMAGE SIZE DET.
4
A/D
ACK
R
G
B
HSYNC
VSYNC

Fig. 16

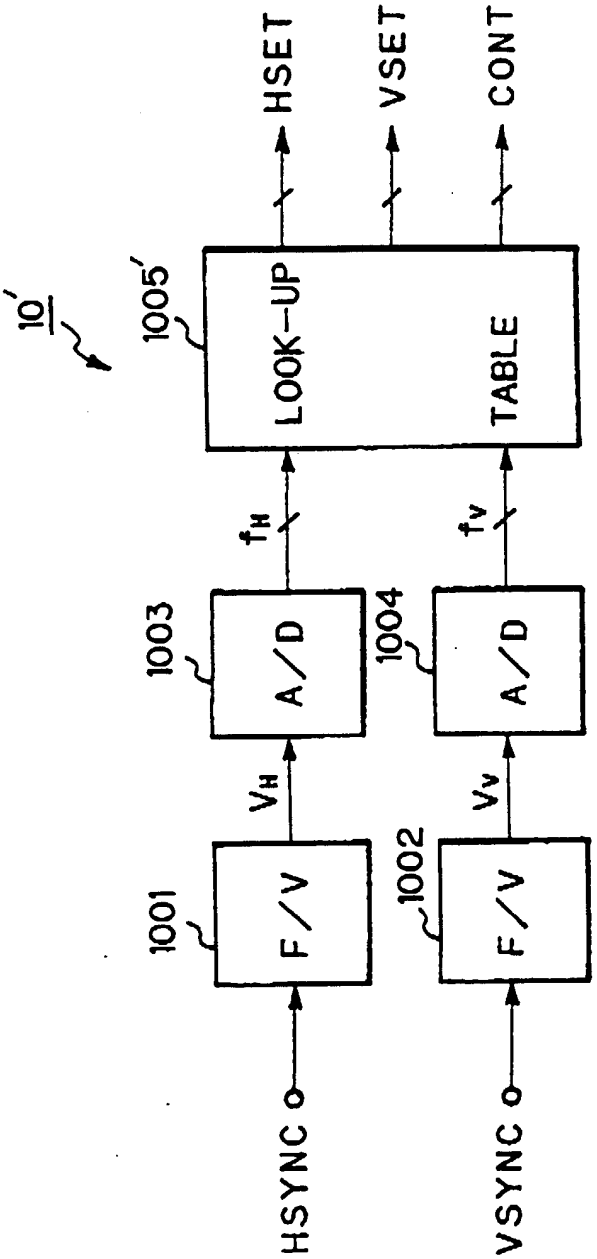

10'
1005'
LOOK-UP TABLE
HSET
VSET
CONT
f_H
f_V
1003
A/D
1004
A/D
V_H
V_V
1001
F/V
1002
F/V
HSYNC
VSYNC

Fig. 17

f_V / f_H	00_H	01_H	-----	FF_H
00_H	HSET(00,00) VSET(00,00) CONT(00,00)	HSET(00,01) VSET(00,01) CONT(00,01)	-----	HSET(00,FF) VSET(00,FF) CONT(00,FF)
01_H	HSET(01,00) VSET(01,00) CONT(01,00)	HSET(01,01) VSET(01,01) CONT(01,01)	-----	HSET(01,FF) VSET(01,FF) CONT(01,FF)
⋮	⋮	⋮		⋮
FF_H	HSET(FF,00) VSET(FF,00) CONT(FF,00)	HSET(FF,01) VSET(FF,01) CONT(FF,01)	-----	HSET(FF,FF) VSET(FF,FF) CONT(FF,FF)

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Fig. 18

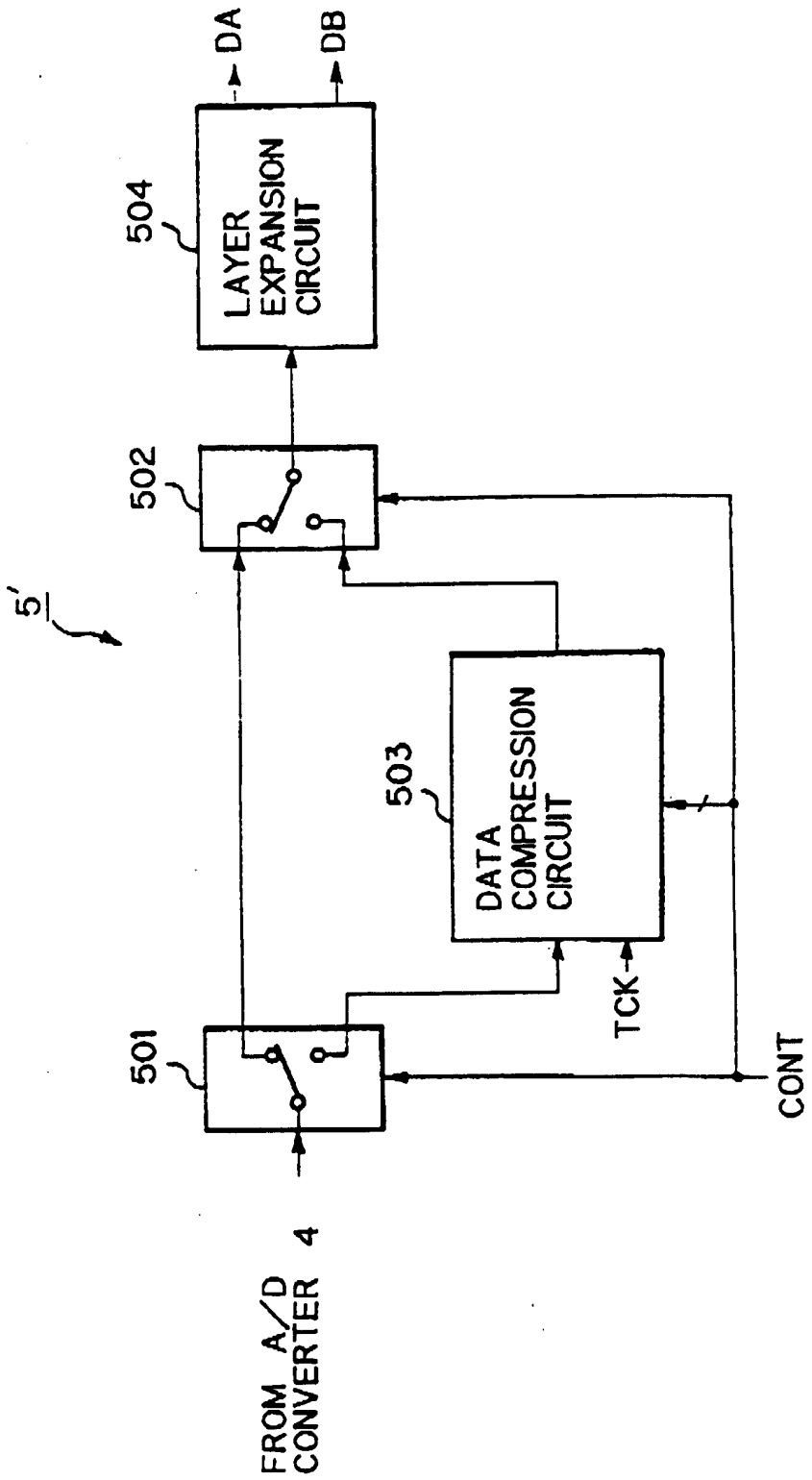
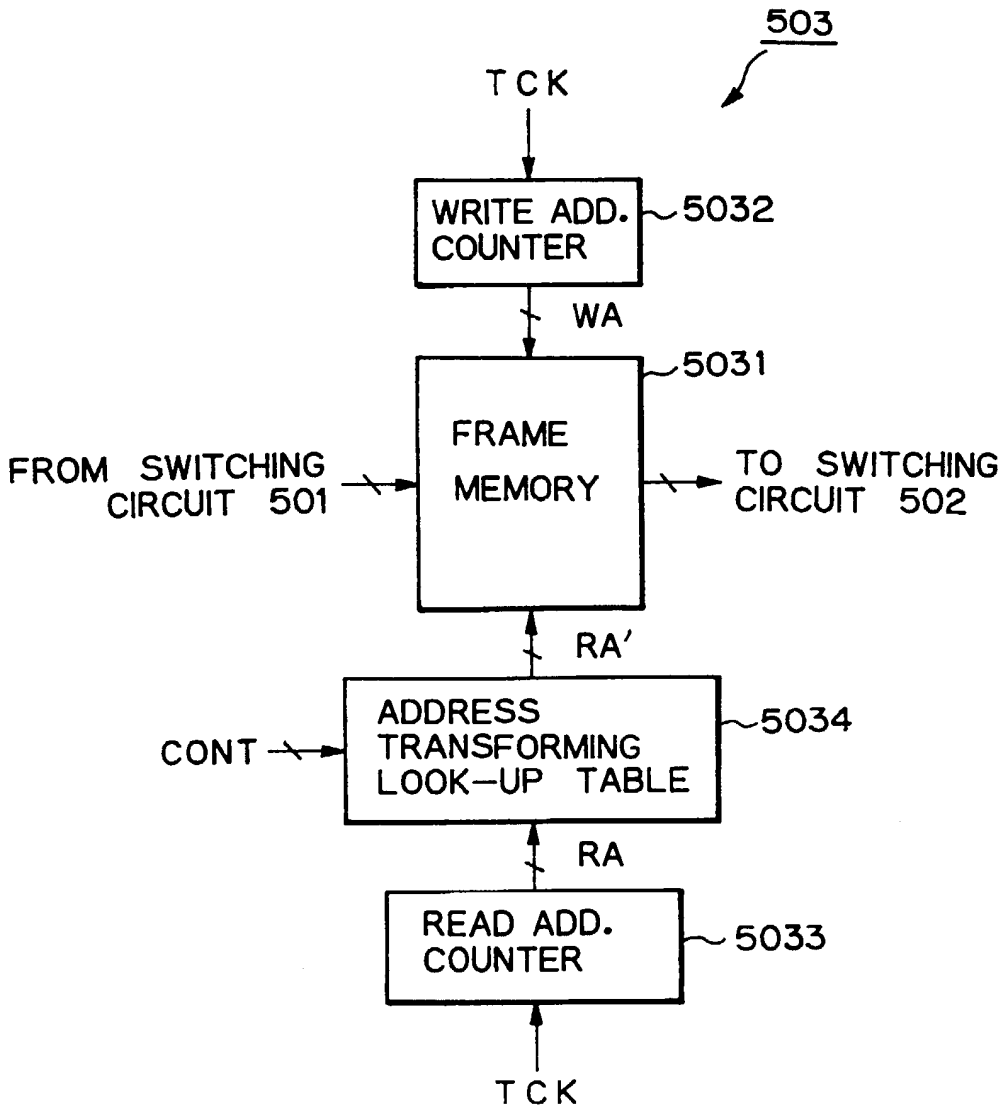

5'
501
502
503
504
LAYER EXPANSION CIRCUIT
DATA COMPRESSION CIRCUIT
DA
DB
TCK
CONT
FROM A/D CONVERTER 4

Fig. 19


503
TCK
WRITE ADD. COUNTER
5032
WA
5031
FRAME MEMORY
FROM SWITCHING CIRCUIT 501
TO SWITCHING CIRCUIT 502
RA'
ADDRESS TRANSFORMING LOOK-UP TABLE
5034
CONT
RA
READ ADD. COUNTER
5033
TCK

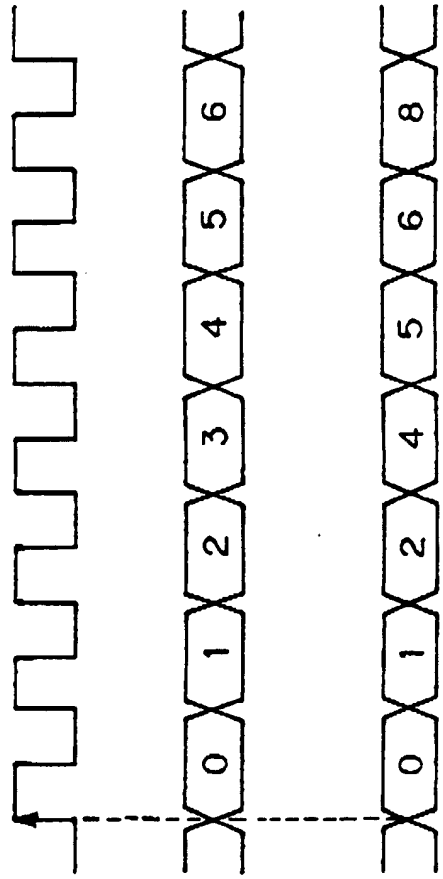
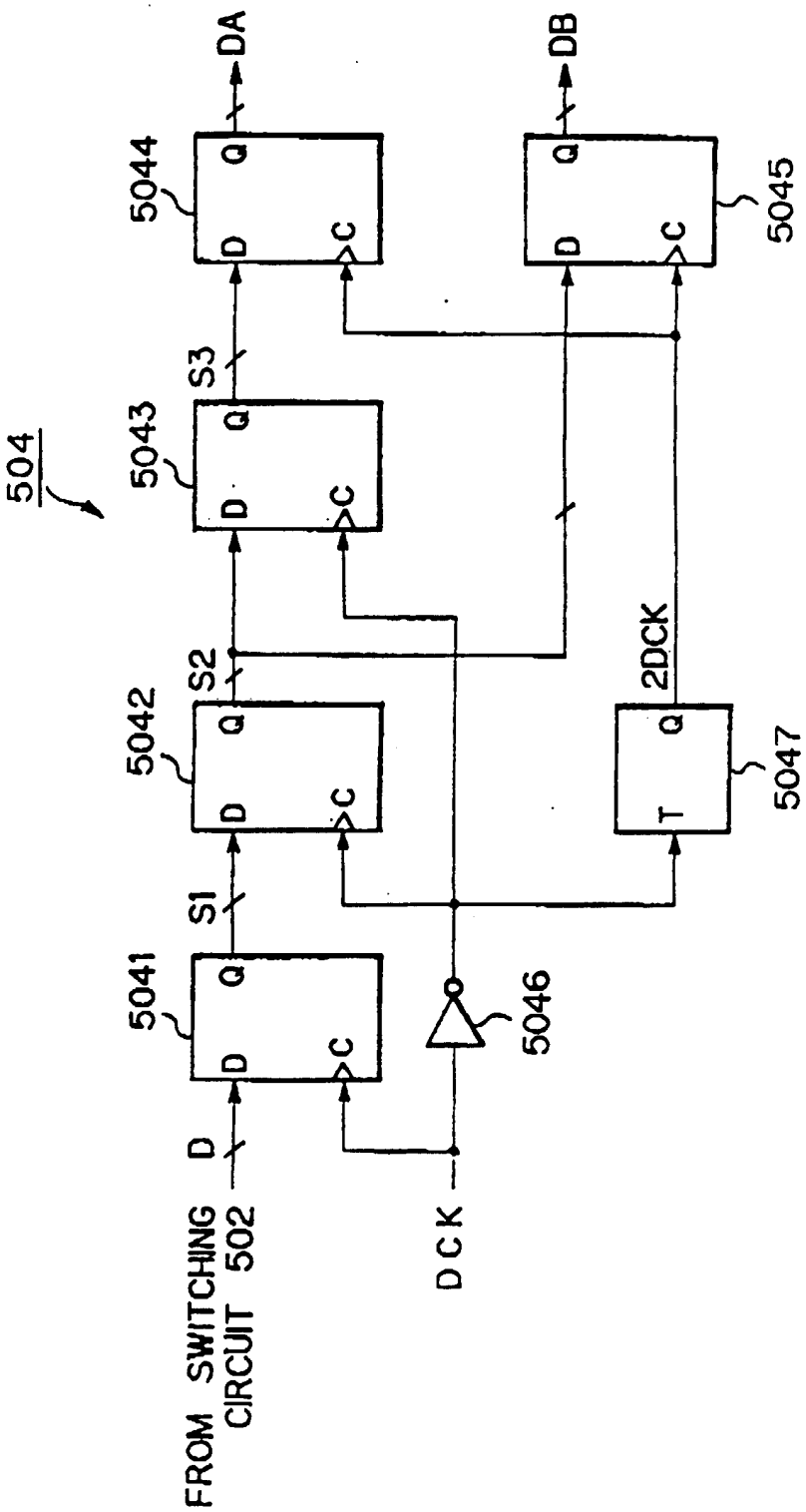


Fig. 20A

Fig. 20B

Fig. 20C

Fig. 21


504
5041
5042
5043
5044
5045
5046
5047
S1
S2
S3
D
DA
DB
2DCK
DCK
FROM SWITCHING CIRCUIT 502
Q
D
C
T

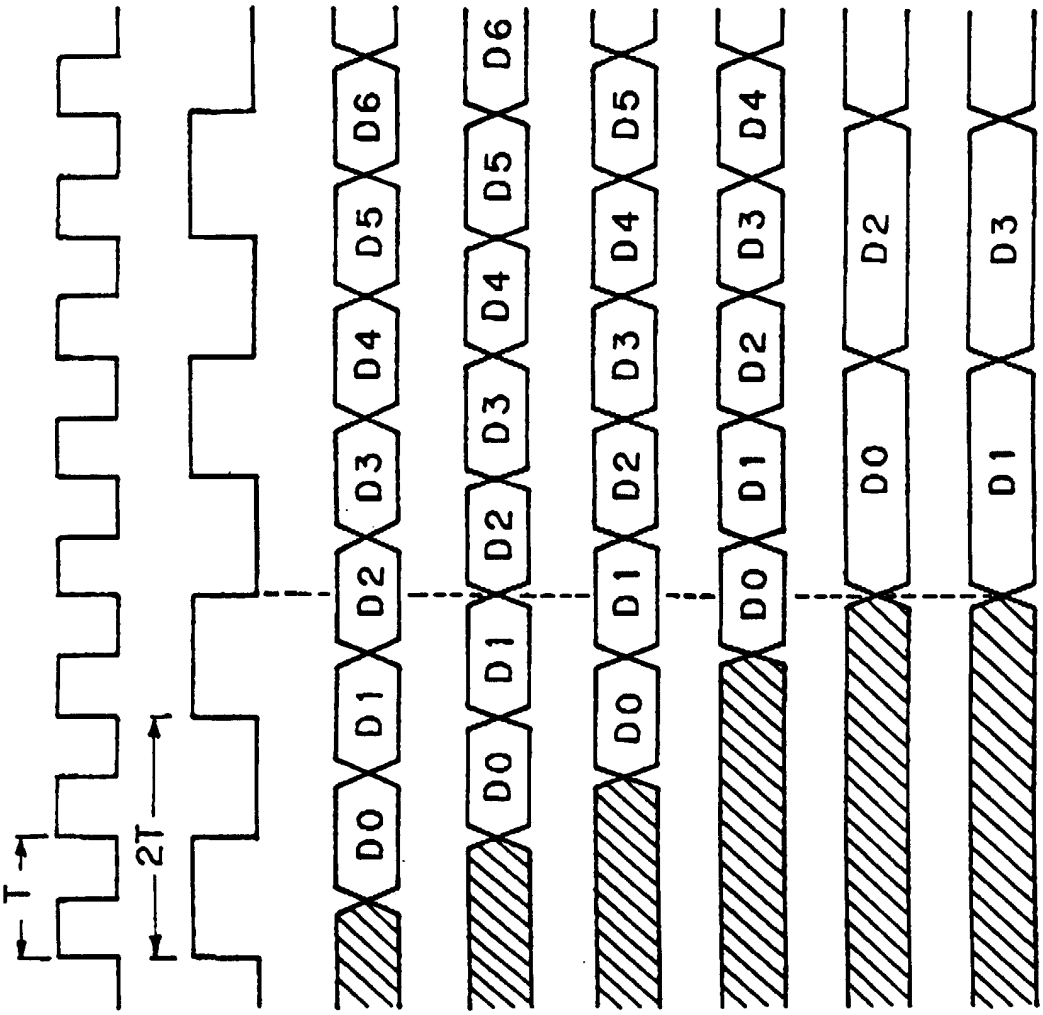


Fig. 22A

Fig. 22B

Fig. 22C

Fig. 22D

Fig. 22E

Fig. 22F

Fig. 22G

Fig. 22H