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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/735,583	04/16/2007	Kiyoharu Takano	TI-62395	2263

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EXAMINER	
SOLLENBERGER, STEPHEN J	
ART UNIT	PAPER NUMBER
1791	

NOTIFICATION DATE	DELIVERY MODE
01/08/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	11/735,583	TAKANO ET AL.	
	Examiner	Art Unit	
	STEPHEN SOLLENBERGER	1791	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-25* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/16/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-14, drawn to apparatus, classified in class 425, subclass 89.0.

II. Claim 15-25, drawn to method, classified in class 264, subclass 272.17.

The inventions are distinct, each from the other because of the following reasons:

Inventions 1-14 and 15-25 are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another and materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case. the method claimed could be performed with an apparatus of different specification, such as a cavity instead of a die as stated in claims 1 through 14.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

During a telephone conversation with Yinsheng Tung on 12/4/2008 a provisional election was made without traverse to prosecute the invention of the method, claims 15-25. Claims 1-14 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Priority

Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date: Certified priority documents have not been received.

Claim Objections

Claim 21 is objected to because of the following informalities: the claim refers to itself. In a conversion with Yinsheng Tung on 12/4/08, the applicant states that the claim is a method claim and refers to claim 20 instead of 21. The examiner thus reads it as such.

Claims 23-25 are objected to because of the following informalities: "in any one of Claims 15" and "in any one of Claims 20" is unclear. The examiner reads these claims as "in Claim 15" for claims 23 and 24 and as "in Claim 20" for Claim 25. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15-18, 20-22, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al. (5,218,759) in view of Yamaji (US 5,394,303).

Regarding claim 15 Juskey et al. teach a method for manufacturing a semiconductor device (Column 1, Line 61); comprising: providing a substrate that includes a first principal surface and a second principal surface opposite the first principal surface (Fig. 1 shows a substrate **12** with two principle surfaces); placing semiconductor elements on the first principal surface (a semiconductor device on a substrate; Column 1, Lines 14-15); placing the substrate on an insulating region of a lower die ("The temporary support substrate may be

selected from a wide variety of materials, but is preferably a thin material such as a printed circuit board, flexible film"; Column 2, Lines 35-38). Note, the examiner considers the "wide variety of materials" to encompass insulators); pressing an upper die in which multiple shape-forming parts are formed against the lower die; and supplying a liquid resin for molding the semiconductor elements ("A plastic material is then transfer-molded about the semiconductor device to form a completed package"; Column 1, Lines 18-20). Juskey et al. does not teach the use of a polymer film pressed by the upper die over the liquid resin. In the same field of endeavor of making semiconductor packages, Yamaji teaches a film over the semiconductor package ("a flexible insulating film"; Column 6, Line 52). Yamaji does not teach the film to be a polymer, but "a flexible insulating film" would most likely be a polymer and an obvious option to one of ordinary skill in the art at the time of the invention. Note, a film to cover the package is common.

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. with Yamaji for the benefit of covering a formed semiconductor package with a film to electrically insulate and further protect the package from damage.

Regarding claim 16, Juskey et al. in view of Yamaji teach the manufacturing method of claim 15. Juskey et al. further teach wherein the lower die includes a ceramic member, and the second principal surface of the substrate is mounted on the ceramic member (Column 2, Lines 35-36). Juskey et al. does not teach the film to be ceramic. Note, it would have been obvious to

one of ordinary skill in the art at the time of the invention that the film could be ceramic.

Regarding claim 17, Juskey et al. in view of Yamaji teach the manufacturing method described in claim 15. Juskey et al. further teach wherein the lower die includes an insulating film (Note, the temporary support substrate **18** of Fig. 1 is considered a film could be of a variety of materials including insulators; Column 2, Lines 35-38), and the second principal surface of the substrate is mounted on the insulating film (Figure 1).

Regarding claim 18, Juskey et al. in view of Yamaji teach the manufacturing method described in claim 15. Juskey et al. further teach wherein the insulating region is larger than the second principal surface of the substrate (See Figure 1; the insulating region **18** is larger than the substrate **19**).

Regarding claim 20, Juskey et al. in view of Yamaji teach the manufacturing method described in claim 15. Juskey et al. further teach wherein the substrate includes a first conductive region on the first principal surface, and the first conductive region is electrically connected to semiconductor elements ("A semiconductor device is electrically and mechanically connected to one side of a circuit carrying substrate"; Column 1, Lines 61-63).

Regarding claim 21, Juskey et al. in view of Yamaji teach the semiconductor manufacturing method described in claim 20. Jusky et al. further teach wherein the first conductive region is uncovered by the molded resin ("transfer molding a plastic material about the semiconductor device and

substantially all of the first major face of the circuit carrying substrate in order to form a second assembly; removing the second assembly from the mold cavity"; Column 6, Lines 31-35).

Regarding claim 22, Juskey et al. in view of Yamaji teach the manufacturing method described in claim 15. Yamaji further teach wherein the substrate includes a second conductive region on the second principal surface, and the second conductive region is electrically connected to the first conductive region or semiconductor elements ("To connect substrate wires 11_1 -11_n of the mounting substrate 10 to the device having the external electrode pads"; Column 3, Lines 12-25).

Regarding claim 25, Juskey et al. in view of Yamaji teach the manufacturing method described in claim 20. Yamaji further teach further comprising a step of stacking terminals of a second semiconductor device onto the first conductive region on the first principal surface of the substrate (Fig. 8 shows multiple semiconductor chips and terminals stacked on a substrate.

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. with Yamaji for the benefit of stacking multiple semiconductor terminals on a substrate and electrically connecting them for the benefit of greater efficiency and capacity.

Claims 19, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey et al. (5,218,759) in view of Yamaji (US 5,394,303) and in further view of Ujiie et al. (US 7,371,606 B2).

Regarding claim 19, Juskey et al. in view of Yamaji teach the manufacturing method described in claim 15. Juskey et al. fails to teach a polymer film held by suction by air intake on the upper die. In the same field of endeavor of making semiconductor packages, Ujiie et al. teach wherein the polymer film is held by suction in the multiple shape-forming parts by air intake from air intake holes formed in the upper die ("Vacuum suction holes 17b9 are formed in the upper die 17b. The laminate film 17c is vacuum-sucked through the vacuum suction holes 17b9 and are brought into close contact with the molding surface of the upper die 17b"; Column 15, Lines 40-44).

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. and Yamaji with Ujiie et al. for the benefit of efficiency covering the package with a film and preventing damage to the film.

Regarding claim 23, Juskey et al. in view of Yamaji teach the manufacturing method described in claims 15. Ujiie et al. further teach wherein the substrate is a multilayer circuit board ("A semiconductor substrate 1S which constitutes the wafer 1W is formed of a single crystal of silicon (Si) for example and elements for forming a memory circuit such as, for example, SRAM (Static Random Access Memory), as well as a multi-layer interconnection, are formed on a main surface of the semiconductor substrate 1S"; Column 5, Lines 66-67 through Column 6, Lines 1-5).

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. and Yamaji with Ujiie et al. for the benefit of forming more complicated circuits including multi-layers.

Regarding claim 24, Juskey et al. in view of Yamaji teach the manufacturing method described in claim 15. Ujiie et al. further teach comprising a step of cutting the substrate into individual semiconductor elements ("covered all together with a sealing resin, and are then cut out into individual semiconductor chips"; Column 1, Lines 36-38).

Thus, it would have been obvious to one skilled in the art at the time of the invention to combine Juskey et al. and Yamaji with Ujiie et al. for the benefit of forming many individual packages.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN SOLLENBERGER whose telephone number is (571) 270-1922. The examiner can normally be reached from 9 am to 5 pm ET, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Del Sole can be reached at 571-272-1130. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

S.J.S.

/Joseph S. Del Sole/

Supervisory Patent Examiner, Art Unit 1791