```
#-----------------------------------------------------------
# Vivado v2016.2 (64-bit)
# SW Build 1577090 on Thu Jun  2 16:32:40 MDT 2016
# IP Build 1577682 on Fri Jun  3 12:00:54 MDT 2016
# Start of session at: Mon Apr 10 18:48:04 2017
# Process ID: 7844
# Current directory: Z:/Documents/EE460M/lab6/lab6_vivado/lab6_vivado.runs/synth_1
# Command line: vivado.exe -log top.vds -mode batch -messageDb vivado.pb -notrace -source
top.tcl
# Log file: Z:/Documents/EE460M/lab6/lab6_vivado/lab6_vivado.runs/synth_1/top.vds
# Journal file: Z:/Documents/EE460M/lab6/lab6_vivado/lab6_vivado.runs/synth_1\vivado.jou
#-----------------------------------------------------------
source top.tcl -notrace
Command: synth_design -top top -part xc7a35tcpg236-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 6812
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:08 ; elapsed = 00:00:12 . Memory (MB): peak =
271.578 ; gain = 64.438
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'top' [Z:/Documents/EE460M/lab6/lab6.v:1]
INFO: [Synth 8-638] synthesizing module 'controller' [Z:/Documents/EE460M/lab6/lab6.v:46]
        Parameter idle bound to: 0 - type: integer
        Parameter push bound to: 1 - type: integer
        Parameter pop bound to: 2 - type: integer
        Parameter reset bound to: 3 - type: integer
        Parameter top bound to: 4 - type: integer
        Parameter inc bound to: 5 - type: integer
        Parameter dec bound to: 6 - type: integer
        Parameter add1 bound to: 7 - type: integer
        Parameter readFirstAdd bound to: 8 - type: integer
        Parameter readSecondAdd bound to: 9 - type: integer
        Parameter add2 bound to: 10 - type: integer
        Parameter sub1 bound to: 11 - type: integer
        Parameter sub2 bound to: 12 - type: integer
        Parameter readFirstSub bound to: 13 - type: integer
        Parameter readSecondSub bound to: 14 - type: integer
        Parameter writeAdd bound to: 15 - type: integer
        Parameter writeSub bound to: 16 - type: integer
INFO: [Synth 8-155] case statement is not full and has no default
[Z:/Documents/EE460M/lab6/lab6.v:115]
```

WARNING: [Synth 8-567] referenced signal 'prevSPR' should be on the sensitivity list [Z:/Documents/EE460M/lab6/lab6.v:103]
WARNING: [Synth 8-567] referenced signal 'prevDAR' should be on the sensitivity list [Z:/Documents/EE460M/lab6/lab6.v:103]
WARNING: [Synth 8-567] referenced signal 'prev_temp1' should be on the sensitivity list [Z:/Documents/EE460M/lab6/lab6.v:103]
WARNING: [Synth 8-567] referenced signal 'prev_temp2' should be on the sensitivity list [Z:/Documents/EE460M/lab6/lab6.v:103]
WARNING: [Synth 8-567] referenced signal 'swtchs' should be on the sensitivity list [Z:/Documents/EE460M/lab6/lab6.v:103]
WARNING: [Synth 8-567] referenced signal 'data_in' should be on the sensitivity list [Z:/Documents/EE460M/lab6/lab6.v:103]
INFO: [Synth 8-638] synthesizing module 'clockDivider' [Z:/Documents/EE460M/lab6/clockDivider.v:1]
INFO: [Synth 8-256] done synthesizing module 'clockDivider' (1#1) [Z:/Documents/EE460M/lab6/clockDivider.v:1]
INFO: [Synth 8-638] synthesizing module 'SevenSeg_Display' [Z:/Documents/EE460M/lab6/lab6.v:324]
INFO: [Synth 8-226] default block is never used [Z:/Documents/EE460M/lab6/lab6.v:340]
INFO: [Synth 8-638] synthesizing module 'binary_seven' [Z:/Documents/EE460M/lab6/lab6.v:368]
INFO: [Synth 8-226] default block is never used [Z:/Documents/EE460M/lab6/lab6.v:374]
INFO: [Synth 8-256] done synthesizing module 'binary_seven' (2#1) [Z:/Documents/EE460M/lab6/lab6.v:368]
INFO: [Synth 8-256] done synthesizing module 'SevenSeg_Display' (3#1) [Z:/Documents/EE460M/lab6/lab6.v:324]
INFO: [Synth 8-256] done synthesizing module 'controller' (4#1) [Z:/Documents/EE460M/lab6/lab6.v:46]
INFO: [Synth 8-638] synthesizing module 'memory' [Z:/Documents/EE460M/lab6/lab6.v:275]
INFO: [Synth 8-256] done synthesizing module 'memory' (5#1) [Z:/Documents/EE460M/lab6/lab6.v:275]
INFO: [Synth 8-638] synthesizing module 'Debounce' [Z:/Documents/EE460M/lab6/lab6.v:297]
INFO: [Synth 8-256] done synthesizing module 'Debounce' (6#1) [Z:/Documents/EE460M/lab6/lab6.v:297]
INFO: [Synth 8-256] done synthesizing module 'top' (7#1) [Z:/Documents/EE460M/lab6/lab6.v:1]

Finished RTL Elaboration : Time (s): cpu = 00:00:10 ; elapsed = 00:00:13 . Memory (MB): peak = 308.922 ; gain = 101.781

Report Check Netlist:

	Item	Errors	Warnings	Status	Description

```
+------+-----------------+-------+---------+-------+-----------------+
|1     |multi_driven_nets |      0|       0|Passed |Multi driven nets |
+------+-----------------+-------+---------+-------+-----------------+
```

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:13 . Memory (MB): peak = 308.922 ; gain = 101.781

INFO: [Device 21-403] Loading part xc7a35tcpg236-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [Z:/Documents/EE460M/lab6/Basys3_Master_Lab6.xdc]
Finished Parsing XDC File [Z:/Documents/EE460M/lab6/Basys3_Master_Lab6.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [Z:/Documents/EE460M/lab6/Basys3_Master_Lab6.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/top_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [.Xil/top_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 597.215 ; gain = 0.000

Finished Constraint Validation : Time (s): cpu = 00:00:20 ; elapsed = 00:00:25 . Memory (MB): peak = 597.215 ; gain = 390.074

Start Loading Part and Timing Information

Loading part: xc7a35tcpg236-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:20 ; elapsed = 00:00:25 . Memory (MB): peak = 597.215 ; gain = 390.074

Start Applying 'set_property' XDC Constraints

Applied set_property RAM_STYLE = BLOCK for ctrl. (constraint file
Z:/Documents/EE460M/lab6/Basys3_Master_Lab6.xdc, line 6).
Applied set_property RAM_STYLE = BLOCK for mem. (constraint file
Z:/Documents/EE460M/lab6/Basys3_Master_Lab6.xdc, line 6).
Applied set_property RAM_STYLE = BLOCK for D. (constraint file
Z:/Documents/EE460M/lab6/Basys3_Master_Lab6.xdc, line 6).
Applied set_property RAM_STYLE = BLOCK for data_bus1_i. (constraint file
Z:/Documents/EE460M/lab6/Basys3_Master_Lab6.xdc, line 6).
Applied set_property RAM_STYLE = BLOCK for data_bus0. (constraint file
Z:/Documents/EE460M/lab6/Basys3_Master_Lab6.xdc, line 6).
Applied set_property RAM_STYLE = BLOCK for data_bus0__0. (constraint file
Z:/Documents/EE460M/lab6/Basys3_Master_Lab6.xdc, line 6).

Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:20 ; elapsed = 00:00:25
. Memory (MB): peak = 597.215 ; gain = 390.074

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent
sharing consider applying a KEEP on the output of the operator
[Z:/Documents/EE460M/lab6/lab6.v:115]
INFO: [Synth 8-5546] ROM "leds0" won't be mapped to RAM because it is too sparse
---
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:21 ; elapsed = 00:00:25 . Memory
(MB): peak = 597.215 ; gain = 390.074

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start RTL Component Statistics

Detailed RTL Component Info :
+---Adders :
	3 Input 8 Bit Adders := 1
	2 Input 7 Bit Adders := 5
+---Registers :
		8 Bit Registers := 1
		1 Bit Registers := 9
+---RAMs :
		1024 Bit RAMs := 1
+---Muxes :
	3 Input 8 Bit Muxes := 1

```
            16 Input      7 Bit       Muxes := 1
             6 Input      7 Bit       Muxes := 1
             8 Input      7 Bit       Muxes := 1
             4 Input      7 Bit       Muxes := 1
             4 Input      5 Bit       Muxes := 1
             2 Input      5 Bit       Muxes := 8
             2 Input      4 Bit       Muxes := 1
            18 Input      3 Bit       Muxes := 2
            18 Input      2 Bit       Muxes := 2
             2 Input      2 Bit       Muxes := 1
             2 Input      1 Bit       Muxes := 1
            18 Input      1 Bit       Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module clockDivider
Detailed RTL Component Info :
+---Registers :
                    1 Bit    Registers := 1
Module binary_seven
Detailed RTL Component Info :
+---Muxes :
            16 Input      7 Bit       Muxes := 1
Module SevenSeg_Display
Detailed RTL Component Info :
+---Registers :
                    1 Bit    Registers := 1
+---Muxes :
             2 Input      4 Bit       Muxes := 1
             2 Input      1 Bit       Muxes := 1
Module controller
Detailed RTL Component Info :
+---Adders :
             3 Input      8 Bit       Adders := 1
             2 Input      7 Bit       Adders := 5
+---Muxes :
             3 Input      8 Bit       Muxes := 1
             6 Input      7 Bit       Muxes := 1
             8 Input      7 Bit       Muxes := 1
             4 Input      7 Bit       Muxes := 1
```

```
               4 Input      5 Bit       Muxes := 1
               2 Input      5 Bit       Muxes := 8
              18 Input      3 Bit       Muxes := 2
              18 Input      2 Bit       Muxes := 2
               2 Input      2 Bit       Muxes := 1
              18 Input      1 Bit       Muxes := 1
Module memory
Detailed RTL Component Info :
+---Registers :
                     8 Bit    Registers := 1
+---RAMs :
                  1024 Bit        RAMs := 1
Module Debounce
Detailed RTL Component Info :
+---Registers :
                     1 Bit    Registers := 6
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 90 (col length:60)
BRAMs: 100 (col length: RAMB18 60 RAMB36 30)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
Start Parallel Synthesis Optimization  : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory
(MB): peak = 597.215 ; gain = 390.074
---------------------------------------------------------------------------------
Start Cross Boundary Optimization
---------------------------------------------------------------------------------
INFO: [Synth 8-5546] ROM "leds0" won't be mapped to RAM because it is too sparse
---------------------------------------------------------------------------------
Finished Cross Boundary Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory
(MB): peak = 597.215 ; gain = 390.074
---------------------------------------------------------------------------------
Finished Parallel Reinference  : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory (MB):
peak = 597.215 ; gain = 390.074

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
```

```
+-+--------------+------------+----------+
+-+--------------+------------+----------+
```

Start ROM, RAM, DSP and Shift Register Reporting

ROM:

```
+------------+------------+--------------+----------------+
|Module Name | RTL Object | Depth x Width | Implemented As |
+------------+------------+--------------+----------------+
|controller  | nextState  | 32x5         | LUT            |
|controller  | temp2      | 32x1         | LUT            |
|controller  | temp1      | 32x1         | LUT            |
|top         | data_bus1  | 2x8          | LUT            |
|controller  | nextState  | 32x5         | LUT            |
|controller  | temp2      | 32x1         | LUT            |
|controller  | temp1      | 32x1         | LUT            |
|top         | data_bus1  | 2x8          | LUT            |
+------------+------------+--------------+----------------+
```

Block RAM: Preliminary Mapping Report (see note below)

```
+------------+------------+----------------------+---+---+----------------------+---+---+-----------------+--------
+--------+
|Module Name | RTL Object | PORT A (Depth x Width) | W | R | PORT B (Depth x Width) | W |
R | Ports driving FF | RAMB18 | RAMB36 |
+------------+------------+----------------------+---+---+----------------------+---+---+-----------------+--------
+--------+
|memory      | RAM_reg    | 128 x 8(READ_FIRST)    | W | R |                      |   |   | Port A          | 1
| 0      |
+------------+------------+----------------------+---+---+----------------------+---+---+-----------------+--------
+--------+
```

Note: The table above is a preliminary report that shows the Block RAMs at the current stage of the synthesis flow. Some Block RAMs may be reimplemented as non Block RAM primitives later in the synthesis flow. Multiple instantiated Block RAMs are reported only once.

Finished ROM, RAM, DSP and Shift Register Reporting

Start Area Optimization

Finished Area Optimization : Time (s): cpu = 00:00:23 ; elapsed = 00:00:28 . Memory (MB): peak = 597.215 ; gain = 390.074

Finished Parallel Area Optimization : Time (s): cpu = 00:00:23 ; elapsed = 00:00:28 . Memory (MB): peak = 597.215 ; gain = 390.074

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start Timing Optimization

Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:34 ; elapsed = 00:00:40 . Memory (MB): peak = 597.215 ; gain = 390.074

Finished Timing Optimization : Time (s): cpu = 00:00:36 ; elapsed = 00:00:41 . Memory (MB): peak = 597.215 ; gain = 390.074

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start Technology Mapping

INFO: [Synth 8-4480] The timing for the instance RAM_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

Finished Technology Mapping : Time (s): cpu = 00:00:36 ; elapsed = 00:00:41 . Memory (MB): peak = 597.215 ; gain = 390.074

Finished Parallel Technology Mapping Optimization : Time (s): cpu = 00:00:36 ; elapsed = 00:00:41 . Memory (MB): peak = 597.215 ; gain = 390.074

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
Finished Parallel Synthesis Optimization : Time (s): cpu = 00:00:36 ; elapsed = 00:00:41 . Memory (MB): peak = 597.215 ; gain = 390.074

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:37 ; elapsed = 00:00:42 . Memory (MB): peak = 597.215 ; gain = 390.074

Report Check Netlist:
+------+-----------------+-------+---------+-------+-----------------+
| |Item |Errors |Warnings |Status |Description |
+------+-----------------+-------+---------+-------+-----------------+
|1 |multi_driven_nets | 0| 0|Passed |Multi driven nets |
+------+-----------------+-------+---------+-------+-----------------+

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:37 ; elapsed = 00:00:42 . Memory (MB): peak = 597.215 ; gain = 390.074

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |

```
+-+--------------+------------+----------+
+-+--------------+------------+----------+
```

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:37 ; elapsed = 00:00:42 . Memory (MB): peak = 597.215 ; gain = 390.074

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:37 ; elapsed = 00:00:43 . Memory (MB): peak = 597.215 ; gain = 390.074

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:37 ; elapsed = 00:00:43 . Memory (MB): peak = 597.215 ; gain = 390.074

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:37 ; elapsed = 00:00:43 . Memory (MB): peak = 597.215 ; gain = 390.074

Start Writing Synthesis Report

Report BlackBoxes:

```
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+
```

Report Cell Usage:

```
+------+---------+------+
|      |Cell     |Count |
+------+---------+------+
```

```
|1    |BUFG     |     1|
|2    |CARRY4   |    22|
|3    |LUT1     |    65|
|4    |LUT2     |    22|
|5    |LUT3     |    37|
|6    |LUT4     |    43|
|7    |LUT5     |    44|
|8    |LUT6     |    59|
|9    |RAMB18E1 |     1|
|10   |FDRE     |   100|
|11   |FDSE     |     2|
|12   |IBUF     |    13|
|13   |OBUF     |    19|
+------+---------+------+

Report Instance Areas:
+------+---------+-----------------+------+
|      |Instance |Module           |Cells |
+------+---------+-----------------+------+
|1    |top      |                 |   428|
|2    |  mem    |memory           |     1|
|3    |  D      |Debounce         |    89|
|4    |    C    |clockDivider_0   |    78|
|5    |  ctrl   |controller       |   304|
|6    |    C    |clockDivider     |    78|
|7    |    S    |SevenSeg_Display |    13|
+------+---------+-----------------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:37 ; elapsed = 00:00:43 . Memory
(MB): peak = 597.215 ; gain = 390.074
--------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:22 ; elapsed = 00:00:31 . Memory (MB):
peak = 597.215 ; gain = 101.781
Synthesis Optimization Complete : Time (s): cpu = 00:00:38 ; elapsed = 00:00:43 . Memory
(MB): peak = 597.215 ; gain = 390.074
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 36 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 2 inverter(s) to 38 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
```

INFO: [Common 17-83] Releasing license: Synthesis
33 Infos, 6 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:37 ; elapsed = 00:00:40 . Memory (MB): peak = 597.215 ; gain = 390.074
report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.031 . Memory (MB): peak = 597.215 ; gain = 0.000
INFO: [Common 17-206] Exiting Vivado at Mon Apr 10 18:48:49 2017...