BeMicro Max 10 FPGA Evaluation Kit

Empty Baseline Project

Version 14.0.2 **10/15/2014** **Example Design**

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1. OVERVIEW

BeMicro Max 10 is a FPGA evaluation kit that is designed to get you started with using an FPGA. BeMicro Max 10 adopts Altera's non-volatile **MAX® 10 FPGA** built on 55-nm flash process.

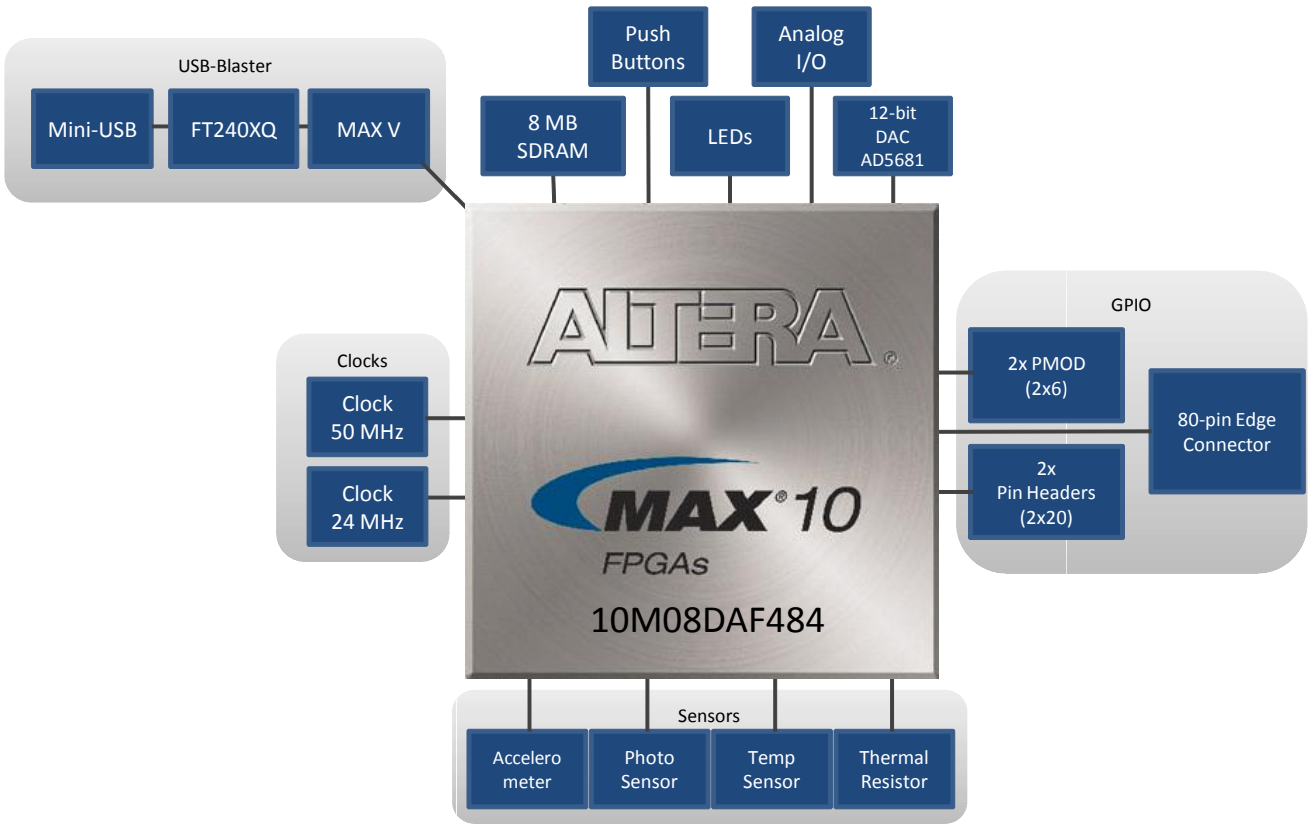
MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor programmable logic device. The devices also include full-featured FPGA capabilities such as digital signal processing, analog functionality, Nios II embedded processor support and memory controllers.

The BeMicro Max 10 includes a variety of peripherals connected to the FPGA device, such as 8MB SDRAM, accelerometer, digital-to-analog converter (DAC), temperature sensor, thermal resistor, photo resistor, LEDs, pushbuttons and several different options for expansion connectivity.

1.1 Block Diagram

Below is a block diagram of the board.

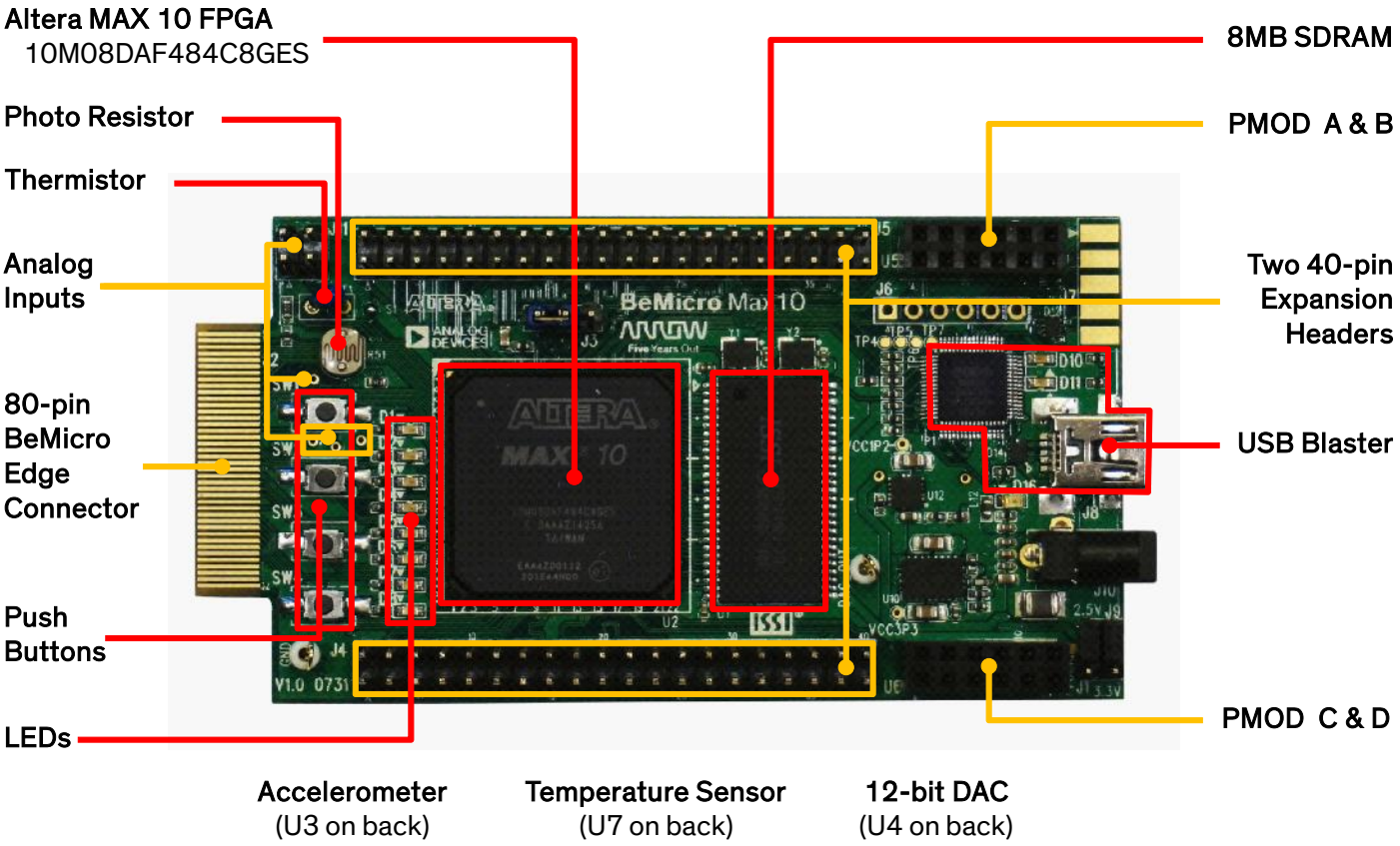
Figure 1-1: BeMicro Max 10 Block Diagram



1.2 Getting To Know Your Kit

Below is an annotated photo of the board to help you get familiar with the kit and locate the various peripherals and expansion connectors.

Figure 1-2: BeMicro Max 10 Development Kit



2. PINOUT INFORMATION FOR MAX 10 FPGA I/O

The BeMicro Max 10 contains a variety of external peripheral devices and expansion headers connected to the MAX 10 FPGA's configurable I/O pins. The details of the board circuitry and these connections can be found in the schematic files included in the MAX 10 FPGA files. (Refer to Section **Error! Reference source not found.** for details on extracting these files.) This section presents the information in the schematic organized into pinout tables by peripheral. While the schematic provides a board level view of all the pins for a given connector or peripherals, the tables in this section focus on the FPGA signals needed for FPGA pin assignment and compilation.

The "Signal Name" column in the tables throughout this section indicates the naming of the signal in the Quartus projects' QSF[1] file provided in the baseline Quartus project.

2.1 Analog Devices External Peripherals

2.1.1 Accelerometer, 3-Axis, SPI interface (ADXL362)

Signal Name	*MAX 10 Pin*
ADXL362_CS	L14
ADXL362_INT1	M15
ADXL362_INT2	M14
ADXL362_MISO	L18
ADXL362_MOSI	L19
ADXL362_SCLK	M18

2.1.2 DAC, 12-bit, SPI interface (AD5681)

Signal Name	*MAX 10 Pin*
AD5681R_LDACn	N18
AD5681R_RSTn	L15
AD5681R_SCL	G17
AD5681R_SDA	H17
AD5681R_SYNCn	N19

[1] A "QSF file" is a Quartus Settings File, a file with extension of *.qsf in which Quartus stores all project settings, including device pin assignments.

2.1.3 Temperature sensor, I2C interface (ADT7420)

Signal Name	MAX 10 Pin
ADT7420_CT	P13
ADT7420_INT	AB14
ADT7420_SCL	W13
ADT7420_SDA	R13

2.2 External Memory Devices

2.2.1 8MB SDRAM

The BeMicro Max 10 contains an ISSI IS42S16400J-7TL SDRAM device , which is connected to the MAX 10 FPGA and provides 8MB of memory which can be accessed by an FPGA design.

Signal Name	MAX 10 Pin
SDRAM_A[0]	T20
SDRAM_A[1]	T19
SDRAM_A[2]	T18
SDRAM_A[3]	AA21
SDRAM_A[4]	AA22
SDRAM_A[5]	U22
SDRAM_A[6]	T22
SDRAM_A[7]	R22
SDRAM_A[8]	P20
SDRAM_A[9]	P22
SDRAM_A[10]	U21
SDRAM_A[11]	P19
SDRAM_A[12]	N20
SDRAM_BA[0]	R20
SDRAM_BA[1]	T21
SDRAM_CASn	N21
SDRAM_CKE	N22
SDRAM_CLK	M22
SDRAM_CSn	P21
SDRAM_DQ[0]	C22
SDRAM_DQ[1]	D22
SDRAM_DQ[2]	E22
SDRAM_DQ[3]	F22
SDRAM_DQ[4]	G22
SDRAM_DQ[5]	H22
SDRAM_DQ[6]	J22
SDRAM_DQ[7]	K22

Signal Name	MAX 10 Pin
SDRAM_DQ[8]	K21
SDRAM_DQ[9]	J21
SDRAM_DQ[10]	H21
SDRAM_DQ[11]	G20
SDRAM_DQ[12]	F21
SDRAM_DQ[13]	E21
SDRAM_DQ[14]	D21
SDRAM_DQ[15]	C21
SDRAM_DQMH	L22
SDRAM_DQML	L20
SDRAM_RASn	M20
SDRAM_WEn	M21

2.2.2 Serial Flash, 16 Mbit

The BeMicro MAX 10 contains a 16 Mbit SPI-interface serial NOR flash device, Micron M25P16-VMN6, which can be used for off-chip storage in case a design's flash storage needs are larger than the internal MAX 10 FPGA User Flash Memory (UFM).

Signal Name	MAX 10 Pin
SFLASH_ASDI	R11
SFLASH_CSn	R10
SFLASH_DATA	P10
SFLASH_DCLK	P11

2.3 User Interaction

2.3.1 LEDs

Board Label	Signal Name	MAX 10 Pin
D1	USER_LED[1]	M2
D2	USER_LED[2]	N1
D3	USER_LED[3]	R2
D4	USER_LED[4]	T1
D5	USER_LED[5]	V4
D6	USER_LED[6]	T6
D7	USER_LED[7]	AB4
D8	USER_LED[8]	AA5

2.3.2 Push Buttons

Board Label	Signal Name	MAX 10 Pin
SW1	PB[1]	M1
SW2	PB[2]	R1
SW3	PB[3]	V5
SW4	PB[4]	AB5

2.4 MAX 10 FPGA Analog Inputs

2.4.1 Analog Input Header

One of the key features of the MAX 10 FPGA is the analog block. Connector J11 can be used to attach input signals to the MAX 10 FPGA device. The signals coming from the connector pass through a signal conditioning RC circuit and then are fed into the analog input pins of the MAX 10 FPGA device.

Signal Name	MAX 10 Pin	MAX 10 ADC channel number	Board Connection Point
AIN[0]	F5	Ch. 1	2x2 header J11, pin 1
AIN[1]	E4	Ch. 9	2x2 header J11, pin 2
AIN[2]	F4	Ch. 2	testpoint TP12 (silkscreen “AIN3” on back)
AIN[3]	E3	Ch. 16	testpoint TP13 (silkscreen “AIN4” on back)
AIN[4]	J8	Ch. 3	testpoint TP15 (silkscreen “AIN5” on back)
AIN[5]	G4	Ch. 11	testpoint TP14 (silkscreen “AIN6” on back)

2.4.2 Photo Resistor

In addition, the BeMicro Max 10 board contains a photo resistor attached to one of the analog input pins of the MAX 10 FPGA device.

Signal Name	MAX 10 Pin	MAX 10 ADC channel number
AIN[6]	J9	Ch. 4

2.4.3 Thermistor (Thermal Resistor)

The BeMicro Max 10 board also contains a thermistor attached to one of the analog input pins of the MAX 10 FPGA device.

Signal Name	MAX 10 Pin	MAX 10 ADC channel number
AIN[7]	F3	Ch. 12

2.5 Expansion Headers and Connectors

2.5.1 BeMicro Edge Connector

The BeMicro Max 10 contains the same 80-pin edge connector used on previous BeMicro kits such as the BeMicro CV and the BeMicro SDK. A Samtec connector part number MEC6-140-02-X-D-RA1 can be used to mate to this edge connector.

Signal Name	*MAX 10 Pin*
EG_P1	C1
EG_P2	D2
EG_P3	D1
EG_P4	D3
EG_P5	E1
EG_P6	F2
EG_P7	F1
EG_P8	G1
EG_P9	H1
EG_P10	J1
EG_P11	K2
EG_P12	L2
EG_P13	N2
EG_P14	P3
EG_P15	P1
EG_P16	R3
EG_P17	T2
EG_P18	R4
EG_P19	T5
EG_P20	Y1
EG_P21	Y2
EG_P22	AA1
EG_P23	AA2
EG_P24	Y3
EG_P25	Y4
EG_P26	AB6
EG_P27	AB7
EG_P28	AA8
EG_P29	AB8

Signal Name	*MAX 10 Pin*
EG_P35	E11
EG_P36	E10
EG_P37	D9
EG_P38	E9
EG_P39	E8
EG_P40	D8
EG_P41	E6
EG_P42	D7
EG_P43	C8
EG_P44	C7
EG_P45	D6
EG_P46	C6
EG_P47	D5
EG_P48	C5
EG_P49	C4
EG_P50	H11
EG_P51	J10
EG_P52	M9
EG_P53	M8
EG_P54	N9
EG_P55	N8
EG_P56	N5
EG_P57	N4
EG_P58	N3
EG_P59	P5
EG_P60	P4
EXP_PRESENT	R5
RESET_EXPn	C2

2.5.2 Two 40-pin Expansion Headers

Two 40-pin prototyping headers, J3 and J4, provide access to single ended digital signals. The pinout for these connectors match the pinout of several daughter cards available from third-party vendors such as Terasic. Please note

that there are Terasic daughter cards containing differential LVDS transmit pairs and differential receive pairs, which can be used with the BeMicro MAX 10; however, to use the differential signaling, there are guidelines regarding neighboring pins that must be followed. Please refer to the "Using LVDS on the BeMicro MAX 10" document for details.

Signal Name	*MAX 10 Pin*	*J3 Pin*
GPIO_01	B2	1
GPIO_02	B1	2
GPIO_03	C3	3
GPIO_04	A2	4
GPIO_05	B3	5
GPIO_06	A3	6
GPIO_07	B4	7
GPIO_08	A4	8
GPIO_09	B5	9
GPIO_10	A5	10
GPIO_11	B7	13
GPIO_12	A6	14
GPIO_J3_15	A7	15
GPIO_J3_16	A8	16
GPIO_J3_17	A9	17
GPIO_J3_18	B8	18
GPIO_J3_19	B10	19
GPIO_J3_20	C9	20
GPIO_J3_21	H12	21
GPIO_J3_22	J11	22
GPIO_J3_23	E12	23
GPIO_J3_24	D13	24
GPIO_J3_25	D14	25
GPIO_J3_26	E13	26
GPIO_J3_27	A14	27
GPIO_J3_28	B14	28
GPIO_J3_31	C14	31
GPIO_J3_32	C13	32
GPIO_J3_33	H14	33
GPIO_J3_34	J13	34
GPIO_J3_35	D17	35
GPIO_J3_36	C17	36
GPIO_J3_37	E16	37
GPIO_J3_38	E15	38
GPIO_J3_39	K14	39
GPIO_J3_40	K15	40

Signal Name	*MAX 10 Pin*	*J4 Pin*
I2C_SDA	AA14	3
I2C_SCL	AB15	4
GPIO_A	AA15	5
GPIO_B	Y16	6
GPIO_J4_11	W3	11
GPIO_J4_12	W4	12
GPIO_J4_13	W6	13
GPIO_J4_14	W5	14
GPIO_J4_15	U7	15
GPIO_J4_16	U6	16
GPIO_J4_19	W8	19
GPIO_J4_20	W7	20
GPIO_J4_21	AA7	21
GPIO_J4_22	AA6	22
GPIO_J4_23	V10	23
GPIO_J4_24	V9	24
GPIO_J4_27	AA10	27
GPIO_J4_28	Y10	28
GPIO_J4_29	Y14	29
GPIO_J4_30	Y13	30
GPIO_J4_31	W14	31
GPIO_J4_32	V13	32
GPIO_J4_35	W15	35
GPIO_J4_36	V14	36
GPIO_J4_37	V16	37
GPIO_J4_38	U15	38
GPIO_J4_39	V17	39
GPIO_J4_40	W17	40

2.5.3 PMOD™ Connectors

The BeMicro MAX 10 provides two 2x6 female PMOD™ connectors, labeled as U5 & U6. PMODs are small I/O interface boards that offer an ideal way to extend the capabilities of our FPGA/CPLD and embedded control board. More information and examples can be found online at: www.digilent.com/pmods.

Signal Name	*MAX 10 Pin*
PMOD_A[0]	C20
PMOD_A[1]	D19
PMOD_A[2]	D18
PMOD_A[3]	E18

Signal Name	*MAX 10 Pin*
PMOD_B[0]	E19
PMOD_B[1]	F18
PMOD_B[2]	F20
PMOD_B[3]	G19

Signal Name	*MAX 10 Pin*
PMOD_C[0]	U18
PMOD_C[1]	U17
PMOD_C[2]	R18
PMOD_C[3]	P18

Signal Name	*MAX 10 Pin*
PMOD_D[0]	R14
PMOD_D[1]	R15
PMOD_D[2]	P15
PMOD_D[3]	P14

2.6 Clock Inputs

The clocking on the BeMicro Max 10 is provided by a 50 MHz oscillator and a 24 MHz oscillator, which connect to the MAX 10 FPGA's clock input pins. The 50 MHz clock input is used in many of the example designs as the primary "system" clock. The 24 MHz is provided as an optional secondary clock source for user designs.

Signal Name	*MAX 10 Pin*	*Description*
SYS_CLK	N14	50 MHz "System" Clock Input
USER_CLK	N15	24 MHz "User" Clock Input