BeMicro Max 10 FPGA Evaluation Kit

Dual Boot Demo

Version 14.0 **10/7/2014** **User Guide**

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1. DUAL BOOT DEMO

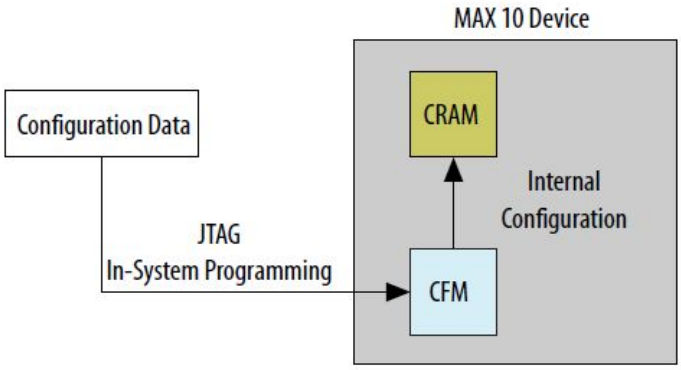
The MAX 10 devices use internal configuration mode to support dual image boot.

Jumper J3 is used to strap the MAX 10 FPGA device's BOOT_SEL pin. The 10M08 device supports holding two FPGA images is its Configuration Flash Memory. The BOOT_SEL pin can be used to allow the user to select which image is loaded by default on power up.

1.1 What is Internal Configuration?

Internal Configuration

Figure 2-1: High-Level Overview of Internal Configuration for MAX 10 Devices



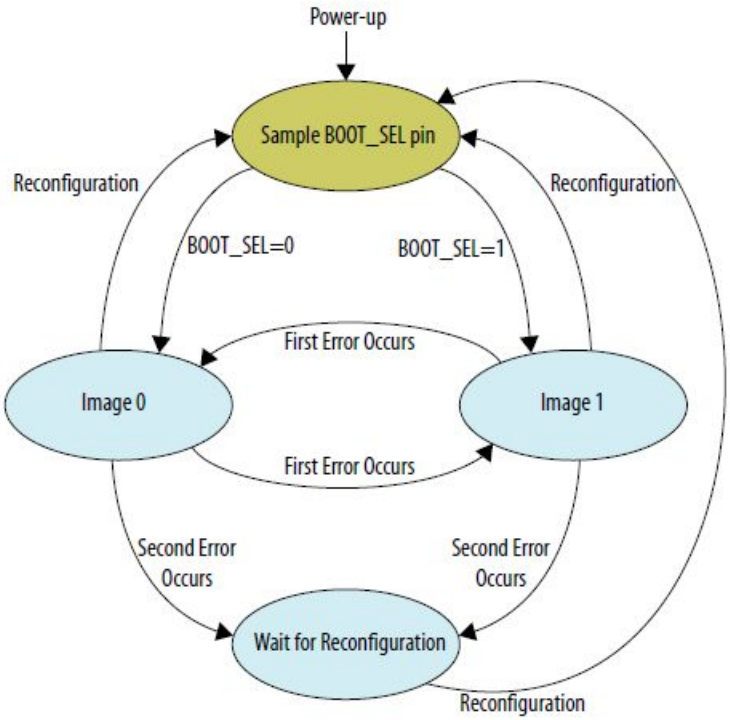
Before internal configuration, you need to program the configuration data into the configuration flash memory (CFM). The CFM will be part of the programmer object file (.pof) programmed into the internal flash through the JTAG In-System Programming (ISP).During internal configuration, MAX 10 devices load the configuration RAM (CRAM) with configuration data from the CFM.

The internal configuration scheme for all MAX 10 devices except for 10M02 consists of the following mode:

- Dual Compressed Images—configuration image is stored as image 0 and image 1 in the CFM
- Single Compressed Image
- Single Compressed Image with Memory Initialization
- Single Uncompressed Image
- Single Uncompressed Image with Memory Initialization

In dual compressed images mode, you can use the BOOT_SEL pin to select the configuration image.

Figure 2-3: Remote System Upgrade Flow for MAX 10 Devices



The operation of the remote system upgrade feature detecting errors is as follows:

1. After power-up, the device samples the BOOT_SEL pin to determine which application configuration image to boot. The BOOT_SEL pin setting can be overwritten by the input register of the remote system upgrade circuitry for the subsequent reconfiguration.

2. If an error occurs, the remote system upgrade feature reverts by loading the other application configuration image. The following lists the errors that will cause the remote system upgrade feature to load another application configuration image:

• Internal CRC error

• User watchdog timer time-out

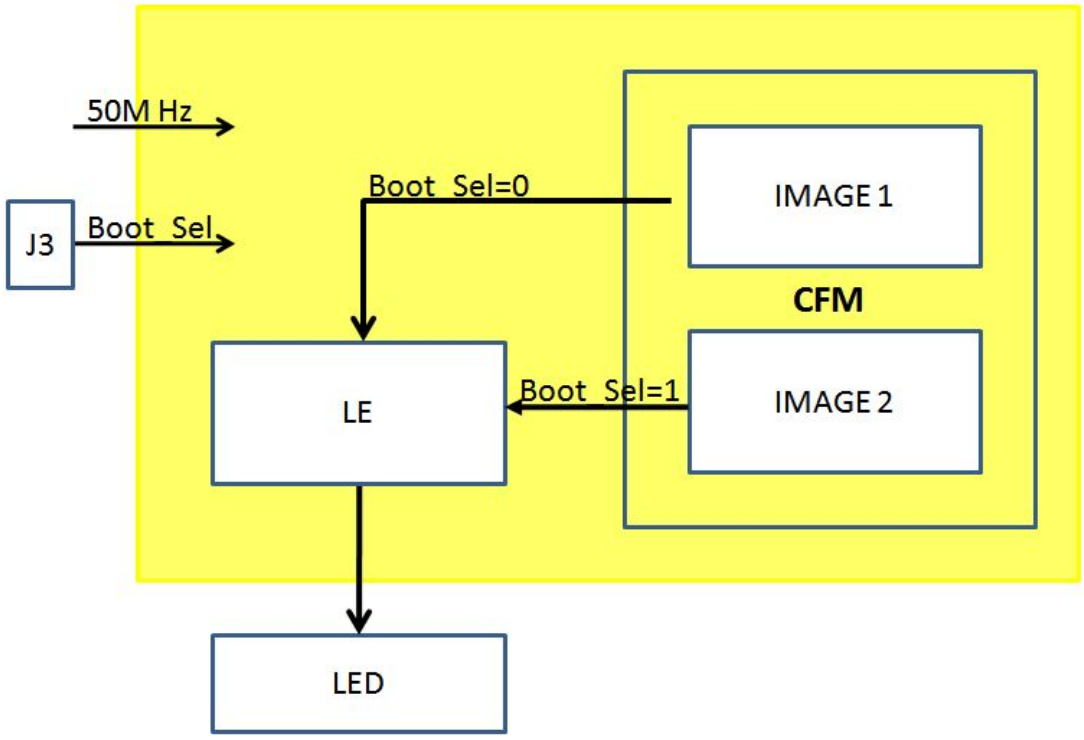
3. Once the revert configuration completes and the device is in the user mode, you can use the remote system upgrade circuitry to query the cause of error and which application image failed.

4. If a second error occurs, the device waits for a reconfiguration source. If the auto-reconfig is enabled, the device will reconfigure without waiting for any reconfiguration source.

5. Reconfiguration is triggered by the following actions:

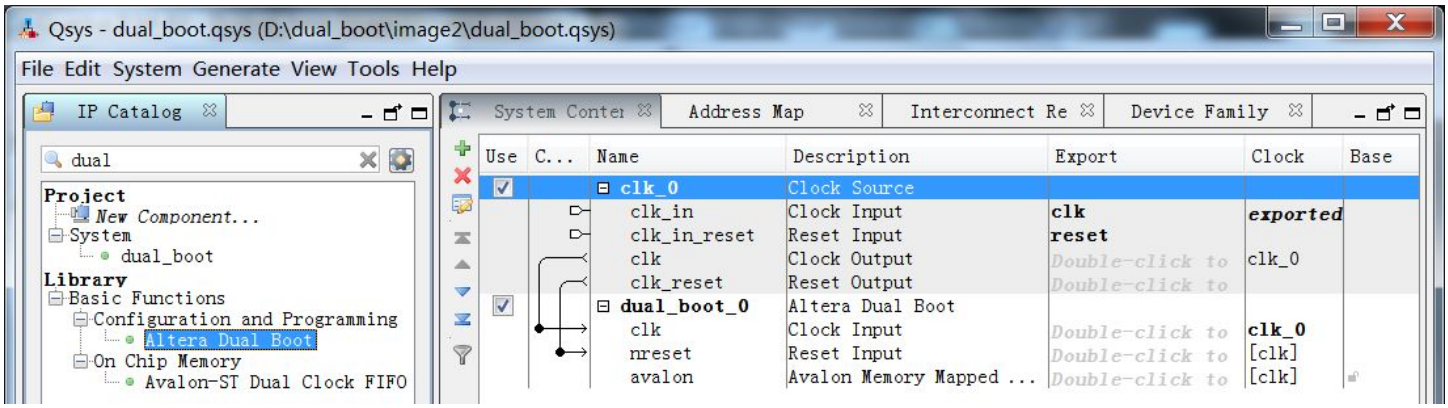
- Driving the nSTATUS low externally
- Asserting internal or external nCONFIG low
- Asserting RU_nCONFIG low

1.2 Dual Boot demo simple chart

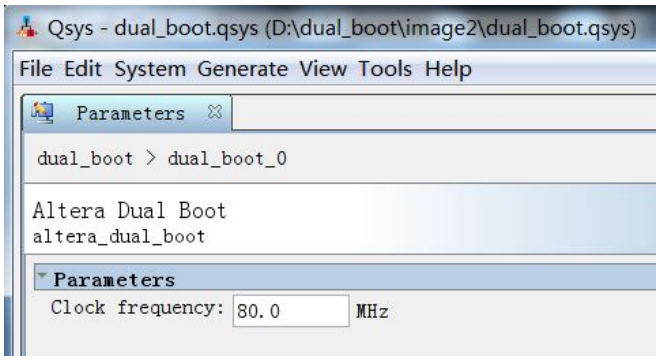


1.3 Dual Boot IP

Add Dual Boot in Qsys and connect the clock and reset signal



set the clock frequency, must below 80.0 MHz



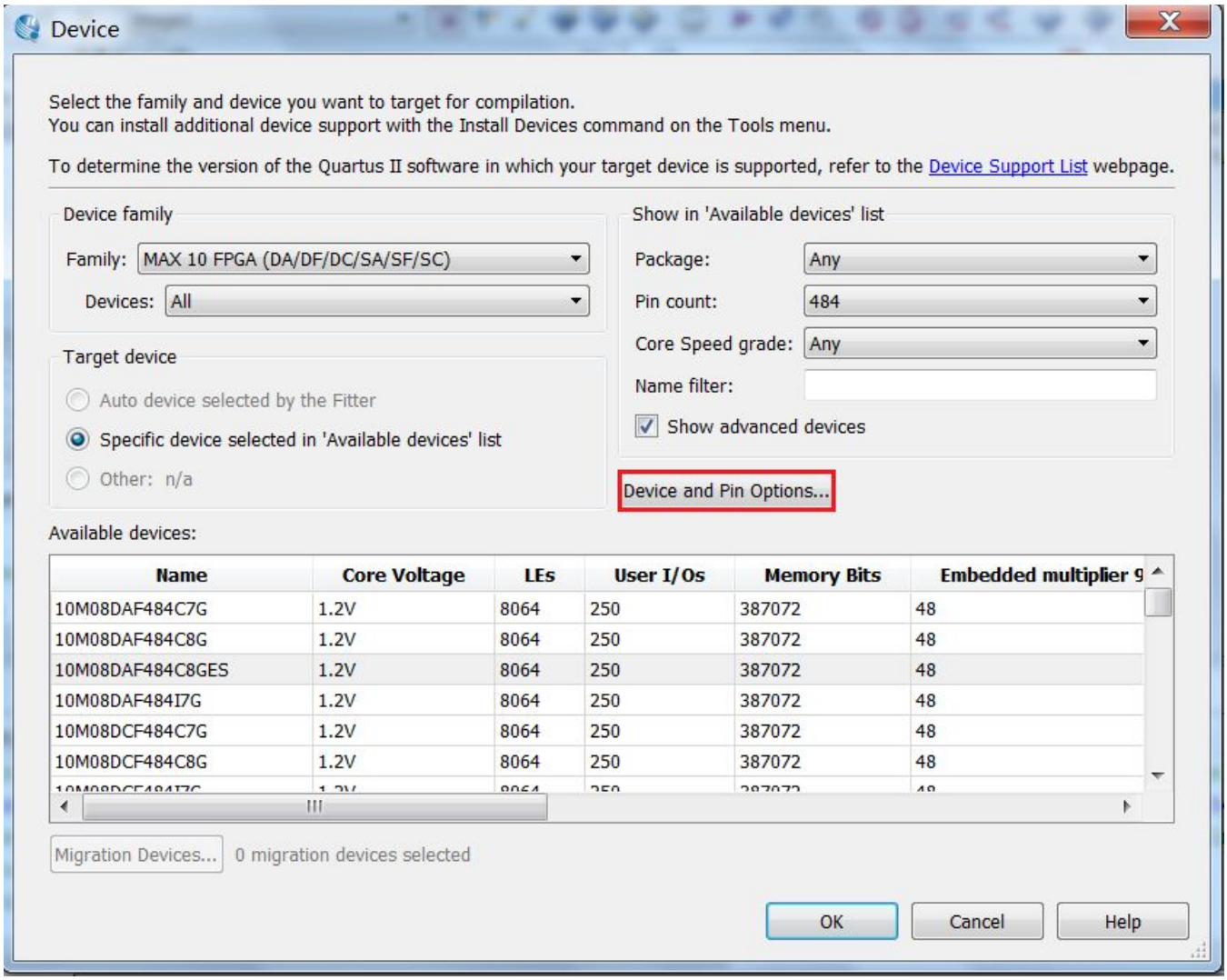
About the Altera Dual Boot IP

Altera Dual Boot IP Core Parameters

Table 5-2: Altera Dual Boot IP Core Parameter for MAX 10

Parameter	Value	Description
Clock frequency	Up to 80MHz	Specifies the number of cycle to assert RU_nRSTIMER and RU_nCONFIG signals. Note that maximum RU_CLK is 40Mhz, Altera Dual Boot IP Core has restriction to run at 80Mhz maximum, which is twice faster than hardware limitation. This is because Altera Dual Boot IP Core generate RU_CLK at half rate of the input frequency.

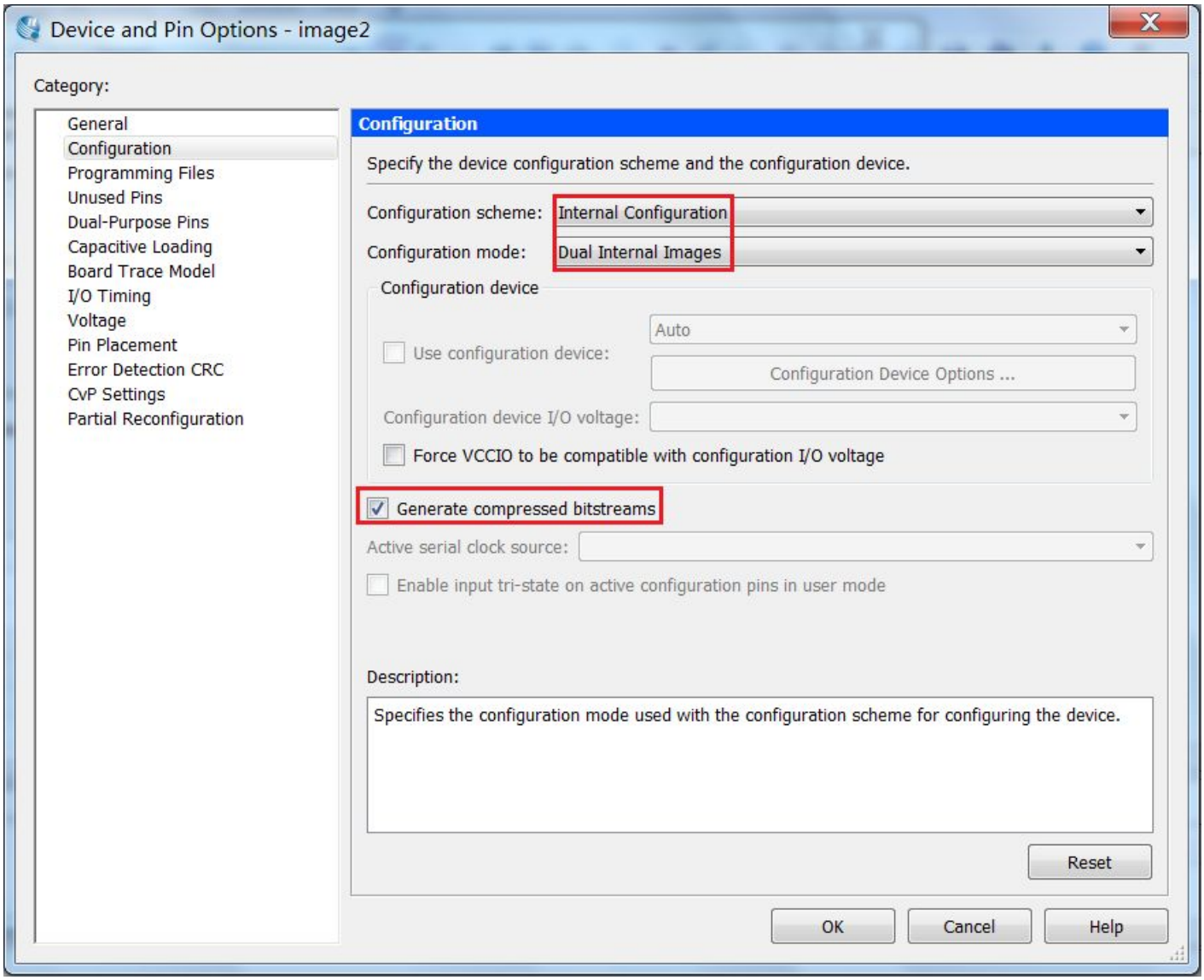
Set the Dual boot option for current project, select Device and Pin Options in Device Option



Set the Configuration Scheme to Internal Configuration.

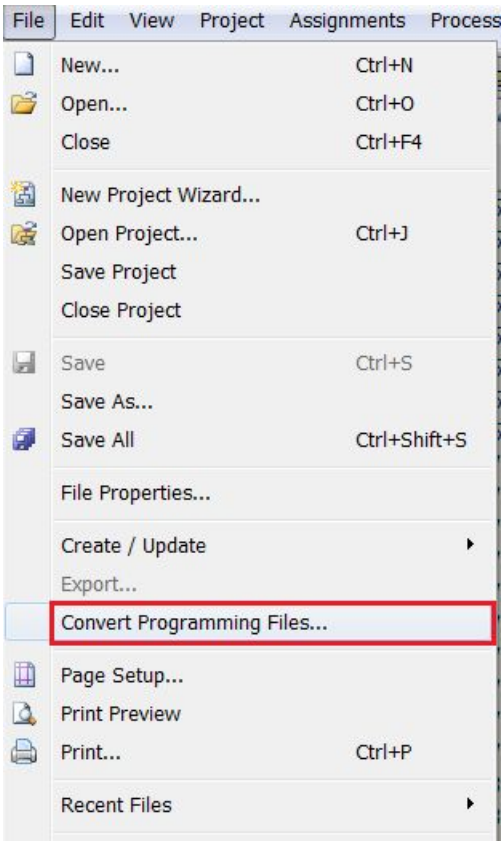
Set the Configuration Mode to Dual Internal Images.

Check the Option of Generate compressed bitstreams.

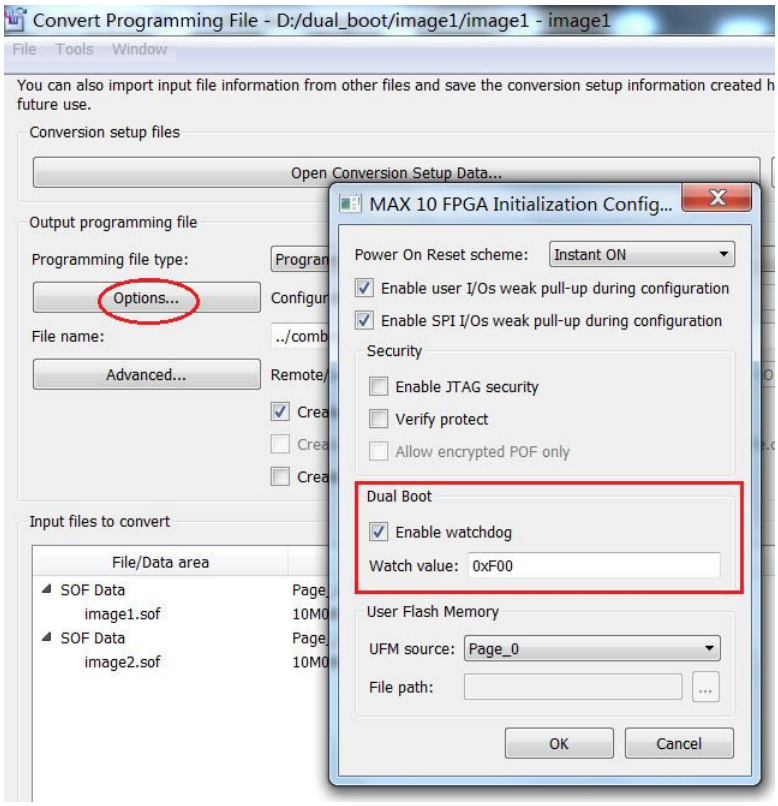


After you obtain the first image file, such as image1.sof, and the second image file, such as image2.sof, you can combine them into one POF file in Quartus.

Use the Covert Programming File menu.



Pay attention to the Options, you can set the watchdog value.



1.4 How to Use the Watchdog Timer

The user watchdog timer prevents a faulty application configuration from stalling the device indefinitely. You can use the timer to detect functional errors when an application configuration is successfully loaded into the device.

The counter is 29 bits wide and has a maximum count value of 229. When specifying the user watchdog timer value, specify only the most significant 12 bits. The granularity of the timer setting is 217 cycles. The cycle time is based on the frequency of the user watchdog timer internal oscillator. Depending on the counter and the internal oscillator of the device, you can set the cycle time from 17ms to 243s.

The timer begins counting as soon as the application configuration enters user mode. When the timer expires, the remote system upgrade circuitry generates a time-out signal, updates the status register, and triggers the loading of the revert configuration image. To reset the timer, pulse the RU_NRSTIMER for a minimum of 250 ns.

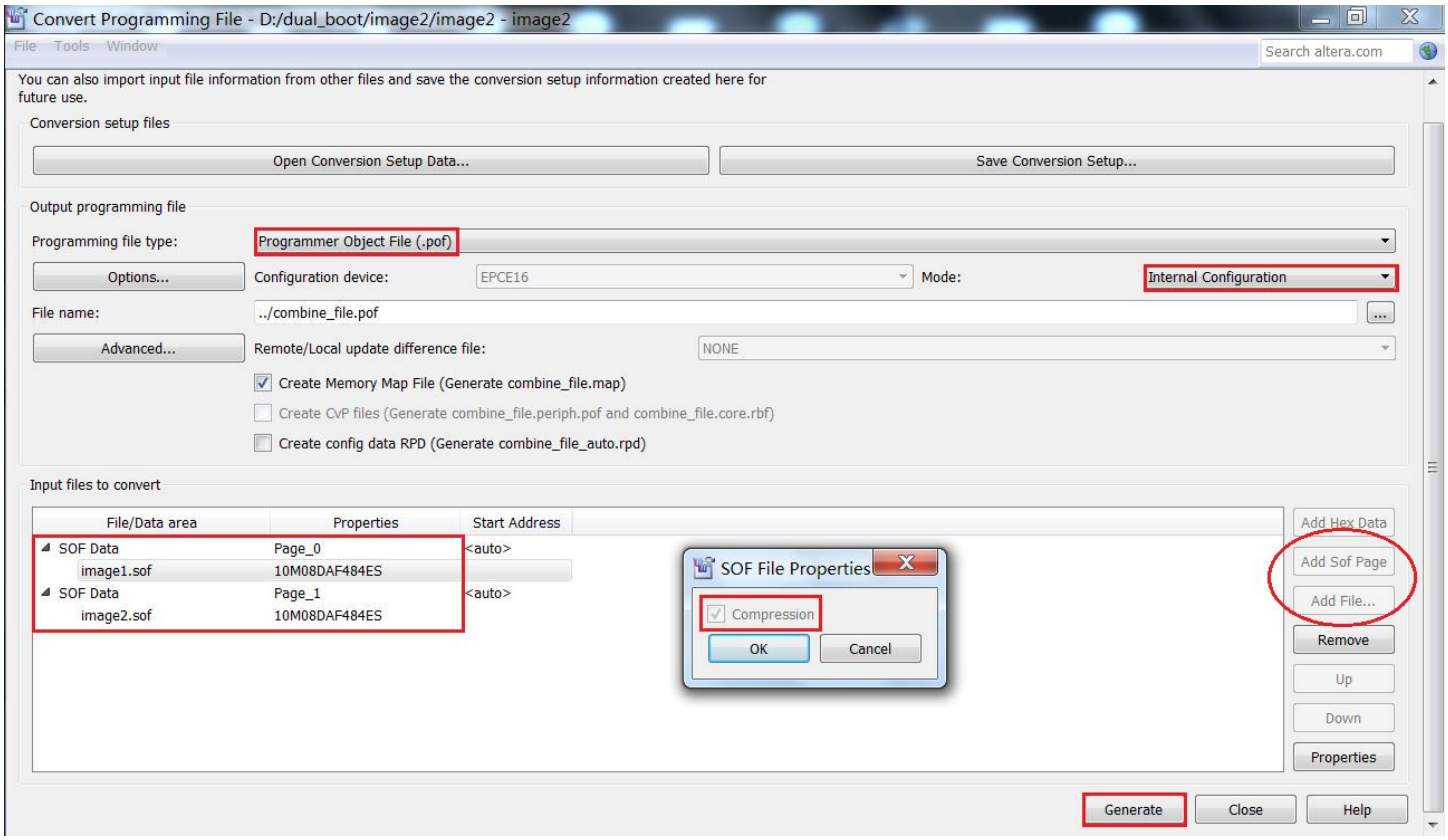
If the watchdog timer is enabled, this setting will apply to all images, all images should contain the soft logic configuration to reset the timer. Application Configuration will reset the control block registers.

Add two Sof Page for the two image, add image1.sof below the Page_0, add image2.sof below the Page_1.

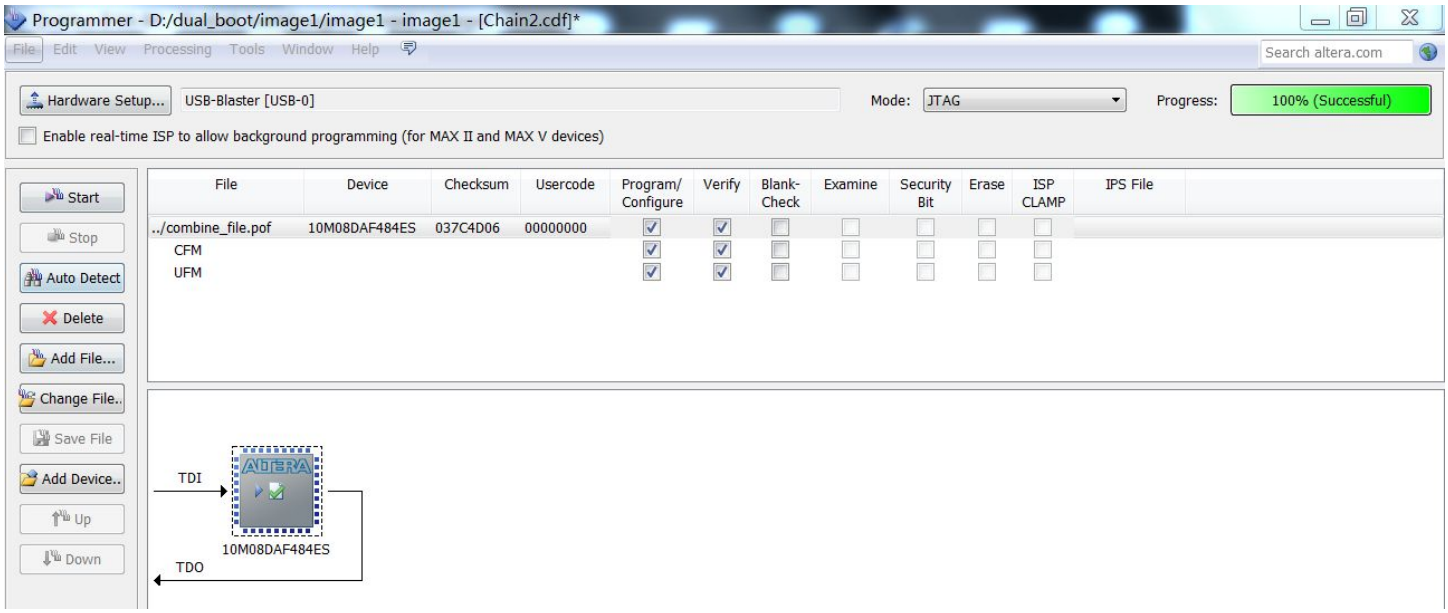
We need select the Programming file type to .pof, and set the Mode to Internal Configration.

Notice that the compression options is checked by default in the SOF File Properties option.

Press the Generate button, you can combine two program file into one POF file and output the file.



After you have the pof file, you can use programmer to program it into CFM of MAX10 directly now.



Now, you can set the BOOT_SEL by JP3, you will find if you set BOOT_SEL=0, the image1 functions would show.

Power down the board, set BOOT_SEL=1, then Power on, you would find the image2 functions show.

When you change the Jumper of J3, you need power off the board.