

# José Hiram Soltren

1201 West Park Street, Cedar Park, TX 78613-2801, United States

✉ jsoltren@alum.mit.edu ☎ +1 (347) 503-9558 🌐 <https://www.linkedin.com/in/jsoltren>

SYNOPSIS	Staff/Principal Software Engineer. Instrument Rated Commercial Pilot. MIT Alum. Seeking Firmware, Quant Dev, Algo Trading, Scientific Computing, Infra roles. <i>Expert in C, C++, systems, Linux, device drivers, hardware accelerators.</i>	
EXPERIENCE	<b>Team Lead/Manager, Build and Release Roku</b>	Jan 2023 - Sep 2023
	<ul style="list-style-type: none"><li>• Responsible for official build, release, and CI infrastructure.</li><li>• Led team of four to implement self-service efforts, reducing ticket counts by 30% while improving turnaround time and throughput.</li><li>• Co-led pre merge CI for Roku firmware. Presented at IEEE ICST 2023.</li></ul>	
	<b>Senior Software Engineer, Roku Players Roku</b>	Jun 2020 - Dec 2022
	<ul style="list-style-type: none"><li>• Software lead for YouTube certification for three generations of player platforms.</li><li>• Software lead and hardware co-lead for Roku Streaming Stick 4K. Solved numerous hardware and software issues to unblock 20M unit program.</li><li>• C++20 based firmware development with a special focus on video decode.</li><li>• Authored a video capture tool widely used by external vendors and internal QA.</li></ul>	
	<b>Deep Learning Software Engineer Nervana / Intel Corp.</b>	Aug 2017 - Feb 2019
	<ul style="list-style-type: none"><li>• Driver development for “Lake Crest”. 10 MLOC multithreaded templated C++11.</li><li>• Ran comparisons, benchmarks, and projections for different numerical formats on novel hardware accelerator for AI deep learning training, e.g. ResNet.</li><li>• Focus on hardware and software to run GEMM and convolution as fast as possible.</li><li>• Designed an algorithm for all-to-all data transfers on our hardware that beat the Bruck Algorithm, the fastest general purpose algorithm.</li><li>• Wrote accelerator kernels for matrix multiplication and multi-chip communication.</li><li>• Implemented support for running multiple jobs on a single chip.</li><li>• Consolidated HW initialization and management for increased perf and simpler code.</li></ul>	
	<b>Software Engineer Cloudera, Inc.</b>	May 2016 - Aug 2017
	<ul style="list-style-type: none"><li>• Hacking on Apache Spark, a big data computation framework written in Scala.</li></ul>	
	<b>Senior System Software Engineer NVIDIA Corporation</b>	May 2011 - Apr 2016
EDUCATION	<ul style="list-style-type: none"><li>• Software dev on 50 MLOC multithreaded C99/C++98 graphics/OpenGL driver.</li><li>• Video decode and post-processing technical lead. Added H.265/HEVC decode support to VDPAU. Wrote stream parser for H.265/HEVC video streams.</li><li>• Fixed hundreds of bugs, including a GPU crash when playing certain videos, and a race condition in the driver when initializing multiple GPUs.</li><li>• Wrote a custom debugger to use hardware watch points to catch data races without perturbing timing.</li></ul>	
	<b>Massachusetts Institute of Technology, Cambridge, MA</b>	
	<i>Master of Engineering and S.B., Electrical Engineering and Computer Science</i>	
	Grad level operating systems course. Build a kernel and hypervisor in C. Lab assistant for undergraduate microcontroller/firmware course.	
CITIZENSHIP	United States	