

José Hiram Soltren

1201 West Park Street, Cedar Park, TX 78613-2801

✉ jsoltren@alum.mit.edu ☎ +1 (347) 503-9558 🌐 <https://www.linkedin.com/in/jsoltren>

SYNOPSIS

System Software Engineer and MIT alum. **Ten years' experience** in various areas: Linux, kernel development, device drivers, computer graphics, firmware, video decoding, end user software, systems administration, Apache Spark. *Additional specialties: aviation, machining, CAD/CAM, mechanical keyboards.*

EXPERIENCE

Software Engineer

Intel Corporation, Austin, TX (work from home)

2017-

- Software development work on Intel's Nervana Neural Network Processor (NNP) in the Artificial Intelligence Product Group (AIPG).
- Focus on NNP work to accelerate deep learning model training using a dedicated hardware accelerator for mathematical operations.
- Software and API architectural design and development for current and future NNP generation hardware.
- Focus on multiple chip workloads and topologies.
- Software implementation and bug fixing for various AI workloads.
- Performance estimation for workloads on current and future hardware.
- *Technologies used: C++11*

Software Engineer

Cloudera, Inc., Austin, TX (work from home)

2016-2017

- Engineering development work on Apache Spark, a distributed computation platform with fault tolerance billed as the successor to MapReduce.
- Worked on fault tolerance and reliability in Spark core code by working with colleagues to implement a blacklisting mechanism for faulty compute resources.
- Designed an addition to Apache Spark that would allow compute resources to report on memory utilization in real time.
- Worked with several teams to scope work needed to support hardware accelerators as first class citizens at deployment and execution time in Apache Spark.
- Worked with QA teams to design, implement, and adopt an internal fault injection framework for endurance and vulnerability testing on Apache Spark.
- Bug and feature work in Apache Spark. Worked on customer escalations.
- *Technologies used: Spark, Scala, Java, JVM, Python, Jenkins, git*

Senior System Software Engineer

NVIDIA Corporation, Santa Clara, CA and Austin, TX

2011-2016

- Firmware and device driver development for resource management, 2D graphics, 3D graphics, and accelerated video decode for NVIDIA desktop/mobile GPUs on Linux/UNIX hosts.
- Technical lead for VDPAU, the accelerated hardware video decoder stack on Linux.
- Technical lead for H.265/HEVC video decoder format implementation on Linux. Added hardware accelerated H.265/HEVC video playback support to the NVIDIA Linux driver stack. Wrote a simple stream parser to play H.265/HEVC video and released it under an open source license. <https://github.com/NVIDIA/vdpau-hevc-example>
- Worked with firmware, kernel, hardware, and ASIC engineers around the clock and around the world on FPGA Quickturn emulators to root cause and fix a critical, stop ship issue related to video decoding on Maxwell GPUs.

EXPERIENCE,
CONTINUED

- Refactored the NVIDIA Linux video decode driver stack to add hardware support for Maxwell and Pascal GPUs. Worked with firmware, hardware, and ASIC engineers to sort out hardware differences from previous generations.
- Rewrote video shaders used in the video decode pipeline from Cg into GLSL, allowing the video shaders to move to a leaner implementation using a new shader compiler.
- Fixed multiple bugs in the NVIDIA Linux driver graphics stack related to performance, system reliability, video quality, and memory economy.
- Served as technical mentor to several engineers over the years. Mentees have gone on to make substantial contributions to OpenGL, Vulkan, X.org, and the Linux kernel.
- *Technologies used: C, C++, OpenGL, Cg, GLSL, assembly (numerous variants), FPGA hardware emulation, Linux kernel, gdb, Perforce, git*

EDUCATION

Massachusetts Institute of Technology, Cambridge, MA

Master of Engineering, Electrical Engineering and Computer Science 2009

- Course work in operating systems, biomedical informatics, network protocols, scientific computation, signal processing, power electronics.
- Wrote thesis on using Semantic Web technologies to determine privacy policy compliance of database queries using a rules-based reasoner.

Bachelor of Science, Electrical Engineering and Computer Science 2007

- Minor in Science, Technology, and Society.

LANGUAGES

Fluent in: English, Spanish, C.
Proficient in: OpenGL, Java, JavaScript, R, C++, Scheme, Perl, Python, PHP, MATLAB, Cg, GLSL, CUDA.

CITIZENSHIP

United States