

Midterm 1 - tranj78

November 5, 2021 4:59 PM

1. Algebraic Manipulations and Transistors (32 Marks Total)

- a) Use algebraic manipulation to simplify the expression or prove equality, as required. At each step, state all axioms, theorems and properties used. Use labelling system provided at end of exam in Question 8.

i) (6 marks) $y_1 \bar{y}_2 \bar{y}_3 + \bar{y}_1 y_2 \bar{y}_3 + y_1 y_2 \bar{y}_3 + y_1 \bar{y}_2 y_3$
ii) (6 marks) $(y_1 + \bar{y}_2 + y_3)(y_1 + y_2 + \bar{y}_3)(\bar{y}_1 + \bar{y}_2 + \bar{y}_3)(y_1 + \bar{y}_2 + \bar{y}_3)$

i) $y_1 \bar{y}_2 \bar{y}_3 + \bar{y}_1 y_2 \bar{y}_3 + y_1 y_2 \bar{y}_3 + y_1 \bar{y}_2 y_3 \quad \langle 10b \rangle$

$\equiv y_1 \bar{y}_2 \bar{y}_3 + y_1 y_2 \bar{y}_3 + y_1 \bar{y}_2 \bar{y}_3 + \bar{y}_1 y_2 \bar{y}_3 \quad \langle 12a \rangle$

$\equiv y_1 \bar{y}_3 (\bar{y}_2 + y_2) + y_1 \bar{y}_2 y_3 + \bar{y}_1 y_2 \bar{y}_3 \quad \langle 9b \rangle$

$\equiv y_1 \bar{y}_3 + y_1 \bar{y}_2 y_3 + \bar{y}_1 y_2 \bar{y}_3 \quad \langle 10b \rangle$

$\equiv y_1 \bar{y}_3 + \bar{y}_1 y_2 \bar{y}_3 + y_1 \bar{y}_2 y_3 \quad \langle 12a \rangle$

$\equiv \bar{y}_3 (y_1 + \bar{y}_1 y_2) + y_1 \bar{y}_2 y_3 \quad \langle 16a \rangle$

$\equiv \bar{y}_3 (y_1 + y_2) + y_1 \bar{y}_2 y_3 \quad \langle 12a \rangle$

$\equiv \bar{y}_3 y_1 + \bar{y}_3 y_2 + y_1 \bar{y}_2 y_3 \quad \langle 10b \rangle$

$\equiv \bar{y}_3 y_1 + y_1 \bar{y}_2 y_3 + \bar{y}_3 y_2 \quad \langle 12a \rangle$

$\equiv y_1 (\bar{y}_3 + \bar{y}_2 y_3) + \bar{y}_3 y_2 \quad \langle 16a \rangle$

$\equiv y_1 (\bar{y}_3 + \bar{y}_2) + \bar{y}_3 y_2 \quad \langle 12a \rangle$

$\equiv y_1 \bar{y}_3 + y_1 \bar{y}_2 + \bar{y}_2 y_2 \quad \langle \text{consensus} \rangle$

$\equiv y_1 \bar{y}_2 + y_2 \bar{y}_3$

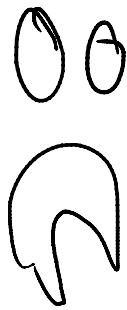
ii) $(y_1 + \bar{y}_2 + y_3)(y_1 + y_2 + \bar{y}_3)(\bar{y}_1 + \bar{y}_2 + \bar{y}_3)(y_1 + \bar{y}_2 + \bar{y}_3) \quad \langle 12.5 \rangle$

$\equiv (y_1 + ((\bar{y}_2 + y_3)(y_2 + \bar{y}_3)))((\bar{y}_2 + y_3)(\bar{y}_1 + y_1)) \quad \langle 9.b \rangle$

$\equiv (y_1 + ((\bar{y}_2 + y_3)(y_2 + \bar{y}_3)))((\bar{y}_2 + y_3)(1)) \quad \langle 6.a \rangle$

$\equiv (y_1 + ((\bar{y}_2 + y_3)(y_2 + \bar{y}_3)))(\bar{y}_2 + y_3)$

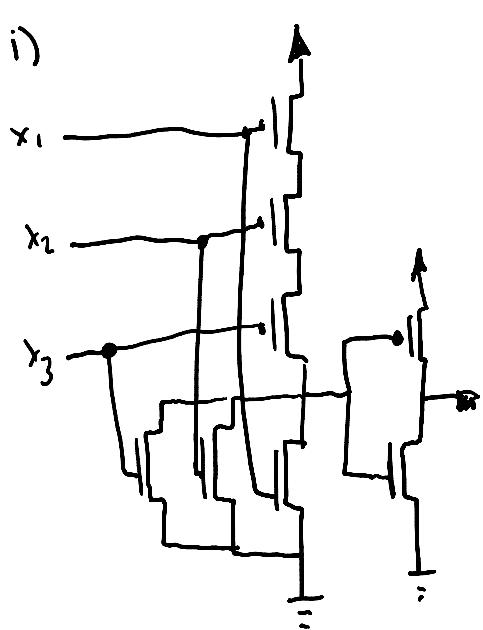
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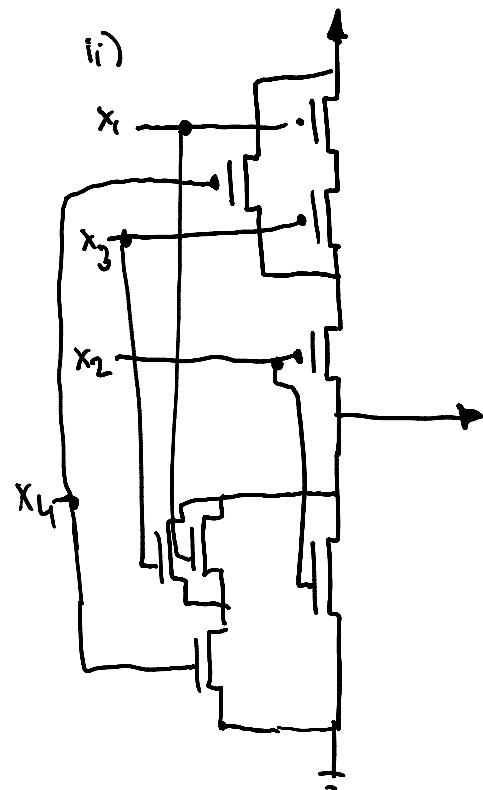
- b) Draw the transistor circuit diagram using the minimum number of transistors for the CMOS gates below.

i) (4 marks) A 3-input OR gate ($f = (x_1 + x_2 + x_3)$).

$$\text{ii) } f = ((\overline{x_1} \cdot \overline{x_3}) + \overline{x_4}) \cdot \overline{x_2}$$



$$\begin{aligned}\bar{f} &= \overline{x_1 + x_2 + x_3} \\ &= \overline{x_1} \overline{x_2} \overline{x_3}\end{aligned}$$



$$\bar{f} = \overline{((\overline{x_1} \cdot \overline{x_3}) + \overline{x_4}) \cdot \overline{x_2}}$$

$$\begin{aligned}
 \hat{f} &= \overline{\overline{(x_1 \bar{x}_3)} + \bar{x}_4} \bar{x}_2 \\
 &= \overline{(\bar{x}_1 \bar{x}_3) + \bar{x}_4} + x_2 \\
 &= \overline{(x_1 \bar{x}_3)} \bar{x}_4 + x_2 \\
 &= (x_1 + x_3)(\bar{x}_4) + x_2
 \end{aligned}$$

- c) i) (6 marks) Consider function $f = (x_1 + x_3)(\bar{x}_1 + x_2 + \bar{x}_3)$. Give the full Verilog code to define a module to implement f .
- ii) (4 marks) Consider function $f = \bar{x}_1 x_4 + x_2 x_4 + \bar{x}_1 x_2 x_3$. How many transistors are needed to build this Sum-of-Products circuit using CMOS AND, OR, and NOT gates only?

i) Module $e(x_1, x_2, x_3, f)$:

input x_1, x_2, x_3 ;
output f ;

assign $f = (x_1 + x_3) \& (\sim x_1 + x_2 + \sim x_3)$;

endmodule

ii) 3 in OR = 8 # = 1(8) + 2(6) + 1(4) + 1(2)
 2 in AND = 6 = 30
 3 in AND = 4
 1 in NOT = 2 ∴ there are 30 transistors

2. Design & Optimisation Part I (8 Marks Total)

In this question you will design a modulo 4 circuit for decimal numbers between 0 and 9, encode as 4 bit binary coded decimal (BCD) numbers. The circuit will have four inputs, x_3, x_2, x_1 , and x_0 , and two outputs, y_1 and y_0 . The input $X = x_3x_2x_1x_0$ represents a single decimal digit as the corresponding 4-bit unsigned integer (e.g. $(0)_{10}$ is $(0000)_2$, $(1)_{10}$ is $(0001)_2$, etc.). Your design only needs to produce correct outputs for decimal numbers between 0 and 9 according to these specifications.

The value modulo 4 of a natural number X , denoted $X \ mod_4$, is simply the integer remainder obtained when dividing X by 4 (e.g. $5 \ mod_4 = 1$). The output of the circuit is a two digit unsigned integer number (hint: equivalent to bits x_1x_0 of BCD number) $Y = y_1y_0$ representing the value of $X \ mod_4$ (e.g. if $X \ mod_4 = 1$ then $Y = y_1y_0 = 01$).

Fill in the truth table below for the two outputs (you will need to either print the table or redraw it by hand):

$(X)_{10}$	$x_3x_2x_1x_0$	y_1	y_0
0	0000	0	0
1	0001	0	1
2	0010	1	0
3	0011	1	1
4	0100	0	0
5	0101	0	1
6	0110	1	0
7	0111	1	1
8	1000	0	0
9	1001	0	1
—	1010	1	1
—	1011	1	1
—	1100	1	1
—	1101	1	1
—	1110	1	1
—	1111	1	0

3. Design & Optimisation Part II (14 Marks Total)

- a) (10 marks) Assume you were given the truth table below (d stands for don't care):

$(X)_{10}$	$x_3x_2x_1x_0$	y_1	y_0
0	0000	1	0
1	0001	1	0
2	0010	1	1
3	0011	1	1
4	0100	1	1
5	0101	1	0
6	0110	0	1
7	0111	0	0
8	1000	0	1
9	1001	0	1
-	1010	d	d
-	1011	d	d
-	1100	d	d
-	1101	d	d
-	1110	d	d
-	1111	d	d

Find a minimum cost Product-of-Sum realization for output y_1 , and a minimum cost Sum-of-Product realization for y_0 . Assume that all input signals and their complements are already available. Use k-maps. (Aside: Questions 2 and 3 were originally one question but was split to accommodate the Avenue format)

- b) (4 marks) Including inverters, compute the costs of the minimal realizations of y_1 and y_0 from Part 3.a.

a) i)

	x_1x_2	00	01	11	10
x_3x_4	1	1	$[d]$	0	
00	1	1	$[d]$	0	
01	1	1	$[d]$	0	
11	1	$[0]$	$[d]$	d	
10	1	$[0]$	$[d]$	d	

$$POS: (\bar{x}_1)(\bar{x}_2 + \bar{x}_3)$$

ii)

	x_1x_2	00	01	11	10
x_3x_4	0	1	$[d]$	1	
00	0	0	$[d]$	1	
01	0	0	$[d]$	1	
11	1	0	$[d]$	d	
10	1	1	$[d]$	d	

$$SOP: x_1 + \bar{x}_2 x_3 + x_2 \bar{x}_4$$

b) cost = $3 + 5 + 3$
 $= 11$

b) cost = $6 + 8 + 2$
 $= 16$

4. Circuit Implementation (16 Marks Total)

- a) (8 marks) Figure 1 contains the simplified schematic for a PLA (you will need to either print the figure, or redraw the portion that you need by hand). Show how this device could be used to implement $f_1 = x_4x_3\bar{x}_2x_1 + \bar{x}_3x_2 + \bar{x}_4\bar{x}_2x_1$ by placing \otimes on the junctions you want to connect.
- b) (8 marks) Show how $f = x_1\bar{x}_2x_4 + \bar{x}_2x_3\bar{x}_4$ can be implemented using four 2-input lookup-tables (LUTs). Label all inputs and outputs of the LUTs and show truth tables. You do not need to show connecting wires.

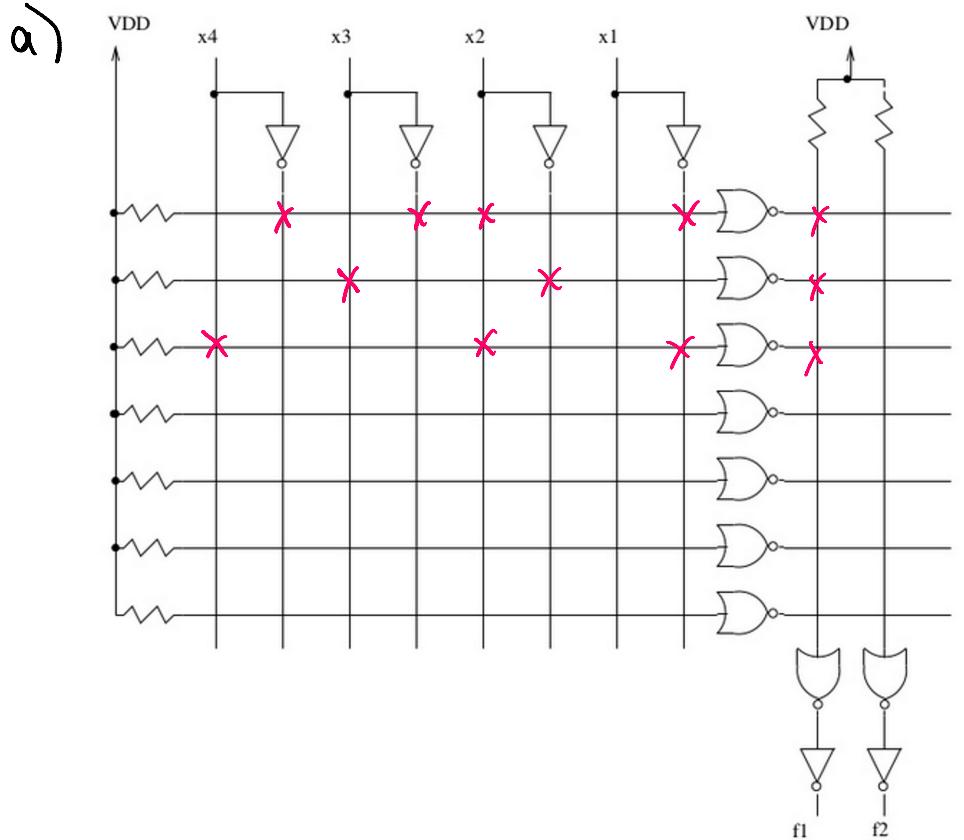
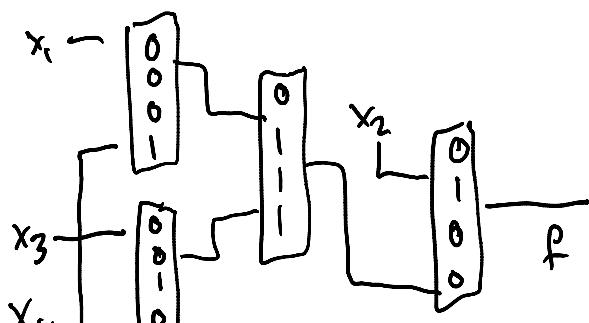
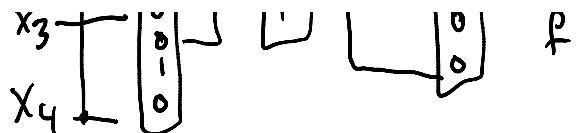


Figure 1: PLD for Question 4.a

$$\begin{aligned} b) \quad f &= x_1 \bar{x}_2 x_4 + \bar{x}_2 x_3 \bar{x}_4 \\ &= \bar{x}_2 (x_1 x_4 + x_3 \bar{x}_4) \end{aligned}$$

x_1	x_4	f_1	x_3	x_4	f_2	f_1	f_2	f_3	\bar{x}_2	f_3	f_4
0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	1	1	0	1	1
1	0	0	1	0	1	1	0	1	1	0	0
1	1	1	1	1	0	1	1	1	1	1	0





5. Circuit Analysis Part I (14 Marks Total)

- a) (8 marks) Draw a timing diagram showing the waveforms that can be observed on all wires in the circuit in Figure 2. Ignore gate delay (ie. a functional timing diagram).

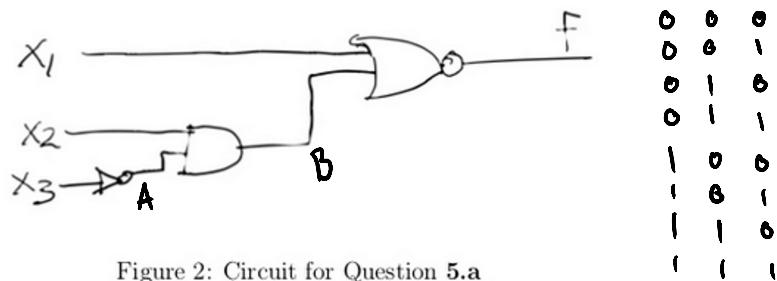
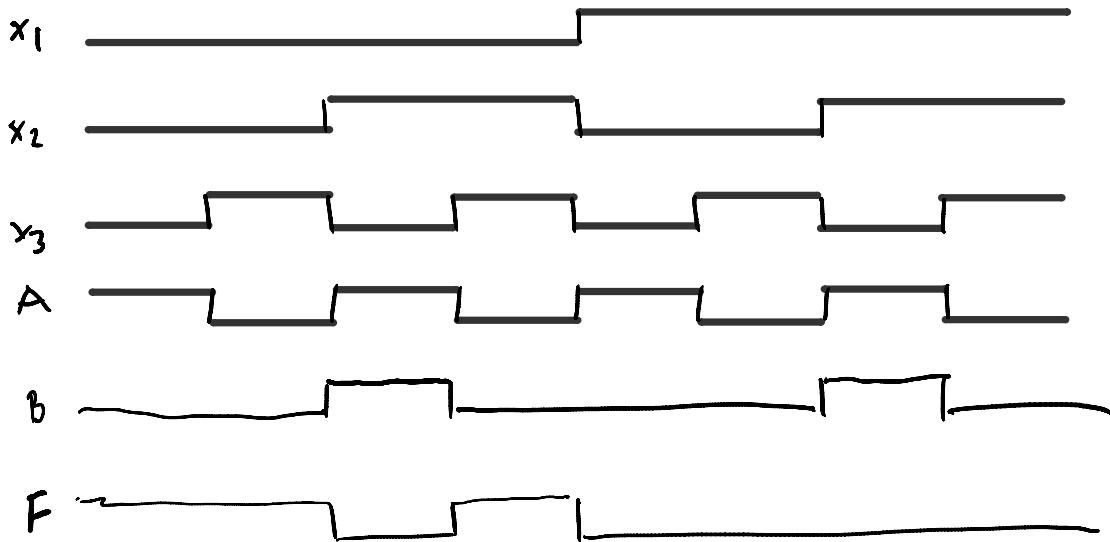


Figure 2: Circuit for Question 5.a



b) (6 marks) Derive an expression for f in Figure 3. Show all steps.

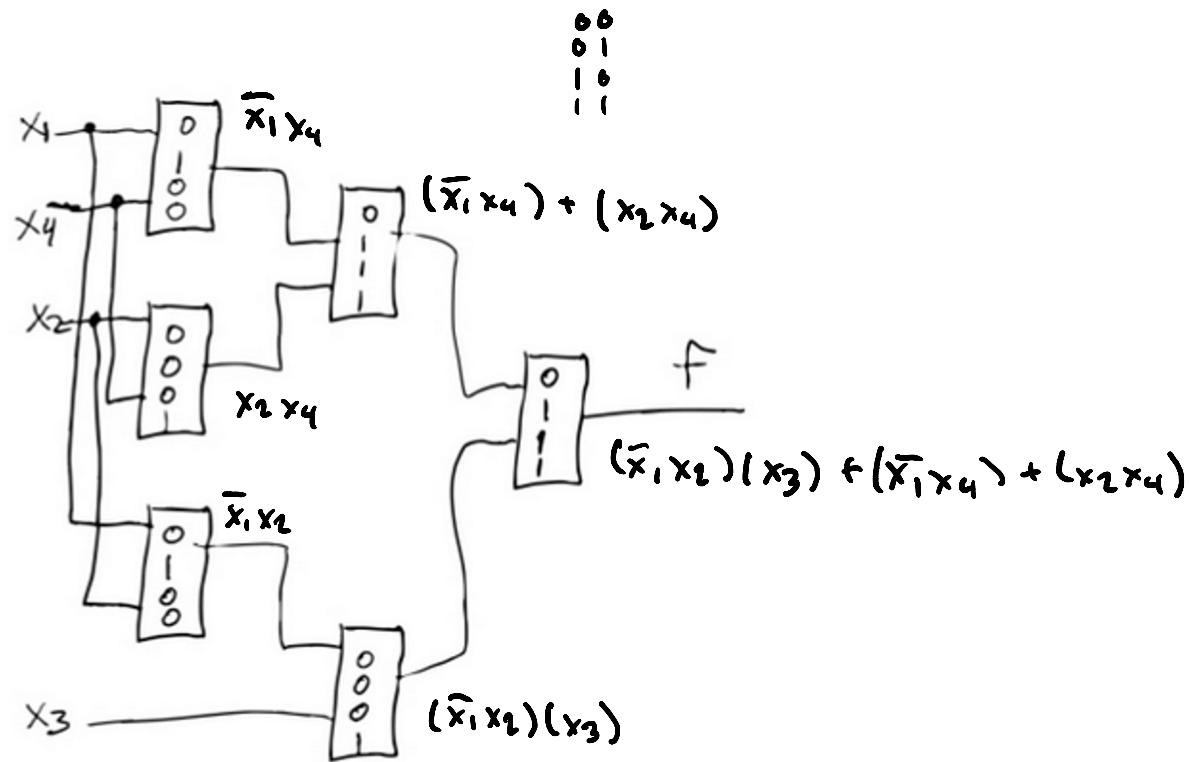
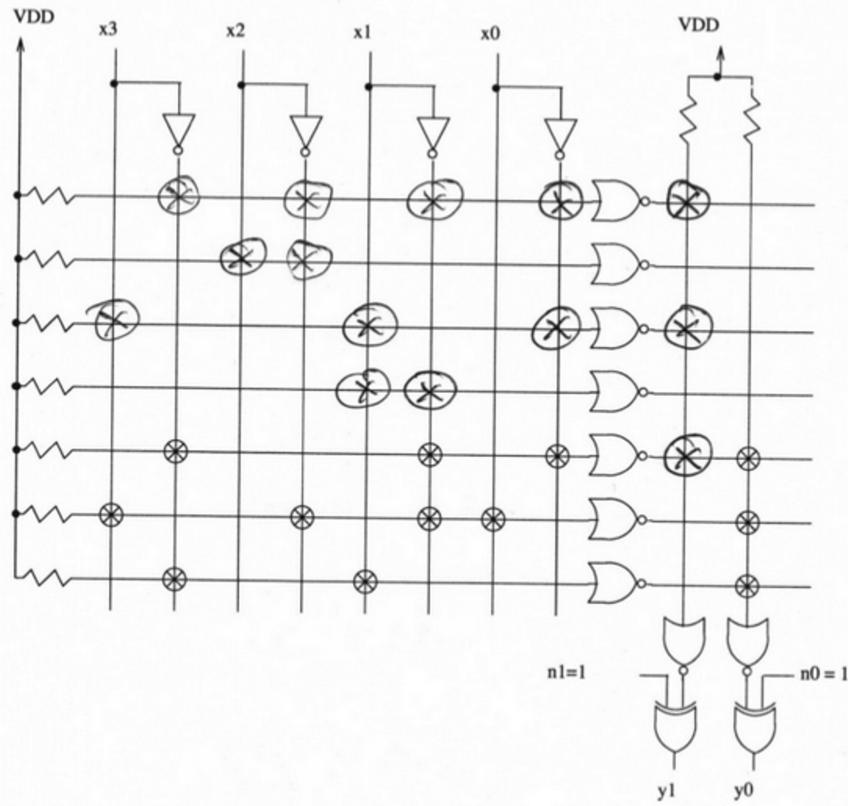


Figure 3: Circuit for Question 5.b

$$f = (\bar{x}_1 \bar{x}_2)(x_3) + (\bar{x}_1 x_4) + (x_2 x_4)$$

6. Circuit Analysis Part II (6 Marks Total)

Derive an expression for y_1 in Figure 4.



$$y_1 = x_3 x_2 x_1 x_0 + \bar{x}_3 \bar{x}_1 x_0 + x_3 x_1 x_0$$

7. Multiple Choice (9 Marks Total) For each of the multiple choice questions below, circle the answer that is most correct. Each correct answer is worth 1 mark.

- i) An XNOR gate can be used to create:
 - a) A bitwise OR circuit.
 - b) A comparator circuit (checks if each bit of two vectors is equal).**
 - c) A bitwise AND circuit.
 - d) None of the above.
- ii) Tri-state buffers are often used as part of:
 - a) 2:1 muxes.
 - b) Devices accessing data busses.**
 - c) Special types of light sabers.
 - d) None of the above.
- iii) The following device can be programmed in circuit:
 - a) 7400 chips.
 - b) PLA.**
 - c) CPLD.**
 - d) VLSI chips.
- iv) Macro cells can be found in:
 - a) CPLD.**
 - b) 7400 chips.
 - c) Custom chips.
 - d) FPGA.
- v) Large transistors are commonly found in which common gate:
 - a) 2:1 muxes**
 - b) Invertors**
 - c) NOR gates**
 - d) Buffers**
- vi) The type of programmable device that can implement the largest circuits are:
 - a) CPLD
 - b) PLA**
 - c) FPGA**
 - d) 7400 chips
- vii) PLA devices contain which gates:
 - a) NAND**
 - b) AND**
 - c) OR**
 - d) NOR**
- viii) An XOR gate is created using:
 - a) T-gates and NOT gates.
 - b) AND, OR, and NOT gates.**
 - c) NMOS transistors.
 - d) None of the above.
- ix) If the output of an inverter is connected to the number of inputs below, which would have the fastest output response:
 - a) 3 inputs.
 - b) 2 inputs.
 - c) 1 input.**
 - d) 4 inputs.