Universidad de Costa Rica

Tarea 4

Temporización

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Grupo 1

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Índice

1. Objetivos

- Generear una descripción conductual sintetizable para cumplir con los requisitos de funcionamiento suministrados
- Sintetizar el componente usando celdas con especificaciones comerciales para realizar una simulación acercada al comportamiento real
- Verificar el funcionamiento de los componentes generados y sintetizados en el ambiente de pruebas creado en la tarea anterior
- Utilizar los resultados de la simulación para determinar el periodo de clock en el que funciona adecuadamente el componente.

2. Definición de funcionamiento

Tomando como base el enunciado dado; se encuentra que el contador tiene cuatro entradas que determinan el comportamiento del componente, osea sus dos salidas. Es necesario definir correctamente lo que se entendió de la especificación dada para poder justificar las conclusiones emitidas al final del documento.

2.1. Entradas

En orden jerárquico de efecto sobre las salidas se tienen las entradas

2.1.1. Clock

La entrada de clock es un pulso cuadrado constante y uniforme que determina el tiempo de operación y los momentos de ejecución del componente.

2.1.2. Enable

Una entrada binaria que determina si el componente opera o no; en caso de operar debe estar en alto (1) en cuyo caso opera según la entrada de modo. En caso de estar en bajo (0) el componente no opera y las salidas mantienen su estado.

2.1.3. Modo

Este componente tiene cuatro modos de operación descritos a continuación

- Suma 1 (00)
- Resta 1 (01)
- Resta 3 (10)
- Load (11)

De esta forma el modo de sumar 1 debe sumar de uno en uno hasta sobrepasar el valor máximo del contador (15) debe volver a 0. El modo de restar 1 funciona de manera similar pero restando y al rebasar el valor de 0 debe regresar al valor máximo de 15. El modo de restar 3 funciona igual al anterior pero restando de tres en tres y al sobre pasar se debe restar el sobrepaso al valor maximo de 15. En el modo de Load se copia el valor en D

2.1.4. D

. Esta entrada solo se utiliza cuando se tiene enabled en alto y el modo es 11; en este caso se copia este valor como la salida Q.

2.2. Salidas

2.2.1. Q

Esta salida representa el valor del contador y está en constante cambio

2.2.2. rco

Esta salida representa el evento de rebase y es la que presenta mayor problema para definir su comportamiento pues las especificaciones dadas no son suficientes para determinar como debe comportarse; no obstante se debe definir un comportamiento esperado para poder realizar un proceso de verificación por lo cual se definió que esta señal debe mantenerse en 0 hasta que exista una condición de rebase que significa que la señal pasa a 1 por un ciclo de reloj y luego regresa a 0. En el modo de carga (modo = 11) la salida de rco debe mantenerse arriba en un valor de 1.

3. Ambiente de Testing

Para el desarrollo de la verificación de estos componentes se utilizó el siguiente esquema de modulo para este desarrollo

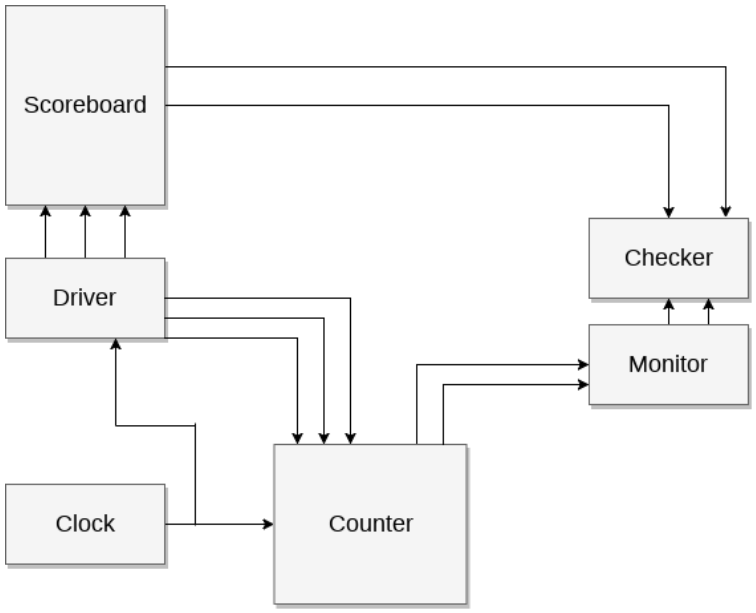


Figura 1: Ambiente de testing. Elaboración propia

Este ambiente de desarrolló se replicó cinco veces para realizar pruebas de manera independiente sobre cada uno de los contadores (conductual y sintetizado) y generar datos de estudio para cada uno. El componente sintetizado se conectó a cuatro valores señales de Clock distintas (2ns, 4ns, 20ns y 200ns) para encontrar el valor de clock donde el componente es capaz de pasar las pruebas

3.1. Plan de pruebas

Como plan de pruebas se realizarán tres etapas; una etapa semi aleatoria en la que se colocan valores aleatorios en enable para evaluar la robustez del componente en al variar esta entrada. De manera seguida se inicia una segunda etapa completamente aleatoria en la que se utilizan variables aleatorias en las tres entradas distintas de Clock para evaluar la robustez en cambios abruptos en el modo y la cuenta desde cualquier valor. Por último se ejecuta la etapa completamente predefinida en la que se evalúan casos de interés para evaluar posibles casos esquina en los que podría fallar el componente. Además resulta importante resaltar que la semilla de números aleatorios se utilizó la predeterminada del sistema en caso de querer recrear resultados.

4. Resultados

4.1. Síntesis

Para la síntesis del componente real se utilizó el programa Yosys con la biblioteca de celdas proporcionada por el profesor (cmos_cells.lib); además se utilizaron los datos de temporización (en temperaturas entre 4.5 C y 5.5 C)de las hojas de fabricante de los componentes mencionados a continuación

- HD74LS04 (NOT): tpdh=9ns; tpdl=10ns
- 74HC00 (NAND): tpdh=7ns; tpdl=7ns
- 74HC02 (NOR): tpdh=9ns; tpdl=9ns
- SN74LVC1G80 (D Flip Flop): tpdh=2.5ns; tpdl=2.5ns; tsetup=1.1ns; thold=0.4ns

Por otra parte al ejecutar el plan de pruebas; se obtuvieron documentos que describen exactamente en que puntos se dieron errores de funcionamiento según la especificación definida en puntos anteriores. De esta forma se han adjuntado como anexo estos documentos (o parte de ellos) al final de este documento para revisión exhaustiva de resultados. En esta sección se adjuntaran las imagenes de simulación para describir las situaciones de error y utilizar esta información para definir si el componente cumple o no estas especificaciones.

4.2. Simulación de descripción conductual con Clock de 2 ns

Se vuelce importante demostrar el funcionamiento de la descripción conductual para demostrar asi que cualquier error post sintetizado se debe a temporización y no es un error que se arrastró desde el conductual; para esto se adjunta un extracto de la respuesta en el plan de pruebas para observar como las salidas calzan con el scoreboard

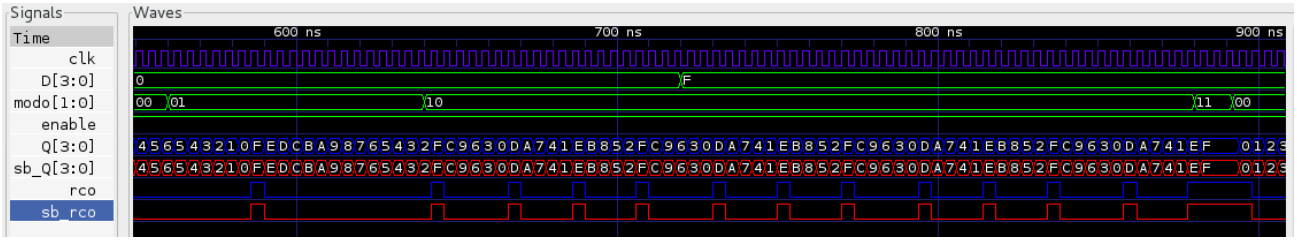


Figura 2: Simulación de componente conductual con Clock en 2ns. Elaboración propia

4.3. Simulación de descripción sintetizada con Clock de 2 ns

Una vez pasado el proceso de sintetizado exitoso (pues no se generó ningún tipo de latch inferido) se procedió a conectar este componente al ambiente de pruebas con un Clock con periodo de 2ns

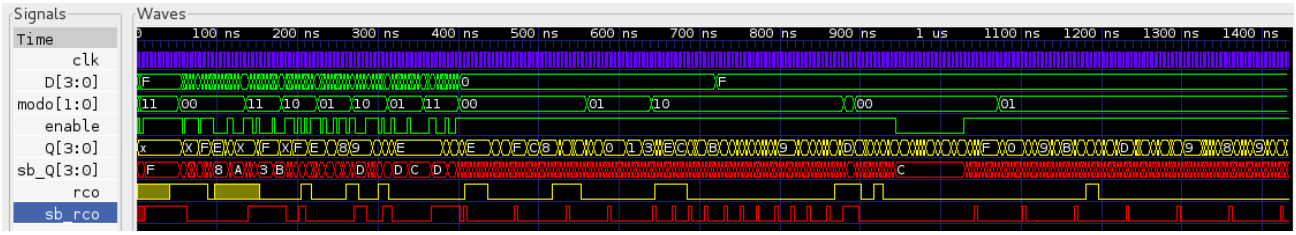


Figura 3: Simulación de componente sintetizado con Clock en 2ns. Elaboración propia

En este caso se notan muchos errores al punto de que parece prácticamente inutilizable a esta frecuencia.

4.4. Simulación de descripción sintetizada con Clock de 4 ns

Siguiendo con el plan de pruebas se conecta el componente sintetizado al ambiente de pruebas con una señal de Clock con periodo de 4ns

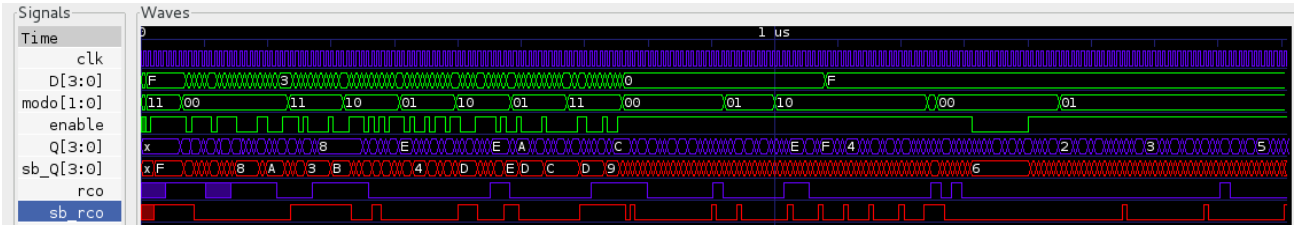


Figura 4: Simulación de componente sintetizado con Clock en 4ns. Elaboración propia

Donde se empieza a notar una cantidad menor de errores pero aún así el contador no parece ser funcional.

4.5. Simulación de descripción sintetizada con Clock de 20 ns

De esta manera se pasa a conectar el sintetizado con el ambiente de pruebas y un Clock de 20ns

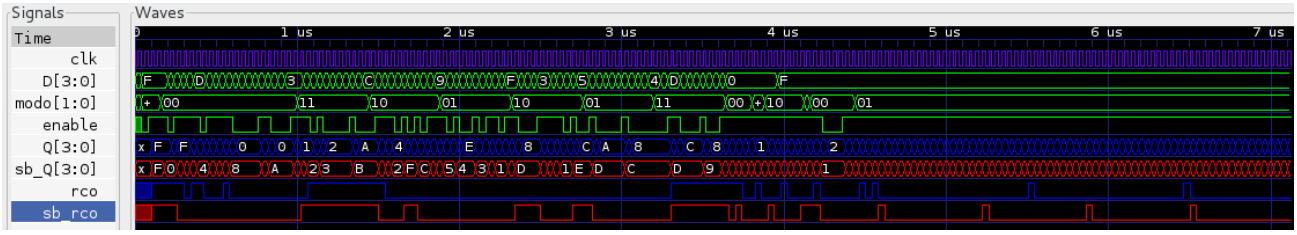


Figura 5: Simulación de componente sintetizado con Clock en 20ns. Elaboración propia

En este caso se siguen notando errores pero en menor cantidad; estos errores hacen que el contador no sea viable en esta frecuencia. Por otra parte se empieza a detectar que la cantidad de errores disminuye al aumentar el periodo de Clock.

4.6. Simulación de descripción sintetizada con Clock de 200 ns

Por último se conecta el sintetizado al ambiente de pruebas y una señal de Clock de 200 ns con lo cual se obtienen los siguientes resultados.

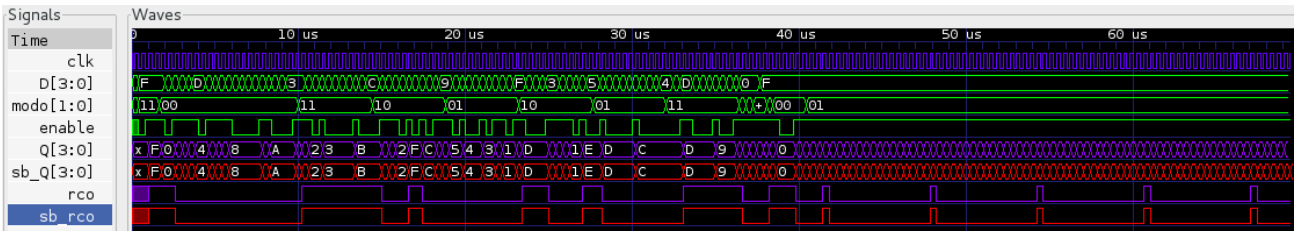


Figura 6: Simulación de componente sintetizado con Clock en 200ns. Elaboración propia

En este caso los resultados demuestran que el contador funciona a la perfección con este periodo de Clock y se considera una prueba exitosa.

5. Conclusiones

A manera de conclusión se determina el problema que puede representar la temporización de los componentes y por qué resulta tan importante el diseño eficiente de componentes; pues entre más eficiente sea este diseño se tendrán más valores de periodo de Clock en los que este podrá funcionar.

En el caso específico de este sintetizado se determinó que el componente funciona bien en periodos de Clock de 200ns mas no funciona de manera esperada en los periodos menores que fueron probados; esto se debe a que los valores de retardo de la señal sobrelapan la señal de clock y se pierden datos en el camino.

6. Anexos

6.1. Especificaciones

IE0411 – Microelectrónica
I – 2020

Tarea Temporización

18 de mayo de 2020

Consideraciones generales:

- La entrega de esta tarea consiste en un informe de resultados, los cuales deben ser debidamente justificados.
- Toda imagen con resultados debe tener una buena calidad y debidamente justificada para ser calificada.
- Se deben entregar todos los ejecutables que comprueben el análisis de resultados.
- Como parte de la solución debe incluir un Makefile con su respectivo README que contenga la forma de ejecutar las pruebas.
- Se castigará severamente cualquier intento o asomo de copia durante el examen o en las soluciones.

Especificaciones

Esta tarea consiste en escribir una descripción conductual del contador usando Verilog. Esta descripción servirá como una especificación detallada y formal del funcionamiento del dispositivo diseñado. Como requisito de diseño deberá utilizar al menos un $case$ en la descripción conductual del contador. El contador deberá tener los siguientes modos de operación:

- Cuenta hacia arriba.
- Cuenta hacia abajo.
- Cuenta de tres en tres hacia abajo.
- Carga en paralelo.

Además del contador se deberá crear una libería de compuertas lógicas dentro del archivo $cmos\_cells.v$ que deben incluir los siguientes módulos:

- Inversor
- NAND 2 entradas
- NOR 2 entradas
- DFF Flip Flop

Como requisito en la descricpción de la compuertas debe incluir los detalles de temporización utilizando el bloque $specify$ en Verilog. Los tiempos a incluir son:

- Tiempo propagación en alto t_{pdh}
- Tiempo propagación en bajo t_{pdl}
- Tiempo de preparación o setup t_{setup}
- Tiempo de sostenimiento o hold t_{hold}

Los valores de los tiempos deben de obtenerse de la hoja de datos del fabricante de su elección. Las mismas deben incluirse como bibliografía. El informe debe incluir el valor unitario o del lote por cada componente. Cada estudiante tiene libertad de seleccionar los parámetros como la capacitancia de carga, temperatura, valores mínimos o máximos para escoger sus tiempos de propagación, solamente deben cumplir con que la selección sea uniforme para todas las compuertas. Deberán utilizar una escala de referencia en ns con una precisión en ps en la implementación del código.

Utilice yosys para sintetizar su modelo utilizando la librería $cmos\_cells.lib$. Luego, guarde la descripción estructural con el nombre $contador\_synt.v$ e incluya este contador en su $top.v$ para ser verificado. Como parte del procedimiento debe incluir la librería $cmos\_cells.v$ en su archivo $contador\_synt.v$ antes de utilizar icarus verilog.

Utilice la estructura de Testbench diseñado en la tarea 3 para verificar el diseño y el netlist generado con yosys.

Realice dos verificaciones:

- Sin tiempos de propagación.
- Con tiempos de propagación.

Para el segundo caso deberá ejecutar la siguiente línea de comando $iverilog$ -o $algo$ -g$specify$ $algo.v$ para que se consideren los valores de temporización. Todas las pruebas deben iniciar con un periodo de 2 ns para el reloj. Puede aumentar el periodo al siguiente valor permitido, pero no puede saltar entre periodos no consecutivos si encuentra problemas en su contador, el aumento del periodo deberá justificarse técnicamente. Los valores permitidos para el periodo del reloj son:

- 2 ns
- 4 ns
- 20 ns
- 200 ns

Especificación de las entradas del contador

1. **CLK**: entrada de reloj del contador. El flanco activo de la señal CLK es el flanco creciente. Entonces, con cada flanco positivo del reloj el contador cambia de estado dependiendo del estado de las señales de MODO y si la señal ENB = 1.
2. **ENB**: entrada de habilitación del contador. Si ENB = 1, el contador funciona normalmente respondiendo a los flancos activos de CLK para cambiar de estado de acuerdo a la señal MODO. Si ENB = 0, el contador mantiene su estado actual sin importar los flancos de CLK.
3. **D[3:0]**: entrada de datos D consta de cuatro líneas. El valor que tengan las entradas D[3:0] será almacenado en Q[3:0] en el flanco activo de CLK si ENB = 1 y MODO = 11.
4. **MODO[1:0]**: entrada de modo que consta de dos líneas y sirve para definir cuál será el próximo estado del contador al llegar el flanco activo del reloj en la entrada CLK. Si el contador se encuentra en el estado Q antes del flanco activo del reloj, luego del flanco activo, su estado será:
   - MODO = 00 $->$ Q + 1
   - MODO = 01 $->$ Q - 1
   - MODO = 10 $->$ Q - 3
   - MODO = 11 $->$ D

Especificación de las salidas del contador

1. **Q[3:0]**: salida Q que consta de cuatro líneas que indican el estado presente del contador. El estado del contador cambia con el flanco activo de la señal CLK mientras ENB = 1 y de acuerdo con el modo seleccionado con las líneas MODO[1:0].
2. **RCO**: salida de llevo “Ripple-Carry Out” que indica cuándo el contador llega a su cuenta límite para que la siguiente etapa, en contadores de más de 4 bits, se habilite para que realice su actualización de estado. RCO se debe poner en 1 cuando el MODO = 11 está activo.

Consideraciones

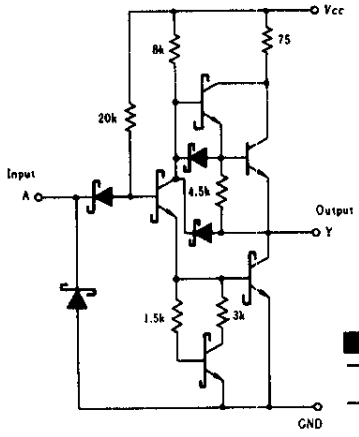
1. El contador no tiene un estado inicial de cuenta, por lo tanto se debe seleccionar el MODO = 11 antes de cualquier otro modo de cuenta.

6.2. Hoja de Fabricante HD74LS04

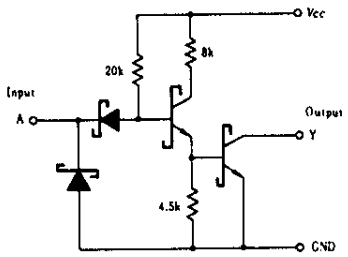
HD74LS04/HD74LS05 ●Hex Inverters ●Hex Inverters (with Open Collector Outputs)

■CIRCUIT SCHEMATIC(1/6)

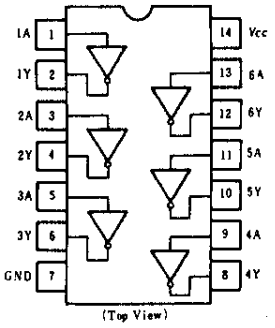
HD74LS04



HD74LS05



■PIN ARRANGEMENT



■HD74LS05 RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output voltage	V_{OH}	–	–	5.5	V
Low level output current	I_{OL}	–	–	8	mA

■ELECTRICAL CHARACTERISTICS (Ta=−20~+75°C)

Item	Symbol	Test Conditions		HD74LS04 min	HD74LS04 typ*	HD74LS04 max	HD74LS05 min	HD74LS05 typ*	HD74LS05 max	Unit
Input voltage	V_{IH}			2.0	–	–	2.0	–	–	V
	V_{IL}			–	–	0.8	–	–	0.8	V
Output voltage	V_{OH}	V_{CC}=4.75V, V_{IL}=0.8V, I_{OH}=−400μA		2.7	–	–	–	–	–	V
	V_{OL}	V_{CC}=4.75V, V_{IH}=2V	I_{OL}=8mA	–	–	0.5	–	–	0.5	V
			I_{OL}=4mA	–	–	0.4	–	–	0.4	
Output current	I_{OH}	V_{CC}=4.75V, V_{IL}=0.8V, V_{OH}=5.5V		–	–	–	–	–	100	μA
Input current	I_{IH}	V_{CC}=5.25V, V_I=2.7V		–	–	20	–	–	20	μA
	I_{IL}	V_{CC}=5.25V, V_I=0.4V		–	–	−0.4	–	–	−0.4	mA
	I_I	V_{CC}=5.25V, V_I=7V		–	–	0.1	–	–	0.1	mA
Short-circuit output current	I_{OS}	V_{CC}=5.25V		−20	–	−100	–	–	–	mA
Supply current	I_{CCH}	V_{CC}=5.25V		–	1.2	2.4	–	1.2	2.4	mA
	I_{CCL}			–	3.6	6.6	–	3.6	6.6	
Input clamp voltage	V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA		–	–	−1.5	–	–	−1.5	V

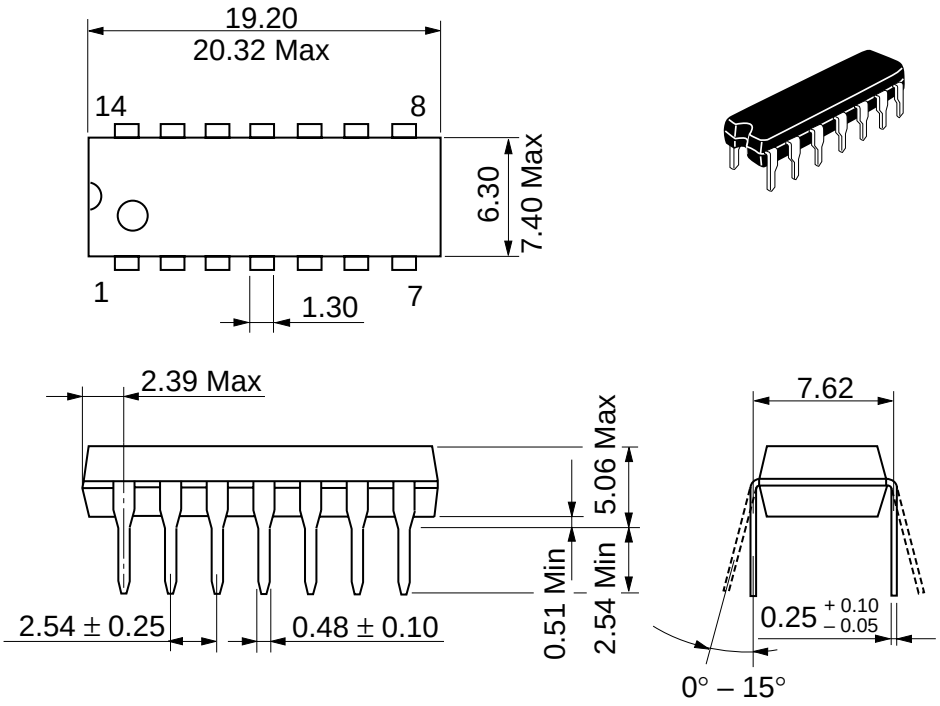
* V_{CC}=5V, Ta=25°C

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

Item	Symbol	Test Conditions	HD74LS04 min	HD74LS04 typ	HD74LS04 max	HD74LS05 min	HD74LS05 typ	HD74LS05 max	Unit
Propagation delay time	t_{PLH}	C_L=15pF, R_L=2kΩ	–	9	15	–	17	32	ns
	t_{PHL}		–	10	15	–	15	28	

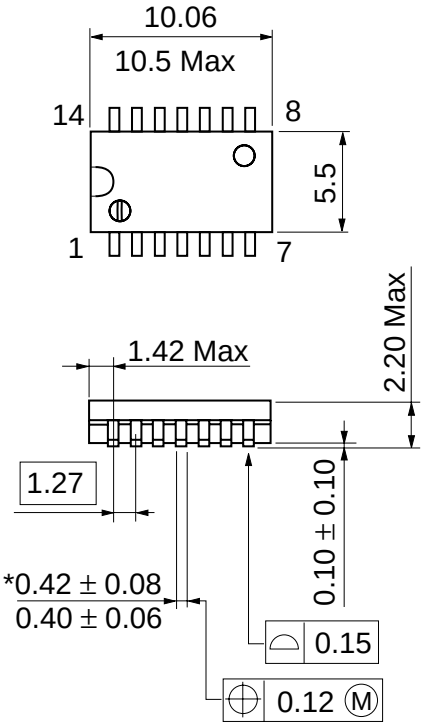
Note) Refer to Test Circuit and Waveform of the Common Item

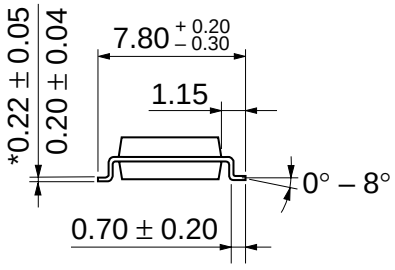
Unit: mm

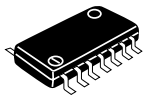


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm



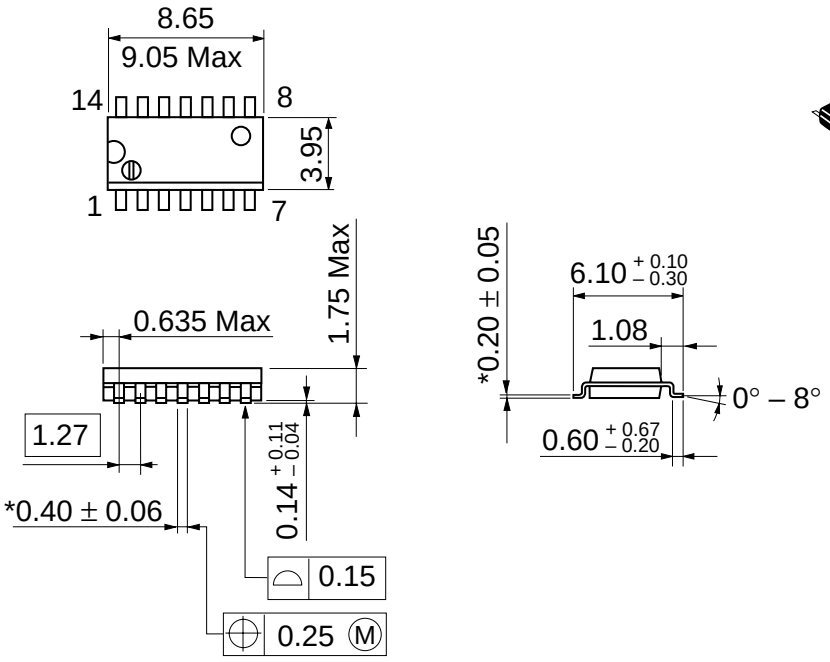




*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

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6.3. Hoja de Fabricante 74HC00

74HC00; 74HCT00

Quad 2-input NAND gate

Rev. 7 — 25 November 2015 **Product data sheet**

1. General description

The 74HC00; 74HCT00 is a quad 2-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC00: CMOS level
  - For 74HCT00: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC00D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT00D				
74HC00DB	−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT00DB				
74HC00PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT00PW				
74HC00BQ	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT00BQ				

nexperia

4. Functional diagram

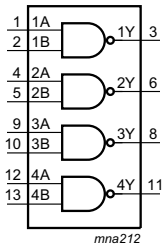


Fig 1. Logic symbol

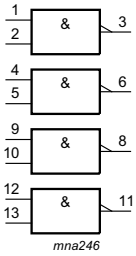


Fig 2. IEC logic symbol

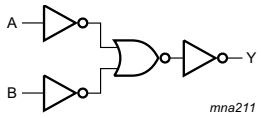


Fig 3. Logic diagram (one gate)

5. Pinning information

5.1 Pinning

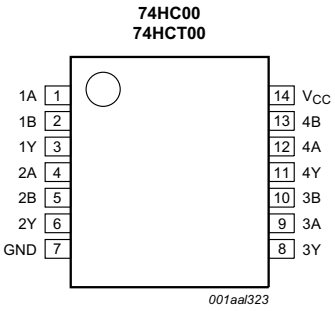
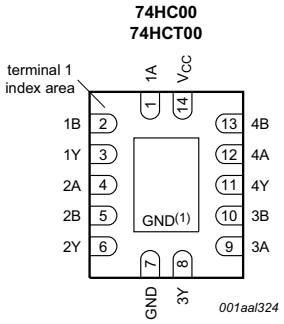


Fig 4. Pin configuration SO14 and (T)SSOP14



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input		Output
nA	**nB**	**nY**
L	X	H
X	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	[2]			
	SO14, (T)SSOP14 and DHVQFN14 packages		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC00			74HCT00			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC00										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	-	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	-	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	-	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	-	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	-	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	-	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	-	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	-	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	-	6.0	-	5.9	-	5.9	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	-	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	-	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	-	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	-	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	-	-	±1	-	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	-	-	20	-	40	μA

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT00										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 μA	-	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA	-	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	-	-	0.1	-	0.1	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.15	-	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	-	-	±1	-	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	-	-	20	-	40	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} – 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	150	-	-	675	-	735	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Figure 7.

Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HC00								
t_{pd}	propagation delay	nA, nB to nY; see Figure 6 [1]						
		V_{CC} = 2.0 V	-	25	-	115	135	ns
		V_{CC} = 4.5 V	-	9	-	23	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	7	-	-	-	ns
		V_{CC} = 6.0 V	-	7	-	20	23	ns
t_t	transition time	see Figure 6 [2]						
		V_{CC} = 2.0 V	-	19	-	95	110	ns
		V_{CC} = 4.5 V	-	7	-	19	22	ns
		V_{CC} = 6.0 V	-	6	-	16	19	ns

Table 7. Dynamic characteristics *…continued*

GND = 0 V; C_L = 50 pF; for test circuit see Figure 7.

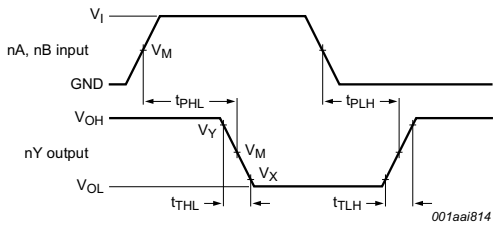
Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} [3]	-	22	-	-	-	pF
74HCT00								
t_{pd}	propagation delay	nA, nB to nY; see Figure 6 [1]						
		V_{CC} = 4.5 V	-	12	-	24	29	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	10	-	-	-	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 6 [2]	-	-	-	29	22	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} − 1.5 V [3]	-	22	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



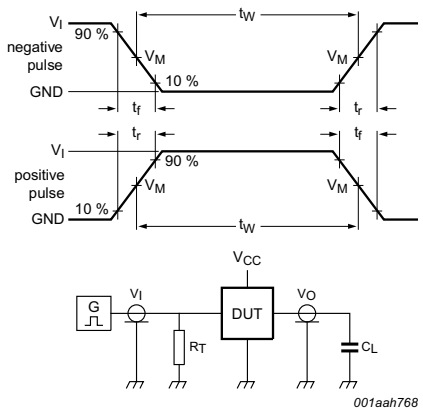
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Input to output propagation delays

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC00	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT00	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

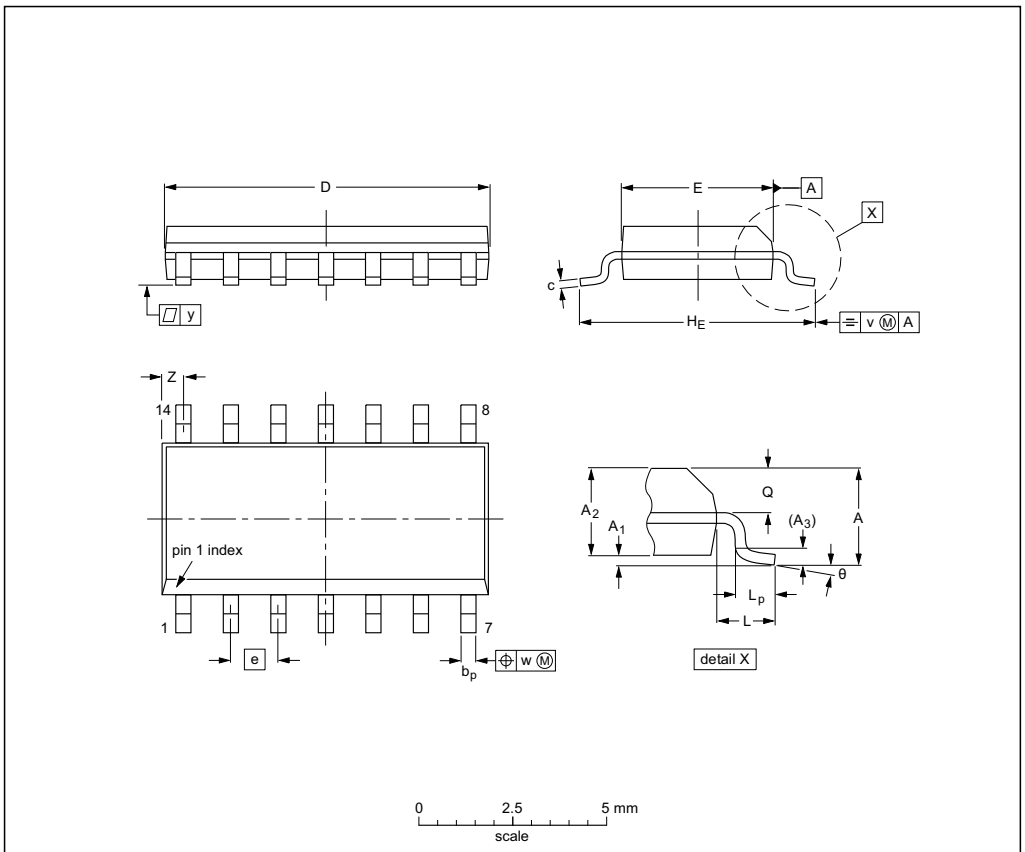
Fig 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC00	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT00	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

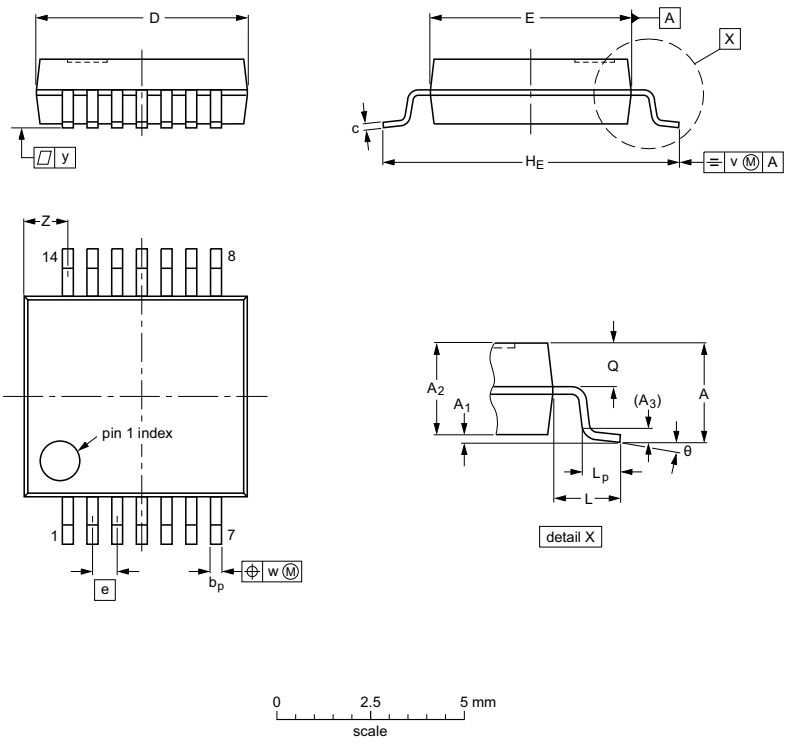
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

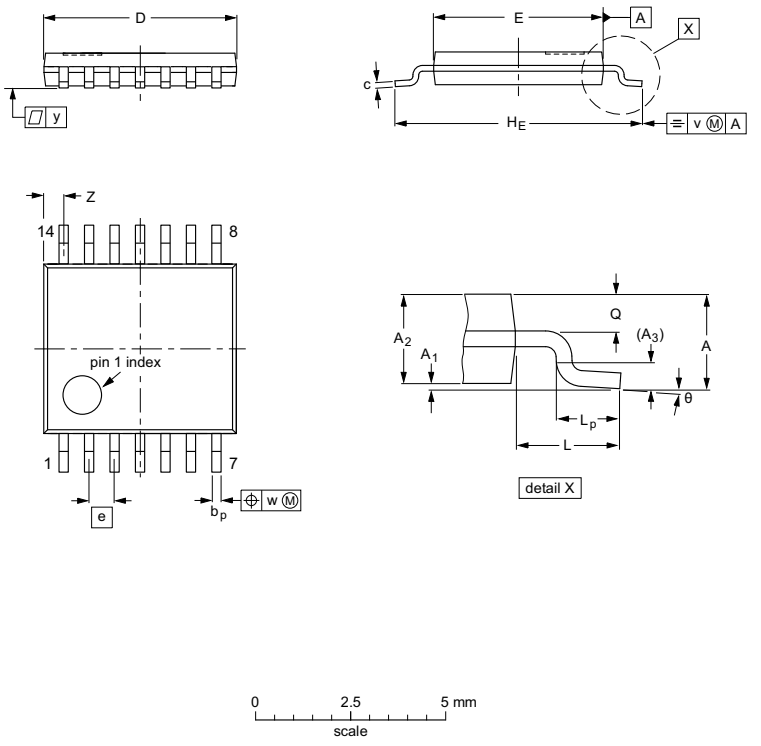
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

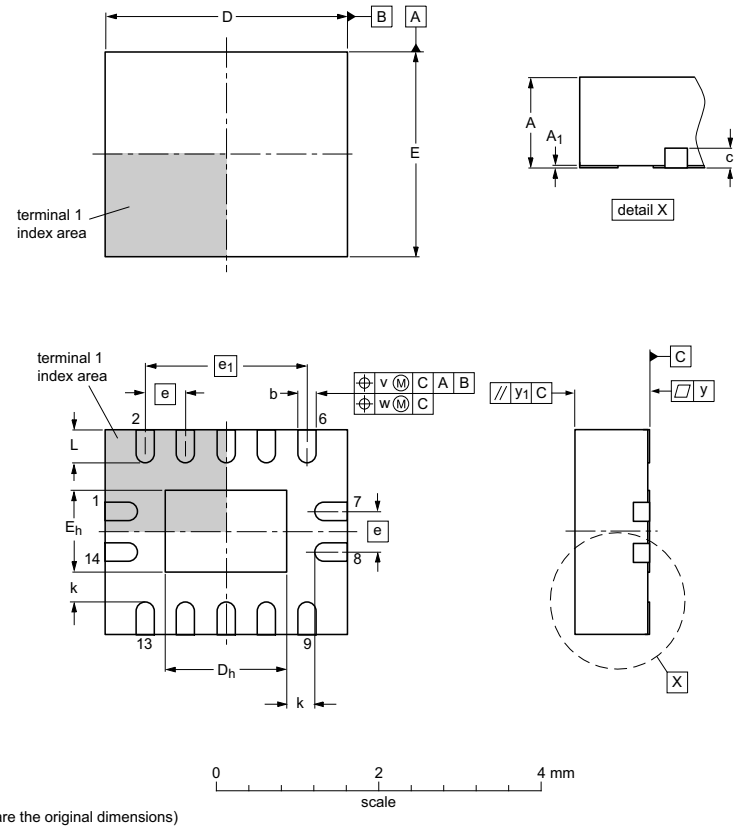
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	k	L	v	w	y	y1
mm	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig 11. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT00 v.7	20151125	Product data sheet	-	74HC_HCT00 v.6
Modifications:	• Type numbers 74HC00N and 74HCT00N (SOT27-1) removed.			
74HC_HCT00 v.6	20111214	Product data sheet	-	74HC_HCT00 v.5
Modifications:	• Legal pages updated.			
74HC_HCT00 v.5	20101125	Product data sheet	-	74HC_HCT00 v.4
74HC_HCT00 v.4	20100111	Product data sheet	-	74HC_HCT00 v.3
74HC_HCT00 v.3	20030630	Product data sheet	-	74HC_HCT00_CNV v.2
74HC_HCT00_CNV v.2	19970826	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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17. Contents

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Date of release: 25 November 2015

6.4. Hoja de Fabricante 74HC02

74HC02; 74HCT02

Quad 2-input NOR gate

Rev. 6 — 7 April 2020 **Product data sheet**

1. General description

The 74HC02; 74HCT02 is a quad 2-input NOR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC02: CMOS level
  - For 74HCT02: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC02D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT02D				
74HC02DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT02DB				
74HC02PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT02PW				
74HC02BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT02BQ				

nexperia

4. Functional diagram

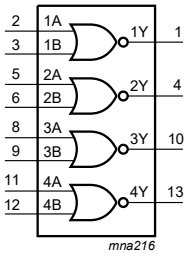


Fig. 1. Logic symbol

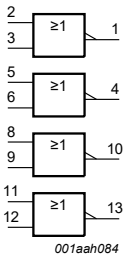


Fig. 2. IEC logic symbol

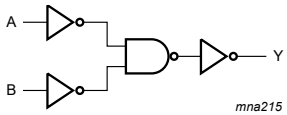


Fig. 3. Logic diagram (one gate)

5. Pinning information

5.1. Pinning

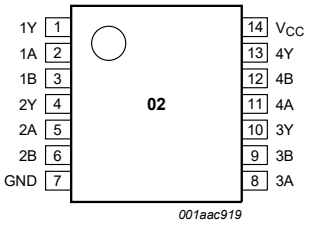
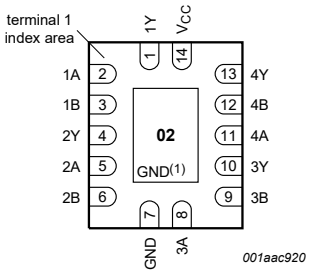


Fig. 4. Pin configuration SOT108-1 (SO14), SOT337-1 (SSOP14) and SOT402-1 (TSSOP14)



Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y to 4Y	1, 4, 10, 13	data output
1A to 4A	2, 5, 8, 11	data input
1B to 4B	3, 6, 9,12	data input
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input		Output
nA	**nB**	**nY**
L	L	H
X	H	L
H	X	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$-0.5 \text{ V} < V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT337-1 (SSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC02			74HCT02			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC02										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	2.0	-	20	-	40	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT02										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 5.2 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2.0	-	20	-	40	µA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	150	540	-	675	-	735	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

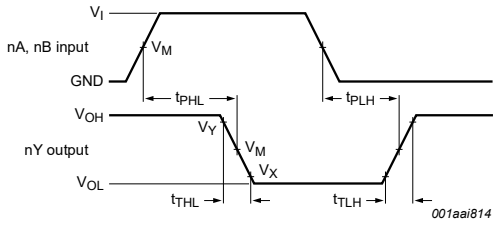
Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC02										
t_{pd}	propagation delay	nA, nB to nY; see Fig. 6 [1]								
		V_{CC} = 2.0 V	-	25	90	-	115	-	135	ns
		V_{CC} = 4.5 V	-	9	18	-	23	-	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	7	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	7	15	-	20	-	23	ns
t_t	transition time	see Fig. 6 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} [3]	-	22	-	-	-	-	-	pF
74HCT02										
t_{pd}	propagation delay	nA, nB to nY; see Fig. 6 [1]								
		V_{CC} = 4.5 V	-	11	19	-	24	-	29	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	9	-	-	-	-	-	ns
t_t	transition time	V_{CC} = 4.5 V; see Fig. 6 [2]	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} - 1.5 V [3]	-	24	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms



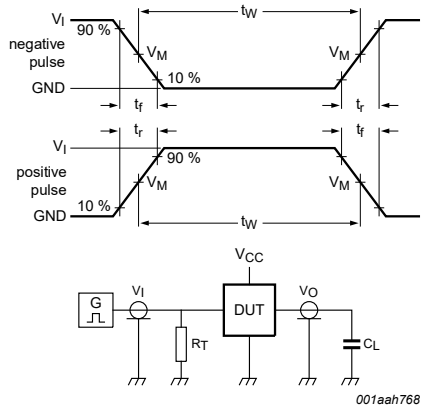
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Input to output propagation delays

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC02	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT02	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

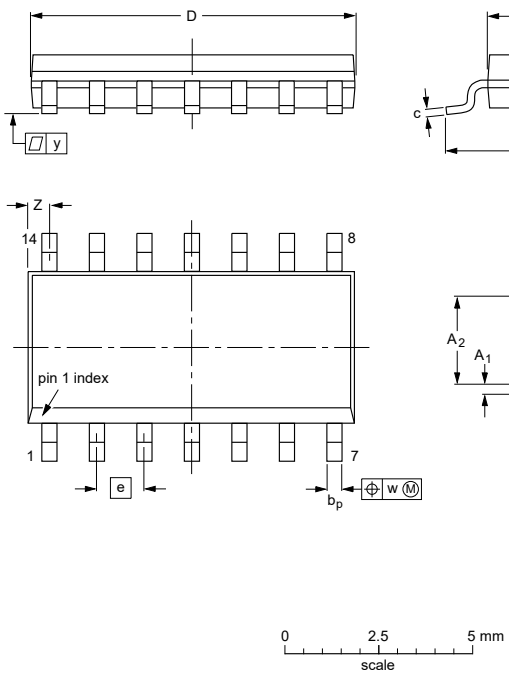
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC02	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT02	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

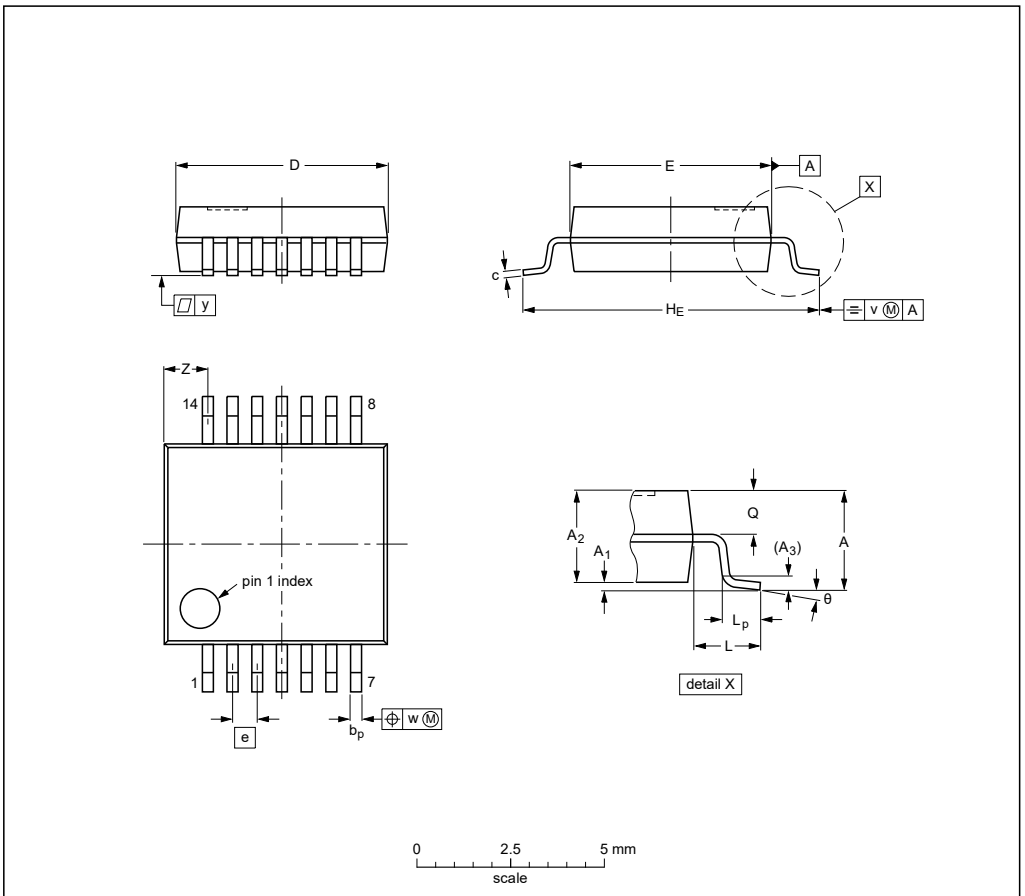
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig. 8. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

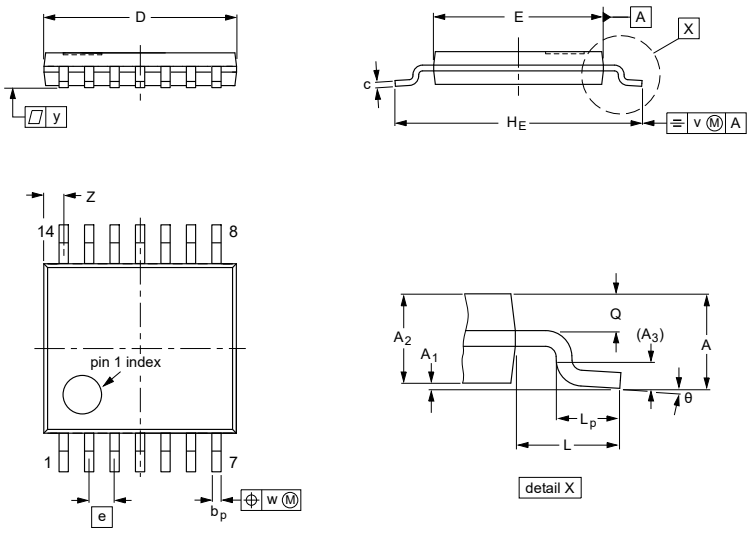
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig. 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

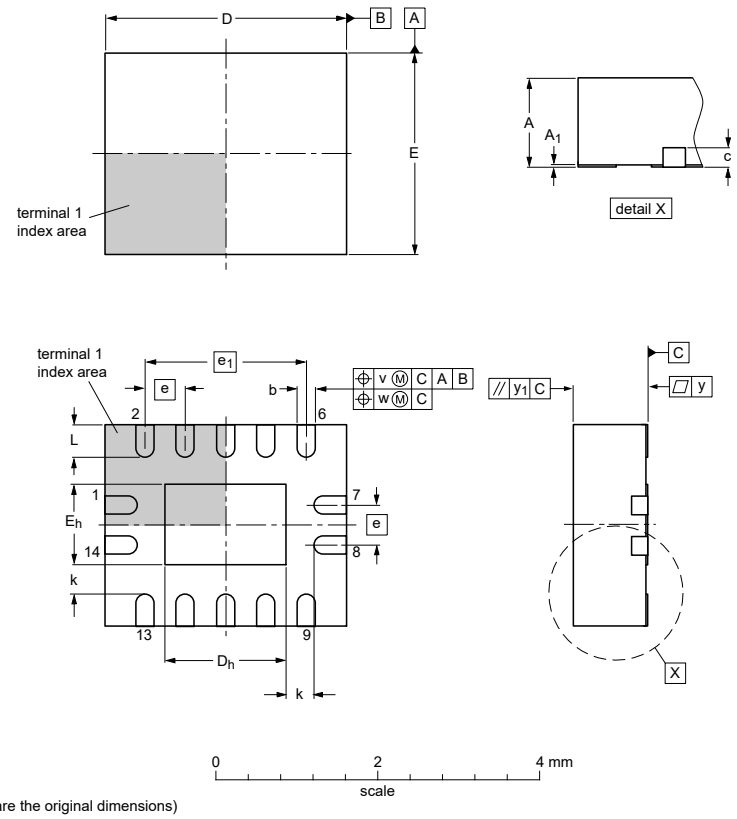
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT02 v.6	20200407	Product data sheet	-	74HC_HCT02 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Table 4: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT02 v.5	20151126	Product data sheet	-	74HC_HCT02 v.4
Modifications:	• Type numbers 74HC02N and 74HCT02N (SOT27-1) removed.			
74HC_HCT02 v.4	20120904	Product data sheet	-	74HC_HCT02 v.3
Modifications:	• Conditions for V_{OH}, I_I and I_{CC} updated to the family specification (errata).			
74HC_HCT02 v.3	20080918	Product data sheet	-	74HC_HCT02_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added type numbers 74HC02BQ and 74HCT02BQ (DHVQFN14 package)			
74HC_HCT02_CNV v.2	19970827	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Contents

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For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 7 April 2020

6.5. Hoja de Fabricante SN74LVC1G80

SN74LVC1G80 Single Positive-Edge-Triggered D-Type Flip-Flop

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V_{CC}
- Maximum t_{pd} of 4.2 ns at 3.3 V
- Low Power Consumption, 10-µA Maximum I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Test and Measurement
- Enterprise Switching
- Telecom Infrastructure
- Motor Drives

3 Description

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the $\overline{Q}$ output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

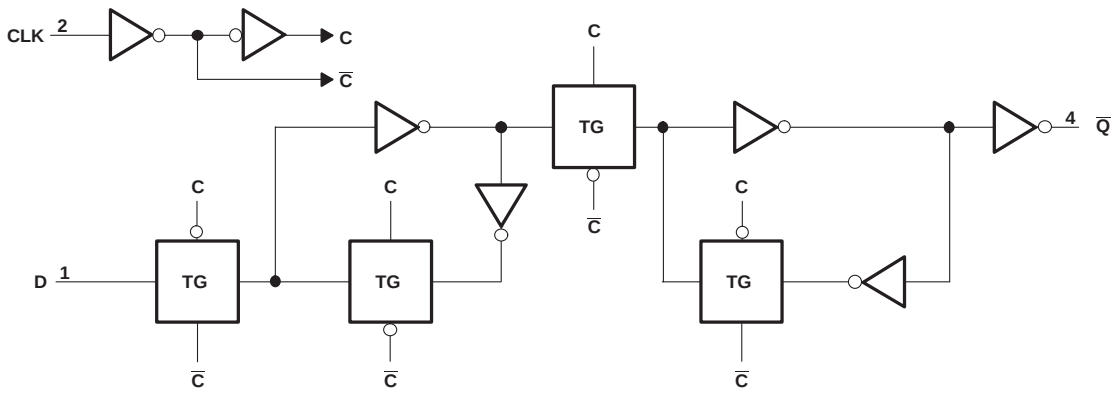
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G80DBV	SOT-23 (5)	2.90 mm × 1.60 mm
SN74LVC1G80DCK	SC70 (5)	2.00 mm × 1.25 mm
SN74LVC1G80YZP	DSBGA (5)	1.41 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



(1) TG - Transmission Gate

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (December 2013) to Revision S **Page**

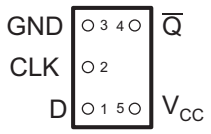
- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added max junction temperature to the *Recommended Operating Conditions* table ... 5
- Added operating free-air temperature for YZP package to the *Recommended Operating Conditions* table ... 5
- Changed $R_{\theta JA}$ value for DBV package from: 206°C/W to: 243.4°C/W ... 5
- Changed $R_{\theta JA}$ value for DCK package from: 252°C/W to: 278.9°C/W ... 5
- Changed $R_{\theta JA}$ value for YZP package from: 132°C/W to: 136.9°C/W ... 5

Changes from Revision Q (January 2007) to Revision R **Page**

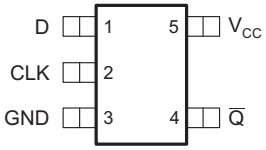
- Updated document to new TI data sheet format. ... 1
- Removed *Ordering Information* table. ... 1
- Updated I_{off} in *Features*. ... 1
- Updated operating temperature range. ... 4
- Added ESD warning ... 15

5 Pin Configuration and Functions

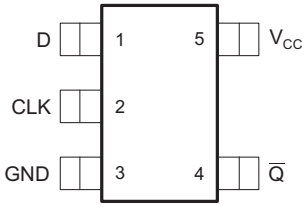
YZP Package
5-Pin DSBGA
Bottom View



DCK Package
5-Pin SC70
Top View



DBV Package
5-Pin SOT-23
Top View



Pin Functions(1)

PIN		I/O	DESCRIPTION
NO.	NAME		
1	D	I	Data input
2	CLK	I	Clocking input
3	GND	—	Ground pin
4	$\overline{Q}$	O	Flip-flop output
5	V_{CC}	—	Power pin

(1) See *Mechanical, Packaging, and Orderable Information* for dimensions

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_J	Junction temperature			150	°C
T_A	Operating free-air temperature	DBV and DCK packages	–40	125	°C
		YZP package	–40	85	

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G80			UNIT
		DBV (SOT-23)	DCK (SC70)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	243.4	278.9	136.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	179	121.3	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.6	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	58.4	7.5	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77	64.9	32.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		1.65 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –4 mA		1.65 V	1.2			
		I_{OH} = –8 mA		2.3 V	1.9			
		I_{OH} = –16 mA		3 V	2.4			
		I_{OH} = –24 mA			2.3			
		I_{OH} = –32 mA		4.5 V	3.8			
V_{OL}		I_{OL} = 100 µA		1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V			0.3	
		I_{OL} = 16 mA		3 V			0.4	
		I_{OL} = 24 mA					0.55	
		I_{OL} = 32 mA		4.5 V			0.55	
I_I	CLK or D inputs	V_I = 5.5 V or GND		0 to 5.5 V			±10	µA
I_{off}		V_I or V_O = 5.5 V		0			±10	µA
I_{CC}		V_I = 5.5 V or GND,	I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 5.5 V			500	µA
C_i		V_I = V_{CC} or GND	T_A = –40°C to 85°C	3.3 V		3.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Timing Requirements: T_A = –40°C to +85°C

over recommended operating free-air temperature range, T_A = –40°C to +85°C (unless otherwise noted) (see Figure 2)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 1.8 V ± 0.15 V		160	MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_w	Pulse duration, CLK high or low		V_{CC} = 1.8 V ± 0.15 V	2.5		ns
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_{su}	Setup time before CLK↑	Data high	V_{CC} = 1.8 V ± 0.15 V	2.3		ns
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
		Data low	V_{CC} = 1.8 V ± 0.15 V	2.5		
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
t_h	Hold time, data after CLK↑		V_{CC} = 1.8 V ± 0.15 V	0		ns
			V_{CC} = 2.5 V ± 0.2 V	0.2		
			V_{CC} = 3.3 V ± 0.3 V	0.9		
			V_{CC} = 5.5 V ± 0.5 V	0.4		

6.7 Timing Requirements: T_A = –40°C to +125°C

over recommended operating free-air temperature range, T_A = –40°C to +125°C (unless otherwise noted) (see Figure 2)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 1.8 V ± 0.15 V		160	MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_w	Pulse duration, CLK high or low		V_{CC} = 1.8 V ± 0.15 V	2.5		ns
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_{su}	Setup time before CLK↑	Data high	V_{CC} = 1.8 V ± 0.15 V	2.3		ns
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
		Data low	V_{CC} = 1.8 V ± 0.15 V	2.5		
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
t_h	Hold time, data after CLK↑		V_{CC} = 1.8 V ± 0.15 V	0		ns
			V_{CC} = 2.5 V ± 0.2 V	0.2		
			V_{CC} = 3.3 V ± 0.3 V	0.9		
			V_{CC} = 5.5 V ± 0.5 V	0.4		

6.8 Switching Characteristics: T_A = –40°C to +85°C, C_L = 15 pF

over recommended operating free-air temperature range, T_A = –40°C to +85°C, C_L = 15 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8 V ± 0.15 V	160		MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5 V ± 0.5 V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	3	9.1	ns
			V_{CC} = 2.5 V ± 0.2 V	1.5	6	
			V_{CC} = 3.3 V ± 0.3 V	1.3	4.2	
			V_{CC} = 5 V ± 0.5 V	1.1	3.8	

6.9 Switching Characteristics: T_A = –40°C to +85°C, C_L = 30 pF or 50 pF

over recommended operating free-air temperature range, T_A = –40°C to +85°C, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8 V ± 0.15 V	160		MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5 V ± 0.5 V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	4.4	9.9	ns
			V_{CC} = 2.5 V ± 0.2 V	2.3	7	
			V_{CC} = 3.3 V ± 0.3 V	2	5.2	
			V_{CC} = 5 V ± 0.5 V	1.3	4.5	

6.10 Switching Characteristics: T_A = –40°C to +125°C, C_L = 30 pF or 50 pF

over recommended operating free-air temperature range, T_A = –40°C to +125°C, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8 V ± 0.15 V	160		MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5 V ± 0.5 V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	4.4	12.5	ns
			V_{CC} = 2.5 V ± 0.2 V	2.3	8.5	
			V_{CC} = 3.3 V ± 0.3 V	2	6	
			V_{CC} = 5 V ± 0.5 V	1.3	5.5	

6.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	V_{CC} = 1.8 V	24	pF
			V_{CC} = 2.5 V	24	
			V_{CC} = 3.3 V	25	
			V_{CC} = 5 V	27	

6.12 Typical Characteristics

This plot shows the different I_{CC} values for various voltages on the data input (D). Voltage sweep on the input is from 0 V to 7 V. V_{CC} = 5 V.

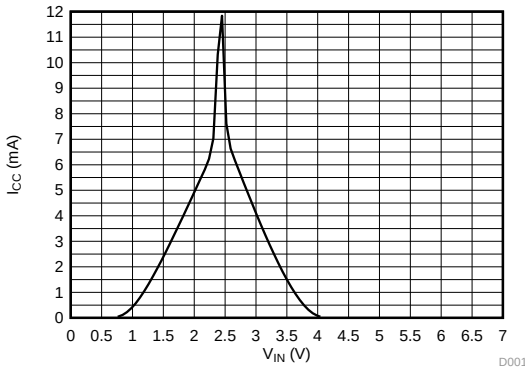


Figure 1. I_{CC} vs V_{IN}

6.6. Resultados conductual

```
time=     0, Simulation Start
time=     0, Starting Reset
time=    52, Reset Completed
time=    52, Starting Test
time=    52, Starting Semi Random Test
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
time=   132, Starting Completely Random Test
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
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PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
time=  396, Starting Scripted Test
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
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PASS
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PASS

```
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
time= 1232, Test Completed
time= 1232, Simulation Completed
```

6.7. Extracto de resultados sintetizado a 2ns

```
time=     0, Simulation Start
time=     0, Starting Reset
time=    52, Reset Completed
time=    52, Starting Test
time=    52, Starting Semi Random Test
Time=56 Error dut: Q=xxxx, rco=1, scoreboard: Q=0000, rco=1
Time=60 Error dut: Q=xxx1, rco=1, scoreboard: Q=0000, rco=1
Time=64 Error dut: Q=xxx1, rco=1, scoreboard: Q=0001, rco=0
Time=68 Error dut: Q=xxx1, rco=1, scoreboard: Q=0010, rco=0
Time=72 Error dut: Q=xxx1, rco=1, scoreboard: Q=0011, rco=0
Time=76 Error dut: Q=xxx1, rco=1, scoreboard: Q=0100, rco=0
Time=80 Error dut: Q=1111, rco=1, scoreboard: Q=0100, rco=0
Time=84 Error dut: Q=1111, rco=1, scoreboard: Q=0101, rco=0
Time=88 Error dut: Q=1111, rco=1, scoreboard: Q=0110, rco=0
Time=92 Error dut: Q=1111, rco=0, scoreboard: Q=0111, rco=0
time=  132, Starting Completely Random Test
Time=136 Error dut: Q=xx00, rco=x, scoreboard: Q=1011, rco=0
Time=140 Error dut: Q=xx00, rco=x, scoreboard: Q=0011, rco=1
Time=144 Error dut: Q=xx00, rco=x, scoreboard: Q=0010, rco=1
Time=148 Error dut: Q=xx00, rco=x, scoreboard: Q=0010, rco=1
Time=152 Error dut: Q=xx01, rco=x, scoreboard: Q=0011, rco=1
Time=156 Error dut: Q=1111, rco=0, scoreboard: Q=0011, rco=1
Time=160 Error dut: Q=1111, rco=0, scoreboard: Q=0011, rco=1
Time=164 Error dut: Q=1111, rco=0, scoreboard: Q=0011, rco=1
Time=168 Error dut: Q=1111, rco=0, scoreboard: Q=0011, rco=1
Time=172 Error dut: Q=1111, rco=0, scoreboard: Q=1011, rco=1
Time=176 Error dut: Q=1111, rco=0, scoreboard: Q=1011, rco=1
Time=180 Error dut: Q=x001, rco=0, scoreboard: Q=1011, rco=1
Time=184 Error dut: Q=x001, rco=0, scoreboard: Q=1011, rco=1
Time=188 Error dut: Q=x001, rco=0, scoreboard: Q=1000, rco=0
Time=192 Error dut: Q=x001, rco=0, scoreboard: Q=0101, rco=0
Time=196 Error dut: Q=1111, rco=0, scoreboard: Q=0010, rco=0
Time=200 Error dut: Q=1111, rco=0, scoreboard: Q=0010, rco=0
Time=204 Error dut: Q=1111, rco=0, scoreboard: Q=1111, rco=1
PASS
Time=212 Error dut: Q=1111, rco=1, scoreboard: Q=1100, rco=0
Time=216 Error dut: Q=1110, rco=1, scoreboard: Q=1100, rco=0
Time=220 Error dut: Q=1110, rco=0, scoreboard: Q=1001, rco=0
Time=224 Error dut: Q=1110, rco=0, scoreboard: Q=0110, rco=0
Time=228 Error dut: Q=1110, rco=0, scoreboard: Q=0101, rco=0
Time=232 Error dut: Q=1110, rco=0, scoreboard: Q=0101, rco=0
Time=236 Error dut: Q=1110, rco=0, scoreboard: Q=0100, rco=0
Time=240 Error dut: Q=1100, rco=0, scoreboard: Q=0100, rco=0
Time=244 Error dut: Q=1100, rco=0, scoreboard: Q=0100, rco=0
```

```
Time=248 Error dut: Q=1100, rco=0, scoreboard: Q=0011, rco=0
Time=252 Error dut: Q=1000, rco=0, scoreboard: Q=0011, rco=0
Time=256 Error dut: Q=1000, rco=0, scoreboard: Q=0010, rco=0
Time=260 Error dut: Q=1000, rco=0, scoreboard: Q=0001, rco=0
Time=264 Error dut: Q=1000, rco=1, scoreboard: Q=0001, rco=0
Time=268 Error dut: Q=1001, rco=1, scoreboard: Q=0000, rco=0
Time=272 Error dut: Q=1001, rco=1, scoreboard: Q=1101, rco=1
Time=276 Error dut: Q=1001, rco=1, scoreboard: Q=1101, rco=1
Time=280 Error dut: Q=1001, rco=0, scoreboard: Q=1101, rco=1
Time=284 Error dut: Q=1001, rco=0, scoreboard: Q=1101, rco=1
Time=288 Error dut: Q=1001, rco=0, scoreboard: Q=1010, rco=0
Time=292 Error dut: Q=1001, rco=0, scoreboard: Q=0111, rco=0
Time=296 Error dut: Q=0001, rco=0, scoreboard: Q=0100, rco=0
PASS
Time=304 Error dut: Q=0001, rco=1, scoreboard: Q=0001, rco=0
Time=308 Error dut: Q=0011, rco=1, scoreboard: Q=1110, rco=1
Time=312 Error dut: Q=0011, rco=1, scoreboard: Q=1110, rco=1
Time=316 Error dut: Q=0010, rco=0, scoreboard: Q=1110, rco=1
Time=320 Error dut: Q=0010, rco=0, scoreboard: Q=1101, rco=0
Time=324 Error dut: Q=1110, rco=0, scoreboard: Q=1101, rco=0
Time=328 Error dut: Q=1110, rco=0, scoreboard: Q=1101, rco=0
Time=332 Error dut: Q=1110, rco=0, scoreboard: Q=1101, rco=0
Time=336 Error dut: Q=1110, rco=0, scoreboard: Q=1101, rco=0
Time=340 Error dut: Q=1110, rco=0, scoreboard: Q=1100, rco=0
Time=344 Error dut: Q=1110, rco=0, scoreboard: Q=1100, rco=0
Time=348 Error dut: Q=1110, rco=0, scoreboard: Q=1100, rco=0
time=  396, Starting Scripted Test
Time=400 Error dut: Q=1110, rco=0, scoreboard: Q=1110, rco=1
PASS
Time=408 Error dut: Q=1111, rco=0, scoreboard: Q=0000, rco=1
Time=412 Error dut: Q=1110, rco=1, scoreboard: Q=0001, rco=0
Time=416 Error dut: Q=1110, rco=1, scoreboard: Q=0010, rco=0
Time=420 Error dut: Q=1110, rco=1, scoreboard: Q=0011, rco=0
Time=424 Error dut: Q=1110, rco=1, scoreboard: Q=0100, rco=0
Time=428 Error dut: Q=1110, rco=1, scoreboard: Q=0101, rco=0
Time=432 Error dut: Q=1110, rco=1, scoreboard: Q=0110, rco=0
Time=436 Error dut: Q=1110, rco=1, scoreboard: Q=0111, rco=0
Time=440 Error dut: Q=1110, rco=0, scoreboard: Q=1000, rco=0
Time=444 Error dut: Q=1111, rco=0, scoreboard: Q=1001, rco=0
Time=448 Error dut: Q=1111, rco=0, scoreboard: Q=1010, rco=0
Time=452 Error dut: Q=1111, rco=0, scoreboard: Q=1011, rco=0
Time=456 Error dut: Q=0111, rco=0, scoreboard: Q=1100, rco=0
Time=460 Error dut: Q=0111, rco=0, scoreboard: Q=1101, rco=0
Time=464 Error dut: Q=0111, rco=0, scoreboard: Q=1110, rco=0
PASS
```

6.8. Extracto de resultados sintetizado a 4ns

```
time=     0, Simulation Start
time=     0, Starting Reset
time=    64, Reset Completed
time=    64, Starting Test
time=    64, Starting Semi Random Test
Time=72 Error dut: Q=xxx1, rco=1, scoreboard: Q=0000, rco=1
Time=80 Error dut: Q=1111, rco=1, scoreboard: Q=0000, rco=1
Time=88 Error dut: Q=1111, rco=1, scoreboard: Q=0001, rco=0
Time=96 Error dut: Q=1110, rco=1, scoreboard: Q=0010, rco=0
Time=104 Error dut: Q=1111, rco=x, scoreboard: Q=0011, rco=0
Time=112 Error dut: Q=1111, rco=x, scoreboard: Q=0100, rco=0
Time=120 Error dut: Q=1110, rco=x, scoreboard: Q=0100, rco=0
Time=128 Error dut: Q=xx00, rco=x, scoreboard: Q=0101, rco=0
Time=136 Error dut: Q=xx00, rco=x, scoreboard: Q=0110, rco=0
Time=144 Error dut: Q=x000, rco=1, scoreboard: Q=0111, rco=0
time=  224, Starting Completely Random Test
Time=232 Error dut: Q=0010, rco=0, scoreboard: Q=1011, rco=0
Time=240 Error dut: Q=0010, rco=0, scoreboard: Q=0011, rco=1
Time=248 Error dut: Q=1110, rco=0, scoreboard: Q=0010, rco=1
Time=256 Error dut: Q=1111, rco=0, scoreboard: Q=0010, rco=1
Time=264 Error dut: Q=1111, rco=0, scoreboard: Q=0011, rco=1
Time=272 Error dut: Q=1100, rco=1, scoreboard: Q=0011, rco=1
Time=280 Error dut: Q=1000, rco=1, scoreboard: Q=0011, rco=1
Time=288 Error dut: Q=1000, rco=1, scoreboard: Q=0011, rco=1
Time=296 Error dut: Q=1000, rco=1, scoreboard: Q=0011, rco=1
Time=304 Error dut: Q=1000, rco=1, scoreboard: Q=1011, rco=1
Time=312 Error dut: Q=1000, rco=1, scoreboard: Q=1011, rco=1
Time=320 Error dut: Q=1000, rco=1, scoreboard: Q=1011, rco=1
Time=328 Error dut: Q=1000, rco=1, scoreboard: Q=1011, rco=1
Time=336 Error dut: Q=1000, rco=1, scoreboard: Q=1000, rco=0
Time=344 Error dut: Q=1000, rco=1, scoreboard: Q=0101, rco=0
Time=352 Error dut: Q=1110, rco=1, scoreboard: Q=0010, rco=0
Time=360 Error dut: Q=1111, rco=0, scoreboard: Q=0010, rco=0
Time=368 Error dut: Q=1111, rco=0, scoreboard: Q=1111, rco=1
Time=376 Error dut: Q=1100, rco=0, scoreboard: Q=1111, rco=1
Time=384 Error dut: Q=0101, rco=0, scoreboard: Q=1100, rco=0
Time=392 Error dut: Q=0100, rco=0, scoreboard: Q=1100, rco=0
Time=400 Error dut: Q=0100, rco=0, scoreboard: Q=1001, rco=0
Time=408 Error dut: Q=1110, rco=0, scoreboard: Q=0110, rco=0
Time=416 Error dut: Q=1110, rco=0, scoreboard: Q=0101, rco=0
Time=424 Error dut: Q=1110, rco=0, scoreboard: Q=0101, rco=0
Time=432 Error dut: Q=0111, rco=0, scoreboard: Q=0100, rco=0
PASS
```

6.9. Extracto de resultados sintetizado a 20ns

```
time=     0, Simulation Start
time=     0, Starting Reset
time=   160, Reset Completed
time=   160, Starting Test
time=   160, Starting Semi Random Test
Time=200 Error dut: Q=1111, rco=1, scoreboard: Q=0000, rco=1
Time=240 Error dut: Q=1110, rco=1, scoreboard: Q=0000, rco=1
Time=280 Error dut: Q=1111, rco=1, scoreboard: Q=0001, rco=0
Time=320 Error dut: Q=1111, rco=0, scoreboard: Q=0010, rco=0
Time=360 Error dut: Q=0000, rco=1, scoreboard: Q=0011, rco=0
Time=400 Error dut: Q=0001, rco=1, scoreboard: Q=0100, rco=0
Time=440 Error dut: Q=0000, rco=0, scoreboard: Q=0100, rco=0
Time=480 Error dut: Q=1111, rco=0, scoreboard: Q=0101, rco=0
Time=520 Error dut: Q=0001, rco=0, scoreboard: Q=0110, rco=0
Time=560 Error dut: Q=0000, rco=1, scoreboard: Q=0111, rco=0
time=   960, Starting Completely Random Test
Time=1000 Error dut: Q=1111, rco=0, scoreboard: Q=1011, rco=0
Time=1040 Error dut: Q=0001, rco=0, scoreboard: Q=0011, rco=1
Time=1080 Error dut: Q=0001, rco=1, scoreboard: Q=0010, rco=1
Time=1120 Error dut: Q=0000, rco=1, scoreboard: Q=0010, rco=1
Time=1160 Error dut: Q=1111, rco=1, scoreboard: Q=0011, rco=1
Time=1200 Error dut: Q=0010, rco=1, scoreboard: Q=0011, rco=1
Time=1240 Error dut: Q=0010, rco=1, scoreboard: Q=0011, rco=1
Time=1280 Error dut: Q=0010, rco=1, scoreboard: Q=0011, rco=1
Time=1320 Error dut: Q=0010, rco=1, scoreboard: Q=0011, rco=1
Time=1360 Error dut: Q=1110, rco=1, scoreboard: Q=1011, rco=1
Time=1400 Error dut: Q=1010, rco=1, scoreboard: Q=1011, rco=1
Time=1440 Error dut: Q=1010, rco=1, scoreboard: Q=1011, rco=1
Time=1480 Error dut: Q=1010, rco=1, scoreboard: Q=1011, rco=1
Time=1520 Error dut: Q=1111, rco=1, scoreboard: Q=1000, rco=0
Time=1560 Error dut: Q=0111, rco=0, scoreboard: Q=0101, rco=0
Time=1600 Error dut: Q=0100, rco=0, scoreboard: Q=0010, rco=0
Time=1640 Error dut: Q=0100, rco=0, scoreboard: Q=0010, rco=0
Time=1680 Error dut: Q=1111, rco=0, scoreboard: Q=1111, rco=1
Time=1720 Error dut: Q=1000, rco=0, scoreboard: Q=1111, rco=1
Time=1760 Error dut: Q=1111, rco=0, scoreboard: Q=1100, rco=0
Time=1800 Error dut: Q=0100, rco=0, scoreboard: Q=1100, rco=0
Time=1840 Error dut: Q=1111, rco=0, scoreboard: Q=1001, rco=0
Time=1880 Error dut: Q=1001, rco=0, scoreboard: Q=0110, rco=0
Time=1920 Error dut: Q=1100, rco=0, scoreboard: Q=0101, rco=0
Time=1960 Error dut: Q=0000, rco=0, scoreboard: Q=0101, rco=0
Time=2000 Error dut: Q=1111, rco=0, scoreboard: Q=0100, rco=0
Time=2040 Error dut: Q=1110, rco=0, scoreboard: Q=0100, rco=0
Time=2080 Error dut: Q=1110, rco=0, scoreboard: Q=0100, rco=0
```

```
Time=2120 Error dut: Q=1111, rco=0, scoreboard: Q=0011, rco=0
Time=2160 Error dut: Q=1100, rco=0, scoreboard: Q=0011, rco=0
Time=2200 Error dut: Q=1111, rco=0, scoreboard: Q=0010, rco=0
Time=2240 Error dut: Q=1011, rco=0, scoreboard: Q=0001, rco=0
Time=2280 Error dut: Q=1010, rco=0, scoreboard: Q=0001, rco=0
Time=2320 Error dut: Q=1111, rco=0, scoreboard: Q=0000, rco=0
Time=2360 Error dut: Q=1001, rco=0, scoreboard: Q=1101, rco=1
Time=2400 Error dut: Q=1000, rco=0, scoreboard: Q=1101, rco=1
Time=2440 Error dut: Q=1000, rco=0, scoreboard: Q=1101, rco=1
Time=2480 Error dut: Q=1000, rco=0, scoreboard: Q=1101, rco=1
Time=2520 Error dut: Q=1111, rco=0, scoreboard: Q=1010, rco=0
Time=2560 Error dut: Q=0101, rco=0, scoreboard: Q=0111, rco=0
PASS
Time=2640 Error dut: Q=0011, rco=0, scoreboard: Q=0001, rco=0
Time=2680 Error dut: Q=0000, rco=0, scoreboard: Q=0001, rco=0
Time=2720 Error dut: Q=1111, rco=0, scoreboard: Q=1110, rco=1
Time=2760 Error dut: Q=1100, rco=0, scoreboard: Q=1110, rco=1
Time=2800 Error dut: Q=1100, rco=0, scoreboard: Q=1110, rco=1
Time=2840 Error dut: Q=1111, rco=0, scoreboard: Q=1101, rco=0
Time=2880 Error dut: Q=1010, rco=0, scoreboard: Q=1101, rco=0
Time=2920 Error dut: Q=1010, rco=0, scoreboard: Q=1101, rco=0
Time=2960 Error dut: Q=1010, rco=0, scoreboard: Q=1101, rco=0
Time=3000 Error dut: Q=1010, rco=0, scoreboard: Q=1101, rco=0
Time=3040 Error dut: Q=1111, rco=0, scoreboard: Q=1100, rco=0
Time=3080 Error dut: Q=1000, rco=0, scoreboard: Q=1100, rco=0
Time=3120 Error dut: Q=1000, rco=0, scoreboard: Q=1100, rco=0
time= 3600, Starting Scripted Test
Time=3640 Error dut: Q=1111, rco=1, scoreboard: Q=1110, rco=1
Time=3680 Error dut: Q=1110, rco=1, scoreboard: Q=1111, rco=0
Time=3720 Error dut: Q=0001, rco=1, scoreboard: Q=0000, rco=1
Time=3760 Error dut: Q=1111, rco=0, scoreboard: Q=0001, rco=0
PASS
Time=3840 Error dut: Q=0001, rco=1, scoreboard: Q=0001, rco=0
Time=3880 Error dut: Q=0001, rco=0, scoreboard: Q=0000, rco=0
Time=3920 Error dut: Q=0000, rco=0, scoreboard: Q=1101, rco=1
Time=3960 Error dut: Q=0111, rco=0, scoreboard: Q=1010, rco=0
Time=4000 Error dut: Q=1101, rco=1, scoreboard: Q=0111, rco=0
Time=4040 Error dut: Q=1100, rco=0, scoreboard: Q=0100, rco=0
Time=4080 Error dut: Q=1011, rco=0, scoreboard: Q=0001, rco=0
Time=4120 Error dut: Q=1001, rco=0, scoreboard: Q=1110, rco=1
Time=4160 Error dut: Q=1000, rco=0, scoreboard: Q=1111, rco=1
Time=4200 Error dut: Q=0001, rco=1, scoreboard: Q=0000, rco=1
Time=4240 Error dut: Q=1111, rco=0, scoreboard: Q=0001, rco=0
Time=4280 Error dut: Q=0010, rco=0, scoreboard: Q=0001, rco=0
Time=4320 Error dut: Q=0010, rco=0, scoreboard: Q=0001, rco=0
Time=4360 Error dut: Q=0010, rco=0, scoreboard: Q=0001, rco=0
```

```
Time=4400 Error dut: Q=1111, rco=0, scoreboard: Q=0010, rco=0
PASS
Time=4480 Error dut: Q=0000, rco=1, scoreboard: Q=0010, rco=0
Time=4520 Error dut: Q=0011, rco=0, scoreboard: Q=0001, rco=0
Time=4560 Error dut: Q=1111, rco=1, scoreboard: Q=0000, rco=0
Time=4600 Error dut: Q=1010, rco=0, scoreboard: Q=1111, rco=1
Time=4640 Error dut: Q=1111, rco=0, scoreboard: Q=1110, rco=0
```

6.10. Resultados sintetizado a 200ns

```
time=     0, Simulation Start
time=     0, Starting Reset
time= 1600, Reset Completed
time= 1600, Starting Test
time= 1600, Starting Semi Random Test
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
time= 9600, Starting Completely Random Test
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
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PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
time=36000, Starting Scripted Test
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
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PASS
PASS
PASS
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PASS
PASS
PASS

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PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
time=69200, Test Completed
time=69200, Simulation Completed
```