Hardware/Software Codesign Lab 3

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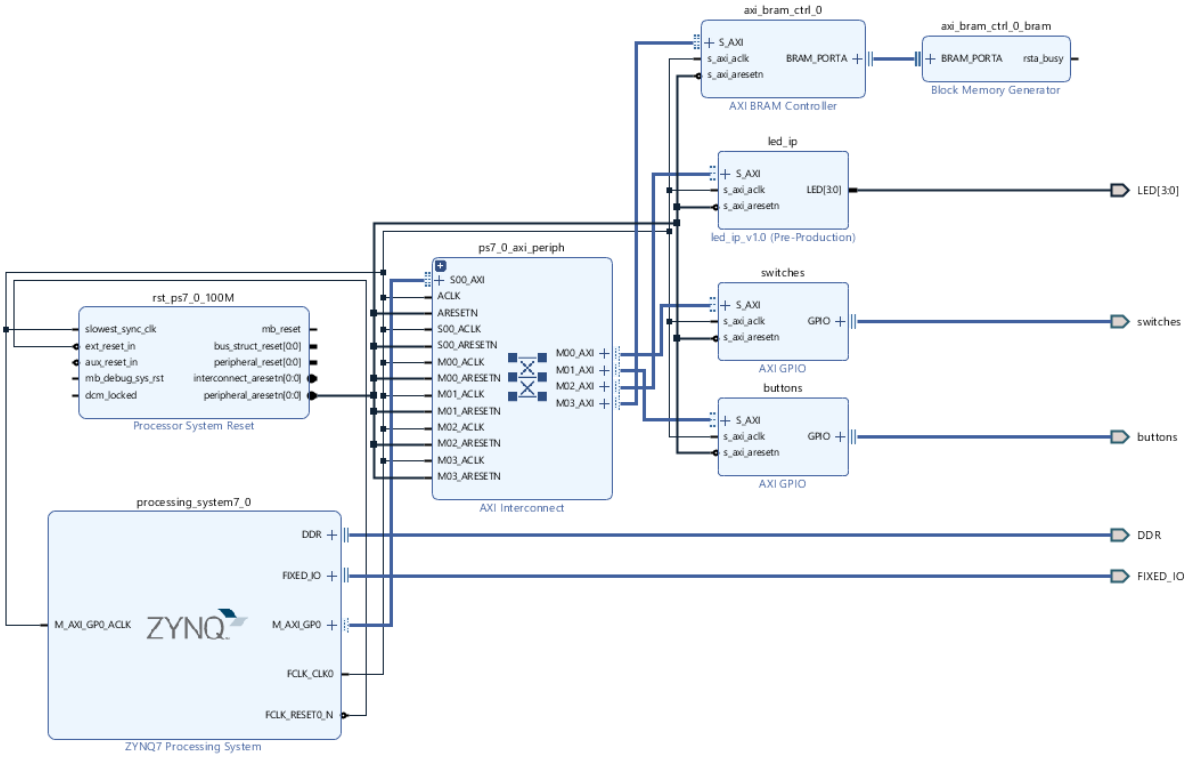
1. Follow the Lab 3 manual finish Lab 3.
2. Copy and paste the following information to the end of this document and submit this document:
   1) Block diagram for your hardware platform.



   2) peripheral memory map

Cell	Slave Interface	Base Name	Offset Address	Range	High Address
processing_system7_0					
Data (32 address bits : 0x40000000 [1G])					
buttons	S_AXI	Reg	0x4121_0000	64K	0x4121_FFFF
switches	S_AXI	Reg	0x4120_0000	64K	0x4120_FFFF
led_ip	S_AXI	S_AXI_reg	0x43C0_0000	64K	0x43C0_FFFF
axi_bra...	S_AXI	Mem0	0x4000_0000	8K	0x4000_1FFF

3) system.hdf: highlight information for the custom IP added and BRAM and BRAM controller.

system_wrapper_hw_platform_0 Hardware Platform Specification

Design Information

Target FPGA Device: 7z010
Part: xc7z010clg400-1
Created With: Vivado 2018.3
Created On: Sun Mar 10 17:17:52 2019

Address Map for processor ps7_cortexa9_[0-1]

Address Map for processor ps7_cortexa9_[0-1]

Cell	Base Addr	High Addr	Slave I/f	Mem/Reg
ps7_intc_dist_0	0xf8f010...	0xf8f01fff		REGISTER
ps7_scutimer_0	0xf8f006...	0xf8f0061f		REGISTER
ps7_slcr_0	0xf80000...	0xf8000fff		REGISTER
ps7_scuwdt_0	0xf8f006...	0xf8f006ff		REGISTER
ps7_l2cachec_0	0xf8f020...	0xf8f02fff		REGISTER
ps7_scuc_0	0xf8f000...	0xf8f000fc		REGISTER
led_ip	0x43c00...	0x43c0ffff	S_AXI	REGISTER
ps7_pmu_0	0xf88930...	0xf8893fff		REGISTER
ps7_afi_1	0xf80090...	0xf8009fff		REGISTER
ps7_afi_0	0xf80080...	0xf8008fff		REGISTER
ps7_afi_3	0xf800b...	0xf800bfff		REGISTER
ps7_afi_2	0xf800a0...	0xf800afff		REGISTER
ps7_globaltimer_0	0xf8f002...	0xf8f002ff		REGISTER
ps7_dma_s	0xf80030...	0xf8003fff		REGISTER
ps7_iop_bus_config_0	0xe0200...	0xe0200fff		REGISTER
ps7_xadc_0	0xf80071...	0xf80071...		REGISTER
ps7_ddr_0	0x00100...	0x3fffffff		MEMORY
ps7_ddrc_0	0xf80060...	0xf8006fff		REGISTER
ps7_ocmc_0	0xf800c0...	0xf800cfff		REGISTER
ps7_pl310_0	0xf8f020...	0xf8f02fff		REGISTER
ps7_uart_1	0xe0001...	0xe0001fff		REGISTER
ps7_coresight_comp_0	0xf88000...	0xf88fffff		REGISTER
axi_bram_ctrl_0	0x40000...	0x40001fff	S_AXI	MEMORY
ps7_scugic_0	0xf8f001...	0xf8f001ff		REGISTER
switches	0x41200...	0x4120ffff	S_AXI	REGISTER
ps7_dev_cfg_0	0xf80070...	0xf80070ff		REGISTER
ps7_dma_ns	0xf80040...	0xf8004fff		REGISTER
ps7_gpv_0	0xf89000...	0xf89fffff		REGISTER
ps7_ram_1	0xffff0000	0xffffdff		MEMORY
ps7_ram_0	0x00000...	0x0002ffff		MEMORY
buttons	0x41210...	0x4121ffff	S_AXI	REGISTER

IP blocks present in the design

ps7_0_axi_periph	axi_interconnect	2.1	
ps7_intc_dist_0	ps7_intc_dist	1.00.a	
axi_bram_ctrl_0_bram	blk_mem_gen	8.4	
rst_ps7_0_100M	proc_sys_reset	5.0	
ps7_scutimer_0	ps7_scutimer	1.00.a	
switches	axi_gpio	2.0	Registers
ps7_slcr_0	ps7_slcr	1.00.a	
ps7_scuwdt_0	ps7_scuwdt	1.00.a	
ps7_l2cachec_0	ps7_l2cachec	1.00.a	
ps7_scuc_0	ps7_scuc	1.00.a	
ps7_m_axi_gp0	ps7_m_axi_gp	1.00.a	
led_ip	led_ip	1.0	
ps7_pmu_0	ps7_pmu	1.00.a	
axi_bram_ctrl_0	axi_bram_ctrl	4.1	
ps7_afi_1	ps7_afi	1.00.a	
ps7_afi_0	ps7_afi	1.00.a	
ps7_afi_3	ps7_afi	1.00.a	
ps7_axi_interconnect_0	ps7_axi_interconnect	1.00.a	
ps7_globaltimer_0	ps7_globaltimer	1.00.a	
ps7_afi_2	ps7_afi	1.00.a	
ps7_dma_s	ps7_dma	1.00.a	
ps7_xadc_0	ps7_xadc	1.00.a	
ps7_iop_bus_config_0	ps7_iop_bus_config	1.00.a	
buttons	axi_gpio	2.0	Registers
ps7_ddr_0	ps7_ddr	1.00.a	
ps7_pl310_0	ps7_pl310	1.00.a	
ps7_ddrc_0	ps7_ddrc	1.00.a	
ps7_ocmc_0	ps7_ocmc	1.00.a	
ps7_uart_1	ps7_uart	1.00.a	
ps7_coresight_comp_0	ps7_coresight_comp	1.00.a	
ps7_cortexa9_1	ps7_cortexa9	5.2	
ps7_scugic_0	ps7_scugic	1.00.a	
processing_system7_0	processing_system7	5.5	
ps7_cortexa9_0	ps7_cortexa9	5.2	
ps7_clockc_0	ps7_clockc	1.00.a	
ps7_dev_cfg_0	ps7_dev_cfg	1.00.a	
ps7_dma_ns	ps7_dma	1.00.a	
ps7_gpv_0	ps7_gpv	1.00.a	
ps7_ram_1	ps7_ram	1.00.a	
ps7_ram_0	ps7_ram	1.00.a	

4) Pin assignment for the four LEDs

LED (4)	OUT					☑	35	LVCMOS33*	
LED[3]	OUT				D18	☑	35	LVCMOS33*	
LED[2]	OUT				G14	☑	35	LVCMOS33*	
LED[1]	OUT				M15	☑	35	LVCMOS33*	
LED[0]	OUT				M14	☑	35	LVCMOS33*	

3.300	12	SLOW	NONE	FP_VTT_50	
3.300	12	SLOW	NONE	FP_VTT_50	
3.300	12	SLOW	NONE	FP_VTT_50	
3.300	12	SLOW	NONE	FP_VTT_50	

3. Answer the following question:
   1) Which register in the custom IP is used to control the leds? Can we use a different one? Show the modified code to use a different register to control the leds.

      No, we cannot use a different register. The registers used in the custom IP to control the LEDs are S_axi read and write registers.

   2) Can we move the instantiation of lab3_user_logic from led_ip_v1_0_S_AXI.v to led_ip_v1_0, why or why not?

      No, we could not instantiate lab3_user_logic to led_ip_v1_0_S_AXI.v to led_ip_v1_0.v because of hierarchical design using Verilog. The top module is led_ip_v1_0.v and the bottom to modules are led_ip_v1_0_S_AXI and lab3_user_logic .