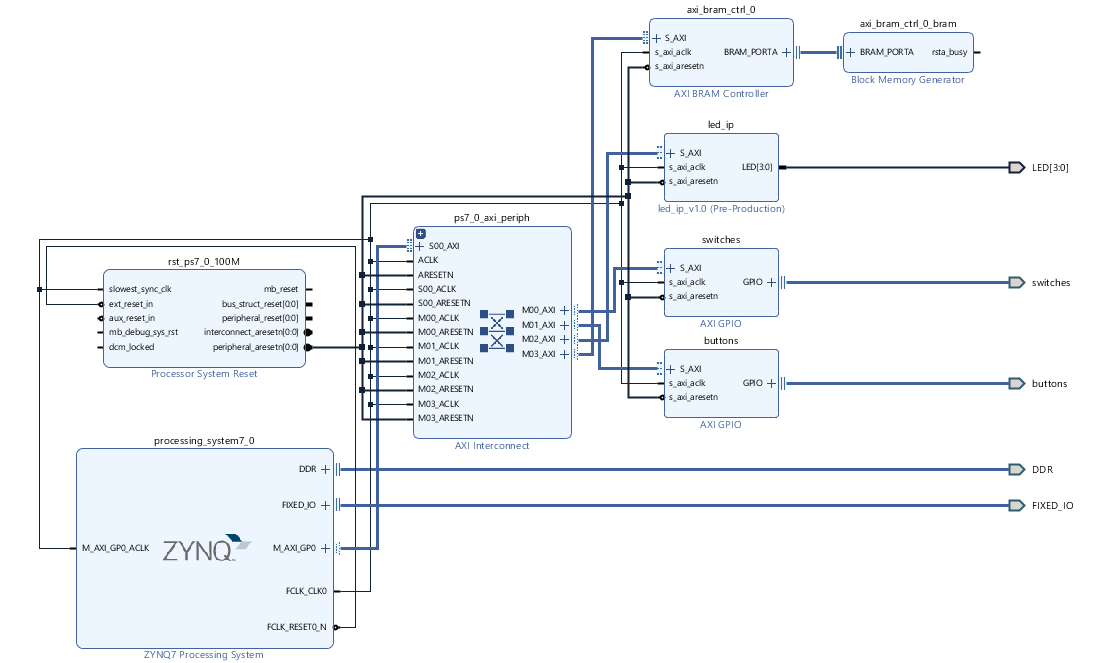
Hardware/Software Codesign Lab 3

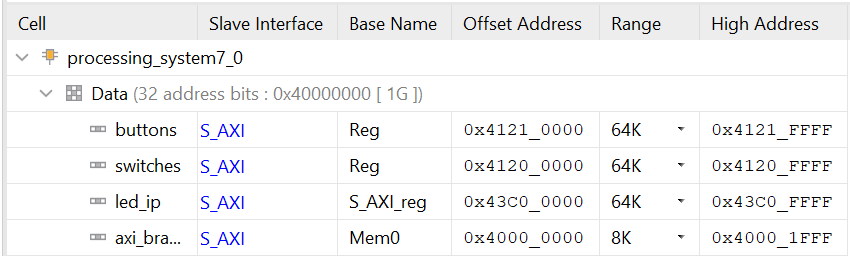
Student Name: Jose Sotelo

Student ID: 013969681

1. Follow the Lab 3 manual finish Lab 3.
2. Copy and paste the following information to the end of this document and submit this document:
3. Block diagram for your hardware platform.

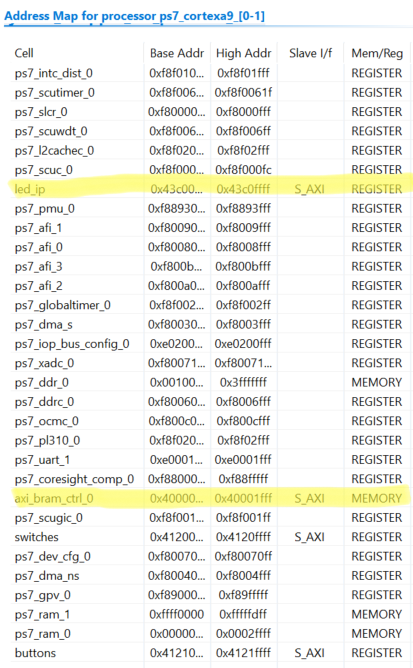


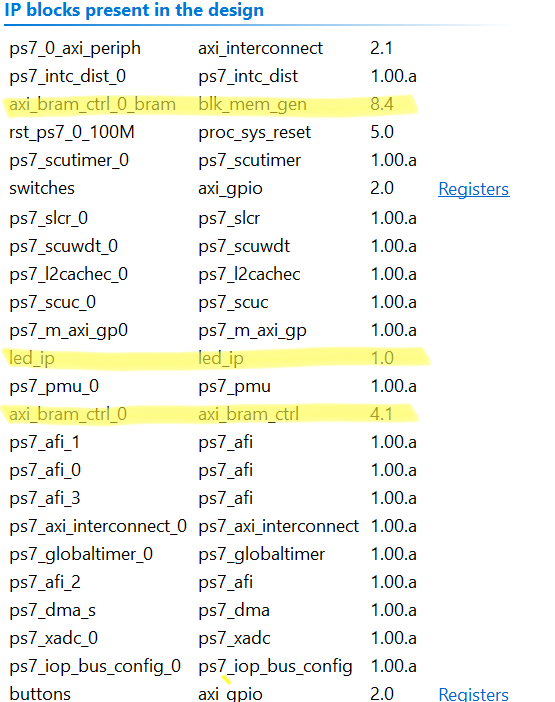
1. peripheral memory map

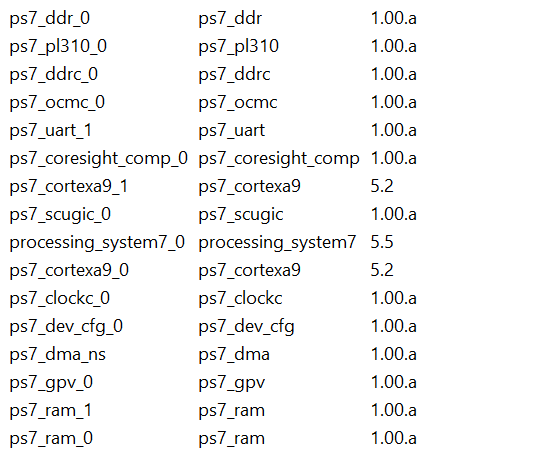


1. system.hdf: highlight information for the custom IP added and BRAM and BRAM controller.



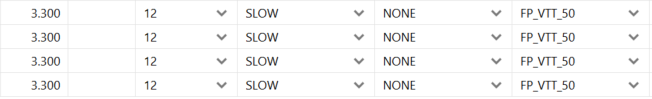






1. Pin assignment for the four LEDs





1. Answer the following question:
2. Which register in the custom IP is used to control the leds? Can we use a different one? Show the modified code to use a different register to control the leds.

No, we cannot use a different register. The registers used in the custom IP to control the LEDs are S\_axi read and write registers.

1. Can we move the instantiation of lab3\_user\_logic from led\_ip\_v1\_0\_S\_AXI.v to led\_ip\_v1\_0, why or why not?

No, we could not instantiate lab3\_user\_logic to led\_ip\_v1\_0\_S\_AXI.v to led\_ip\_v1\_0.v because of hierarchical design using Verilog. The top module is led\_ip\_v1\_0.v and the bottom to modules are led\_ip\_v1\_0\_S\_AXI and lab3\_user\_logic .