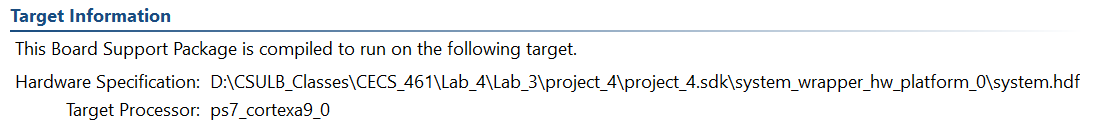
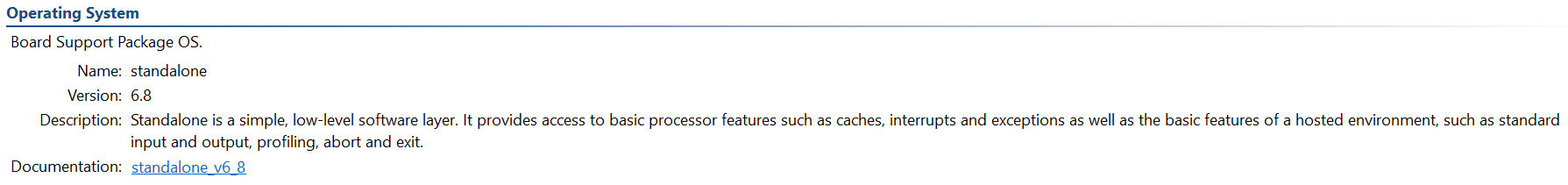
Hardware/Software Codesign Lab 4

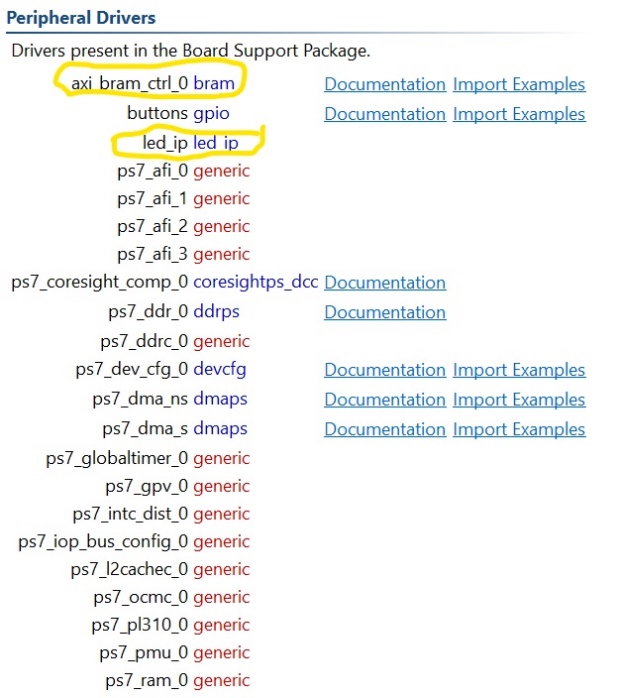
Student Name: Jose Sotelo

Student ID: 013969681

1. Follow the Lab 4 manual finish Lab 4.
2. Copy and paste the following information to the end of this document and submit this document:
3. system.mss: highlight information for the custom IP added and BRAM and BRAM controller.



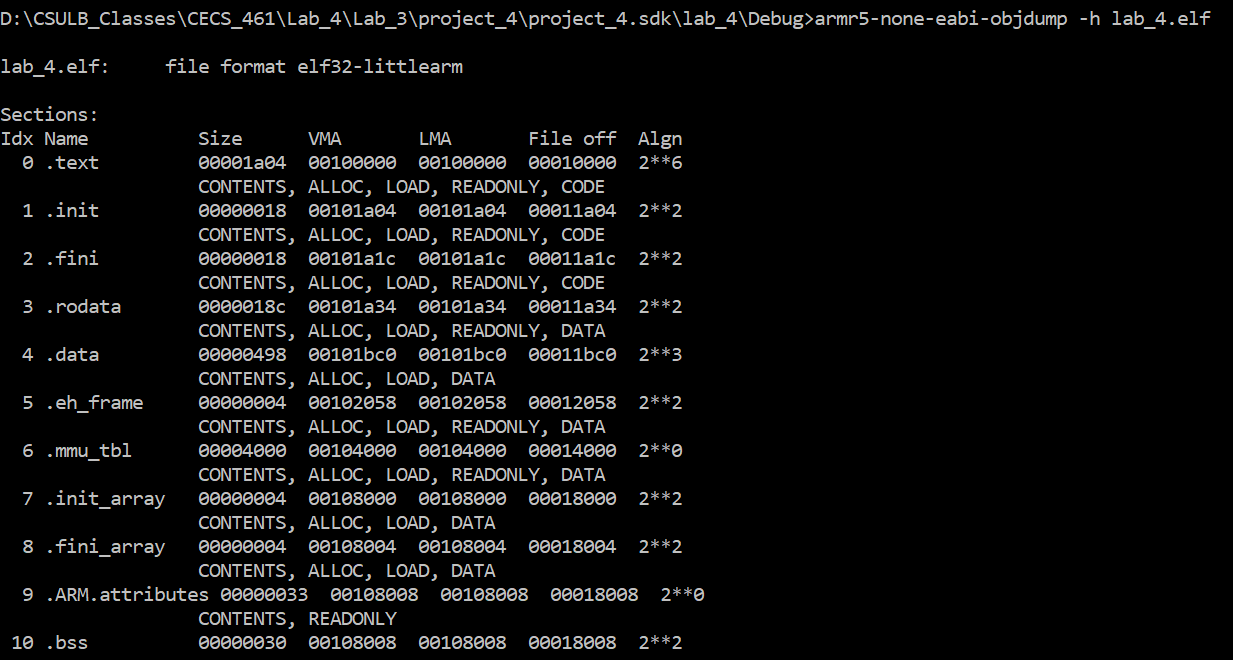


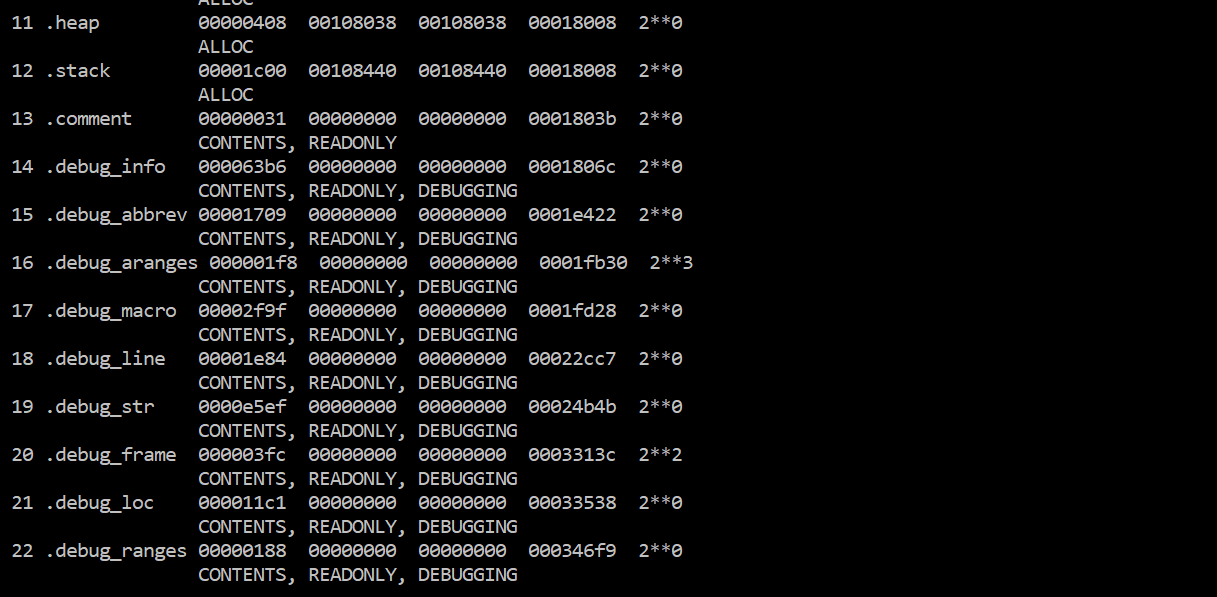




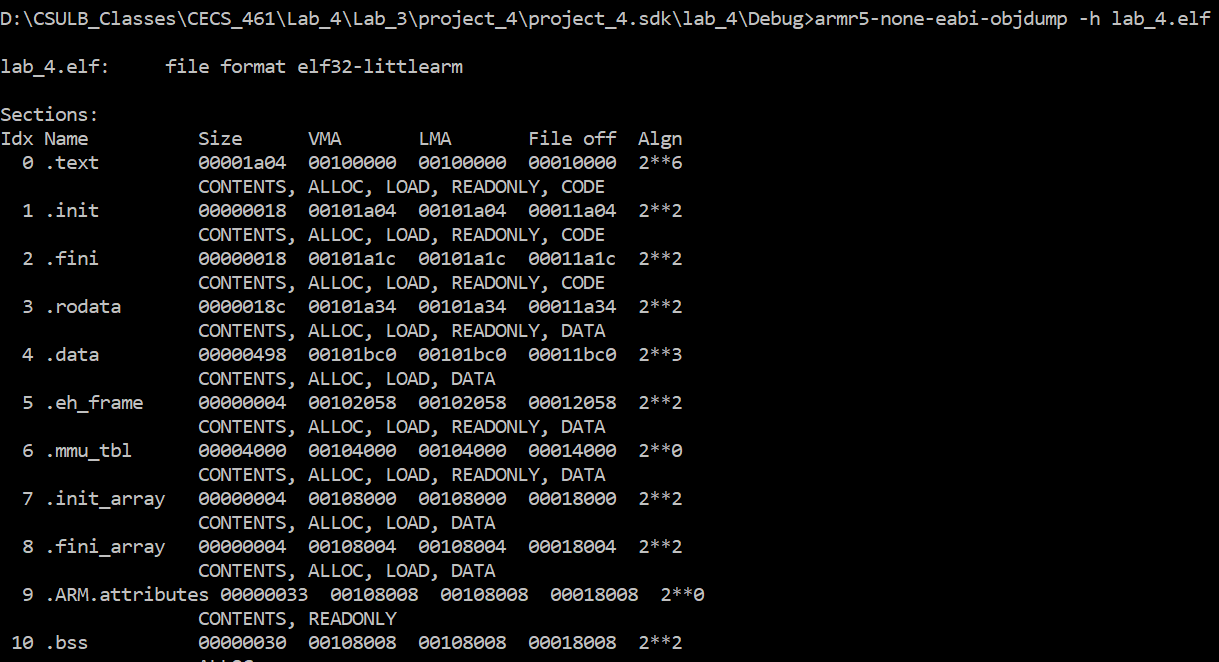
1. Memory dump information for two cases: Case 1: all four sections of executable are in DDR3; Case 2. code and data in DDR3, stack and heap in BRAM.

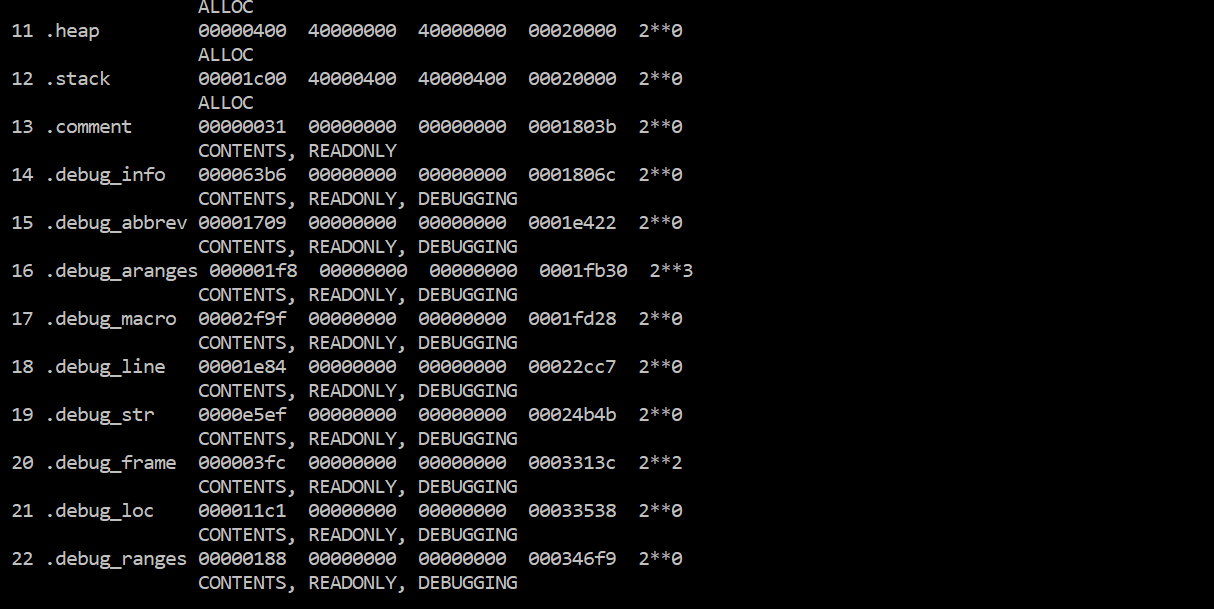
Case 1:





Case 2:





1. Answer the following question:
2. Specify the location(s) for the DDR3 Controller and DDR3 memory: inside [Xilinx Zynq-7000 (XC7Z010-1CLG400C)](http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices.html) or outside? If inside, specify if it is a hard core or soft cores and where does it locate in XC7Z010-1CLG400C: in PS or PL.

The DDR3 controller is located inside the Zynq PS, hard core.

The DDR3 Memory is located outside the Zynq.

1. Specify the location(s) for the AXI-BRAM Controller and BRAM in this lab: inside [Xilinx Zynq-7000 (XC7Z010-1CLG400C)](http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices.html) or outside? If inside, specify if it is a hard core or soft cores and where does it locate in XC7Z010-1CLG400C: in PS or PL.

The AXI-BRAM and BRAM are located both inside Zynq PL, soft core.

1. Specify the locations assigned to the code, data, stack and heap section of your software executable for the two linker script settings tested in the lab.

They are located in DDR3 Memory and in BRAM.

1. List all the external peripherals in the embedded system you build in this lab.

In this lab we used, LEDs, push buttons, dip switches, DDR3 Memory and UART.