Chip Specification Template

Prepared by:	Loc/Dept	Date:	Document Number and Filename	Revision:
C. Liebeck/J. Tramel	I/DES	January 11, 2002		1

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1 Introduction

This Chip Specification Template is intended to provide a starting point for capturing the design data for the chips developed at Valence Semiconductor. The design team should own the document. If a paragraph in the Template is not appropriate for the chip being documented then it should be omitted. If additional information is required it should be added. Any obvious omissions from the Template should be forwarded to the authors for inclusion in the next revision.

1.1 Purpose

The Purpose of this document is to specify the requirements of YourChip, and issues related to its development.

1.2 Scope

This document applies to all design centers and contracted design services of Valence Semiconductor, Inc. that are contributing to systems or sub-systems that may be included within a System-On-Chip (SOC) ASIC.

2 Applicable Documents

2.1 External Documents

2.1.1 Customer specifications

2.1.2 Industry standards

2.1.3 References

2.2 Internal Documents

2.2.1 Internally generated specifications

2.2.2 Applicable methodology documents

2.2.3 Chip test plan

2.2.4 Analyses or trade studies (includes MRD)

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3 Requirements

3.1.1 Performance Requirements
This section would define the performance requirements of the ASIC.

3.1.2 Interface Requirements
This section would define the interfaces of the ASIC and would distinguish between industry standard interfaces and custom interfaces. It should also define if subsets of interface standards are expected to be used rather that the complete standard.

3.1.3 Partitioning Requirements
This section should discuss any partitioning requirements imposed upon the architecture.

3.1.4 Physical Requirements
This section should define any limitations placed on the design with respect to gate count, pin count, etc.

3.1.5 Power Requirements
3.1.5.1 Power-on Requirements
3.1.5.2 Sleep Mode
3.1.5.3 Idle Mode
3.1.5.4 Power-down Mode

3.1.6 Environmental Requirements
This section should define the operating temperature requirements and any other constraints that might be imposed by the targeted environment. Commercial 0 – 70 C, Industrial 0 – 85 C, etc

4 Implementation

4.1 Design Description

4.2 Block Diagram

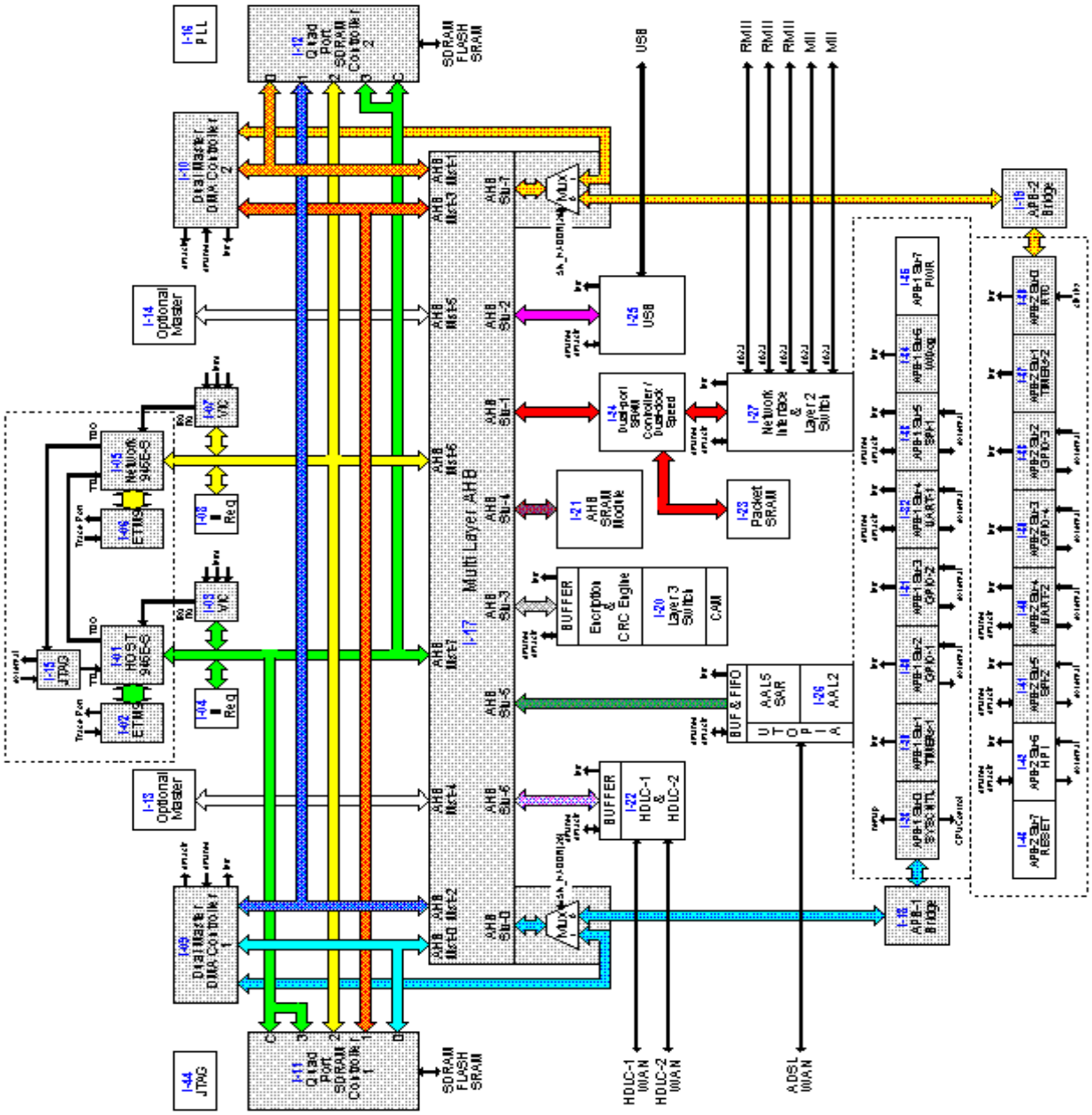

Figure 1 Chip Block Diagram

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4.3 Data Flow Description

The purpose of this section is to define the data flow into, through and out of the chip. It should include the definition of the data transfers at all major interfaces with a description of the data and the appropriate timing. The data movement within the chip along with the processing performed on the data should also be included.

The goal of this section is two-fold: 1) to assist the implementers of the design in understanding the requirements of the system and the inter-dependencies, and 2) to assist in the development of the verification environment for the chip. Care should be taken to ensure that the specification is not merely a “programmer’s guide” but rather a performance specification for the device.

4.4 Embedded Memories

This section should provide a summary of all memory cores and register files present in the design. All relevant information regarding the structures should be included. This information would detail memory dimensions, single-port vs. dual-port, multi-access, etc.

4.5 Input/Output Interface Description

4.5.1 Chip Mode Definition

Describe any alternate chip modes that will affect the chip IO. The example below uses scan mode as an example. When scan is enabled certain outputs switch from the "normal" use to another. This is where all such functionality is defined.

4.5.2 Pin List

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	PIN1	9	PIN9	17	PIN17	25	PIN25
…	…	…	…	…	…	…	…
8	PIN8	16	PIN16	24	PIN24	32	PIN32

Table 1 Pin List for 32 TQFP

PAD List and Bonding Table

Pad #	Side / Position	Name	I/O	Cell Name	Reset State	32 TQFP Pin #	Package 2 Pin #
1	B1	PAD1	I	pjd00n		1	
2	B2	PAD2	I	pjd00u		2	
3	B3	PAD3	O	plt01n		3	
4	B4	PAD4	O	plt03n		4	
5	B5	PAD5	O	pjt02n		NC	
6	B6	PAD6				NC	
…							
12	R1	PAD12				9	
…							
22	T1	PAD22				NC	
…							
33	L1	PAD33				25	
…							

Table 2 PAD List

I/O Type	Description	Reference
Ij	+5V Tolerant JTAG Input, C_{IN} = 8 pF	pjd00n
Ijpu	+5V Tolerant JTAG Input, internal 75k ± 25k Ω pull-up, C_{IN} = 8 pF	pjd00u
…		

Table 3 Description of I/O Types

Pad Signal Description

Name	I/O Type	Active State	BIT Pos.	Description
PAD2	I	HIGH		
PAD4	O			
PAD5	I	LOW		
PAD6	O			
PAD12	O	LOW		
PAD13	I	HIGH		
PAD14	I			
PAD15	O		MSB	
PAD17	O		LSB	

Table 4 Pad Signal Description

4.6 Address Memory Map

Section	Address Range
CPU Boot Address	0x0000_0000
I/O	0xC000_0000 ~ 0xFFFF_FFFF
MEM	0x0000_0000 ~ 0xBFFF_FFFF
VIC_1	0xFE00_0000 ~ 0xFFFF_FFFF
VIC_0	0xFE00_0000 ~ 0xFFFF_FFFF
ML-AHB	0xC000_0000 ~ 0xEFFF_FFFF
SDRAM_B	0x6000_0000 ~ 0xBFFF_FFFF
SDRAM_A	0x0000_0000 ~ 0x5FFF_FFFF

Table 5 Address Memory Map

4.7 Clocking

4.7.1 Oscillator Interface
The interface to the oscillator should be defined here.

4.7.2 Clocks
All clocks required within the system by mnemonic/frequency. This should also include a description of all interfaces between clock domains.

4.7.3 PLL
This should define the functionality of the PLL along with any associated timing budgets.

4.8 Reset

4.8.1 Reset Sources
Itemization of all resets required: power-on, software, etc.

4.8.2 Reset type
Each reset should be identified as HIGH or LOW active. Each reset should have its characteristic defined whether it is synchronous, asynchronous, asynchronous-in/synchronous-out, etc.

4.8.3 Timing Requirements
This section should define any specific startup timing requirements for the system. The following is a suggested list of issues to consider.

4.8.3.1 Initialization Routines
4.8.3.1.1 Embedded Processors
4.8.3.1.2 Analog Electronics
4.8.3.1.3 Memories

5 Externally Acquired Blocks

5.1 *BlockName* – (Repeat for each acquired block)

5.1.1 Description

5.1.2 Functional Requirements

5.1.3 Performance Requirements

5.1.4 Block diagram

5.1.5 I/O Definition

This should include an itemization of all I/O of the block. It should define the mnemonic of each signal and should specify whether it is an input or an output. Any specific timing requirements for each I/O should also be included.

5.1.6 I/O Timing

This should define the switching characteristics of the I/O of this block.

5.1.7 State Machine(s) Description

Where applicable.

5.1.8 Register Map Description

Type	Definition
R	Read only
W	Write only (not to be used)
RW	Read and Write
RC	Read and Clear

Table 4 Type Definition of Registers

Offset (0x)	Acronym	Type	Reset state (0x)	Description
00	BLK_CTRL	R/W	0000_0000	General block control
04	IF_PHASE	R	0000_0000	Output of IF NCO
1C	SOFT_RESET	R/W	0000_0000	Soft Reset Control Register

Register 1 Register map of DDC (Base address 0x0132_0d00)

Bits	Acronym	Reset state (0x)	Reset state
0	Rst_app	0	Soft reset control, which clears the entire block, excluding register bits. This bit is self -clearing. 0: no reset 1: reset (self clearing)
1	Rst_reg	0	Soft reset control, which clears only the control registers. This bit is self -clearing. 0: no reset 1: reset (self clearing)

Register 2 Bit description of register: SOFT_RESET (Offset 0x1C)

The format of this data should be adapted to best convey the most information about the contents of the registers. This information should include if the register is multi-port, byte writeable, special RESET considerations, etc

5.1.9 Verification Plan

5.1.9.1 Testbench Description

This paragraph should define the testbench created around the block. It should describe how each interface is being driven and should include all relevant information.

5.1.9.2 Itemization of Tests

This paragraph should define each of the tests performed during verification of the design of the block. It should include an accounting of which system requirements are being verified by each test.

6 Internally Developed Blocks (Digital)

6.1 *BlockName* – (Repeat for each developed block)

6.1.1 Description

6.1.2 Functional Requirements

6.1.3 Performance Requirements

6.1.4 Block Diagram

6.1.5 I/O Definition

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The format of this data should be adapted to best convey the most information about the contents of the registers. This information should include if the register is multi-port, byte writeable, special RESET considerations, etc.

6.1.9 Verification Plan

6.1.9.1 Testbench Descriptions

This paragraph should define the testbench created around the block. It should describe how each interface is being driven and should include all relevant information.

6.1.9.2 Itemization of Tests

This paragraph should define each of the tests performed during verification of the design of the block. It should include an accounting of which system requirements are being verified by each test.

6.1.10 Design For Reuse

6.1.10.1 Custom Design

This paragraph should justify the custom design of a block when there was the potential to either use a commercially available, silicon proven block instead.

6.1.10.2 Custom Interfaces

This paragraph should justify the custom design of an interface when there was the potential to use an industry standard interface instead.

7 Internally Developed Blocks (Analog)

7.1 *BlockName* – (Repeat for each developed block)

7.1.1 Description

Describe the function/purpose of the block.

7.1.2 Performance Requirements

Provide a detailed specification table; Example:

Parameter	Value
Supply Voltage	
Power Supply Noise	
Total Harmonic Distortion	
DC Offset Voltage	
SNR	
PSRR	
CMRR	
Load resistance at output	
Load Capacitance at output	
Power Consumption	

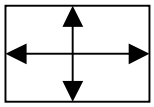
Table 7 Performance Requirements

7.1.3 Block Diagram

7.1.3.1 I/O Definition

This should include an itemization of all I/O of the block. It should define the mnemonic of each signal and should specify whether it is an input or an output. Any specific timing requirements for each I/O should also be included.

7.1.4 Block Physical Dimensions and Pinouts



7.1.5 Verification Plan

7.1.5.1 Testbench Descriptions

This paragraph should define the testbench created around the block. It should describe how each interface is being driven and should include all relevant information.

7.1.5.2 Itemization of Tests

This paragraph should define each of the tests performed during verification of the design of the block. It should include an accounting of which system requirements are being verified by each test.

7.1.6 Usage Guidelines

Describe any special conditions or exclusions that apply to the usage of this block.

8 Chip Verification Plan

8.1 Simulation Test Environment

8.1.1 Testbench Description

This paragraph should define the top-level testbench. It should describe how each interface is being driven and should describe what approach was followed in establishing the top-level test environment.

8.1.2 Bus Functional Models

This paragraph should describe all bus functional models created. This should include a definition of the I/O of the model and a description of its operation.

8.1.3 Itemization of Tests

This paragraph should define each of the tests performed during verification of the design. It should include an accounting of which system requirements are being verified by each test.

8.2 Formal Verification

This paragraph should define where is the design flow formal verification will be utilized.

8.3 FPGA Emulation

8.3.1 Emulation Plan

This paragraph should define how FPGA emulation will be utilized in the verification of the design. It should specify which portions of the design will be mapped to an FPGA. It should also include a description of the FPGA environment required. Any external devices required for emulation should be defined here. This may include processors, memories, standard interface chips, etc.

8.3.2 Resources required

This paragraph should define required development systems, external computing resources, power supplies, etc.

8.3.3 Software Requirements

This paragraph should define the software required to support the FPGA emulation activities.

8.4 Design For Test

8.4.1 BIST Methodology

Describe the BIST approach utilized for the chips embedded memories.

8.4.2 Chip Scan Methodology

This paragraph should define whether full or partial scan will be utilized. It should identify the estimated number of scan chains. It should also include any scan insertion methodology recommendations.

8.4.3 Boundary Scan Methodology

Define boundary scan if used along with insertion methodology.

8.4.4 Trace Module Methodology

If any trace capability is added to the chip it should be defined here. This may include both commercially available trace mechanisms as well as custom developed.

8.4.5 Custom Test Access Methodology

Describe here if any signals are muxed out via test interfaces. This should also define if there are any other schemes being implemented to provide access to internal signals.

8.4.6 TAP Controller and Mapping

This paragraph should define the TAP implementation and itemize all TAP instructions implemented.

8.4.7 Tester Limitations

This paragraph should define any known tester limitations such as: depth of memory, presence of mixed-signal capability, availability of serial memory, etc.

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9 Physical Requirements

9.1 Input power requirements

9.1.1 Required Voltages
I/O, core, analog, special cells (PLL, XOSC)

9.1.2 Voltage Regulator

9.1.3 Charge Pump

9.1.4 Power Calculations
core, simultaneously switching outputs

9.1.5 Supply Voltage Ripple Requirements

9.1.6 Ground Requirements
Identify any special grounding requirements such as split planes, etc.

9.2 Die Size Estimates

Core Logic Matrix

	I	Module	Est. Gate Count	Est. Area mm2
				95000
1.		ARM CELLS		
2.	1	Host1 ARM9xxE (HARD MACRO CELL 5 mm^2 384000 gates)		8.600000
3.	2	Host1 Interrupt Controller	20480	.215579
4.	3	Host1 L3 SRAM AHB I/F	12288	.129347
5.	4	Host1 Quad Port Memory Controller	22016	.231747
6.	5	Dual Master DMA Controller	12288	.129347
7.	6	ETM	56320	.592842
8.	7	Multi-Layer AHB Decoder/Arbiter	8192	.086232
9.	8	RTC	10240	.107789
10.	9	SPI	8192	.086232
11.	10	SPI	8192	.086232
12.	11	GPIO1	820	.008632
13.	12	GPIO2	820	.008632
14.	13	GPIO3	820	.008632
15.	14	UART	7886	.083011
16.	15	Timer	10240	.107789
17.	16	APB Bridge	10240	.107789
18.	17	APB Bridge	10240	.107789
		DUBAI LAN*		
20.	18	L3 Switch/CRC	256000	2.694737
21.	19	L2 Switch	204800	2.155789
22.	20	MAC	17408	.183242
23.	21	MAC	17408	.183242
24.	40	MAC	17408	.183242
25.	41	MAC	17408	.183242
26.	42	MAC	17408	.183242
27.	22	Dual Port SRAM Controller	24576	.258695
28.		IRVINE WAN*		
29.	23	HDLC1	6144	.064674
30.	24	HDLC2	6144	.064674
31.	25	WAN	131072	1.379705
32.		IRVINE I/O Purchased IP		
33.	28	USB	15360	.161684
34.	30	PLL (50 MHz in, 300MHz, 150MHz, 75MHz, 50 MHz, 33.3MHz, 25 MHz Out)	1024	.010779
35.		IRVINE I/O		
36.	26	Control and Status	16384	.172463

37.	27	HPI	35850	.377368
38.	29	Reset	10240	.107789
39.	31	JTAG	10240	.107789
		Total Gate Count (Excluding ARM Cores)	1004148	24.169977

Table 8 Core Logic Matrix

9.2.1 Memory Matrix

	I	Module	Est. Gate Count	Est. Area mm^2
1	32	Packet Sram 64KB	524288	3.276800
2	33	L3 SRAM1 64KB	524288	3.276800
3	26	WAN BUFFER 2KB	16384	**!Zero Divide**
4	37	HDLC BUFFER 2KB	16384	**!Zero Divide**
5	38	HDLC BUFFER 2KB	16384	**!Zero Divide**
6	39	L3 BUFFER 2KB	16384	**!Zero Divide**

Table 9 Memory Area Matrix

9.2.2 Die Size Matrix

24.169977	6.963200	31.133177		5.579711
Core mm^2	Mem mm^2	mm^2		mm per side
PIN	Straight			
423	423	107	8555	9.6050
Signal Pins	Pins + Power & Ground	Pins per side	Microns	mm per side
Metrics				
Core to finger	200	Microns		
Finger length	240	Microns		
Finger width	40	Microns		
Bond pad	75	Microns		
Bond pad / Finger clearance	5	Microns		
Bond pad to scribe	10	Microns		
Bond pad to pad trace	1	Microns		
Pad trace	2	Microns		
PIN	Staggered			
423	423	107	4815	6.7837
Signal Pins	Pins + Power & Ground	Pins per side	Microns	mm per side

Table 10 Die Size Matrix

9.3 Synthesis Plan

This is the section of the document that specifies how the chip will be assembled from a synthesis perspective. Issues to consider:

- Will the chip be synthesized from a top down as one block, or will it be synthesized as sub-modules. If it is to be synthesized as sub-modules, what are they?
- What tool will be used to do Static timing?
- Are their any blocks that are not synthesized or captured manually?
- Is there a clock block?
- Will the clock tree be synthesized or hand generated?
- Will boundary scan be inserted? If so will it be done manually or using synthesis?

9.4 Layout Plan

9.5 Package requirements

9.5.1 Package type (QFP,BGA,etc.)

9.5.2 Thermal requirementsDC Characteristics

9.5.2.1 Absolute Maximium Ratings

9.5.2.2 Recommended Operating Conditions

9.5.2.3 DC Electrical Characteristics Over Operating Range

9.5.2.4 Lead Inductance

9.5.3 Thermal Data

Thermal Resistance: junction to ambient 0 fr./s airflow (Θ_{ja})

9.5.4 Mechanical Drawing

9.5.5 Netlist Cross-reference File

Bond finger to package pin relationship

10 Electrical Characteristics

10.1 DC Specifications

10.1.1 Operating Conditions

10.1.2 Power DC Specifications

10.1.3 Input Leakage Current

10.1.4 Output Leakage Current

10.1.5 Input Specifications

10.1.6 Output Specifications

10.2 AC Characteristics

10.2.1 Clock

10.2.2 Power Sequencing

10.2.3 RESET

10.2.4 Interface Timing

A. Glossary / Definitions

AMBA.....Advanced Microcontroller Bus Architecture

AHB.....Advanced High-performance Bus

APB.....Advanced Peripheral Bus

ATE.....Automatic Test Equipment

BFM .....Bus Functional Model

BIST.....Built-In Self-Test

DFT.....Design for Test

DUT.....Device Under Test

IC .....Integrated Circuit

IP.....Intellectual Property

LFSR.....Linear Feedback Shift Register, a.k.a. PRPG

PRPG.....Pseudo Random Pattern Generator, a.k.a. LFSR

SOC .....System-On-Chip

TIC .....Test Interface Controller

TVM .....Transaction Verification Module

B. Revision History

Rev	Description	Initials	Date
-	Initial Document Creation (Draft Version)	JMF	09/12/01
1.0	1) Paragraphs now NORMAL format 2) Insert captions on figures, registers and tables 3) Added Electrical Characteristics section	JCT/TO	01/09/02