CSULB
CECS 360

VGA Design

Introduction

- VGA (video graphics array) is a video display standard introduced in the late 1980's
- All of the Diligent boards (Nexys 2/3/4) support VGA
- Our design will be a basic 640 x 480 resolution (with the number of colors determined by your board)
- We will design the interface logic, create test fixtures to verify it, and then run on the board

Basic Operation of a Cathode Ray Tube (CRT)

- An electron gun (cathode) generates a focused electron beam, which transverses a vacuum tube and hits the phosphorescent screen

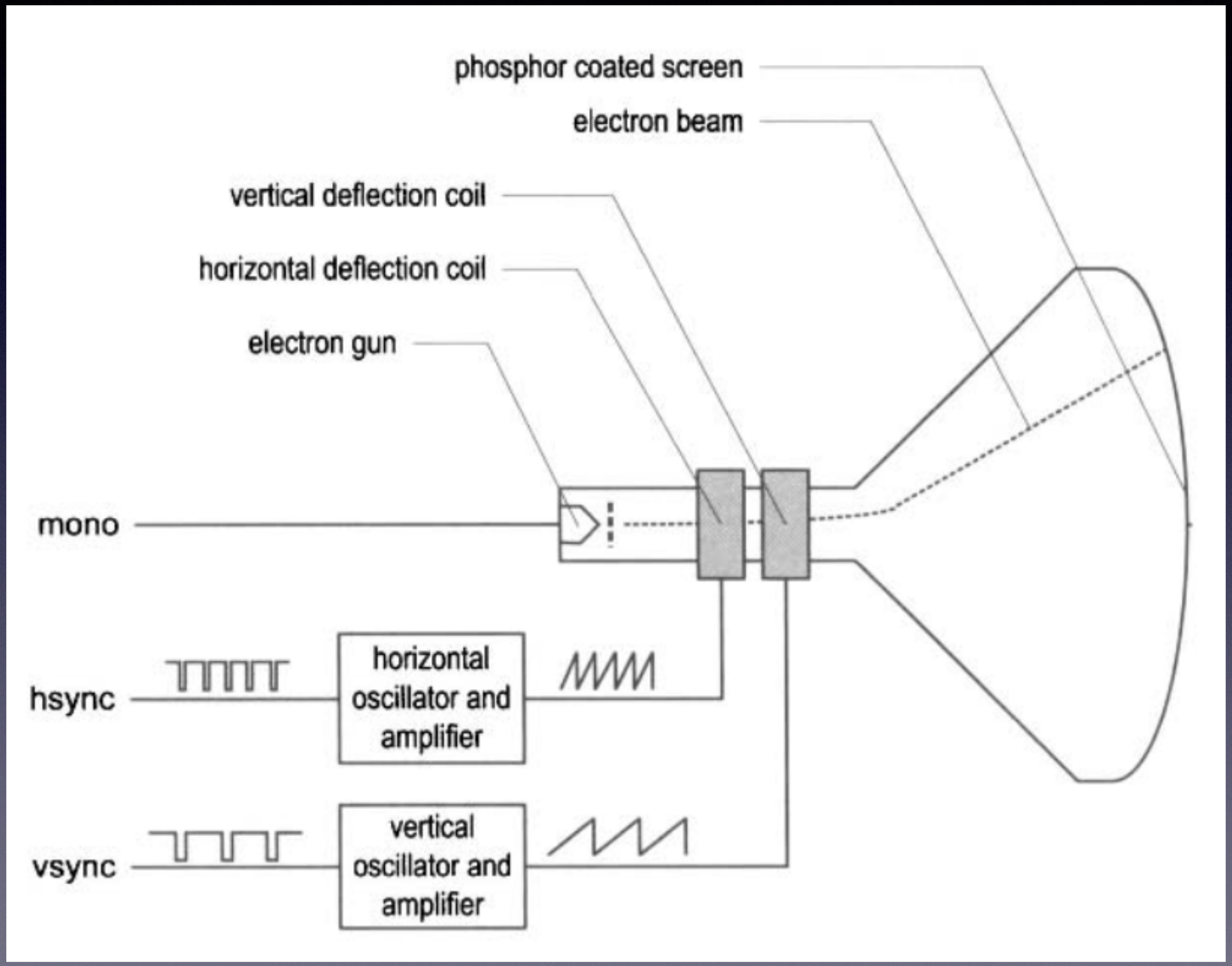
- Light is emitted when the electrons hit a phosphor dot on the screen

- The intensity and the brightness of the dot are determined by the voltage level

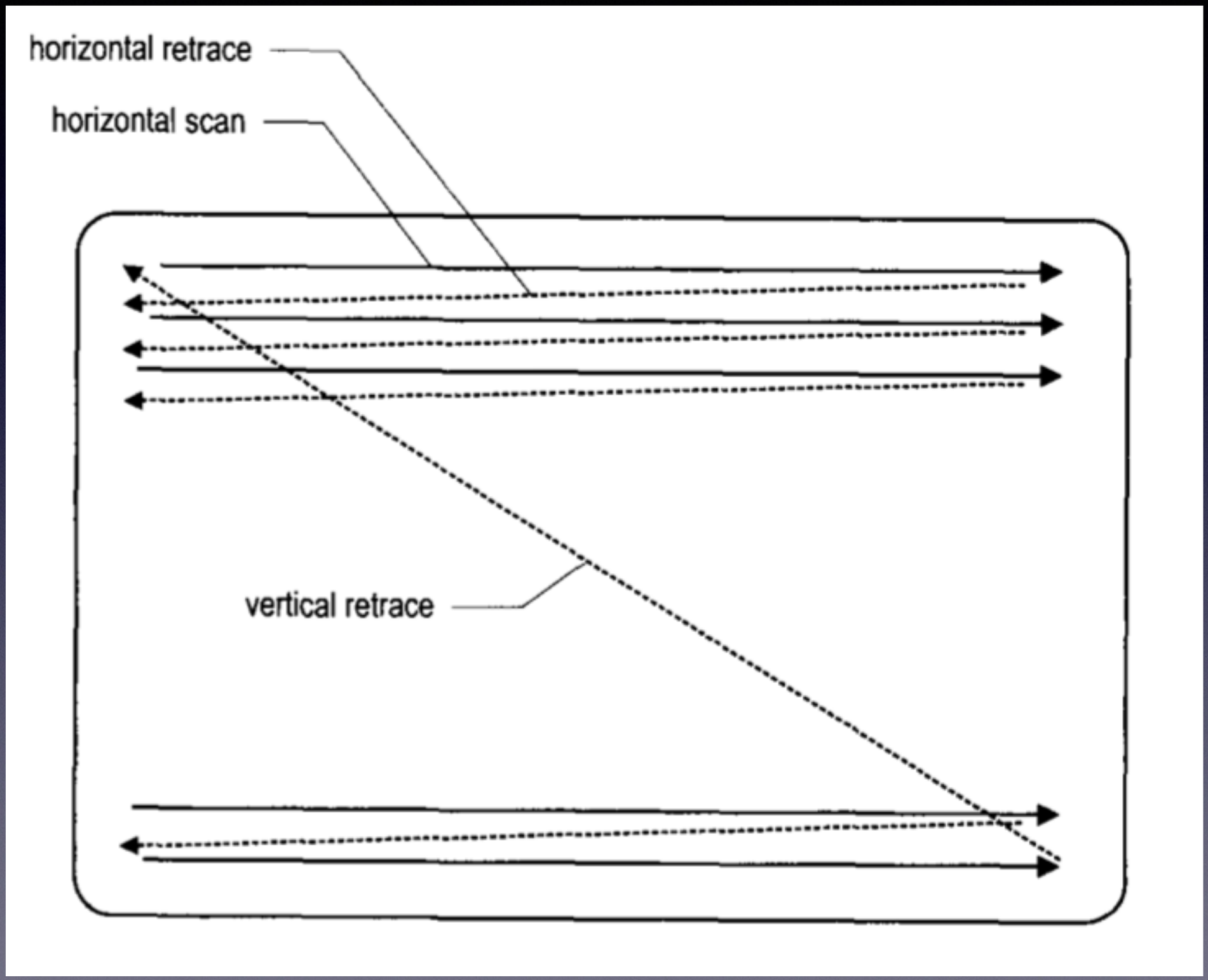
- Deflection coils (H/V) control where the electrons hit

- The beam scans the screen from left to right, top to bottom

Conceptual Diagram of a CRT Monitor



CRT Scanning Pattern



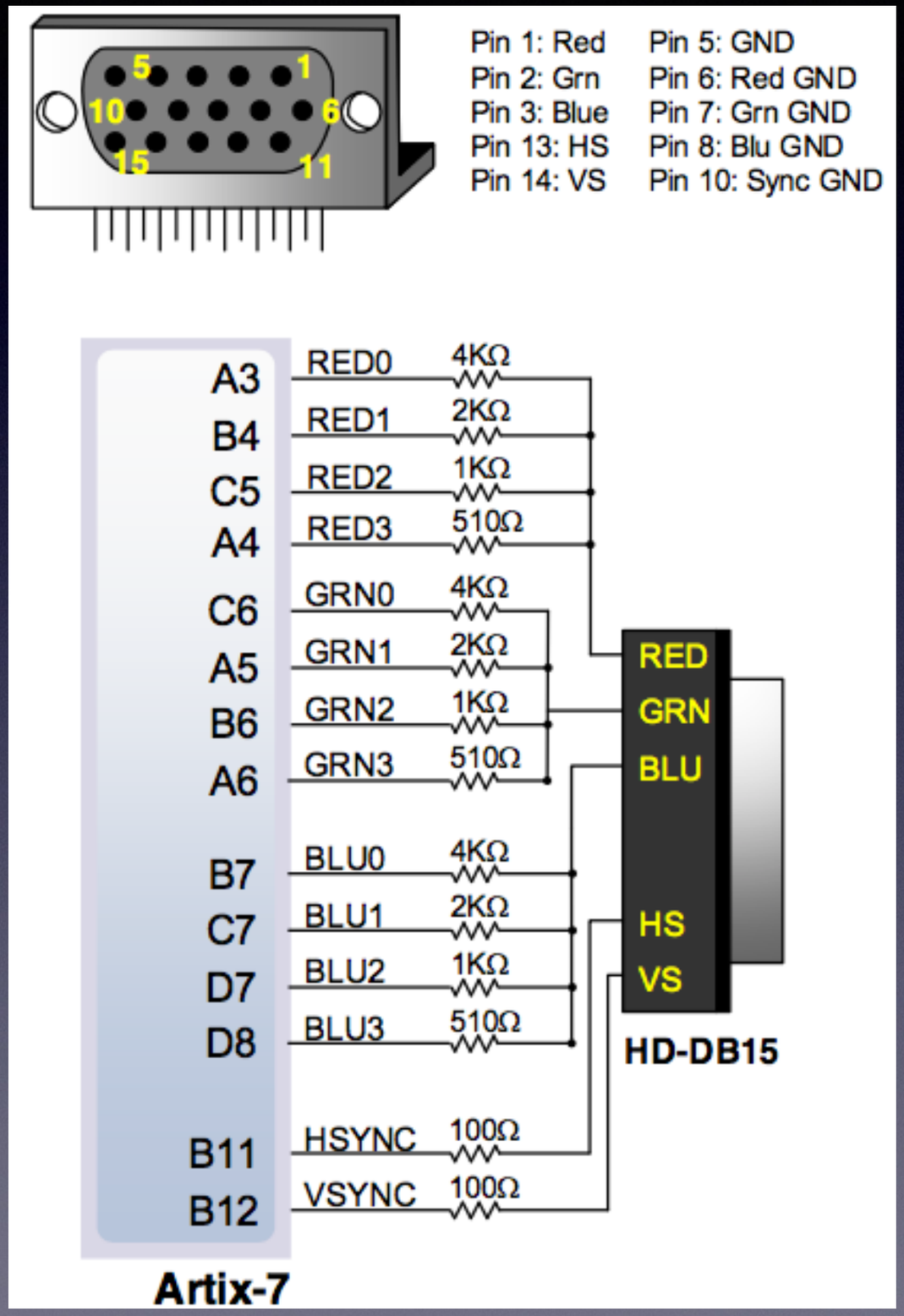
Color Control

- The older boards have three bits for color (R/G/B) while the newer boards have more
- Combinations of these bits produce the various colors seen on the display

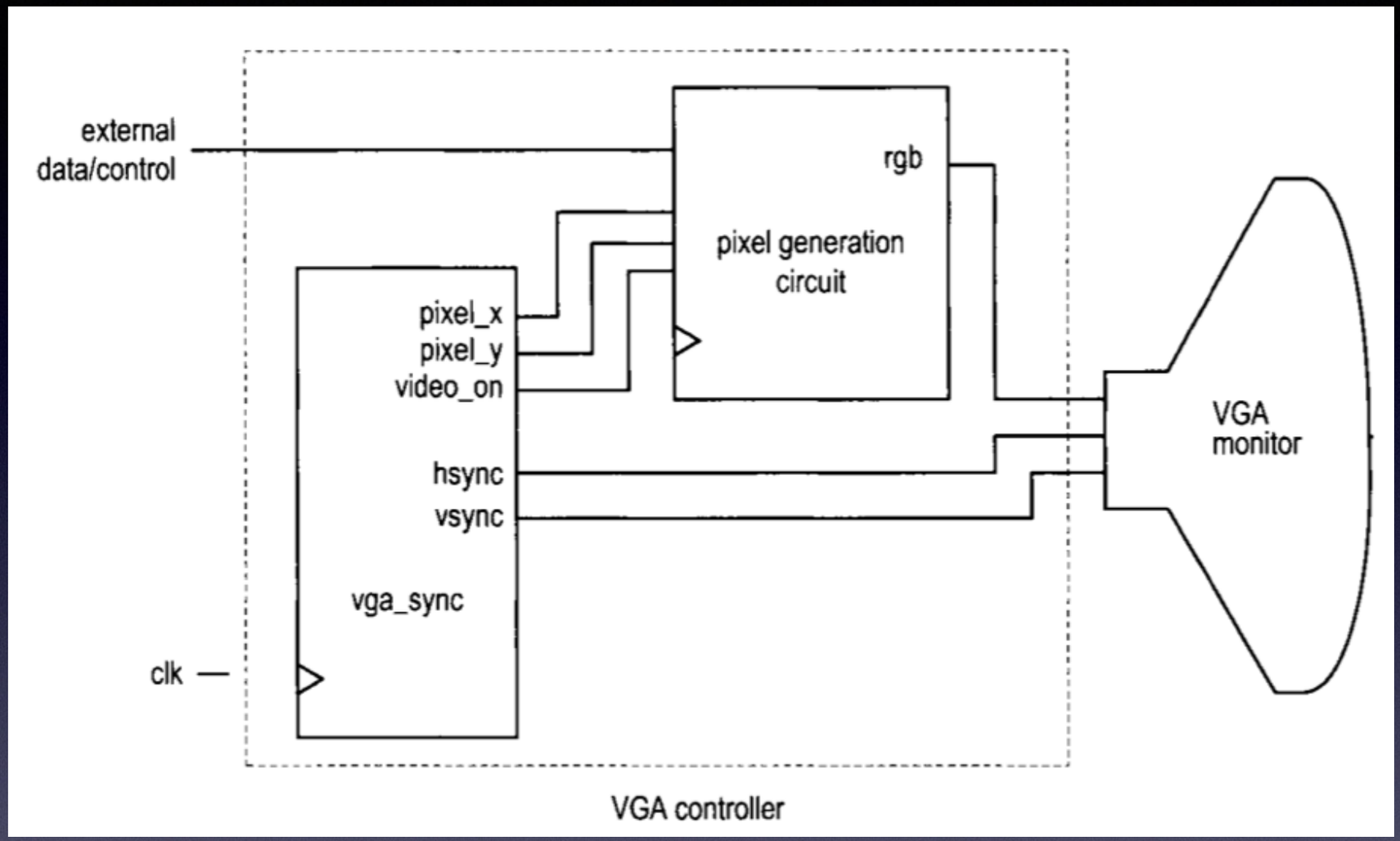
Red (R)	Green (G)	Blue (B)	Resulting color
0	0	0	black
0	0	1	blue
0	1	0	green
0	1	1	cyan
1	0	0	red
1	0	1	magenta
1	1	0	yellow
1	1	1	white

VGA Port

- Nexys4 uses 14 FPGA signals to create a VGA port with 4 bits per color and two standard sync signals (HS-Horizontal Sync, VS-Vertical Sync)
- With this board 4096 different colors may be displayed
- We need to create the video controller circuit to drive the syncs and color signals to produce our display



VGA Controller



- Our design will have two blocks: the vga_sync and the pixel generation circuit (what color where)
- The syncs go directly to the monitor while the pixel indication goes to the generation circuit to identify where on the monitor the output is being displayed

VGA Synchronization

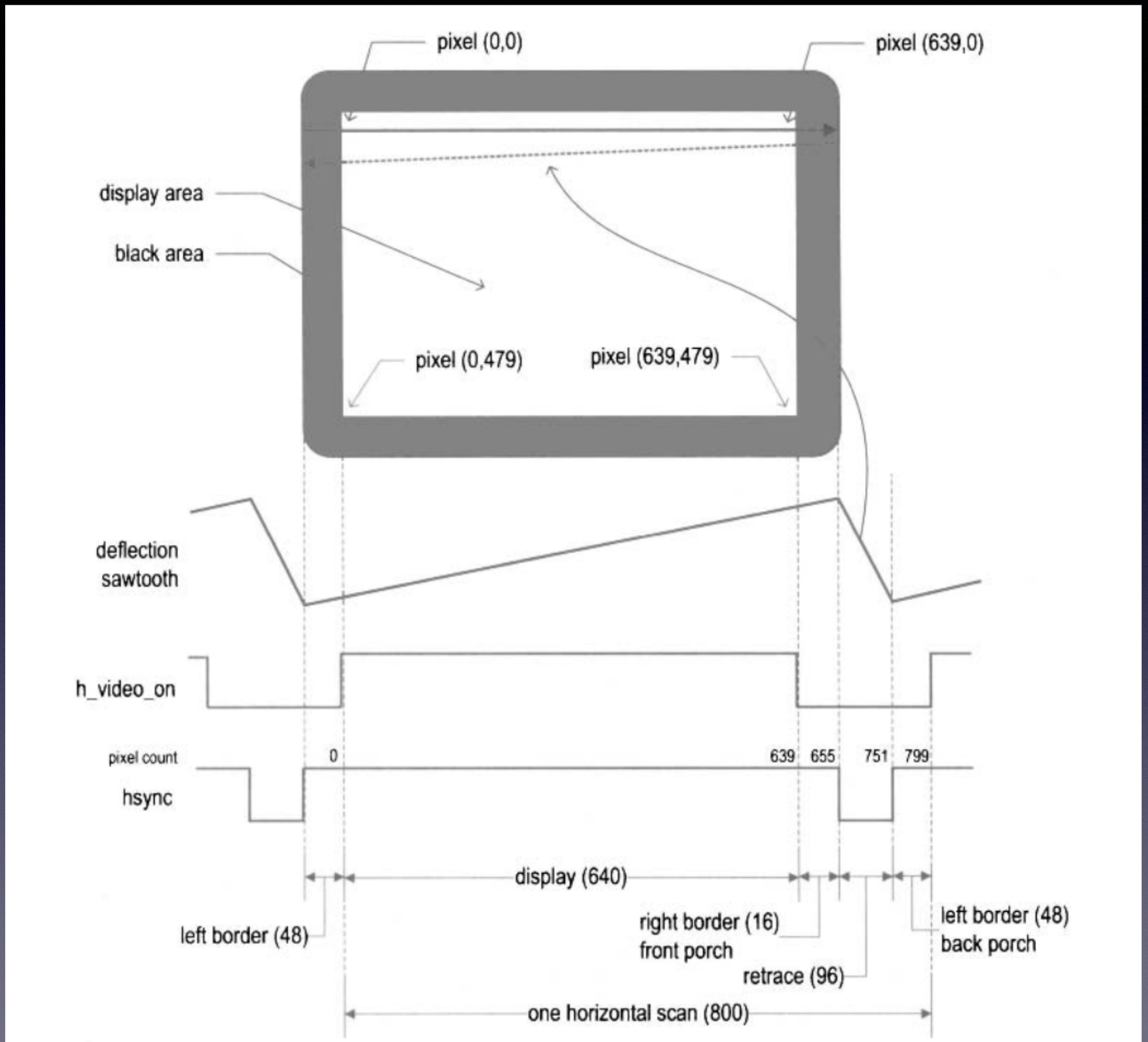
- The video synchronization circuit generates the *hsync* signal - the required time to traverse a row, and the *vsync* signal - the required time to transverse the entire screen

- We will utilize a 25 MHz *pixel rate*, which means that 25M pixels are processed in one second (VGA mode)

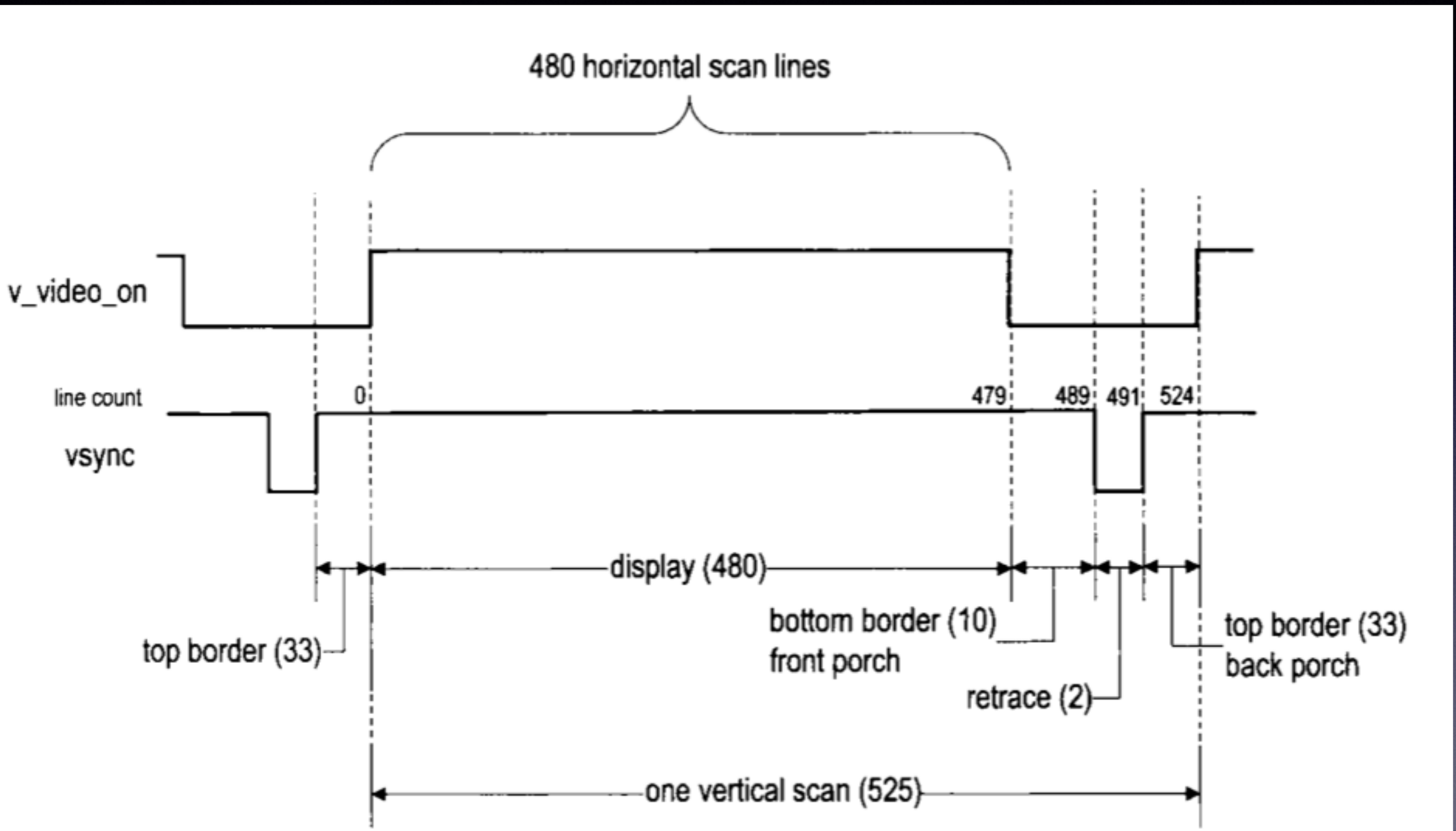
- The CRT monitor includes a small black border around the middle rectangle (visible portion)

- Note top-left (0,0) and bottom right (639,479)

Horizontal Scan



Vertical Scan



Horizontal Definitions

- *Display:* region where pixels are displayed on the screen (640 pixels)
- *Retrace:* region in which the electron beams return to the left edge. The video signal should be disabled (black) and the length here is 96 pixels
- *Right border:* region forming the right border of the display (front porch) - 16 pixels
- *Left border:* region forming the left border of the display (back porch) - 48 pixels

Vertical Definitions

- *Display:* region where the horizontal lines are displayed on the screen - 480 lines
- *Retrace:* region that the electron beams return to the top of the screen. Video should be disabled - 2 lines
- *Bottom border:* region forming the bottom border. (also front porch) - video disabled - 10 lines
- *Top border:* region forming the top border of the display (back porch) - 33 lines

hsync and vsync

- The *hsync* signal may be obtained from a mod-800 counter and a decoding circuit. The counts are used as the milestones for the display

- The *vsync* signal may be obtained from a mod-525 counter and a decoding circuit. This count is also used as milestones for the display

Timing Calculation for VGA

As mentioned earlier, we assume that the pixel rate is 25 MHz. It is determined by three parameters:

- p: the number of pixels in a horizontal scan line. For 640-by-480 resolution, it is

$$p = 800 \frac{pixels}{line}$$

- l: the number of lines in a screen (i.e., a vertical scan). For 640-by-480 resolution, it is

$$l = 525 \frac{lines}{screen}$$

- s: the number of screens per second. For flickering-free operation, we can set it to

$$s = 60 \frac{screens}{second}$$

The s parameter specifies how fast the screen should be refreshed. For a human eye, the refresh rate must be at least 30 screens per second to make the motion appear to be continuous. To reduce flickering, the monitor usually has a much higher rate, such as the 60 screens per second specification above. The pixel rate can be calculated by the three parameters:

$$\text{pixel rate} = p * l * s \approx 25M \frac{pixels}{second}$$

The pixel rate for other resolutions and refresh rates can be calculated in a similar fashion. Clearly, the rate increases as the resolution and refresh rate grow.

Timing Calculation for VGA

VGA Signal 640 x 480 @ 25MHz Pixel Frequency

General Timing			
Screen refresh rate	59.523809 Hz		
Pixel Frequency	25.0 MHz		
Horizontal Timing (Line)	**Pixels**	**Time**	
Visible Area	640	25.6 us	
Front Porch	16	640 ns	
Sync Pulse	96	3.84 us	
Back Porch	48	1.92 us	
Whole Line	800	32.0 us	
Vertical Timing (Frame)	**Lines**	**Time**	
Visible Area	480	25.0 ms	480 * 32 us
Front Porch	10	320.0 us	10 * 32 us
Sync Pulse	2	64.0 us	2 * 32 us
Back Porch	33	1.056 ms	33 * 32 us
Whole Frame	525	16.8 ms	525 * 32 us

VGA Synchronization Requirements

VGA SYNCHRONIZATION REQUIREMENTS

1. The VGA Synchronization Logic shall be updated at a 25 MHz rate.
2. The Horizontal Scan Count shall range from 0 to 799.
3. The Horizontal Scan Count shall be updated at the 25 MHz rate.
4. The Horizontal Sync signal shall be LOW ACTIVE and shall be active from Horizontal Scan Count 656 through 751.
5. The Horizontal Video On signal shall be HIGH ACTIVE and shall be active from Horizontal Scan Count 0 through 639.
6. The Vertical Scan Count shall range from 0 to 524.
7. The Vertical Scan Count shall be updated at the completion of a Horizontal Scan.
8. The Vertical Sync signal shall be LOW ACTIVE and shall be active from Vertical Scan Count 490 through 492.
9. The Vertical Video On signal shall be HIGH ACTIVE and shall be active from Vertical Scan Count 0 through 479.
10. The Video On signal shall be HIGH ACTIVE and shall be active when Horizontal Video On and Vertical Video On are active at the same time.

Assignment

- Before writing any Verilog you should create a document that will serve as your guide in writing the HDL - you should detail the behavior and include a detailed block diagram

- Utilizing your document of the vga_sync circuit based on the VGA presentation along with the supplied requirements - write the *vga_sync* module

- The second portion of this assignment will be to write the Verilog test fixture to verify your implementation (next lecture)