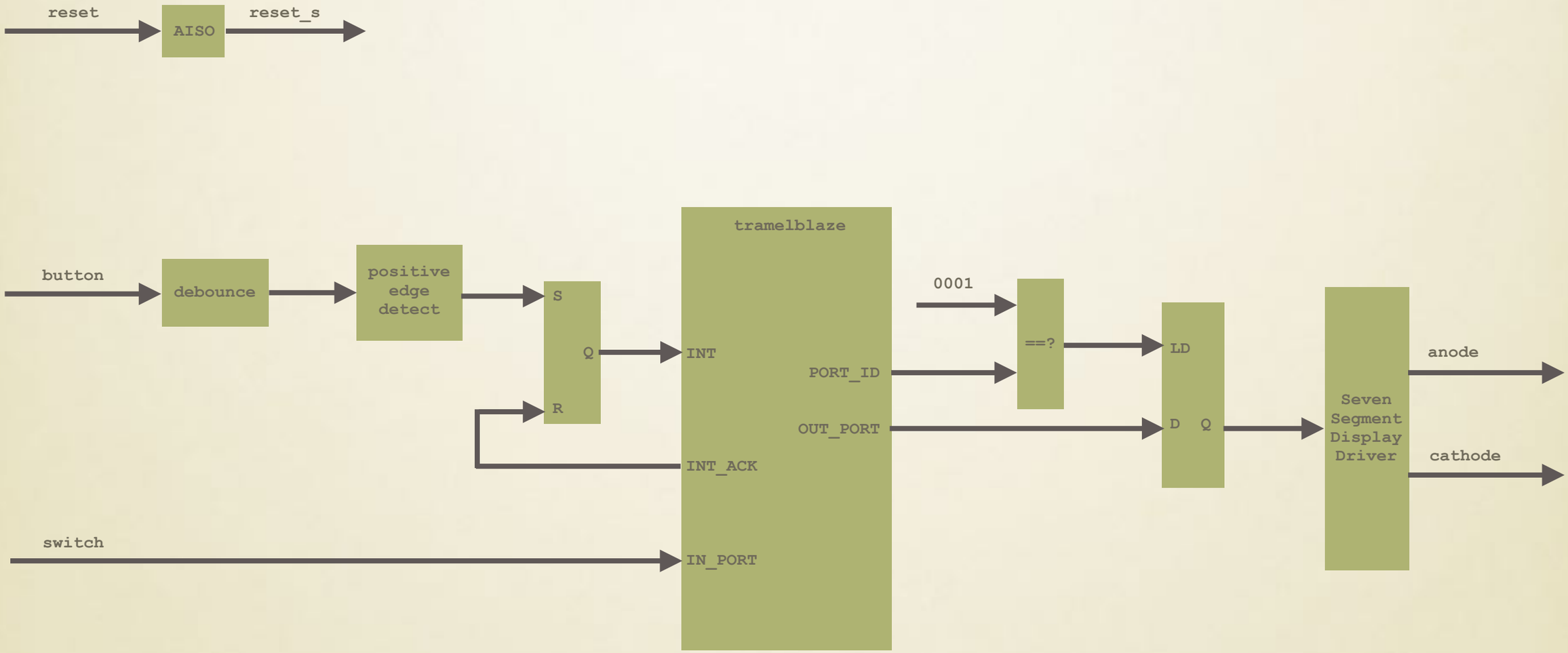
CECS 460
Spring 2018

Project One
Due: 2/8/2018

Synchronous Design Review

- This project is a review of the topics covered in 201, 301 and 360
- This lays the foundation for the rest of the semester for proper design practices and techniques
- Demonstrates synchronous design techniques and refreshes the process of porting designs to Xilinx based boards
- All modules must use the published header at the beginning of every file created

Top Level Block Diagram



Description

- Use momentary switches (buttons) for reset (HA) and count (HA)
- Use slide switch for increment (H)/decrement (L)
- AISO - Asynchronous In Synchronous Out - generate HA synchronous reset to design. Ensure this meets requirements of synchronization
- Debounce implements Pong Chu algorithm
- Positive edge detect detects rising edge issuing one clock wide output
- Tramelblaze interrupt service routine reads switch to determine if count up or down. Then write updated count to the register driving the seven segment display
- Seven segment drives the display using proper synchronous techniques

Deliverables

- Technical description of project
- Top level block design including names of signals between major functional blocks (your work)
- Detailed description of each functional block
- Source code (HDL/Assembly code)
- Test fixture code with evidence of successful simulation

Completed Project

- At the time of demonstration to instructor you should have a hard copy of the final report to give to the instructor
- Demonstration of completed project running on Digilent board
- Upload of completed project to BeachBoard
  - All .v files should be loaded directly - no zip files
  - Assembly code should be text file
  - Document may be word of pdf format