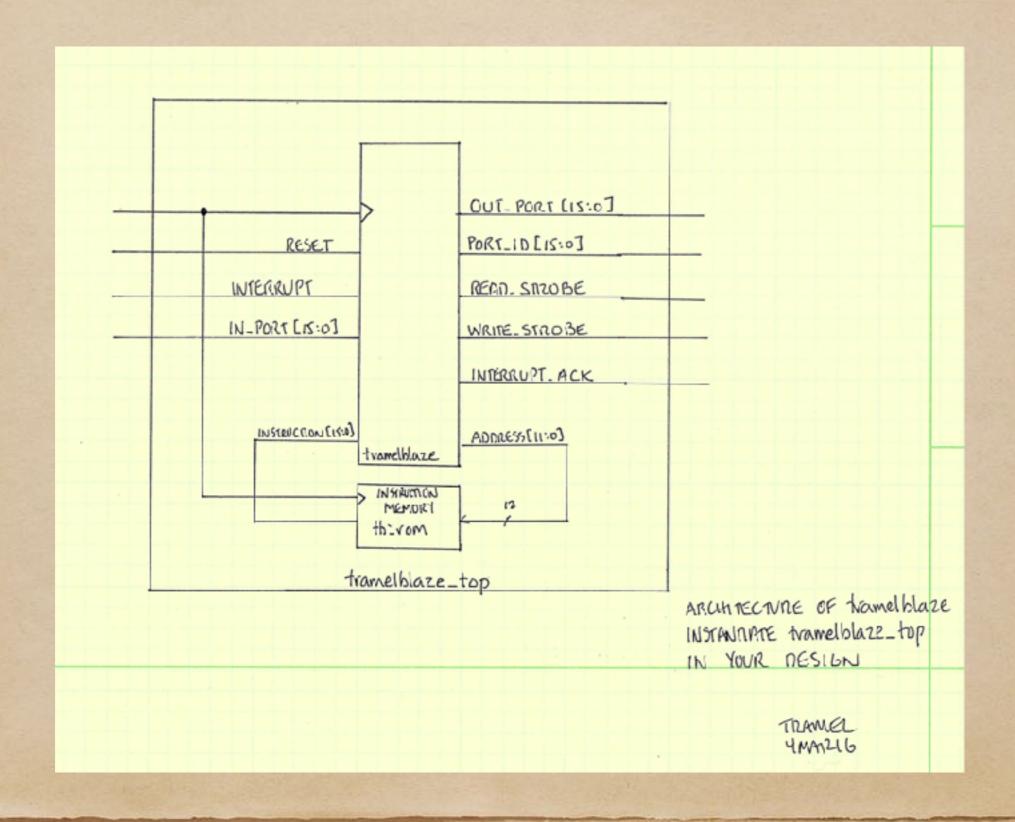
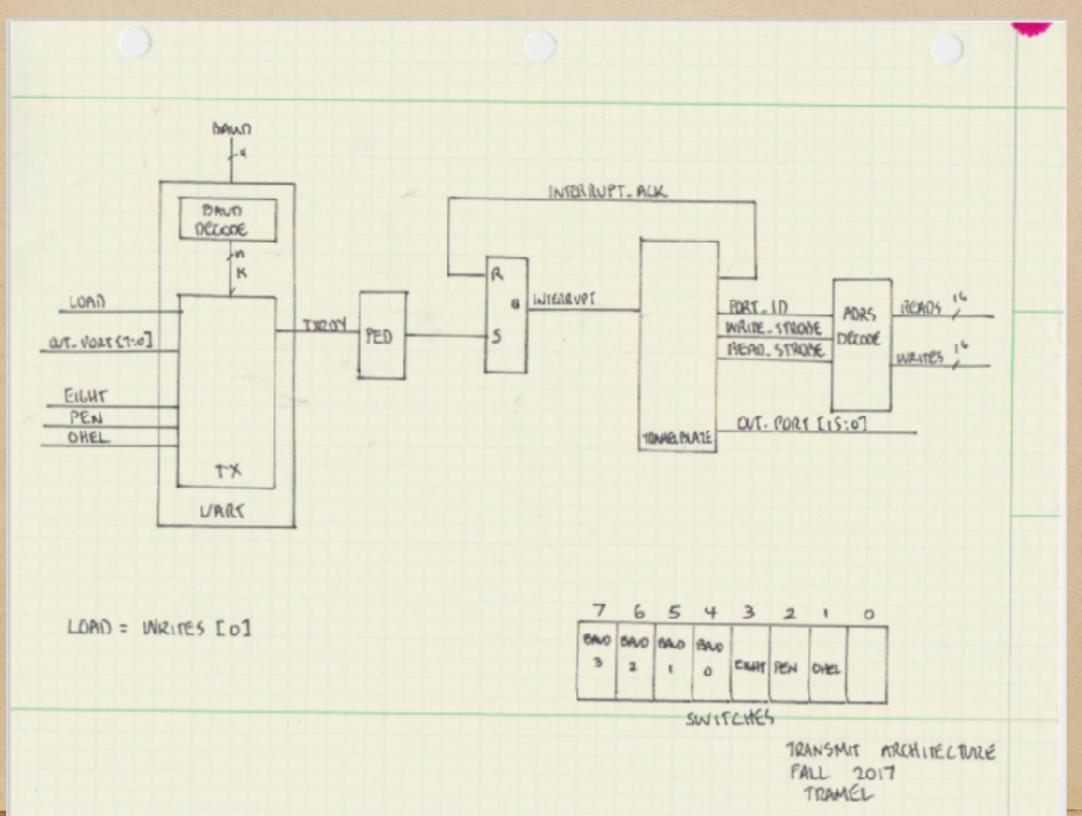
CECS 460 Project 2

Transmit Engine plus tramelblaze

tramelblaze Architecture



Block Diagram



Block Diagram Discussion

- This is meant to convey the TRANSMIT
 function but by looking ahead we can save
 ourselves time when we construct our design
- Please use recommended bit positions for the status/data and the configuration switches
- Reset should continue to be sourced by a
 High-Active momentary button

Project Discussion

- * Make sure you simulate your design before you program your board. This allows you to see how the inward parts of your design are operating you might be surprised (not simulating is a big mistake).
- I recommend you verify your decode block between the load and shift registers independently. Verifying its operation in the context of the TX machine is more difficult.
- * The software to be written is simple: Respond to the TXRDY bit setting the interrupt to let you know it is time to output another character
- * When in the main loop (not servicing interrupt) you should walk a one through the available LEDs. This is an immediate feedback that your software is running in the main loop.
- When you see the TXRDY induced interrupt you should continuously transmit the sequence "CSULB CECS 460 - [COUNT] <CR><LF>"
- * The COUNT keeps track of how many times you have output a value to the terminal and should increment by one each time

Deliverables

- Due Tuesday March 7 keep in mind I will assign the RECEIVE engine on this date. Do your best to keep up with the project work in a timely fashion. Not completing the projects will affect your final grade.
- Complete the documentation using the recommended style from the chip specification presentation
- Please include: Technical discussion, source code (leave out the detailed tramelblaze files), the tba and ucf files
- Please upload the files to Dropbox
- Please demonstrate to instructor with hard copy of deliverables