PIC32MZ EMBEDDED CONNECTIVITY (EC)

PIC32MZ Embedded Connectivity (EC) Family Silicon Errata and Data Sheet Clarification

The PIC32MZ Embedded Connectivity (EC) family devices that you have received conform functionally to the current Device Data Sheet (DS60001191**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Embedded Connectivity (EC) family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections (if applicable) start on page 12, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ Embedded Connectivity (EC) family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A3	A4
PIC32MZ1024ECG064	0x05103053	0x3	0x4
PIC32MZ1024ECH064	0x05108053		
PIC32MZ1024ECM064	0x05130053		
PIC32MZ2048ECG064	0x05104053		
PIC32MZ2048ECH064	0x05109053		
PIC32MZ2048ECM064	0x05131053		
PIC32MZ1024ECG100	0x0510D053		
PIC32MZ1024ECH100	0x05112053		
PIC32MZ1024ECM100	0x0513A053		
PIC32MZ2048ECG100	0x0510E053		
PIC32MZ2048ECH100	0x05113053		
PIC32MZ2048ECM100	0x0513B053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001191**B**) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A3	A4
PIC32MZ1024ECG124	0x05117053	0x3	0x4
PIC32MZ1024ECH124	0x0511C053		
PIC32MZ1024ECM124	0x05144053		
PIC32MZ2048ECG124	0x05118053		
PIC32MZ2048ECH124	0x0511D053		
PIC32MZ2048ECM124	0x05145053		
PIC32MZ1024ECG144	0x05121053		
PIC32MZ1024ECH144	0x05126053		
PIC32MZ1024ECM144	0x0514E053		
PIC32MZ2048ECG144	0x05122053		
PIC32MZ2048ECH144	0x05127053		
PIC32MZ2048ECM144	0x0514F053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001191**B**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item #	Issue Summary	Affected Revisions(1)	
				A3	A4
ADC	INT0 Trigger	1.	When using INT0 as a trigger source for ADC conversion, the INT0EP bit in the INTCON register controls which edge triggers the conversion (rising or falling). However, only a rising edge will trigger the conversion.	X	X
ADC	Data Format	2.	Two's complement (signed) input mode does not produce expected results.	X	X
Boot Flash	Boot Sequence	3.	When Boot Flash 1 is selected to be mapped to a Lower Boot Alias memory, the device may instead incorrectly map Boot Flash 2.	X	X
Comparator Voltage Reference	Range Selection	4.	The Comparator Voltage Reference (CV_{REF}) module range selection (CVRR bit in the CVRCON register) does not function.	X	X
Ethernet Controller	Alternate MII and RMII Configurations	5.	The Alternate Ethernet pins, AERXDV and AERXCLK, are not available on 100-pin devices.	X	X
Ethernet Controller	MII Configuration	6.	MII mode is not available on 64-pin devices.	X	X
Ethernet Controller	RMII Mode	7.	MII pins that are not used by the Ethernet module during RMII operation may not be available for other functions.	X	X
I/O Port	Open Drain	8.	The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output. the Open Drain feature is not available for dedicated or remappable Peripheral Pin Select (PPS) output features.	X	X
Oscillator	FRC Tuning	9.	Changing values in the OSCTUN register has no effect on the FRC accuracy.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions(1)	
				A3	A4
Oscillator	Ceramic Resonator	10.	The Ceramic Resonator cannot be used as an input to the Oscillator module (OSC1/OSC2 pins).	X	X
Secondary Oscillator	Crystal Oscillator	11.	A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSCI/SOSCO pins).	X	X
Reserved	—	12	—	—	—
Power-Saving Modes	Dream Mode	13.	Dream mode does not function.	X	X
Power-Saving Modes	Sleep Mode	14.	The device may not exit Sleep mode.	X	X
SPI	Maximum Speed Operation	15.	The SPI clock speed does not meet the published specification.	X	X
Reserved	—	16	—	—	—
System Bus	Permission Access	17.	When Permission Access is enabled, any access by an initiator that is not allowed will not succeed; however, the status registers may not accurately report the violations.	X	X
USB	Suspend Mode	18.	The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.	X	X
USB	—	19.	The USB module requires a start-up delay.	X	X
USB	Endpoint FIFO	20.	Endpoint FIFOs cannot be read using 32-bit reads.	X	X
Reserved	—	21	—	—	—
Watchdog Timer	Window Mode	22.	When the Watchdog Timer is used in Window mode, the module may issue a Reset even if the user tries to clear the module within the allowed window.	X	X
Watchdog Timer	Reset Trigger	23.	When the Watchdog Timer expires during Sleep mode, it causes a Reset rather than a non-maskable interrupt (NMI).	X	X
PMP	Address Lines	24.	PMP address lines are not available for use as general purpose I/O when PMAEN = 0x0000.	X	X
I^2C	Master Stop	25.	At speeds above 100 kHz, setting the PEN bit to send a Stop does not release the SDA line.	X	X
Crypto Engine	Byte Ordering	26.	The Crypto Engine processes data in big-endian order rather than little-endian.	X	X
Random Number Generator	True Random Number Generator (TRNG) Mode	27.	TRNG mode does not function.	X	X
Flash	Code-Protect	28.	Once the Code-Protect feature is enabled, a device cannot be erased using ICSP or JTAG.	X	
ADC	Group Interrupt	29.	When using Channel Scan, Class 3 inputs are always part of the Group Interrupt regardless of the setting of the AGIENx bits in the AD1IRQENx register.	X	X
SQI	Soft Reset	30.	A Soft Reset is only possible when clock divider values are '0' and '1'.	X	X
SQI	XIP Mode	31.	XIP mode is not operational.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions(1)	
				A3	A4
SQI	Buffer Thresholds	32.	Transmit and receive operation may not function properly.	X	X
SQI	Interrupts	33.	Some Interrupt Signal Enable bits are set upon a Reset.	X	X
SQI	Read Clock Speed	34.	Clock for read operations does not meet the published specification.	X	X
SQI	Transmit Buffer Empty Status	35.	Upon a reset, the Transmit Buffer Empty Status (TXEMPTYIF) bit in the SQI1INTSTAT register is cleared to zero instead of being set to one.	X	X
Comparator	Idle Mode	36.	The Comparator cannot be disabled when the device is in Idle mode.	X	X
Comparator	Offset	37.	The Comparator offset does not meet the published specification	X	X
I/O Pins	SOSCO Function	38.	I/O pins shared with the SOSCO function cannot be used as general purpose input or output.	X	X
I^2C	Overrun Interrupt	39.	A Slave interrupt is not generated during an overrun condition.	X	X
Flash Memory	Program Write Protect	40.	The Program Write Protect (PWP) bits protect all Program Memory.	X	X
Oscillator	POSC	41.	A crystal oscillator cannot be used as an input to the Primary Oscillator (OSC1/OSC2 pins).	X	X
5V Tolerant I/O Pins	Pull-ups	42.	Internal pull-up resistors may not guarantee a logical '1' on digital inputs on 5V tolerant pins.	X	X
ADC	—	43.	Dedicated Sample and Hold circuits as well as Automatic Channel scan mode are not supported.	X	X
ADC	—	44.	ADC module does not meet published specifications.	X	X
Prefetch	Module Disable	45.	Disabling the Prefetch does not invalidate contents.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: ADC

When using INT0 as a trigger source for ADC conversion, the INT0EP bit in the INTCON register controls which edge triggers the conversion (rising or falling). However, only a rising edge will trigger the conversion.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

2. Module: ADC

Two's complement (signed) input mode does not produce expected results. Signed mode selections are SHxMOD<1:0> = 01 for single-ended or SHxMOD<1:0> = 11 for differential inputs.

Work arounds

Work around 1:

Use two's complement format for all inputs. The Two's complement format works properly when all sample and holds are set for this format. Single ended or differential mode can still be selected independently. Use one of the following settings for SH0MOD through SH5MOD:

- SHxMOD<1:0> = 01, for signed single ended
  or,
- SHxMOD<1:0> = 11, for signed differential inputs

Work around 2:

Use unipolar (unsigned) mode selections for all sample and holds. Where needed, convert the unsigned results to signed values. Unsigned 12-bit results can be converted to signed values by subtracting 2048 from the signed result. Use one of the following settings for SH0MOD through SH5MOD:

- SHxMOD<1:0> = 00, for unsigned single ended
  or,
- SHxMOD<1:0> = 10, for unsigned differential inputs

Affected Silicon Revisions

A3	A4						
X	X						

3. Module: Boot Flash

When Boot Flash 1 is selected to be mapped to a Lower Boot Alias memory, the device may instead incorrectly map Boot Flash 2.

Work around

Program an invalid sequence number (such as 0xFFFFFFFF or 0x00000000) into Boot Flash 2. This will force the device to map Boot Flash 1 into the Lower Boot Alias memory.

Affected Silicon Revisions

A3	A4						
X	X						

4. Module: Comparator Voltage Reference

The Comparator Voltage Reference (CV_{REF}) module range selection (CVRR bit in the CVRCON register) does not function. The default setting of the CV_{REF} Range Selection bit (CVRR) is set to 0 to 0.67 CV_{RSRC}, with a step size of $CV_{RSRC}/24$, and cannot be changed.

Work around

Use an External Voltage Reference and adjust it appropriately to achieve the desired CV_{REF} output.

Affected Silicon Revisions

A3	A4						
X	X						

5. Module: Ethernet Controller

The Alternate Ethernet pins, AERXDV and AERXCLK, are not available on 100-pin devices.

Work around

Only use either the MII or RMII configuration.

Affected Silicon Revisions

A3	A4						
X	X						

6. Module: Ethernet Controller

MII mode is not available on 64-pin devices. In this mode, the Ethernet pin, ERXD2, is not available.

Work around

Use the RMII or Alternate RMII configurations.

Affected Silicon Revisions

A3	A4						
X	X						

7. Module: Ethernet Controller

MII pins that are not used by the Ethernet module during RMII operation are not released, and therefore, lower priority functions on these pins are not available in this mode. However, higher priority functions on these pins, such as EBI and analog inputs (for ADC and Comparators), can still be used.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

8. Module: I/O Port

The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output. the Open Drain feature is not available for dedicated or remappable Peripheral Pin Select (PPS) output features.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

9. Module: Oscillator

Changing values in the OSCTUN register has no effect on the FRC accuracy.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

10. Module: Oscillator

The Ceramic Resonator cannot be used as an input to the Oscillator module (OSC1/OSC2 pins).

Work around

Instead, use either a crystal oscillator or the external clock.

Affected Silicon Revisions

A3	A4						
X	X						

11. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSCI/SOSCO pins).

Work around

Instead, use the external clock.

Affected Silicon Revisions

A3	A4						
X	X						

12. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

13. Module: Power-Saving Modes

Dream mode is intended as a feature allowing DMA operation while the CPU is in Idle mode; however, Dream mode does not function.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

14. Module: Power-Saving Modes

The device may not exit Sleep mode.

Work arounds

Enable Flash in Sleep mode by clearing the Flash Sleep Mode Configuration bit, FSLEEP, in the DEVCFG0/ADEVCFG0 configuration register.

Affected Silicon Revisions

A3	A4						
X	X						

15. Module: SPI

The SPI clock speed does not meet the published specification. The maximum supported SPI clock speed is 27 MHz.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

16. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

17. Module: System Bus

When Permission Access is enabled, any access by an initiator that is not allowed will not succeed; however, the status registers may not accurately report the violations.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

18. Module: USB

The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.

Work around

Keep the USB PHY operational in Sleep mode by setting the USBSSEN bit to '0'.

Affected Silicon Revisions

A3	A4						
X	X						

19. Module: USB

The USB module requires a start-up delay.

Work around

When enabling the USB PLL, add a three second delay before turning on the USB module.

Affected Silicon Revisions

A3	A4						
X	X						

20. Module: USB

Endpoint FIFOs cannot be read using 32-bit reads.

Work around

Use 8-bit reads, reading each portion and copying into a 32-bit value.

Affected Silicon Revisions

A3	A4						
X	X						

21. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

22. Module: Watchdog Timer

When the Watchdog Timer is used in Window mode, the module may issue a Reset even if the user tries to clear the module within the allowed window.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

23. Module: Watchdog Timer

When the Watchdog Timer expires during Sleep mode, it causes a Reset rather than a Non-maskable Interrupt (NMI).

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

24. Module: PMP

PMP address lines are not available for use as general purpose I/O when PMAEN = 0x0000.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

25. Module: I^2C

At speeds above 100 kHz, setting the PEN bit to send a Stop does not release the SDA line.

Work around

The I^2C module must be turned ON before every transaction, and turned OFF after the transaction completes.

Affected Silicon Revisions

A3	A4						
X	X						

26. Module: Crypto Engine

The Crypto Engine processes data in big-endian order rather than little-endian.

Work around

Use the SWAPEN bit (CECON<5>) to byte-reverse the data on input. After the data is processed, it must be byte-reversed by software or programmable DMA.

Affected Silicon Revisions

A3	A4						
X	X						

27. Module: Random Number Generator

True RNG mode does not function.

Work around

Instead, use Pseudo-Random Number Generator (PRNG) mode.

Affected Silicon Revisions

A3	A4						
X	X						

28. Module: Flash

Under normal conditions, once the Code-Protect feature is enabled, a device cannot be accessed (read and/or write) through external interfaces such as ICSP or JTAG. To gain access through these interfaces, the Code-Protect bit must be erased, either by issuing an erase command (using ICSP or JTAG) or with the help of RTSP code. However, the device erase command using ICSP or JTAG does not function, once the Code-Protect feature is enabled.

Work arounds

Work around 1:

Use the RTSP method to update code in a Code-Protect enabled device. In this mode, Flash memory can be erased and programmed with desired data.

Work around 2:

Use the RTSP method with the Live-Update feature of the device to erase the Code-Protect bit. Using this method, the application will erase the Code-Protect bit located in the inactive Boot Flash memory, and update this Boot Flash sequence to a higher number versus the active Boot Flash memory. On the next POR, Boot Flash memory with the erased Code-Protect bit will be used to configure the device, including Code-Protect configuration.

Affected Silicon Revisions

A3	A4						
X							

29. Module: ADC

When using Channel Scan, Class 3 inputs are always part of the Group Interrupt regardless of the setting of the AGIENx bits in the AD1IRQENx register. Conversions should only be part of the Group interrupt if a AGIENx bit is set.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

30. Module: SQI

A SQI Soft Reset, which is controlled by the RESET bit in the SQI1CFG register does work when the CLKDIV<7:0> bits in the SQI1CLKCON register have a value of two or higher.

Work around

Set the CLKDIV<7:0> bits to a value of zero or one.

Affected Silicon Revisions

A3	A4						
X	X						

31. Module: SQI

XIP mode is not operational (MODE<2:0> bits = `011` in the SQI1CFG register).

Work around

Use PIO mode (MODE<2:0> bits = `001`) or DMA mode (MODE<2:0> bits = `010`).

Affected Silicon Revisions

A3	A4						
X	X						

32. Module: SQI

Transmit and receive operation may not function properly.

Work around

Set the TXCMDTHR<5:0> and RXCMDTHR<5:0> bits in the SQI1CMDTHR register to multiples of 4 (32-bit aligned data buffers).

Affected Silicon Revisions

A3	A4						
X	X						

33. Module: SQI

The TXEMPTYISE, TXTHRISE, RXEMPTYISE, RXTHRISE, and CONEMPTYISE Interrupt Signal Enable bits in the SQI1INTSEN register are enabled on a device Reset.

Work around

Clear these bits by software.

Affected Silicon Revisions

A3	A4						
X	X						

34. Module: SQI

Clock speed for read operations does not meet the maximum specification (SQ10) of 50 MHz. For read operations the maximum clock is 25 MHz.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

35. Module: SQI

For all resets, the Transmit Buffer Empty Status (TXEMPTYIF) bit in the SQI1INTSTAT register is cleared to zero instead of being set to one.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

36. Module: Comparator

The SIDL bit in the CMSTAT register is intended to stop all Comparator modules when the CPU enters Idle mode. However, this bit does not function, and all enabled modules will continue to operate.

Work around

Disable the Comparator module by clearing the ON bit in the CMxCON register prior to entering idle mode

Affected Silicon Revisions

A3	A4						
X	X						

37. Module: Comparator

The Input Offset Voltage parameter (D300) is not within the published data sheet specification. The typical value is ±30 mV.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

38. Module: I/O Pins

When the Secondary Oscillator is disabled via the FSOSCEN bit (DEVCFG1<6>), the SOSCO pin does not tri-state and is driven to Vss. An I/O pin shared with the SOSCO function cannot be used as a general purpose input or output.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

39. Module: I^2C

When operating in Slave mode, the I^2C module does not trigger an interrupt when an overrun condition occurs.

Work around

Monitor the I2COV bit in the I2CxSTAT register using software.

Affected Silicon Revisions

A3	A4						
X	X						

40. Module: Flash Memory

Under normal conditions, setting the Program Write Protect (PWP) bits sets a mark below which the program memory is protected. Memory above this setting may be erased or written. However, the device protects all of program memory when any PWP bits are set.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

41. Module: Oscillator

A crystal oscillator cannot be used as the input to the Primary Oscillator (OSC1/OSC2 pins).

Work around

Use an external clock or an internal FRC.

Affected Silicon Revisions

A3	A4						
X	X						

42. Module: 5V Tolerant I/O Pins

When internal pull-ups are enabled on 5V tolerant pins, the level as measured on the pin and available to external device inputs may not exceed the minimum value of V_{IH}, and therefore qualify as a logic “high”. However, with respect to the PIC32 device, as long as $V_{DD} \geq 3V$ and the load doesn't exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic “high” internally to the device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic “high” for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA or $V_{DD} < 3V$

Affected Silicon Revisions

A3	A4						
X	X						

43. Module: ADC

The ADC module has the following restrictions:

1. SH0 through SH4 functionality is not supported. Sampling must be performed on SH5 only.
2. Automatic Channel Scan mode is not supported. Channel Scan must be performed manually in software.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

44. Module: ADC

The ADC module does not meet the published Throughput Rate (AD51) and Full-Scale Input Range (AD12) specifications. The updated Maximum Throughput Rate (AD51) specification is 125 ksps, assuming 16x Oversampling mode. The updated Maximum Full-Scale Input Range is 2.5V for both Differential and Singled-Ended modes. The updated Minimum Full-Scale Input Range is -2.5V for Differential mode.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

45. Module: Prefetch

The Prefetch module does not invalidate buffer contents when the module is disabled by setting PREFEN<1:0> to b00.

Work around

To disable the Prefetch module, execute four 32-bit NOPs before and after setting PREFEN<1:0> to b00.

Affected Silicon Revisions

A3	A4						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001191**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Power-Down Current

Certain specifications in Table 36-8 were stated incorrectly in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 3: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended		
Param. No.	Typical(2)	Maximum	Units	Conditions	
Power-Down Current (I_{PD}) (Note 1)					
DC40k	**3**	—	**mA**	-40°C	Base Power-Down Current
DC40l	**4**	—	**mA**	+25°C	
DC40n	**10**	—	mA	+85°C	
DC40m	**—**	—	mA	+125ºC	

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled, PBCLKx divisor = 1:128 ('x' ≠ 7)
- CPU is in Sleep mode
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0)

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2. Module: Operating Conditions

The Standard Operating Conditions in the current version of the data sheet were incorrectly stated as 2.2V to 3.6V. The correct range is **2.3V** to 3.6V.

Operating Conditions (See the first page of the data sheet)

- **2.3V** to 3.6V, -40ºC to +85ºC, DC to 200 MHz
- **2.3V** to 3.6V, -40ºC to +125ºC (Planned)

Absolute Maximum Ratings (see page 555 of the data sheet)

Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ **2.3V** (Note 3) ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < **2.3V** (Note 3) ..... -0.3V to +3.6V

Electrical Specification Table Headings

All tables in **36.0 "Electrical Specifications"**, which include the Standard Operating Conditions in their headings, should show the amended range, as follows:

Standard Operating Conditions: **2.3V** to 3.6V
(unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for Industrial
-40°C ≤ TA ≤ +125°C for Extended

DC Characteristics (See page 556 and 557 of the data sheet)

TABLE 36-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp. Range (in °C)	Max. Frequency	Comment
			PIC32MZ EC Devices	
DC5	**2.3V**-3.6V	-40°C to +85°C	200 MHz	—
DC5b	**2.3V**-3.6V	-40°C to +125°C	200 MHz	Planned

TABLE 36-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Operating Voltage							
DC10	VDD	Supply Voltage	**2.3**	—	3.6	V	—

TABLE 36-5: ELECTRICAL CHARACTERISTICS: BOR

Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD transition high-to-low	**1.9**	—	**2.3**	V	—

AC Characteristics (see page 590 in the data sheet)

TABLE 36-37: ADC1 MODULE SPECIFICATIONS

Param.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or **2.3**	—	Lesser of VDD + 0.3 or 3.6	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 1.2	—	AVDD	V	(Note 1)
AD05a			**2.3**	—	3.6	V	VREFH = AVDD (Note 3)

3. Module: Internal FRC Accuracy

Certain specifications in Table 36-19 were stated incorrectly in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 36-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal FRC Accuracy @ 8.00 MHz						
F20	FRC	**-0.9**	**—**	**+0.9**	%	0°C ≤ TA ≤ +70°C
		-5	**—**	**+5**	%	-40°C ≤ TA ≤ +85°C

4. Module: Internal LPRC Accuracy

Certain specifications in Table 36-20 were stated incorrectly and omitted in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 36-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal LPRC @ 32.768 kHz						
F21	LPRC	**-5**	**—**	**+5**	%	**0°C ≤ TA ≤ +85°C**
		-20	**—**	**+20**	**%**	**-40°C ≤ TA ≤ +85°C**

5. Module: Internal Backup FRC (BFRC) Accuracy

Certain specifications in Table 36-21 were stated incorrectly in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 36-21: INTERNAL BACKUP FRC (BFRC) ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal BFRC Accuracy @ 8 MHz						
F22	BFRC	**-10**	**—**	**+10**	%	—

6. Module: ADC1 Module Specifications and Timing Requirements

a) Certain specifications in Table 36-37 were stated incorrectly in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 36-37: ADC1 MODULE SPECIFICATIONS

AC CHARACTERISTICS[5,6]			Standard Operating Conditions (see Notes **3**,**5**): **2.3V** to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or **2.3**	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 1.2	—	**AVDD**	V	VREFH = **VREF+** (Note 1)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 1.2	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	1.2	—	**AVDD**	V	(Notes 4)
AD08 AD08a	IREF	Current Drain	— —	**100** .002	**150** 1	μA μA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Range	**– VREFH** 0	— —	**+ VREFH** **+ VREFH**	V V	Differential Single-ended
AD14	VINCM	Common Mode Input Voltage	AVSS + VREF/2	—	AVDD – VREF/2	V	—
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	**—**	**200**	Ω	(Note 1) For minimum sampling time
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	**10** data bits			bits	—
AD21c	INL	Integral Nonlinearity	—	**±2**	—	LSb	VINL = **VREF-** = VREFL = 0V, **VREF+** = VREFH = **3.0**V
AD22c	DNL	Differential Nonlinearity	—	**±2**	—	LSb	VINL = **VREF-** = VREFL = 0V, **VREF+** = VREFH = **3.0**V
AD23c	GERR	Gain Error	—	**±8**	—	LSb	VINL = **VREF-** = VREFL = 0V, **VREF+** = VREFH = **3.0**V
AD24c	EOFF	Offset Error	—	**±10**	—	LSb	**VINL = VREF- = VREFL = 0V, VREF+ = VREFH = 3.0V**
AD25e	**—**	**Monotonicity**	**—**	**—**	**—**	**—**	**Guaranteed**
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	**48**	—	> **54**	dB	(Notes 2)
AD34b	ENOB	Effective Number of bits	**8**	—	**9**	bits	(Notes 2)

Note 1: These parameters are not characterized or tested in manufacturing.

2: Characterized with a 1 kHz sine wave.

3: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

4: The BOOST bit (AD1CON2<6>) must be set to '1' when VREF ≤ 1.8V.

5: Specifications are based on adherence to the requirements listed in 28.1 "ADC Configuration Requirements".

6: External precision VREF+ and VREF- must be used at all times.

b) Certain specifications in Table 36-38 were stated incorrectly in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 36-38: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS[2,5]			Standard Operating Conditions (see Note 2,**5**): **2.3V** to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typ.[1]	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period	**62.5**	—	1000	ns	—
Throughput Rate							
AD51	FTP	SH0 – SH4 (Class 1 Inputs)	—	—	**—**	**—**	—
		SH5 (Class 2 and 3 Inputs)	—	—	**500**	**ksps**	Single Class 2 or 3 input, **16** MHz ADC Clock, Source impedance ≤ 200 Ω, SAMC = **3**, Assumes there are no pending sample conversion operations at time of trigger. **(Notes 3, 4)**
		Conversion Pipeline	—	—	**16**	Msps	—
Timing Parameters							
AD60	TSAMP	Sample Time for SH0-SH4 (Class 1 Inputs)	—	**—**	—	TAD	—
		Sample Time for SH5 (Class 2 and 3 Inputs)	3 6 9 35 68 133 256	—	—	TAD	Source Impedance ≤ 200 Ω, **16** MHz ADC clock Source Impedance ≤ 500 Ω, **16** MHz ADC clock Source Impedance ≤ 1 KΩ, **16** MHz ADC clock Source Impedance ≤ 5 KΩ, **16** MHz ADC clock Source Impedance ≤ 10 KΩ, **16** MHz ADC clock Source Impedance ≤ 20 KΩ, **16** MHz ADC clock Source Impedance ≤ 35 KΩ, **16** MHz ADC clock
AD62	TCONV	Conversion Time (after sample time is complete)	—	—	10	TAD	For SH5, TSAMP + TCONV provides Trigger to data ready timing;
AD64	TCAL	Calibration Time	—	160	—	TAD	—
AD65	TWAKE	Wake-up time from Low-Power Mode	—	2	—	TAD	—

Note 1: These parameters are not characterized, or tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

3: Assuming correct PLL configuration (i.e., 192 MHz system clock).

4: Assuming 4x Oversampling mode.

5: Specifications are based on adherence to the requirements listed in 28.1 "ADC Configuration Requirements".

7. Module: ADC Configuration Requirements

To meet ADC specifications, the following steps must be performed:

1. Set the ADC Configuration words, as follows:

```
AD1CAL1 = 0xF8894530;
AD1CAL2 = 0x01E4AF69;
AD1CAL3 = 0x0FBBBBB8;
AD1CAL4 = 0x000004AC;
AD1CAL5 = 0x02000002;
```

2. Perform self-calibration. The input mode for SH0-SH5 must be set to the unipolar differential input mode by setting the SHxMOD<1:0> bits (AD1MOD<1:0>) = `10`.

Note:	SH0 through SH4 functionality is not supported, but is required for auto-calibration. Sampling must be performed on SH5 only.

3. ADC module access directly by the CPU of any Special Function Registers while the module is operating is not supported. ADC must be configured in DMA mode to read result registers.
4. After any Reset, a software offset calibration must be performed by connecting the ADC to the Internal Band Gap Reference (IVREF) source and taking the average of 256 – 16 sequential measurements, discarding the first 16 of 256 results by the ADC in 16x hardware oversampling, (i.e., 256 * 16x = 4096), using the DMA. Then, compute the difference to the specified 1.2V IVREF voltage versus the actual. The LSB count difference error must be applied by software to subsequent user application ADC conversion results to compensate for the offset error according to the following:
   a) If the IVREF ADC average count measured is ≥ 1.2V ideal count:
      ADC normalized result = (User ADC Result count – (IVREF ADC average count – Ideal 1.2V count))
   b) If the IVREF ADC AVG count measured is < 1.2V ideal count:
      ADC normalized result = (User ADC Result count + (Ideal 1.2V count – IVREF ADC average count))
5. The ADC Clock (i.e.,TAD) must be limited to 1 MHz ≤ TAD ≤ 16 MHz (i.e., 1000 ns ≤ TAD ≤ 62.5 ns.
6. ADC maximum conversion rate:
   a) 125 ksps
   b) For ADC SH5: SR = ((Samc + 1)TAD + 4TAD), Samc(min) = 3.
7. ADC ≥ 16x hardware oversampling is required.

Note:	16x hardware oversampling gives a 14-bit ADC result, 256x hardware oversampling gives a 16-bit ADC result.

8. The first (16) conversion in 16x Oversampling mode after enabling the ADC, regardless of the ADC hardware oversampling filter selected, must be discarded.
9. External precision VREF+ and VREF- must be used at all times (set the VREFSEL<2:0> bits (AD1CON3<12:10>) = `'b011`).

8. Module: SQI Timing Requirements

Specifications for parameter SQ10 (F_{CLK}) in Table 36-33 were stated incorrectly in the data sheet. The correct values are shown in the following table.

TABLE 36-33: SQI TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
SQ10	F_{CLK}	Serial Clock Frequency (1/T_{SQI})	—	—	50	MHz	

9. Module: DC Temperature and Voltage Specifications

Specifications for parameter DC17 (SV_{DD}) in Table 36-4 were stated incorrectly in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 36-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Operating Voltage							
DC17	SV_{DD}	V_{DD} Rise Rate to Ensure Internal Power-on Reset Signal	**0.00004**	—	**0.0004**	V/µs	—

10. Module: Recommended Minimum Connection

Note 1 in Figure 2-1: Recommended Minimum Connection in the data sheet incorrectly states that the V_{USB3V3} pin must be connected to V_{DD} if the USB module is not used.

The correct configuration is for this pin to be connected to **Vss** when the USB module is not used.

11. Module: USB OTG Electrical Specifications and System Timing Requirements

Note 2 for the Characteristics column was omitted from Table 36-43: USB OTG Electrical Specifications. The notes should read: See OS51 for system frequency requirements.

Specifications for parameter OS51 (FSYS) in Table 36-17: System Timing Requirements, were omitted in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 36-17: SYSTEM TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Minimum	Typical	Maximum	Units	Conditions
OS51	FSYS	System Frequency	DC	—	200	MHz	**USB module disabled**
			30	**—**	**200**	**MHz**	**USB module enabled**

APPENDIX A: REVISION HISTORY

Rev A Document (11/2013)

Initial release of this document, issued for revision A3 silicon.

This version includes the following issues: 1 (ADC), 2 (ADC), 3 (Boot Flash), 4 (Comparator Voltage Reference), 5 (Ethernet Controller), 6 (Ethernet Controller), 7 (Ethernet Controller), 8 (I/O Port), 9 (Oscillator), 10 (Oscillator), 11 (Secondary Oscillator), 12 (LPRC Oscillator), 13 (Power-Saving Modes), 14 (Power-Saving Modes), 15 (SPI), 16 (SQI), 17 (System Bus), 18 (USB), 19 (USB), 20 (USB), 21 (USB), 22 (Watchdog Timer), 23 (Watchdog Timer), 24 (PMP), 25 (I^2C), 26 (Crypto Engine), and 27 (Random Number Generator).

Rev B Document (12/2013)

Updated issues 7 (Ethernet Controller) and 14 (Power-Saving Modes).

Content in issue 21, which was included in a previous errata version, was removed and this issue has been marked as **Reserved**.

Added data sheet clarification issues 1 (Power-Down Current) and 2 (Operating Conditions), and silicon issues 28 (Flash) and 29 (ADC).

Rev C Document (4/2014)

Updated for revision A4 silicon.

Content in issues 12 and 16, which was included in a previous errata version, was removed and these issues have been marked as **Reserved**.

Added silicon issues 30 (SQI), 31 (SQI), 32 (SQI), 33 (SQI), 34 (SQI), 35 (SQI), 36 (Comparator), 37 (Comparator), 38 (I/O Pins), 39 (I^2C), 40 (Flash Memory), 41 (Oscillator), 42 (5V Tolerant I/O Pins), 43 (ADC), 44 (ADC), and 45 (Prefetch).

Added data sheet clarification issues 3 (Internal FRC Accuracy), 4 (Internal LPRC Accuracy), 5 (Internal Backup FRC (BFRC) Accuracy), 6 (ADC1 Module Specifications and Timing Requirements), 7 (ADC Configuration Requirements), 8 (SQI Timing Requirements), 9 (DC Temperature and Voltage Specifications), 10 (Recommended Minimum Connection), and 11 (USB OTG Electrical Specifications and System Timing Requirements).

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