Hex D Flip-Flop with Master Reset

The MC74AC174/74ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

- Outputs Source/Sink 24 mA
- 'ACT174 Has TTL Compatible Inputs

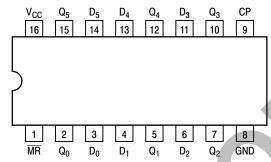


Figure 1. Pinout: 16-Lead Packages Conductors (Top View)

PIN ASSIGNMENT

Figur	1 2 MR Q ₀ e 1. Pir	D ₀	4 5 D ₁ Q ₁ S-Lead Paci (Top View)	6 7 8 D ₂ Q ₂ GND kages Conductors	CEIRO	16 16 16
PIN		FUNCT	TON		7,10, 4	
D ₀ -D ₅		Data In	puts		X - 11V	ORDI
CP		Clock F	Pulse Input	.5		Device
MR		Master	Reset Input	141 16		MC74AC174N
Q_0-Q_5		Outputs	3		4	MC74ACT174N
				~O, C		MC74AC174D
TRUTI	H TABL	.E		1,0 4,5		MC74ACT174D
	Inputs		Output	6000		MC74AC174DR
MR	CP	D	Q	> ()		MC74ACT174D
L	Х	X	L			MC74AC174DT
H H	7	H L	H			MC74ACT174D
Н	L	X	Q			MC74AC174DT

TRUTH TABLE

	Inputs	Output	
MR	CP	D	Q
L	Х	Х	L
Н		Н	Н
Н	工	L	Ľ
Н	L	Х	Q

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

_ LOW-to-HIGH Transition of Clock



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DIP-16 **N SUFFIX CASE 648**



SO-16 **D SUFFIX** CASE 751B



TSSOP-16 **DT SUFFIX** CASE 948F



EIAJ-16 **M SUFFIX CASE 966**

ORDERING INFORMATION

Device	Package	Shipping
MC74AC174N	PDIP-16	25 Units/Rail
MC74ACT174N	PDIP-16	25 Units/Rail
MC74AC174D	SOIC-16	48 Units/Rail
MC74ACT174D	SOIC-16	48 Units/Rail
MC74AC174DR2	SOIC-16	2500 Tape & Reel
MC74ACT174DR2	SOIC-16	2500 Tape & Reel
MC74AC174DT	TSSOP-16	96 Units/Rail
MC74ACT174DT	TSSOP-16	96 Units/Rail
MC74AC174DTR2	TSSOP-16	2500 Tape & Reel
MC74AC174M	EIAJ-16	50 Units/Rail
MC74ACT174M	EIAJ-16	50 Units/Rail
MC74AC174MEL	EIAJ-16	2000 Tape & Reel
MC74ACT174MEL	EIAJ-16	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.

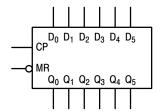
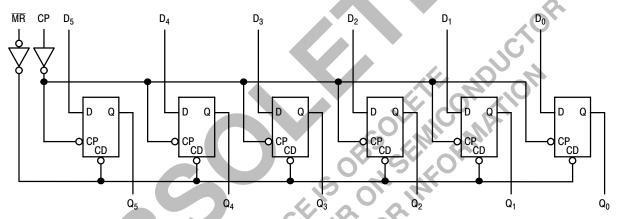


Figure 2. Logic Symbol

FUNCTIONAL DESCRIPTION

The MC74AC174/74ACT174 consists of six edge–triggered D flip–flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (\overline{MR}) are common to all flip–flops. Each D input's state is transferred to the corresponding flip–flop's output following the

LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset (\overline{MR}) will force all outputs LOW independent of Clock or Data inputs. The MC74AC174/ 74ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	٧
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

^{*}Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Тур	Max	Unit		
.,	O and Mallana	'AC	2.0	5.0	6.0		
V _{CC}	Supply Voltage	'ACT	4.5	5.0	5.5	V	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	-	V _{CC}	V	
t _r , t _f		V _{CC} @ 3.0 V	-	150	-		
	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 4.5 V	-	40	-	ns/V	
	// Borrood oxoopt Committee impate	V _{CC} @ 5.5 V	-	25	-		
	Input Rise and Fall Time (Note 2)	V _{CC} @ 4.5 V	-	10	-	0/	
t _r , t _f	'ACT Devices except Schmitt Inputs	V _{CC} @ 5.5 V	_	8.0	-	ns/V	
TJ	Junction Temperature (PDIP)		7- ,	_	140	°C	
T _A	Operating Ambient Temperature Range	-40	25	85	°C		
I _{OH}	Output Current – High		4	-	-24	mA	
I _{OL}	Output Current - Low		-	-	24	mA	

^{1.} V_{IN} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times. 2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

			74/	AC	74AC		1
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C	Unit	Conditions
			Тур	Guar	anteed Limits		
V _{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	>	$V_{OUT} = 0.1 V$ or $V_{CC} - 0.1 V$
V _{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	٧	I _{OUT} = -50 μA
	CON	3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	٧	$^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ -12 mA $I_{OH} -24 \text{ mA}$ -24 mA
V _{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	Ι _{ΟUT} = 50 μΑ
	Maximum Low Level Output Voltage	3.0 4.5 5.5	1 1 1	0.36 0.36 0.36	0.44 0.44 0.44	٧	$^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL} \qquad 24 \text{ mA}$ 24 mA
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μΑ	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic	5.5	-	-	75	mA	V _{OLD} = 1.65 V Max
I _{OHD}	Output Current	5.5	-	ı	-75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80	μΑ	V _{IN} = V _{CC} or GND

^{*}All outputs loaded; thresholds on input associated with output under test. \dagger Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC} .

AC CHARACTERISTICS (For Figures and Waveforms - See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

			74AC			74AC			
Symbol	Parameter		T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Unit	Fig. No.
			Min	Тур	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	90 100	100 125	1 1	70 100	-	MHz	3–3
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0	2.0 1.5	9.0 6.0	11.5 8.5	1.5 1.0	12.5 9.5	ns	3–6
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0	2.0 1.5	8.5 6.0	11.0 8.0	1.5 1.0	12.0 9.0	ns	3–6
t _{PHL}	Propagation Delay \overline{MR} to Q_n	3.3 5.0	2.5 1.5	9.0 7.0	11.5 9.0	2.0 1.5	12.5 10.5	ns	3–6

^{*}Voltage Range 3.3 V is 3.3 V ±0.3 V.

AC OPERATING REQUIREMENTS

				74AC	74AC			
Symbol	Parameter		T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF	Unit	Fig. No.	
			Тур	Guaranteed	d Minimum			
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0	2.5 2.0	6.5 5.0	7.0 5.5	ns	3–9	
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0	1.0 0.5	3.0 3.0	3.0 3.0	ns	3–9	
t _w	MR Pulse Width, LOW	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	ns	3–6	
t _w	CP Pulse Width	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	ns	3–6	
t _{rec}	Recovery Time MR to CP	3.3 5.0	0	2.5 2.0	2.5 2.0	ns	3–6	
	MR to CP ge 3.3 V is 3.3 V ±0.3 V. ge 5.0 V is 5.0 V ±0.5 V.							

^{*}Voltage Range 5.0 V is 5.0 V ±0.5 V.

^{*}Voltage Range 3.3 V is 3.3 V ± 0.3 V. *Voltage Range 5.0 V is 5.0 V ± 0.5 V.

DC CHARACTERISTICS

			744	СТ	74ACT		
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C	Unit	Conditions
			Тур	Guar	anteed Limits		
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = -50 μA
		4.5 5.5	- -	3.86 4.86	3.76 4.76	V	$^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{-}24 \text{ mA}$ ^{1}OH $^{-}24 \text{ mA}$
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5	-	0.36 0.36	0.44 0.44	v,C	$^{*}V_{IN}$ = V_{IL} or V_{IH} 24 mA I_{OL} 24 mA
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μΑ	V _I = V _{CC} , GND
ΔI_{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5	mA	V _I = V _{CC} - 2.1 V
I _{OLD}	†Minimum Dynamic	5.5	-	0	75	mA	V _{OLD} = 1.65 V Max
I _{OHD}	Output Current	5.5	- ($\mathcal{O}_{\mathbf{Y}}$	-75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	(5)	8.0	80	μΑ	V _{IN} = V _{CC} or GND

^{*}All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms - See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

			74ACT			74ACT			
Symbol	Parameter		T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Unit	Fig. No.
	,0,00		Min	Тур	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	165	-	-	140	-	MHz	3–3
t _{PLH}	Propagation Delay CP to Q _n	5.0	1.5	ı	10.5	1.5	11.5	ns	3–6
t _{PHL}	Propagation Delay CP to Q _n	5.0	1.5	ı	10.5	1.5	11.5	ns	3–6
t _{PHL}	Propagation Delay MR to Q _n	5.0	1.5	ı	9.5	1.5	11.0	ns	3–6

^{*}Voltage Range 5.0 V is 5.0 V ± 0.5 V.

AC OPERATING REQUIREMENTS

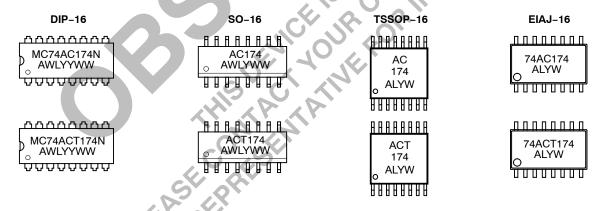
	Parameter			74ACT	74ACT		
Symbol				դ = +25°C L = 50 pF	T _A = -40°C to +85°C C _L = 50 pF	Unit	Fig. No.
			Тур	Guaranteed	Minimum	1	
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	-	1.5	1.5	ns	3–9
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	-	2.0	2.0	ns	3–9
t _w	MR Pulse Width, LOW	5.0	-	3.0	3.5	ns	3–6
t _w	CP Pulse Width HIGH or LOW	5.0	-	3.0	3.5	ns	3-6
t _{rec}	Recovery Time MR to CP	5.0	-	0.5	0.5	ns	3–6

^{*}Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	85	pF	V _{CC} = 5.0 V

MARKING DIAGRAMS

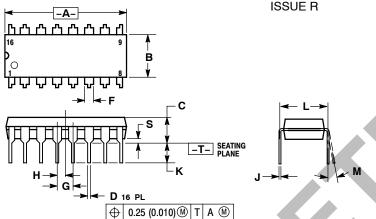


A = Assembly Location

WL, L = Wafer Lot YY, Y = Year WW, W = Work Week

PACKAGE DIMENSIONS

PDIP-16 **N SUFFIX** 16 PIN PLASTIC DIP PACKAGE CASE 648-08

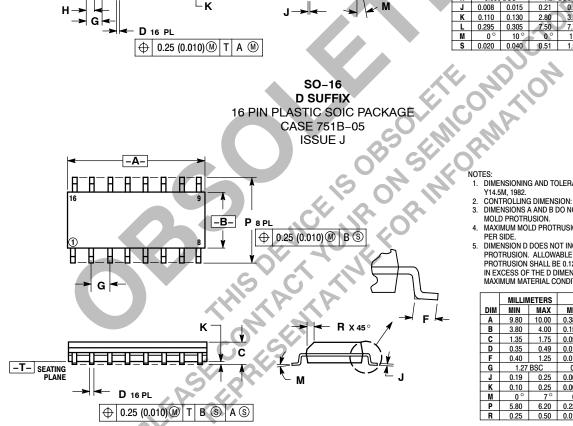


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- DIMENSIONING AND TOLERANCING FER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL DIMENSION B DOES NOT INCLUDE MOLD FLASH. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
Н	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10 °
S	0.020	0.040	0.51	1.01

SO-16 D SUFFIX 16 PIN PLASTIC SOIC PACKAGE CASE 751B-05 CASE 751B-05 ISSUE J



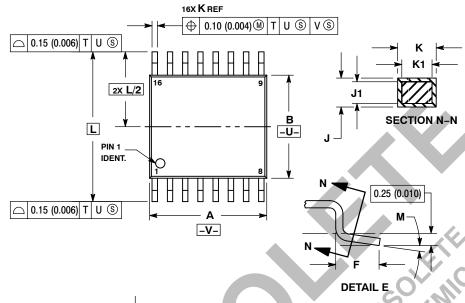
- DIMENSIONING AND TOLERANCING PER ANSI

- THE TOTAL THE TOTAL AND TOTAL AND TOTAL AND TOTAL AND TOTAL AND THE TOTAL AND T
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

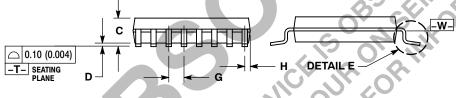
TSSOP-16 **DT SUFFIX** 16 PIN PLASTIC TSSOP PACKAGE CASE948F-01 **ISSUE O**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
 - Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH.
 PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE INTERLEAD
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE. DIMENSION K DOES NOT INCLUDE DAMBAR
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0,08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

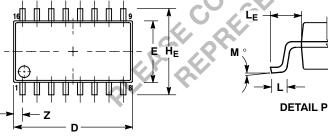
 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

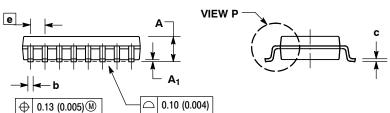
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
C	1	1.20		0.047
D (0.05	0.15	0.002	0.006
E	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°





 Q_1





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD
 FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
 THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

 DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD

10 BE 0.40 (0.010).					
	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A ₁	0.05	0.20	0.002	0.008	
p	0.35	0.50	0.014	0.020	
С	0.18	0.27	0.007	0.011	
D	9.90	10.50	0.390	0.413	
Ε	5.10	5.45	0.201	0.215	
е	1.27 BSC		0.050 BSC		
ΗE	7.40	8.20	0.291	0.323	
٦	0.50	0.85	0.020	0.033	
П	1.10	1.50	0.043	0.059	
M	0 °	10 °	0°	10 °	
Q ₁	0.70	0.90	0.028	0.035	
Z		0.78		0.031	



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