5.1 SX1512 16-channel GPIO with LED Driver and Keypad Engine

Address	Name	Description	Default
Device and IO Banks			
0x00	**RegInputDisableB**	Input buffer disable register - I/O[15-8] (Bank B)	0000 0000
0x01	**RegInputDisableA**	Input buffer disable register - I/O[7-0] (Bank A)	0000 0000
0x02	**RegLongSlewB**	Output buffer long slew register - I/O[15-8] (Bank B)	0000 0000
0x03	**RegLongSlewA**	Output buffer long slew register - I/O[7-0] (Bank A)	0000 0000
0x04	**RegLowDriveB**	Output buffer low drive register - I/O[15-8] (Bank B)	0000 0000
0x05	**RegLowDriveA**	Output buffer low drive register - I/O[7-0] (Bank A)	0000 0000
0x06	**RegPullUpB**	Pull-up register - I/O[15-8] (Bank B)	0000 0000
0x07	**RegPullUpA**	Pull-up register - I/O[7-0] (Bank A)	0000 0000
0x08	**RegPullDownB**	Pull-down register - I/O[15-8] (Bank B)	0000 0000
0x09	**RegPullDownA**	Pull-down register - I/O[7-0] (Bank A)	0000 0000
0x0A	**RegOpenDrainB**	Open drain register - I/O[15-8] (Bank B)	0000 0000
0x0B	**RegOpenDrainA**	Open drain register - I/O[7-0] (Bank A)	0000 0000
0x0C	**RegPolarityB**	Polarity register - I/O[15-8] (Bank B)	0000 0000
0x0D	**RegPolarityA**	Polarity register - I/O[7-0] (Bank A)	0000 0000
0x0E	**RegDirB**	Direction register - I/O[15-8] (Bank B)	1111 1111
0x0F	**RegDirA**	Direction register - I/O[7-0] (Bank A)	1111 1111
0x10	**RegDataB**	Data register - I/O[15-8] (Bank B)	1111 1111*
0x11	**RegDataA**	Data register - I/O[7-0] (Bank A)	1111 1111*
0x12	**RegInterruptMaskB**	Interrupt mask register - I/O[15-8] (Bank B)	1111 1111
0x13	**RegInterruptMaskA**	Interrupt mask register - I/O[7-0] (Bank A)	1111 1111
0x14	**RegSenseHighB**	Sense register for I/O[15:12]	0000 0000
0x15	**RegSenseLowB**	Sense register for I/O[11:8]	0000 0000
0x16	**RegSenseHighA**	Sense register for I/O[7:4]	0000 0000
0x17	**RegSenseLowA**	Sense register for I/O[3:0]	0000 0000
0x18	**RegInterruptSourceB**	Interrupt source register - I/O[15-8] (Bank B)	0000 0000
0x19	**RegInterruptSourceA**	Interrupt source register - I/O[7-0] (Bank A)	0000 0000
0x1A	**RegEventStatusB**	Event status register - I/O[15-8] (Bank B)	0000 0000
0x1B	**RegEventStatusA**	Event status register - I/O[7-0] (Bank A)	0000 0000
0x1C	**RegLevelShifter1**	Level shifter register	0000 0000
0x1D	**RegLevelShifter2**	Level shifter register	0000 0000
0x1E	**RegClock**	Clock management register	0000 0000
0x1F	**RegMisc**	Miscellaneous device settings register	0000 0000
0x20	**RegLEDDriverEnableB**	LED driver enable register - I/O[15-8] (Bank B)	0000 0000
0x21	**RegLEDDriverEnableA**	LED driver enable register - I/O[7-0] (Bank A)	0000 0000
Debounce and Keypad Engine			
0x22	**RegDebounceConfig**	Debounce configuration register	0000 0000
0x23	**RegDebounceEnableB**	Debounce enable register - I/O[15-8] (Bank B)	0000 0000
0x24	**RegDebounceEnableA**	Debounce enable register - I/O[7-0] (Bank A)	0000 0000
0x25	**RegKeyConfig1**	Key scan configuration register	0000 0000
0x26	**RegKeyConfig2**	Key scan configuration register	0000 0000
0x27	**RegKeyData1**	Key value (column)	1111 1111
0x28	**RegKeyData2**	Key value (row)	1111 1111
LED Driver (PWM, blinking, breathing)			
0x29	**RegTOn0**	ON time register for I/O[0]	0000 0000
0x2A	**RegIOn0**	ON intensity register for I/O[0]	1111 1111
0x2B	**RegOff0**	OFF time/intensity register for I/O[0]	0000 0000
0x2C	**RegTOn1**	ON time register for I/O[1]	0000 0000
0x2D	**RegIOn1**	ON intensity register for I/O[1]	1111 1111
0x2E	**RegOff1**	OFF time/intensity register for I/O[1]	0000 0000
0x2F	**RegTOn2**	ON time register for I/O[2]	0000 0000
0x30	**RegIOn2**	ON intensity register for I/O[2]	1111 1111
0x31	**RegOff2**	OFF time/intensity register for I/O[2]	0000 0000
0x32	**RegTOn3**	ON time register for I/O[3]	0000 0000
0x33	**RegIOn3**	ON intensity register for I/O[3]	1111 1111
0x34	**RegOff3**	OFF time/intensity register for I/O[3]	0000 0000
0x35	**RegTOn4**	ON time register for I/O[4]	0000 0000
0x36	**RegIOn4**	ON intensity register for I/O[4]	1111 1111
0x37	**RegOff4**	OFF time/intensity register for I/O[4]	0000 0000

Address	Name	Description	Default
0x38	**RegTRise4**	Fade in register for I/O[4]	0000 0000
0x39	**RegTFall4**	Fade out register for I/O[4]	0000 0000
0x3A	**RegTOn5**	ON time register for I/O[5]	0000 0000
0x3B	**RegIOn5**	ON intensity register for I/O[5]	1111 1111
0x3C	**RegOff5**	OFF time/intensity register for I/O[5]	0000 0000
0x3D	**RegTRise5**	Fade in register for I/O[5]	0000 0000
0x3E	**RegTFall5**	Fade out register for I/O[5]	0000 0000
0x3F	**RegTOn6**	ON time register for I/O[6]	0000 0000
0x40	**RegIOn6**	ON intensity register for I/O[6]	1111 1111
0x41	**RegOff6**	OFF time/intensity register for I/O[6]	0000 0000
0x42	**RegTRise6**	Fade in register for I/O[6]	0000 0000
0x43	**RegTFall6**	Fade out register for I/O[6]	0000 0000
0x44	**RegTOn7**	ON time register for I/O[7]	0000 0000
0x45	**RegIOn7**	ON intensity register for I/O[7]	1111 1111
0x46	**RegOff7**	OFF time/intensity register for I/O[7]	0000 0000
0x47	**RegTRise7**	Fade in register for I/O[7]	0000 0000
0x48	**RegTFall7**	Fade out register for I/O[7]	0000 0000
0x49	**RegTOn8**	ON time register for I/O[8]	0000 0000
0x4A	**RegIOn8**	ON intensity register for I/O[8]	1111 1111
0x4B	**RegOff8**	OFF time/intensity register for I/O[8]	0000 0000
0x4C	**RegTOn9**	ON time register for I/O[9]	0000 0000
0x4D	**RegIOn9**	ON intensity register for I/O[9]	1111 1111
0x4E	**RegOff9**	OFF time/intensity register for I/O[9]	0000 0000
0x4F	**RegTOn10**	ON time register for I/O[10]	0000 0000
0x50	**RegIOn10**	ON intensity register for I/O[10]	1111 1111
0x51	**RegOff10**	OFF time/intensity register for I/O[10]	0000 0000
0x52	**RegTOn11**	ON time register for I/O[11]	0000 0000
0x53	**RegIOn11**	ON intensity register for I/O[11]	1111 1111
0x54	**RegOff11**	OFF time/intensity register for I/O[11]	0000 0000
0x55	**RegTOn12**	ON time register for I/O[12]	0000 0000
0x56	**RegIOn12**	ON intensity register for I/O[12]	1111 1111
0x57	**RegOff12**	OFF time/intensity register for I/O[12]	0000 0000
0x58	**RegTRise12**	Fade in register for I/O[12]	0000 0000
0x59	**RegTFall12**	Fade out register for I/O[12]	0000 0000
0x5A	**RegTOn13**	ON time register for I/O[13]	0000 0000
0x5B	**RegIOn13**	ON intensity register for I/O[13]	1111 1111
0x5C	**RegOff13**	OFF time/intensity register for I/O[13]	0000 0000
0x5D	**RegTRise13**	Fade in register for I/O[13]	0000 0000
0x5E	**RegTFall13**	Fade out register for I/O[13]	0000 0000
0x5F	**RegTOn14**	ON time register for I/O[14]	0000 0000
0x60	**RegIOn14**	ON intensity register for I/O[14]	1111 1111
0x61	**RegOff14**	OFF time/intensity register for I/O[14]	0000 0000
0x62	**RegTRise14**	Fade in register for I/O[14]	0000 0000
0x63	**RegTFall14**	Fade out register for I/O[14]	0000 0000
0x64	**RegTOn15**	ON time register for I/O[15]	0000 0000
0x65	**RegIOn15**	ON intensity register for I/O[15]	1111 1111
0x66	**RegOff15**	OFF time/intensity register for I/O[15]	0000 0000
0x67	**RegTRise15**	Fade in register for I/O[15]	0000 0000
0x68	**RegTFall15**	Fade out register for I/O[15]	0000 0000
Miscellaneous			
0x69	**RegHighInputB**	High input enable register - I/O[15-8] (Bank B)	0000 0000
0x6A	**RegHighInputA**	High input enable register - I/O[7-0] (Bank A)	0000 0000
Software Reset			
0x7D	**RegReset**	Software reset register	0000 0000
Test (not to be written)			
0x7E	**RegTest1**	Test register	0000 0000
0x7F	**RegTest2**	Test register	0000 0000

*Bits set as output take "1" as default value.

Table 12 – SX1512 Configuration Registers Overview

Addr	Name	Default	Bits	Description	
0x00	**RegInputDisableB**	0x00	7:0	Disables the input buffer of each IO 0 : Input buffer is enabled (input actually being used) 1 : Input buffer is disabled (input actually not being used or LED connection)	
0x01	**RegInputDisableA**	0x00	7:0	Disables the input buffer of each IO 0 : Input buffer is enabled (input actually being used) 1 : Input buffer is disabled (input actually not being used, LED connection)	
0x02	**RegLongSlewB**	0x00	7:0	Enables increased slew rate of the output buffer of each [output-configured] IO 0 : Increased slew rate is disabled 1 : Increased slew rate is enabled	
0x03	**RegLongSlewA**	0x00	7:0	Enables increased slew rate of the output buffer of each [output-configured] IO 0 : Increased slew rate is disabled 1 : Increased slew rate is enabled	
0x04	**RegLowDriveB**	0x00	7:0	Enables reduced drive of the output buffer of each [output-configured] IO 0 : Reduced drive is disabled 1 : Reduced drive is enabled	
0x05	**RegLowDriveA**	0x00	7:0	Enables reduced drive of the output buffer of each [output-configured] IO 0 : Reduced drive is disabled 1 : Reduced drive is enabled	
0x06	**RegPullUpB**	0x00	7:0	Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled	
0x07	**RegPullUpA**	0x00	7:0	Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled	
0x08	**RegPullDownB**	0x00	7:0	Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled	
0x09	**RegPullDownA**	0x00	7:0	Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled	
0x0A	**RegOpenDrainB**	0x00	7:0	Enables open drain operation for each [output-configured] IO 0 : Regular push-pull operation 1 : Open drain operation	
0x0B	**RegOpenDrainA**	0x00	7:0	Enables open drain operation for each [output-configured] IO 0 : Regular push-pull operation 1 : Open drain operation	
0x0C	**RegPolarityB**	0x00	7:0	Enables polarity inversion for each IO 0 : Normal polarity : RegData[x] = IO[x] 1 : Inverted polarity : RegData[x] = !IO[x] (for both input and output configured IOs)	
0x0D	**RegPolarityA**	0x00	7:0	Enables polarity inversion for each IO 0 : Normal polarity : RegData[x] = IO[x] 1 : Inverted polarity : RegData[x] = !IO[x] (for both input and output configured IOs)	
0x0E	**RegDirB**	0xFF	7:0	Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input	
0x0F	**RegDirA**	0xFF	7:0	Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input	
0x10	**RegDataB**	0xFF	7:0	Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured.	
0x11	**RegDataA**	0xFF	7:0	Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured.	
0x12	**RegInterruptMaskB**	0xFF	7:0	Configures which [input-configured] IO will trigger an interrupt on NINT pin 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt	
0x13	**RegInterruptMaskA**	0xFF	7:0	Configures which [input-configured] IO will trigger an interrupt on NINT pin 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt	
0x14	**RegSenseHighB**	0x00	7:6	Edge sensitivity of RegData[15]	00 : None 01 : Rising 10 : Falling 11 : Both
			5:4	Edge sensitivity of RegData[14]	
			3:2	Edge sensitivity of RegData[13]	
			1:0	Edge sensitivity of RegData[12]	
0x15	**RegSenseLowB**	0x00	7:6	Edge sensitivity of RegData[11]	00 : None 01 : Rising 10 : Falling 11 : Both
			5:4	Edge sensitivity of RegData[10]	
			3:2	Edge sensitivity of RegData[9]	
			1:0	Edge sensitivity of RegData[8]	
0x16	**RegSenseHighA**	0x00	7:6	Edge sensitivity of RegData[7]	00 : None 01 : Rising 10 : Falling 11 : Both
			5:4	Edge sensitivity of RegData[6]	
			3:2	Edge sensitivity of RegData[5]	
			1:0	Edge sensitivity of RegData[4]	
0x17	**RegSenseLowA**	0x00	7:6	Edge sensitivity of RegData[3]	00 : None 01 : Rising
			5:4	Edge sensitivity of RegData[2]	

			3:2	Edge sensitivity of RegData[1]	
			1:0	Edge sensitivity of RegData[0]	
0x18	**RegInterruptSourceB**	0x00	7:0	Interrupt source (from IOs set in RegInterruptMask) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occured). Writing '1' clears the bit in RegInterruptSource and in RegEventStatus When all bits are cleared, NINT signal goes back high.	
0x19	**RegInterruptSourceA**	0x00	7:0	Interrupt source (from IOs set in RegInterruptMask) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occured). Writing '1' clears the bit in RegInterruptSource and in RegEventStatus When all bits are cleared, NINT signal goes back high.	
0x1A	**RegEventStatusB**	0x00	7:0	Event status of all IOs. 0 : No event has occured on this IO 1 : An event has occured on this IO (an edge as configured in relevant RegSense register occured). Writing '1' clears the bit in RegEventStatus and in RegInterruptSource if relevant. If the edge sensitivity of the IO is changed, the bit(s) will be cleared automatically	
0x1B	**RegEventStatusA**	0x00	7:0	Event status of all IOs. 0 : No event has occured on this IO 1 : An event has occured on this IO (an edge as configured in relevant RegSense register occured). Writing '1' clears the bit in RegEventStatus and in RegInterruptSource if relevant. If the edge sensitivity of the IO is changed, the bit(s) will be cleared automatically	
0x1C	**RegLevelShifter1**	0x00	7:6	Level shifter mode for IO[7] (Bank A) and IO[15] (Bank B)	00 : OFF 01 : A->B 10 : B->A 11 : Reserved
			5:4	Level shifter mode for IO[6] (Bank A) and IO[14] (Bank B)	
			3:2	Level shifter mode for IO[5] (Bank A) and IO[13] (Bank B)	
			1:0	Level shifter mode for IO[4] (Bank A) and IO[12] (Bank B)	
0x1D	**RegLevelShifter2**	0x00	7:6	Level shifter mode for IO[3] (Bank A) and IO[11] (Bank B)	00 : OFF 01 : A->B 10 : B->A 11 : Reserved
			5:4	Level shifter mode for IO[2] (Bank A) and IO[10] (Bank B)	
			3:2	Level shifter mode for IO[1] (Bank A) and IO[9] (Bank B)	
			1:0	Level shifter mode for IO[0] (Bank A) and IO[8] (Bank B)	
0x1E	**RegClock**	0x00	7	Unused	
			6:5	Oscillator frequency (fOSC) source 00 : OFF. LED driver, keypad engine and debounce features are disabled. 01 : External clock input (OSCIN) 10 : Internal 2MHz oscillator 11 : Reserved	
			4	OSCIO pin function (Cf. §4.8) 0 : OSCIO is an input (OSCIN) 1 : OSCIO is an output (OSCOUT)	
			3:0	Frequency of the signal output on OSCOUT pin: 0x0 : 0Hz, permanent "0" logical level (GPO) 0xF : 0Hz, permanent "1" logical level (GPO) Else : fOSCOUT = fOSC/(2^(RegClock[3:0]-1))	
0x1F	**RegMisc**	0x00	7	LED Driver mode for Bank B's fading capable IOs (IO15-12) 0: Linear 1: Logarithmic	
			6:4	Frequency of the LED Driver clock ClkX of all IOs: 0 : OFF. LED driver functionality is disabled for all IOs. Else : ClkX = fOSC/(2^(RegMisc[6:4]-1))	
			3	LED Driver mode for Bank A's fading capable IOs (IO7-4) 0: Linear 1: Logarithmic	
			2	NRESET pin function when externally forced low (Cf. §4.4.1 and §4.9.5) 0: Equivalent to POR 1: Reset PWM/Blink/Fade counters (not user programmed values) This bit is can only be reset manually or by POR, not by NRESET.	
			1	Auto-increment register address (Cf. §4.5) 0: ON. When several consecutive data are read/written, register address is incremented. 1: OFF. When several consecutive data are read/written, register address is kept fixed.	
			0	Autoclear NINT on RegData read (Cf. §4.7) 0: ON. RegInterruptSourceA/B is also automatically cleared when RegDataA/B is read. 1: OFF. RegInterruptSourceA/B must be manually cleared, either directly or via RegEventStatusA/B.	
0x20	**RegLEDDriverEnableB**	0x00	7:0	Enables LED Driver for each [output-configured] IO 0 : LED Driver is disabled 1 : LED Driver is enabled	

0x21	**RegLEDDriverEnableA**	0x00	7:0	Enables LED Driver for each [output-configured] IO 0 : LED Driver is disabled 1 : LED Driver is enabled
0x22	**RegDebounceConfig**	0x00	7:3	Unused
			2:0	Debounce time (Cf. §4.6.1) 000: 0.5ms x 2MHz/fOSC 001: 1ms x 2MHz/fOSC 010: 2ms x 2MHz/fOSC 011: 4ms x 2MHz/fOSC 100: 8ms x 2MHz/fOSC 101: 16ms x 2MHz/fOSC 110: 32ms x 2MHz/fOSC 111: 64ms x 2MHz/fOSC
0x23	**RegDebounceEnableB**	0x00	7:0	Enables debouncing for each [input-configured] IO 0 : Debouncing is disabled 1 : Debouncing is enabled
0x24	**RegDebounceEnableA**	0x00	7:0	Enables debouncing for each [input-configured] IO 0 : Debouncing is disabled 1 : Debouncing is enabled
0x25	**RegKeyConfig1**	0x00	7	Reserved
			6:4	Auto Sleep time (no key press within this time will set keypad engine to sleep) 000 : OFF 001 : 128ms x 2MHz/fOSC 010 : 256ms x 2MHz/fOSC 011 : 512ms x 2MHz/fOSC 100 : 1sec x 2MHz/fOSC 101 : 2sec x 2MHz/fOSC 110 : 4sec x 2MHz/fOSC 111 : 8sec x 2MHz/fOSC
			3	Unused
			2:0	Scan time per row (must be set above debounce time). 000 : 1ms x 2MHz/fOSC 001 : 2ms x 2MHz/fOSC 010 : 4ms x 2MHz/fOSC 011 : 8ms x 2MHz/fOSC 100 : 16ms x 2MHz/fOSC 101 : 32ms x 2MHz/fOSC 110 : 64ms x 2MHz/fOSC 111 : 128ms x 2MHz/fOSC
0x26	**RegKeyConfig2**	0x00	7:6	Unused
			5:3	Number of rows (outputs) + key scan enable 000 : Key scan OFF 001 : 2 rows – IO[0:1] 010 : 3 rows – IO[0:2] 011 : 4 rows – IO[0:3] 100 : 5 rows – IO[0:4] 101 : 6 rows – IO[0:5] 110 : 7 rows – IO[0:6] 111 : 8 rows – IO[0:7]
			2:0	Number of columns (inputs) 000 : 1 column – IO[8] 001 : 2 columns – IO[8:9] 010 : 3 columns – IO[8:10] 011 : 4 columns – IO[8:11] 100 : 5 columns – IO[8:12] 101 : 6 columns – IO[8:13] 110 : 7 columns – IO[8:14] 111 : 8 columns – IO[8:15]
0x27	**RegKeyData1**	0xFF	7:0	Column which generated NINT (active low) Ex: RegKeyData1=11011111 => IO13 has generated NINT The register is automatically cleared when RegKeyData2 is read.
0x28	**RegKeyData2**	0xFF	7:0	Row which generated NINT (active low) Ex: RegKeyData2=11111110 => IO0 has generated NINT When the register is read both RegKeyData1 & RegKeyData2 are automatically cleared together with NINT and key scan continues.
0xXX	**RegTOnX**	0x00	7:5	Unused
			4:0	ON Time of IO[X]: 0 : Infinite (Static mode, TOn directly controlled by RegData, Cf §4.9.2) 1 - 15 : TOnX = 64 * RegTOnX * (255/ClkX) 16 - 31 : TOnX = 512 * RegTOnX * (255/ClkX)
0xXX	**RegIOnX**	0xFF	7:0	ON Intensity of IO[X] - Linear mode : IOnX = RegIOnX - Logarithmic mode (fading capable IOs only) : IOnX = f(RegIOnX) , Cf §4.9.5

0xXX	**RegOffX**	0x00	7:3	OFF Time of IO[X]: 0 : Infinite (Single shot mode, TOff directly controlled by RegData, Cf §4.9.3) 1 - 15 : TOffX = 64 * RegOffX[7:3] * (255/ClkX) 16 - 31 : TOffX = 512 * RegOffX[7:3] * (255/ClkX)
			2:0	OFF Intensity of IO[X] - Linear mode : IOffX = 4 x RegOff[2:0] - Logarithmic mode (fading capable IOs only) : IOffX = f(4 x RegOffX[2:0]) , Cf §4.9.5
0xXX	**RegTRiseX**	0x00	7:5	Unused
			4:0	Fade In setting of IO[X] 0 : OFF 1 - 15 : TRiseX = (RegIOnX-(4xRegOffX[2:0])) * RegTRiseX * (255/ClkX) 16 - 31 : TRiseX = 16 * (RegIOnX-(4xRegOffX[2:0])) * RegTRiseX * (255/ClkX)
0xXX	**RegTFallX**	0x00	7:5	Unused
			4:0	Fade Out setting of IO[X] 0 : OFF 1 - 15 : TFallX = (RegIOnX-(4xRegOffX[2:0])) * RegTFallX * (255/ClkX) 16 - 31 : TFallX = 16 * (RegIOnX-(4xRegOffX[2:0])) * RegTFallX * (255/ClkX)
0x69	**RegHighInputB**	0x00	7:0	Enables high input mode for each [input-configured] IO 0 : OFF. VIH max = 3.6V and VCCx min = 1.2V 1 : ON. VIH max = 5.5V and VCCx min = 1.65V
0x6A	**RegHighInputA**	0x00	7:0	Enables high input mode for each [input-configured] IO 0 : OFF. VIH max = 3.6V and VCCx min = 1.2V 1 : ON. VIH max = 5.5V and VCCx min = 1.65V
0x7D	**RegReset**	0x00	7:0	Software reset register Writing consecutively 0x12 and 0x34 will reset the device (same as POR) Always reads 0.

Table 13 – SX1512 Configuration Registers Description