ECE 205: Lab 3

BJT LTspice Simulation

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1 Statement of Purpose

The purpose of this lab was to develop familiarity with transistors, specifically the 2N3904 transistor in LTspice. We accomplished this by modeling a circuit with various input voltages and constructed the characteristic transistor I-V plot and the collector-emitter amplifier voltage transfer graph. To construct this model, we utilized the software LTspice.

2 PreLab Deliverables

For the first prelab deliverable, we drew the the I-V characteristic curve for I_C and V_{CE} using the parameters: $\beta = 100$, $V_{BE,on} = 0.7$ V, and $V_{CE,sat} = 0.2$ V, which is pictured below.

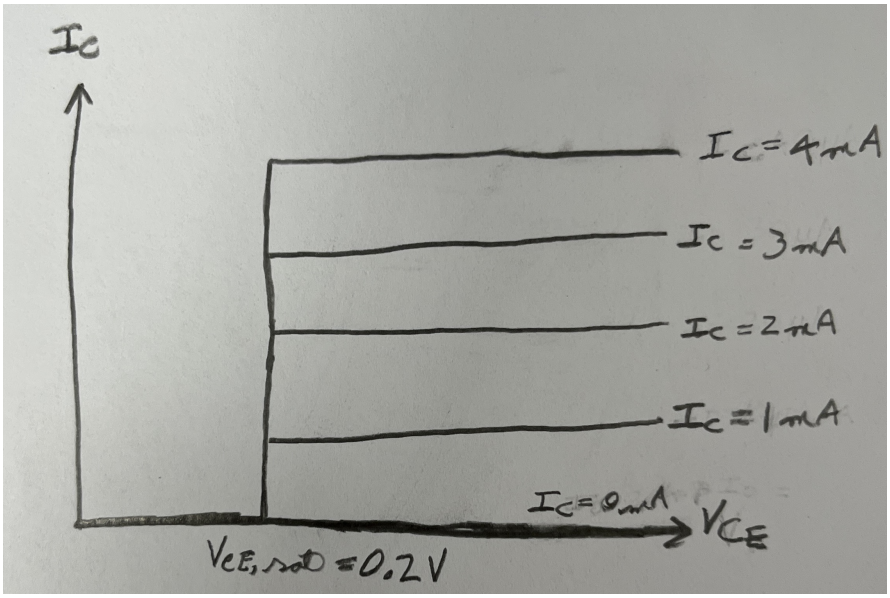

Figure 1: I-V characteristic curve using the Offset Ideal Model (OIM) for I_C and V_{CE}.

In Fig. 1, the I_C values pictured of 0 -, 1 -, 2 -, 3 -, and 4 mA correspond to I_b values of 0 -, 10 -, 20 -, 30 -, 40 μA respectively, which can be obtained via the following equation:

$$I_C = \beta I_b \tag{1}$$

Fig. 1 is different from the the I-V characteristic curve drawn in class as the simplified model in the figure has a constant saturation voltage while the curve drawn in class has a saturation voltage proportional to I_C.

For the second prelab deliverable, we determined the value for V_{out} given values of V_{in} for the schematic given below.

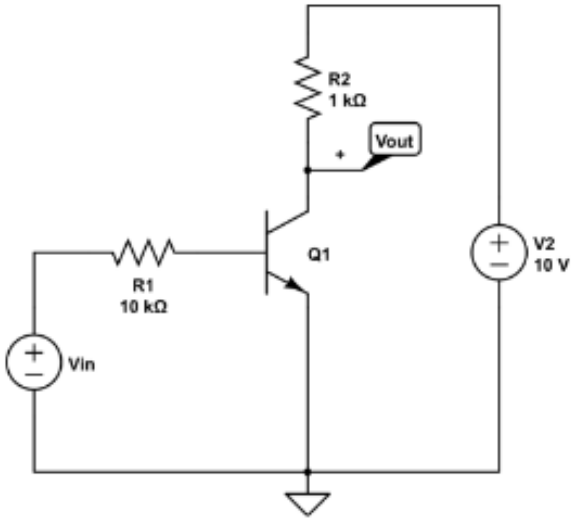

Figure 2: Common Emitter Amplifier

Using the parameters in Fig. 2 and from prelab 1, we generated a voltage transfer graph, which is given as follows:

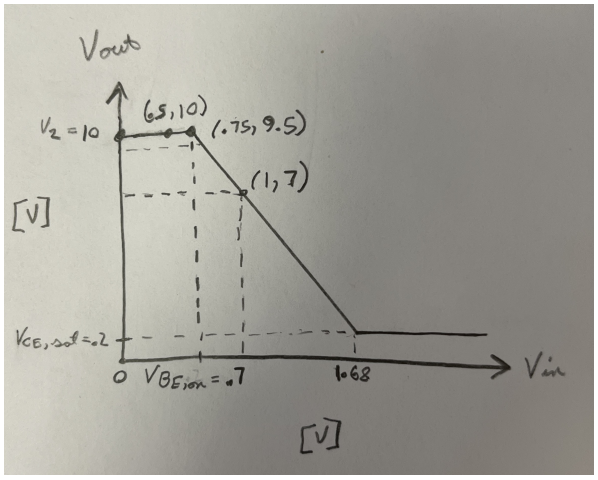

Figure 3: Voltage Transfer Graph of V_{in} vs V_{out}

The values in Fig. 3 were obtained by BJT analysis. We know for all values below $V_{BE,on}$, the BJT is in cutoff mode, so for V_{in} values of 0 -, 0.25 -, and 0.5 V, we can say $V_{out} = V_2 = 10$ V. For any V_{in} value greater than $V_{BE,on}$, we can obtain the V_{out} using the following relation:

$$V_{out} = V_2 - R_2 \cdot \beta \left(\frac{V_{in} - V_{BE,on}}{R_2} \right) \tag{2}$$

From Eq (**??**), we can obtain the value for V_{in} where the $V_{out} = V_{CE,sat}$, which is 1.68 V. Any

V_{out} value between 0.7 V and 1.68 V can be obtained via Eq 2 as this equation applies in forward active mode. Thus, we found the V_{out} values corresponding to V_{in} values of 0.75 - and 1 V to be 9.5 - and 7 V, respectively.

3 Procedure

We constructed two circuits, the first to obtain the transistor characteristic I-V curve, and the second to obtain the collector-emitter amplifier voltage transfer graph.

First, to obtain the first aforementioned jawn, we constructed a two loop circuit. The left loop contained a current source, I_1, with variant strength from 0-16 μA aswell as the base of the 2N3904 transistor. The right loop had three components: a voltage source, V_1, with variant strength from 0-10 V; a resistor, R_1, with resistance of 1 $k\Omega$; and the collector and emitter parts of the 2N3904 transistor. The schematic we constructed in LTspice is presented below in Fig. 4.

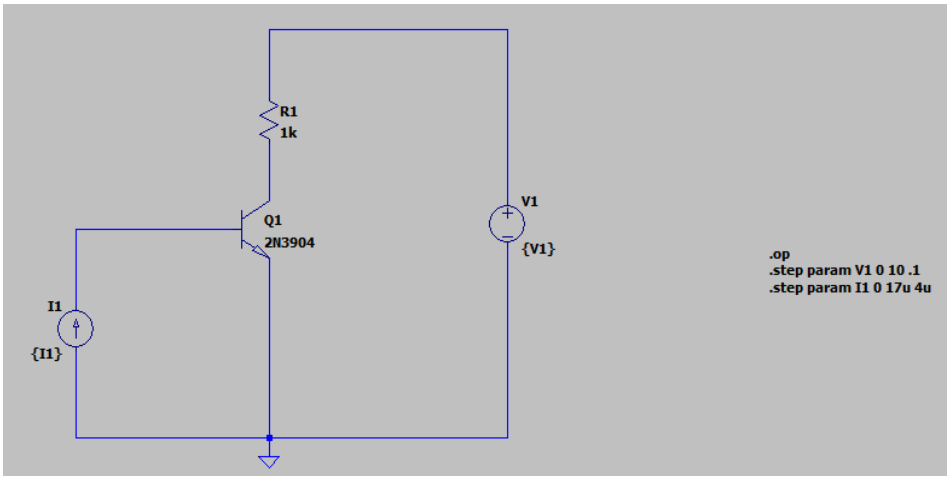

Figure 4: Schematic of circuit used to construct the characteristic I-V curve.

Second, to obtain the collector-emitter amplifier voltage transfer graph, we utilized a similar schematic as before. The only difference being we removed the variant voltage source in the right loop, and replaced the current source with a variant strength voltage source,V_2 and a resistor R_2 with resistance of 10 $k\Omega$. This schematic is presented in Fig. 5.

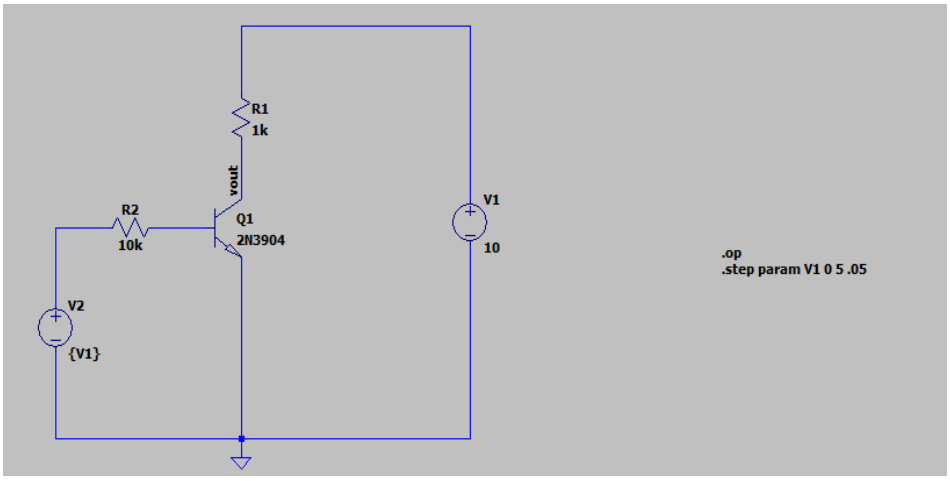

Figure 5: Schematic of circuit used to construct the collector-emitter amplifier voltage transfer plot.

4 Observation and Data

To begin, utilizing the schematic presented in Fig. 4, we constructed the characteristic I-V plot of the 2N3904 transistor. We utilized 17 different current source strengths, but only present 8 as all 17 created a cluttered plot. The resulting characteristic I-V plot is presented below in Fig. 6. So as to not clutter the plot further, a description of the three important regimes will be written as opposed to labeling and circling the regions on the plot. The region in which the current across the resistor R_1 is 0 is where the transistor is off, the region in which the current across the resistor is increasing rapidly is the forward active region, and finally the region in which the current across the resistor plateaus is the saturated region of the transistor.

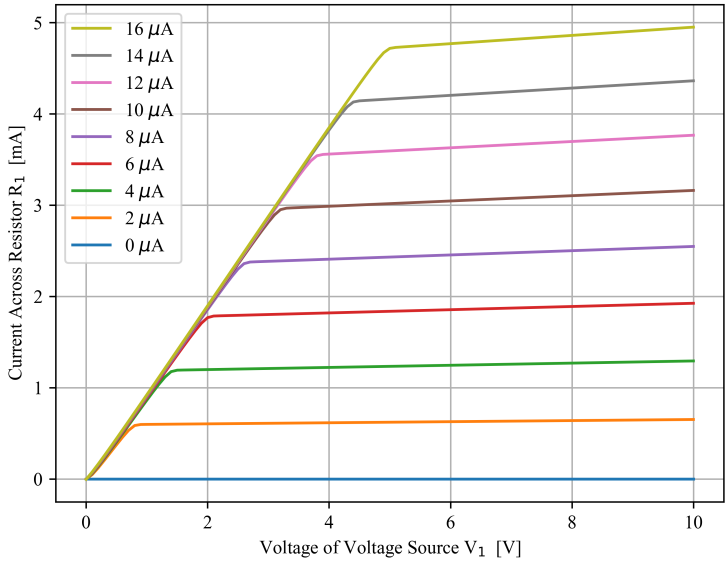

Figure 6: Simulated characteristic I-V plot of the 2N3904 transistor.

To continue, utilizing the schematic presented in Fig. 5, we constructed the collector-emitter amplifier voltage transfer plot. This plot has three distinct regions, separated by the vertical black-dashed lines. The first region, all the way to the left, is where the transistor is off. The second region, in which the voltage of the node labeled V_{out} (in Fig. 5) is decreasing, is when the transistor is forward-active. Finally, the right most region, in which the voltage of the V_{out} node is essentially constant, the transistor is saturated.

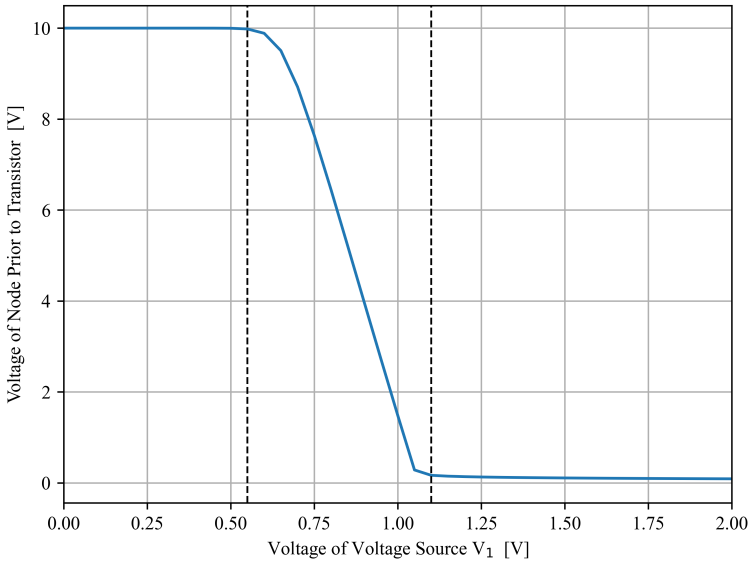

Figure 7: Simulated collector-emitter amplifier voltage transfer plot of the 2N3904 transistor.

5 Analysis

To begin, there is a stark difference between the two I-V plots, Figs. 1 and 6, seen specifically in the forward-active region, or lack thereof. In class we utilized a simplified model that does not take into account the exponential nature of the transistor, and thus lacks an active region, where LTspice is an advanced simulation tool and uses a much more realistic model. Further, while the trend observed in the collector-emitter amplifier voltage transfer plots presented in Figs. 3 and 7, the values of note are different. First, the 'on' voltage, V_{BE}, in the pre-lab is assumed to be 0.7 V, but in LTspice we see this value is closer to 0.55 V. Further, in the prelab we found the maximum input voltage prior to saturation to be 1.68 V, whereas in LTspice we observe this value to be closer to 1.1 V. These discrepancies are likely due to the utilization of rough estimates for generalized parameters regarding transistors and the use of a simplified model in class to describe the behavior of these transistors.

6 Conclusions

In conclusion, we are now more familiar with the use of transistors in LTspice, as well as their behavior in circuits. We constructed I-V and collector-emitter voltage drop plots analytically and through simulation, and found poor agreement. We determined this poor agreement is due to the use of simplified models and generalized parameters in the analytical approximations.

7 Appendix

All output files and LTspice screenshots are in this google folder.