Homework 3

1. Install OpenLane to you computers using the instructions in https://openlane.readthedocs.io/en/latest/
2. Try spm example given in OpenLane directory. Give the results shown in reports and results in run directory.
3. Write a Verilog code for an adder for addition of two 8-bit positive integers, X, Y. Save this file by giving name as "ADDER.v". Synthesize this module in OpenLane and add the resulting **dot schematics** to your report. Examine what type of elements are used to model the written HDL code.
4. Write a test bench file with name "ADDER_tb.v" to test your design. Perform a **behavioral simulation** for your design in **Icarus Verilog (iverilog)**, covering 10 inputs calculated using Eq. (1). Add the console output results and **gtkwave** waveform) to your report to prove that the circuit is working as expected.

For $0 \leq i \leq 10$, $\{X, Y\} = ((\text{Student ID number} + i) \bmod 2^{16})_2$ (1)

5. Complete the OpenLane flow for ADDER.v. Give the results shown in reports and results in run directory.