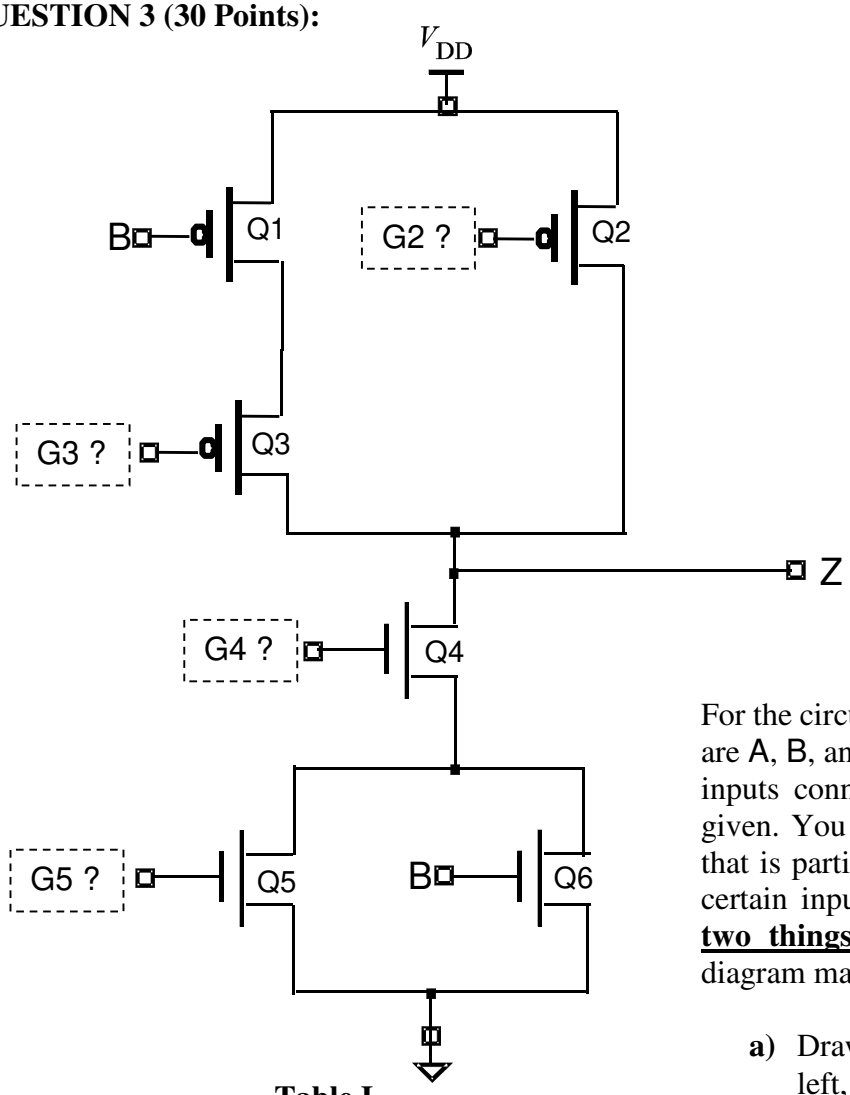
BLG 231E DIGITAL CIRCUITS FINAL EXAM QUESTION 3

Rules:

1. The duration of this question is **40 minutes**. You may upload your file to Ninova until **17:20**.
2. **Answer the question on its own sheet** and upload it during the time allotted for that question, as explained in the file "Exam policies". Create a separate zip file for this question.
3. **You may not ask any questions during the exam.** State any assumptions you have to make.
4. Any cheating or any attempt to cheat will be subject to University disciplinary proceedings.
5. Please **show ALL work**. Answers with no supporting explanations or work will be given no partial credit. If we cannot read or follow your solution, no partial credit will be given. PLEASE BE NEAT!

QUESTION 3 (30 Points):



For the circuit given on the top left, the inputs are A, B, and C, and the output is Z. Only the inputs connected to Q1 and Q6 have been given. You are also given a table on the left that is partially filled in with values of Z for certain input combinations. You need to do **two things in parallel** so that the circuit diagram matches the truth table:

a) Draw a table similar to **Table I** on the left, and fill in which inputs (A, B, or C) are connected to the gates of which transistors (G2, G3, G4, G5) (*15 points*)

b) Fill in **Table II given on the left**. For all combinations of inputs A, B, and C given in the table, show the states of all transistors (ON or OFF) and the value at the output Z (L or H). (*15 points*)

Explain your reasoning fully. Do not just fill in some labels.

Table I

Transistor Gate	Input Value (A, B, or C) Connected To This Gate
G2	
G3	
G4	
G5	

Table II

			Transistors						
A	B	C	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	H	H							H
H	L	L							H
H	L	H							L
H	H	L							
H	H	H							