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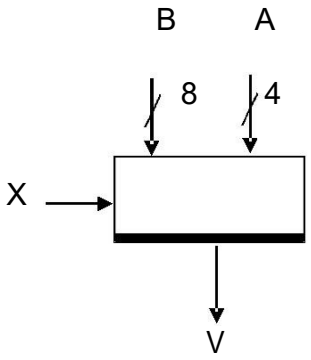
BLG 231E DIGITAL CIRCUITS SUPPLEMENTARY 1 EXAM

Regulations:

1. The exam duration is **2 hours**. The exam itself should take **a maximum of 2 hours** to complete. You may use additional time to scan your papers properly and submit your file.
2. In case of unexpected technical problems, such as power outages, Internet unavailability, software failures, you may upload your files to Ninova until 20:00.
3. Read the file "exam policies" in the "class-files" directory in Ninova carefully, and submit your solutions to Ninova as explained in this file. **You must submit 4 zip files.**
4. Do not send your solutions by e-mail. We will only accept files that have been uploaded to the official e-learning system Ninova before the deadline.
5. There are **4 questions**; you must **answer each question on its own sheet** as explained in the file "exam policies". Create a separate zip file for each question.
6. **You may not ask any questions during the exam.** If you think something is missing in a question, explain it, make the necessary assumption, and solve the question.
7. Any cheating or any attempt to cheat will be subject to the University disciplinary proceedings.
8. Please **show ALL work**. Answers with no supporting explanations or work will be given no partial credit. If we cannot read or follow your solution, no partial credit will be given. PLEASE BE NEAT!

QUESTION 1 (25 Points):

- The combinational circuit shown on the right performs the subtraction operation on two **signed** integers, A and B, as explained in the table given below and determines if this operation causes an overflow or not.
- A is a 4-bit integer ($A=A_3\ A_2\ A_1\ A_0$).
- B is an 8-bit integer ($B=B_7\ B_6\ B_5\ B_4\ B_3\ B_2\ B_1\ B_0$).
- The input X determines direction of the operation, and the value of the output V is
  - '0', if there is no overflow, and
  - '1', if there is overflow after the operation.



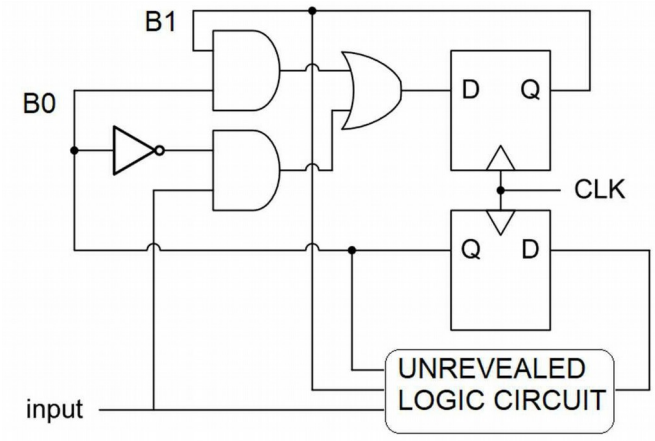
X	Operation
0	A-B
1	B-A

Hint: This circuit contains three parts for the following functions: 1) Extending the shorter integer, 2) Performing the subtraction, 3) Determining if there is overflow or not.

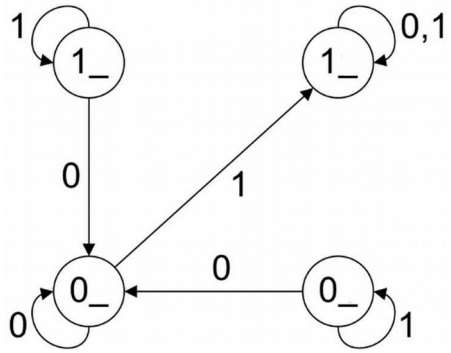
a) Construct the truth table and write the logical expression for the output V. (*10 points*)

b) Implement and draw this circuit using **one** parallel adder and other necessary logic units (i.e., gates and devices that were explained in the lectures). Make your circuit design as simple as possible by using the fewest possible number of logic units. Do not show the internal structure of the parallel adder; show it only as a block. Label all inputs and outputs properly. (*15 points*)

QUESTION 2 (25 Points):
Consider the partially defined sequential logic circuit with a single input that is given below.



a) Find the value for the LSB (least significant bit or rightmost bit) of the state coding, B0, in each state circle of the state transition graph. To do this, use the values given in the incomplete state transition graph and the next state circuit for the MSB (most significant bit) of the state coding, B1. (*15 points*)

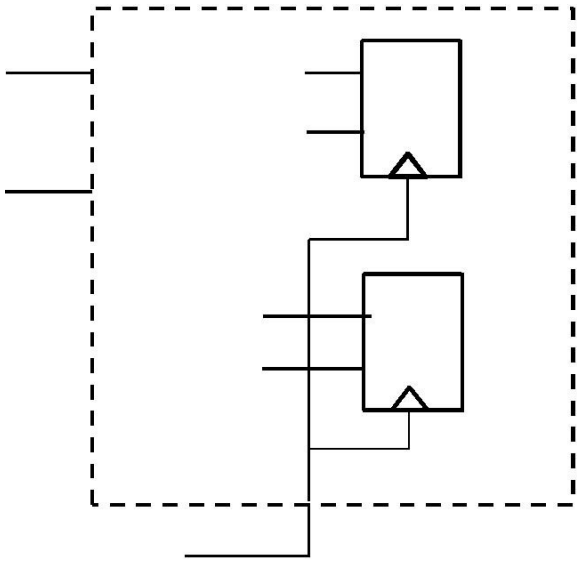


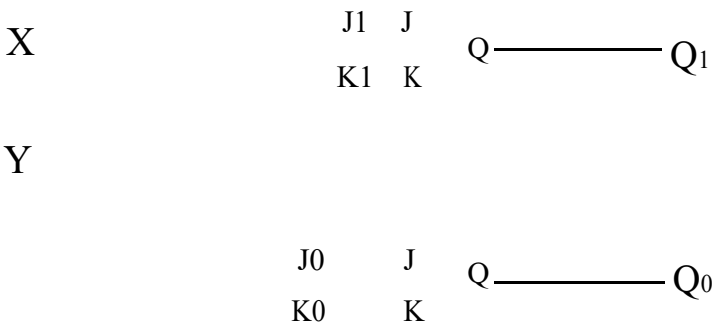
b) Write the expression D = f(Input, B0, B1) for the "unrevealed logic circuit" shown in the figure above. (*10 points*)

QUESTION 3 (25 Points):

Consider the following circuit with 2 inputs (X and Y) and 2 J-K flip flops.

- When X=0, the output (Q_1Q_0) preserves its value regardless of the value of Y.
- When X=1 and Y=1, the output (Q_1Q_0) counts up by one (00-01-10-11-00 …).
- When X=1 and Y=0, the output (Q_1Q_0) counts down by one (00-11-10-01-00 …).




X
J1
J
K1
K
Q
Q1
Y
J0
J
K0
K
Q
Q0

CLK

a) Derive the state transition, output table. (*5 points*)
b) Derive flip-flop excitations (logic expressions). (*10 points*)
c) Draw the circuit implementation using **only 2-input NAND gates** to drive the inputs J0 and K0, and **only multiplexers (MUX)** to drive the inputs J1 and K1. (*10 points*)

QUESTION 4 (25 Points):

a) Design and implement the CMOS circuit for the logic function f(a,b,c) given below using MOS transistors. Label all transistors as T1, T2, etc. (*15 points*)

b) For your circuit, fill in the table given below. For the given values of the inputs a, b, c, show the states of all transistors (ON or OFF) and the value at the output z (L or H). (*10 points*)

Transistors

A	B	C		Z
H	L	L		
L	H	H		