İTÜ Computer Engineering Department
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BLG 231E DIGITAL CIRCUITS FINAL EXAM QUESTION 2

Rules:

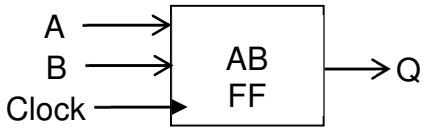
1. The duration of this question is **50 minutes**. You may upload your file to Ninova until **16:40**.
2. **Answer the question on its own sheet** and upload it during the time allotted for that question, as explained in the file "Exam policies". Create a separate zip file for this question.
3. **You may not ask any questions during the exam.** State any assumptions you have to make.
4. Any cheating or any attempt to cheat will be subject to University disciplinary proceedings.
5. Please **show ALL work**. Answers with no supporting explanations or work will be given no partial credit. If we cannot read or follow your solution, no partial credit will be given. PLEASE BE NEAT!

QUESTION 2 (35 Points):

Note: To solve Part (b), you do not need the solution to Part (a).

The table below on the left explains the behavior of the AB flip-flop shown on the right below:

A	B	Behavior (operation)
0	0	Q(t+1) = 0 (Reset)
0	1	Don't change
1	0	Don't change
1	1	Q(t+1) = 1 (Set)



a) [**25 points**] We want to implement this AB flip-flop using only a single T flip-flop and other necessary logic gates.

Hint: A flip-flop is a sequential circuit.

- **i.** Construct the state/output table for the given AB flip-flop. (*10 points*)
- **ii.** Design this AB flip-flop using only a single T flip-flop and other necessary logic gates. Draw your circuit. (*15 points*)

b) [**10 points**] We want to add an Enable (E) input to the AB flip-flop. If the enable input (E) is "1", the flip-flop operates as given in the table above and its value can be changed. On the other hand, if the enable input (E) is "0", the flip-flop preserves its value regardless of its inputs.

Implement and draw the AB flip-flop with the enable input (E) using only **only a single multiplexer** and other logic units, if necessary. Use the **fewest possible** number of logic units to make your circuit design as simple as possible. Do not show the internal structure of the AB flip-flop; **show it only as a block**. Fully label all inputs and outputs.

Do not connect any gates to the clock input of the flip-flop because that is not a proper solution.