



Very Large Scale Integration II - VLSI II

Introduction to Digital World

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Syllabus (Tentative)

- Week 1 (Project 1: OpenLane Instalation and First Try)
 - Introduction to Digital World
 - Digital Design Methodology
- Week 2
 - Verilog Basics
- Week 3 (Project 2: Combinational Circuit RTL Design)
 - Verilog Basics
- Week 4
 - Functional Verification
- Week 5 (Project 3: Sequential Circuit RTL Design and Verification)
 - Synthesis
 - Place and Route
- Week 6
 - Layout
- Week 7 (Project 4: Sequential Circuit RTL to GDS and Verification)I
 - Instruction Set Architecture
 - RISCV Instruction Set Architecture



Syllabus (Tentative)

- Week 8
 - Memory Structures
 - Cache Hierarchies
- Week 9 (Project 5: Memory Design, Synthesis)
 - Hardware Arithmetic
- Week 10
 - RF & Datapath & Single Cycle Control
- Week 11 (Project 6: ALU Design)
 - Basic Pipelining
- Week 12
 - Hazard Handling
- Week 13 & 14 (Project 7: Pipeline Design)
 - Q&A
- Final Project: Implementation of hazard handling, writing an application and test



Text Books

- Morris Mano, Charles Kime, Tom Martin, Logic and Computer Design Fundamentals, Pearson Education Limited, 5th Edition, 2015.
- John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann, 6th Edition, 2017.
- Frank Vahid, Digital Design with RTL Design, Verilog and VHDL, Wiley, 2nd Edition, 2010.
- Frank Vahid, Tony Givargis, Embedded System Design: A Unified Hardware/Software Introduction, John Wiley & Sons, 2002.



Grading

- Average of first 5 homeworks will be grade for midterm
- Average of last 3 will be grade for final
- Term grade = $\text{midterm} \times 0,6 + \text{final} \times 0,4$



Outline

- Why Digital?
- Why NOT Digital?
- Considerations of Digital Technology
- Limitations of Digital Technology



Why Digital?

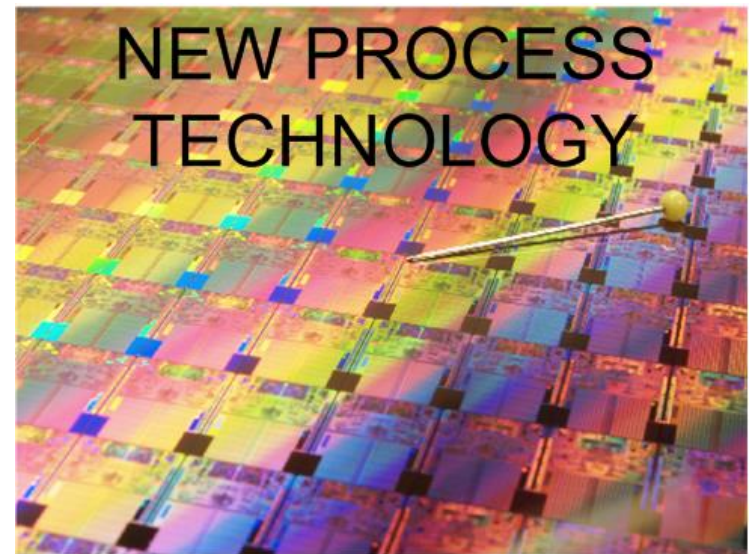
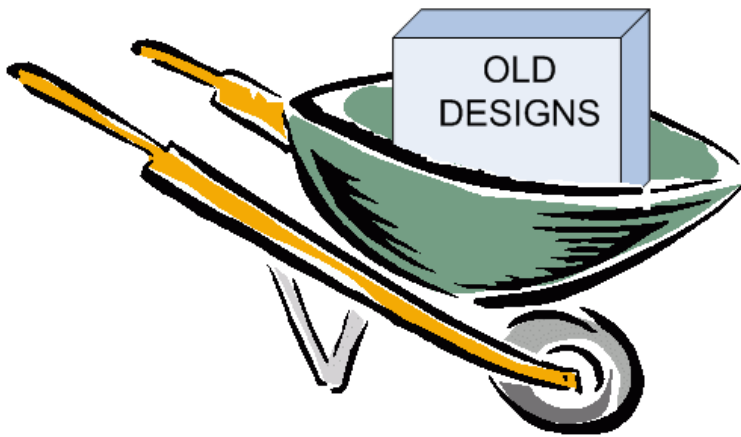
- Ease of Design
 - Low Idea-to-Product Time





Why Digital?

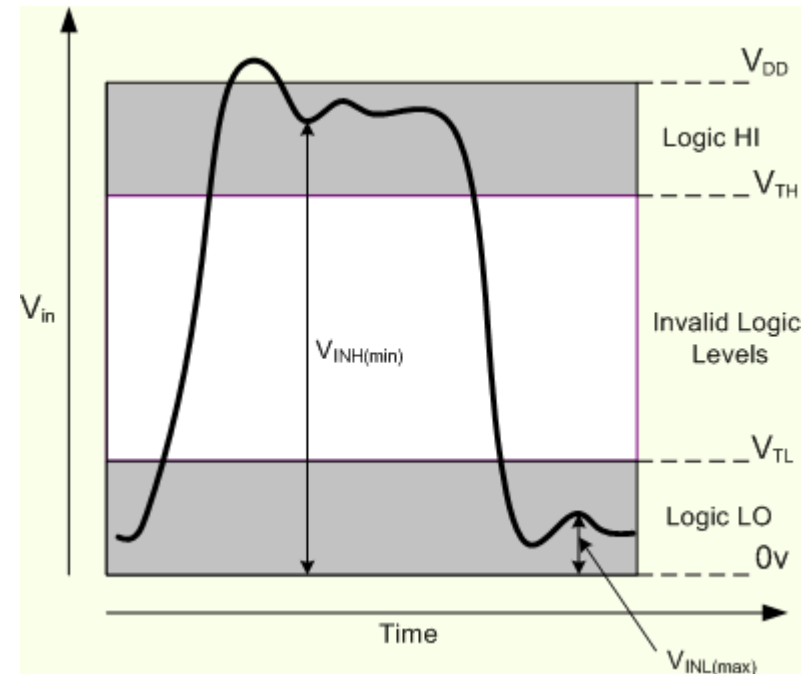
- Ease of Design
 - Portability





Why Digital?

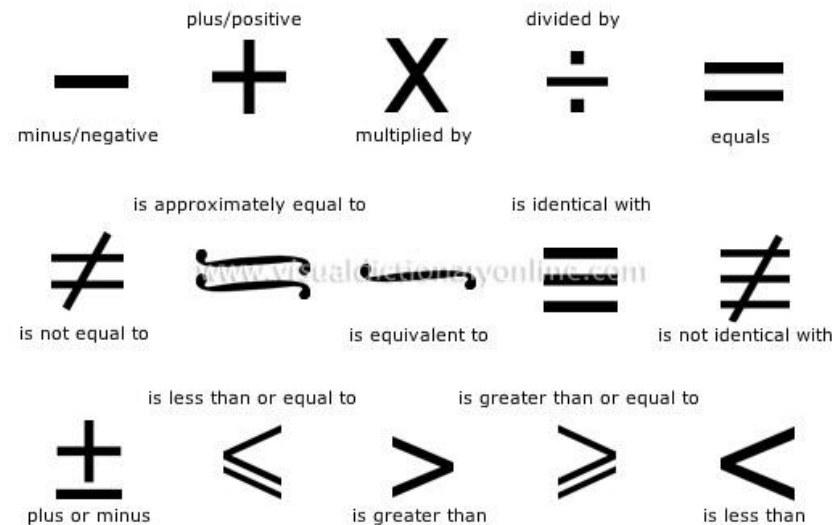
- Ideal World
 - Immunity to Noise





Why Digital?

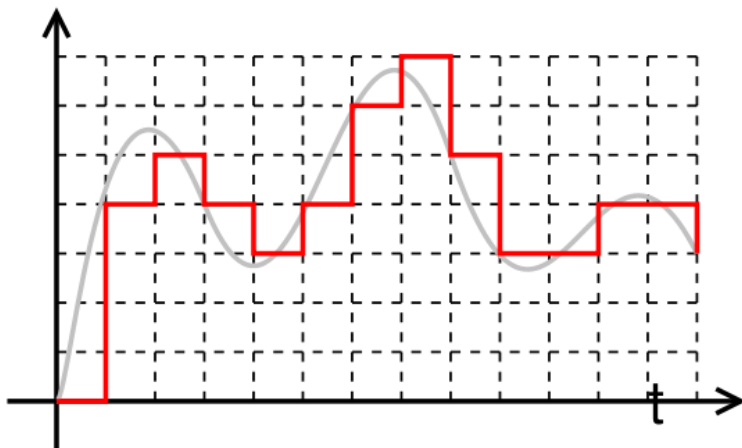
- Ideal World
 - Only mathematical and logical operations
 - Zero error for some operations
 - Customizable precision





Why Digital?

- Ideal World
 - Easy Signal Processing





Why Digital?

- Programmability
 - Can be programmable on the fly
 - Can change the behavior completely

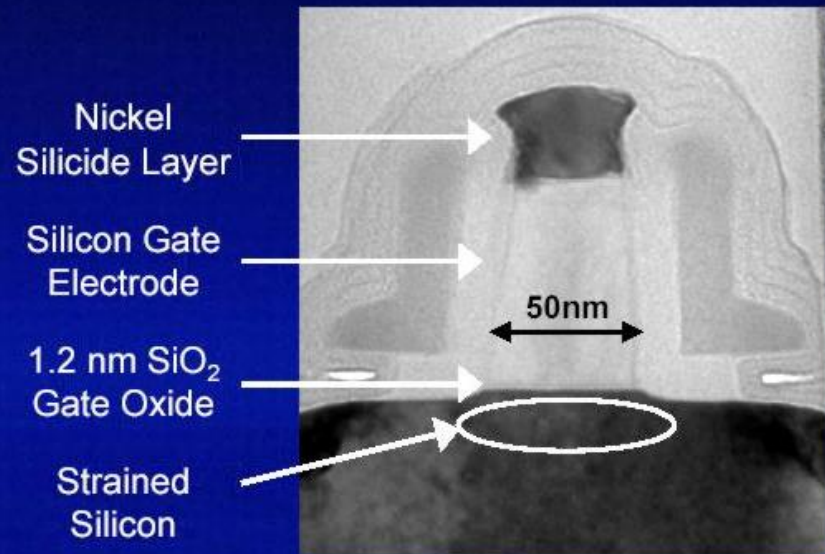




Why Digital?

- Technology (scaling) driven

90 nm Generation Transistor





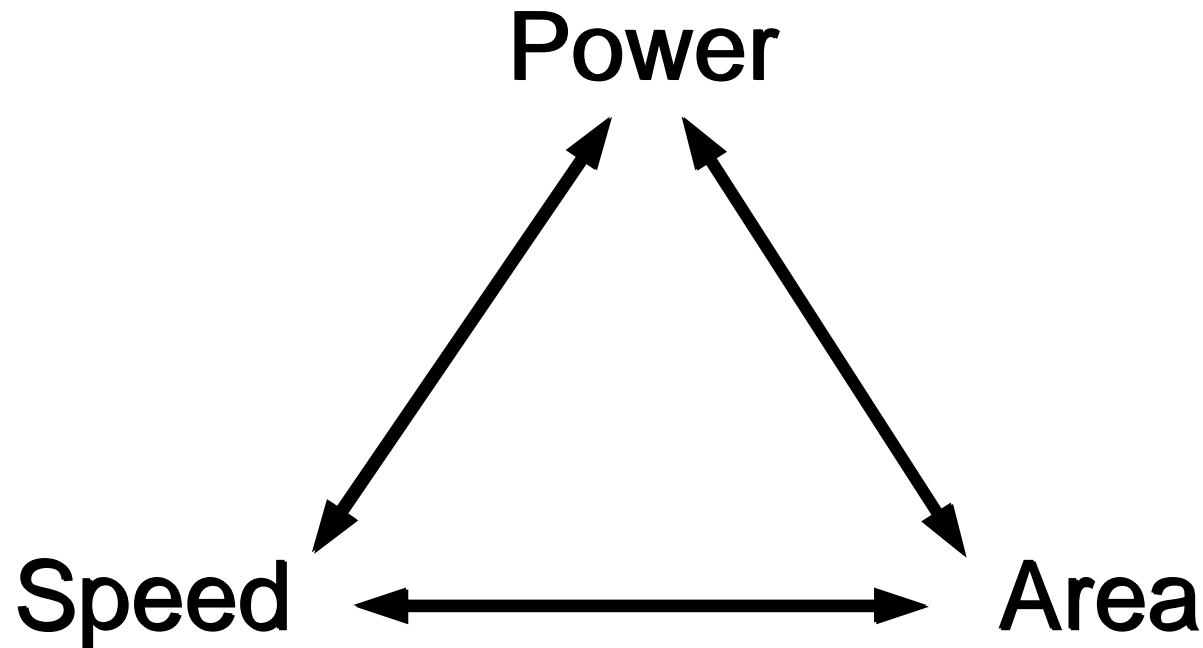
Why NOT Digital?

- Sound
- Electromagnetic Waves
 - Light etc.
- All other sensory data
 - Pressure
 - Temperature
 - Humidity etc.
- Short, The World is **ANALOG**



Considerations of Digital Technology

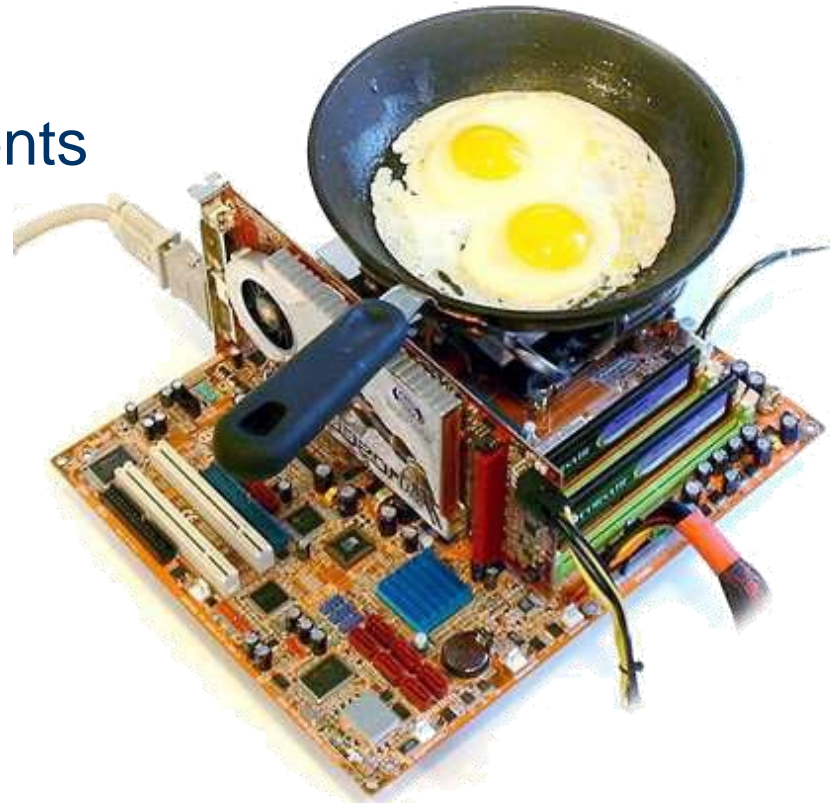
Trade-off Triangle





Limitations of Digital Technology

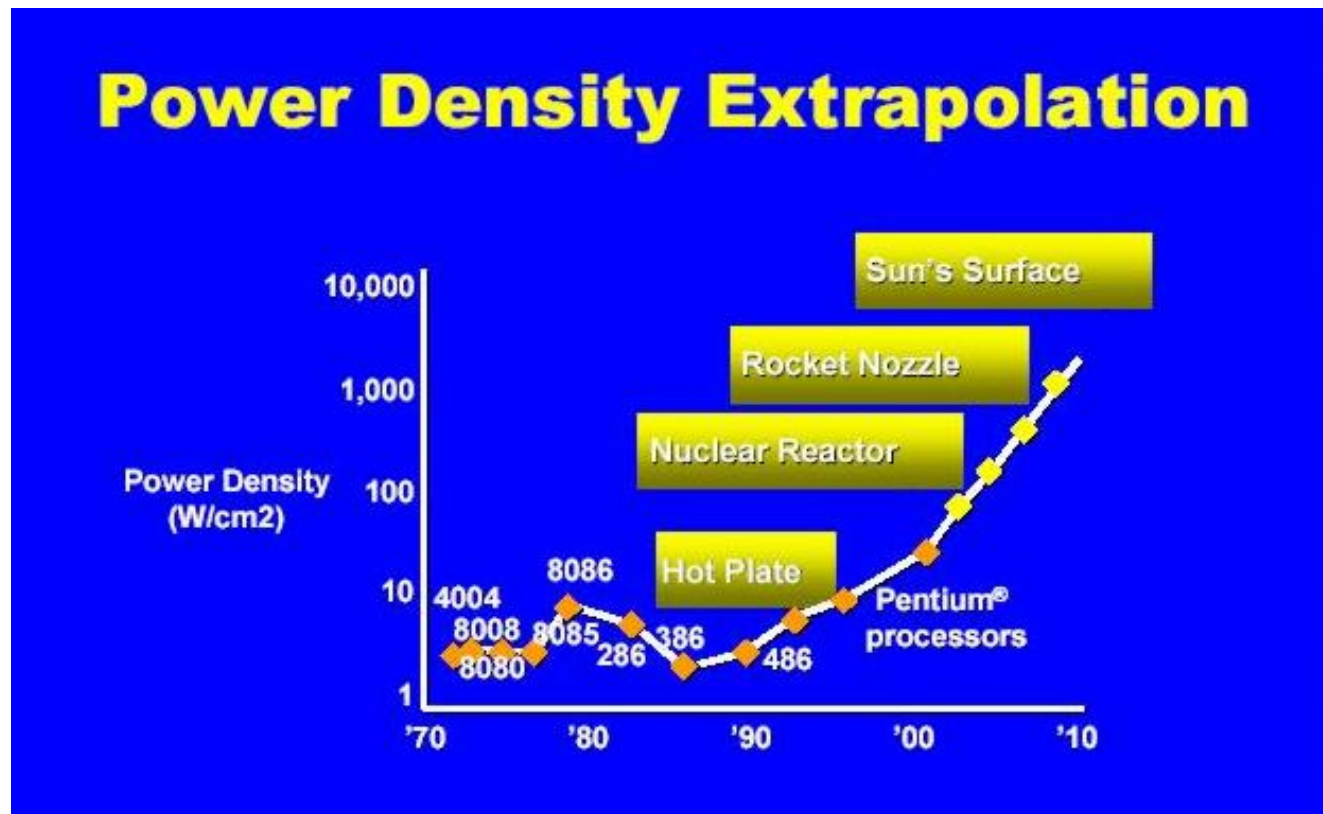
- Total Power = Dynamic Power + Static Power
- Dynamic Power $\rightarrow C.f.V_{DD}^2$
- Static Power \rightarrow Leakage Currents





Limitations of Digital Technology

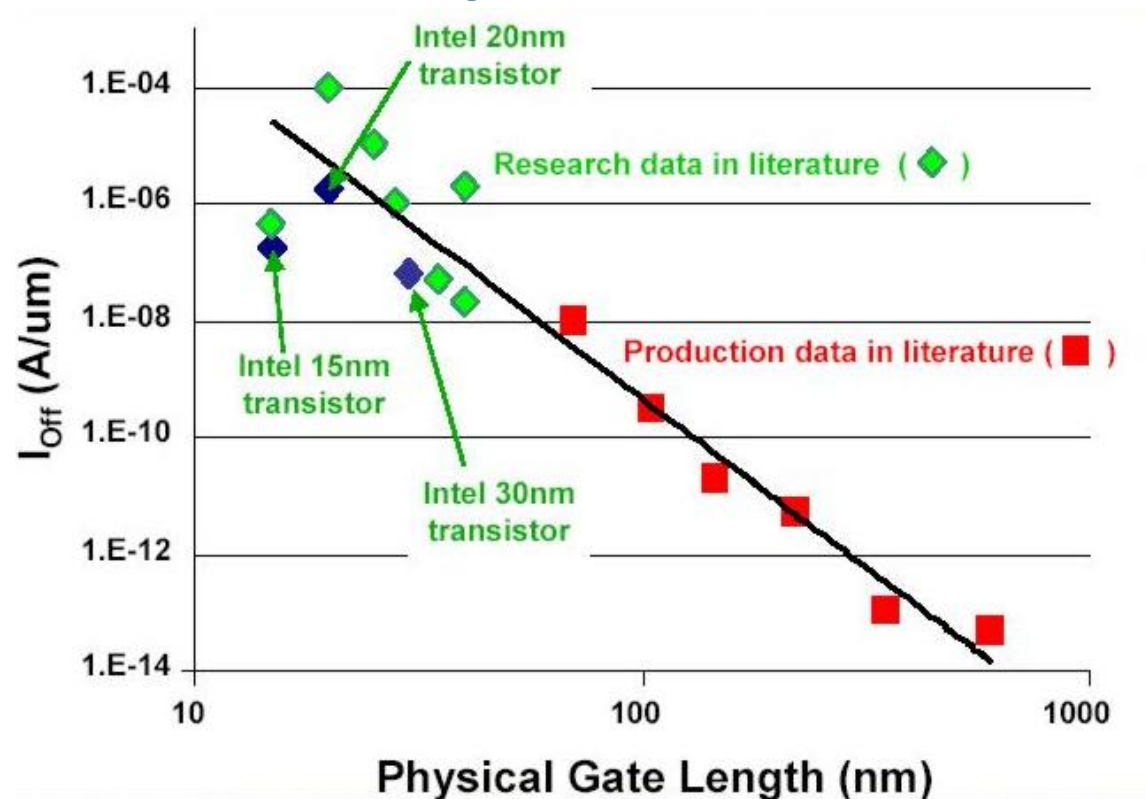
- Power Density = Power Consumption per Unit Area





Limitations of Digital Technology

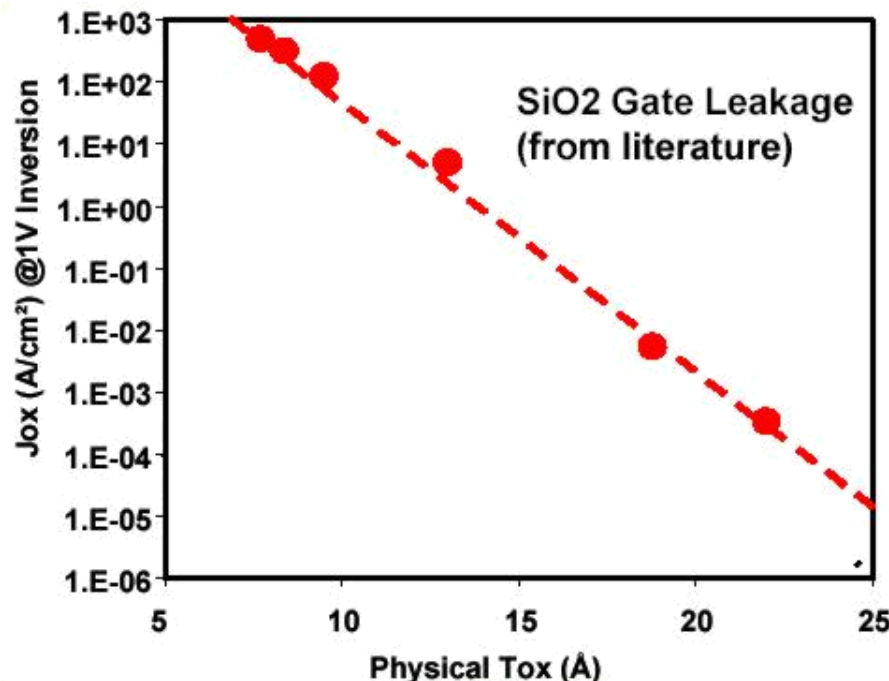
- Subthreshold Leakage Currents





Limitations of Digital Technology

- Gate Leakage
 - Thinner gates → faster transistors but more leakage





References

- <http://download.intel.com/pressroom/kits/45nm/pin.jpg>
- http://www.clipartheaven.com/show/clipart/tools_&_hardware/wheelb arrow-gif.html
- <http://www.topnews.in/health/files/Aircraft-noise.jpg>
- http://www.ami.ac.uk/courses/ami4822_dsi/u02/index.asp
- http://en.wikipedia.org/wiki/Digital_signal_processor
- <http://upload.wikimedia.org/wikipedia/commons/thumb/9/9a/Digital.signal.svg/567px-Digital.signal.svg.png>
- <http://upload.wikimedia.org/wikipedia/en/2/24/Lenna.png>
- <http://ixbtlabs.com/articles2/intel-65nm/>
- <http://www.tomshardware.com/reviews/cheap-thrills,1335.html>