

ADVANCED MEMORY CONTROLLERS

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Memory Controller

- Memory controller connects CPU and DRAM
- Receives requests after cache misses in LLC
 - ▣ Possibly originating from multiple cores
- Complicated piece of hardware, handles:
 - ▣ DRAM refresh management
 - ▣ Command scheduling
 - ▣ Row-buffer management policies
 - ▣ Address mapping schemes

DRAM Control Tasks

- Refresh management
 - ▣ Periodically replenish the DRAM cells (burst vs. distributed)
- Address mapping
 - ▣ Distribute the requests to destination banks (load balancing)
- Request scheduling
 - ▣ Generate a sequence of commands for memory requests
 - Reduce overheads by eliminating unnecessary commands
- Power management
 - ▣ Keep the power consumption under a cap
- Error detection/correction
 - ▣ Detect and recover corrupted data

Address Mapping

- A memory request

Type	Address	Data
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- Address is used to find the location in memory

- ▣ Channel, rank, bank, row, and column IDs

- Example physical address format

Row ID	Channel ID	Rank ID	Bank ID	Column ID
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- A 4GB channel, 2 ranks, 4 banks/rank, 8KB page

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- Example physical address format

Row ID	Channel ID	Rank ID	Bank ID	Column ID
16	0	1	2	13

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Example Problem

- Start with empty row buffers, find the total number of commands if all the request are served in order
 - Address= row(1 2):channel(0):rank(1):bank(3):column(1 6)

addr

00000010

20000001

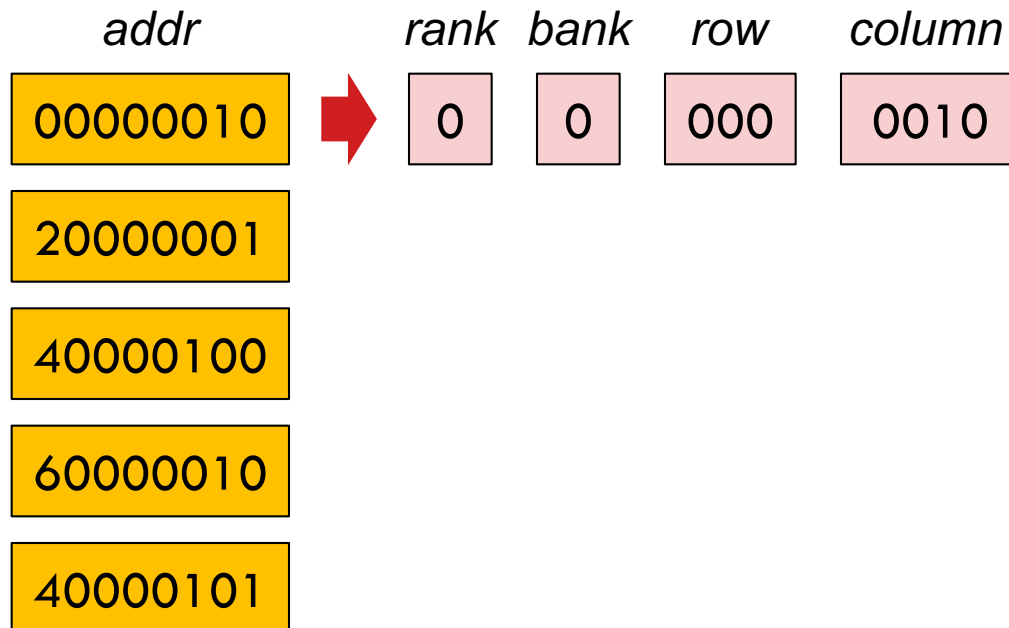
40000100

60000010

40000101

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<i>addr</i>		<i>rank</i>	<i>bank</i>	<i>row</i>	<i>column</i>
00000010	➡	0	0	000	0010
20000001	➡	0	0	200	0001
40000100	➡	0	0	400	0100
60000010	➡	0	0	600	0010
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00000010	➡	0	0	000	0010	➡
20000001	➡	0	0	200	0001	➡
40000100	➡	0	0	400	0100	➡
60000010	➡	0	0	600	0010	➡
40000101	➡	0	0	400	0101	➡

Example Problem

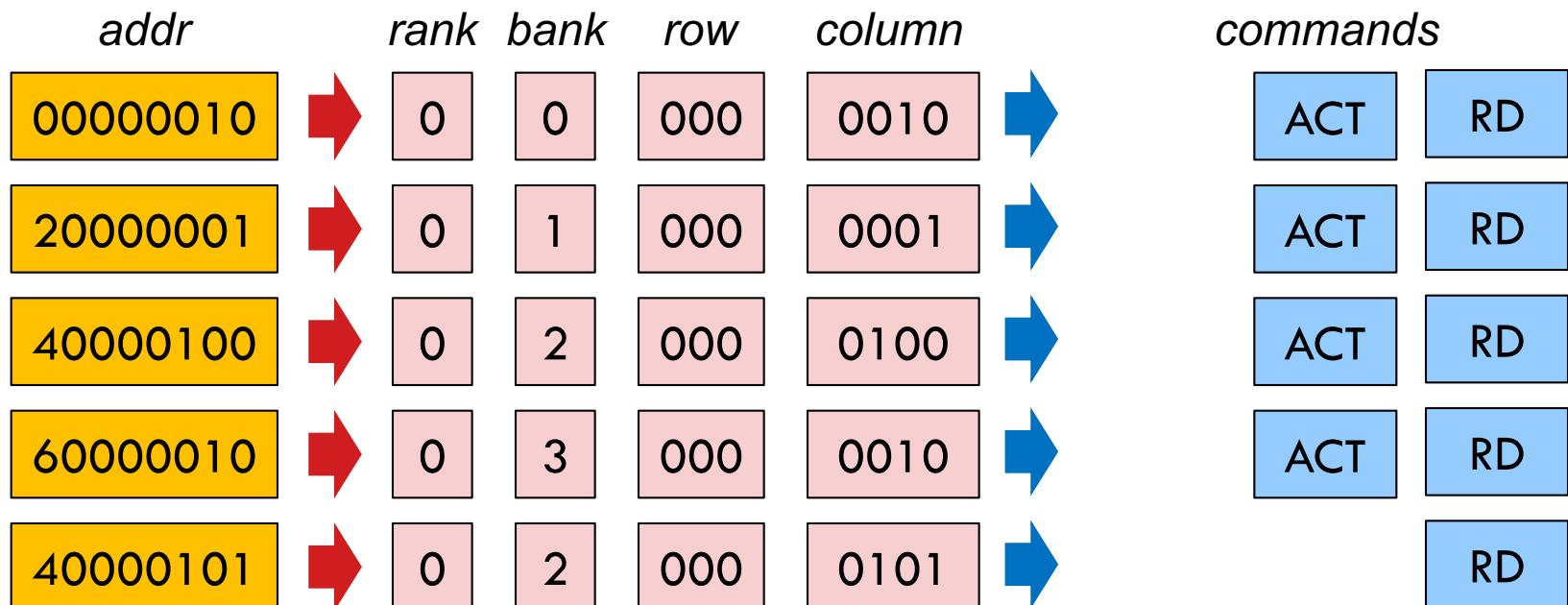
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<i>addr</i>		<i>rank</i>	<i>bank</i>	<i>row</i>	<i>column</i>		<i>commands</i>		
00000010	➡	0	0	000	0010	➡	ACT	RD	
20000001	➡	0	0	200	0001	➡	PRE	ACT	RD
40000100	➡	0	0	400	0100	➡	PRE	ACT	RD
60000010	➡	0	0	600	0010	➡	PRE	ACT	RD
40000101	➡	0	0	400	0101	➡	PRE	ACT	RD

Example Problem

- Find the total number of commands using the following address mapping scheme

■ $\text{Address} = \text{bank}(3):\text{rank}(1):\text{channel}(0):\text{row}(1\ 2):\text{column}(1\ 6)$



Example Problem

- Find the total number of commands using the following address mapping scheme
 - Address = bank(3):rank(1):channel(0):row(12):column(16)

addr

00000010

20000001

40000100

60000010

40000101

Example Problem

- Find the total number of commands using the following address mapping scheme

■ $\text{Address} = \text{bank}(3):\text{rank}(1):\text{channel}(0):\text{row}(12):\text{column}(16)$

<i>addr</i>		<i>rank</i>	<i>bank</i>	<i>row</i>	<i>column</i>
00000010	➔	0	0	000	0010
20000001	➔	0	1	000	0001
40000100	➔	0	2	000	0100
60000010	➔	0	3	000	0010
40000101	➔	0	2	000	0101

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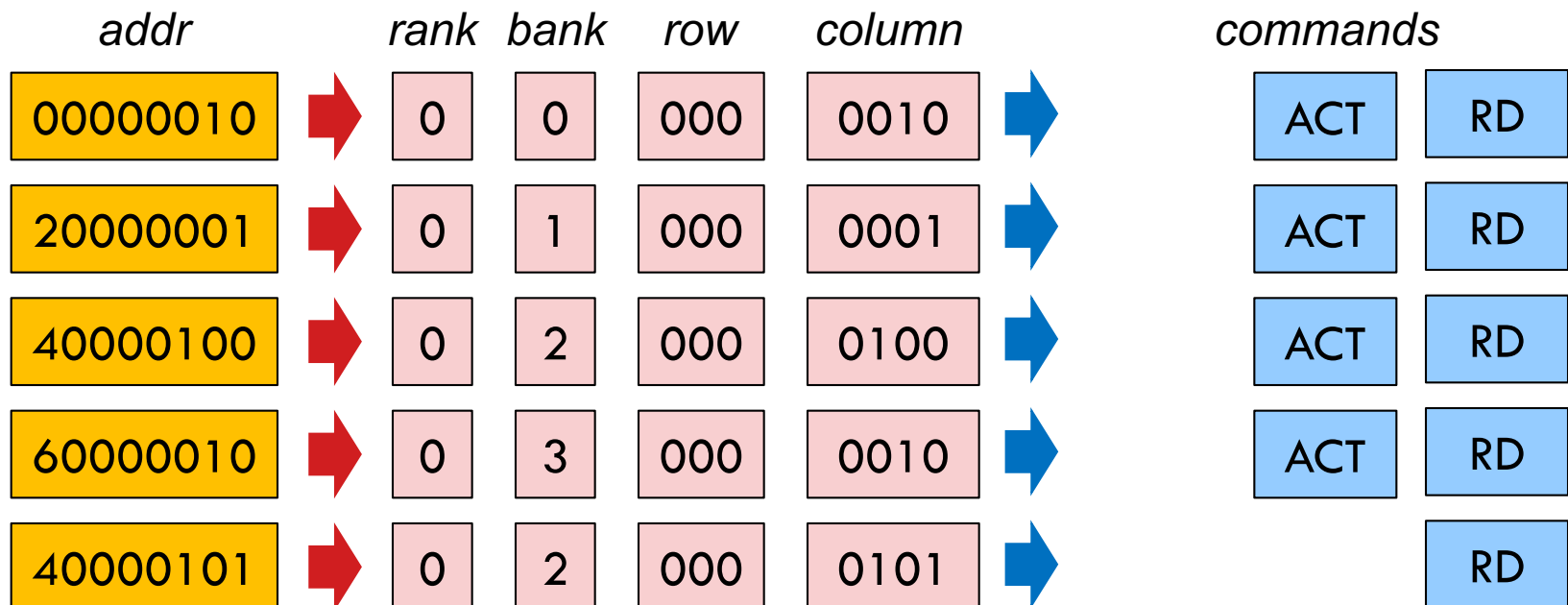
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<i>addr</i>		<i>rank</i>	<i>bank</i>	<i>row</i>	<i>column</i>	<i>commands</i>
00000010	➡	0	0	000	0010	➡
20000001	➡	0	1	000	0001	➡
40000100	➡	0	2	000	0100	➡
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Command Scheduling

- Write buffering
 - ▣ Writes can wait until reads are done
- Controller queues DRAM commands
 - ▣ Usually into per-bank queues
 - ▣ Allows easily reordering ops. meant for same bank
- Common policies
 - ▣ First-Come-First-Served (FCFS)
 - ▣ First-Ready First-Come-First-Served (FR-FCFS)

Command Scheduling

- First-Come-First-Served
 - ▣ Oldest request first
- First-Ready First-Come-First-Served
 - ▣ Prioritize column changes over row changes
 - ▣ Skip over older conflicting requests
 - ▣ Find row hits (on queued requests)
 - Find oldest
 - If no conflicts with in-progress request → good
 - Otherwise (if conflicts), try next oldest

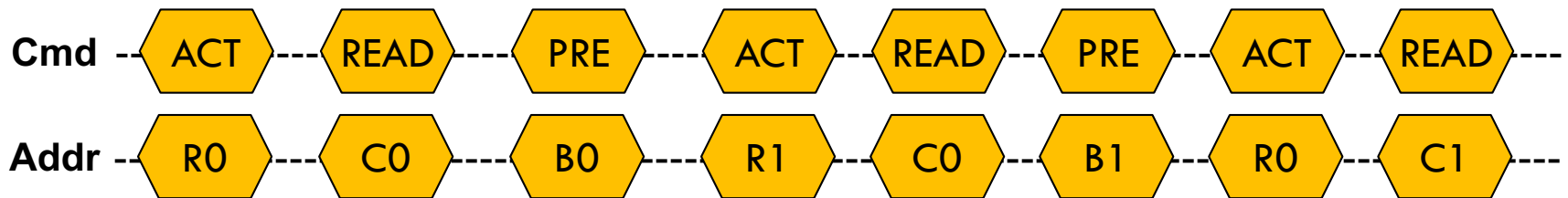
FCFS vs. FR-FCFS

- READ(B0,R0,C0) READ(B0,R1,C0) READ(B0,R0,C1)
 - FCFS

FCFS vs. FR-FCFS

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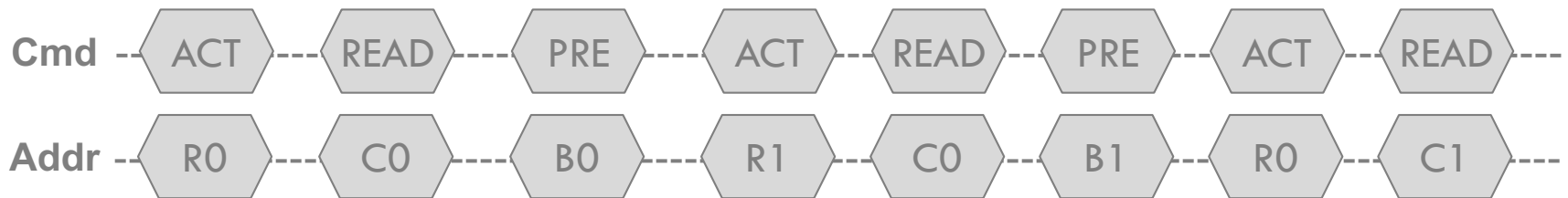
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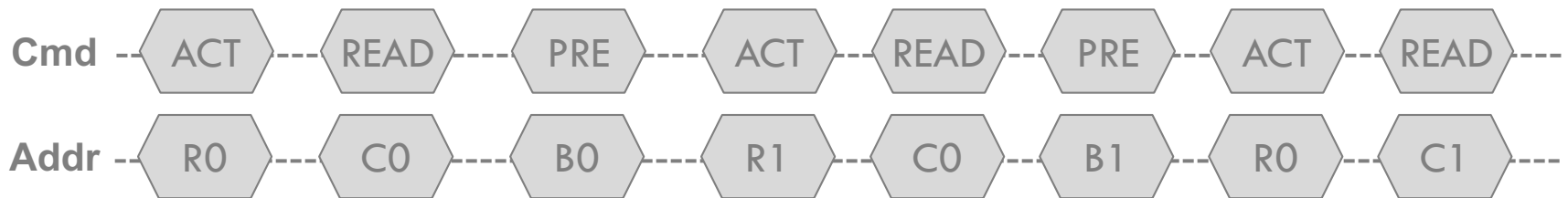


■ FR-FCFS

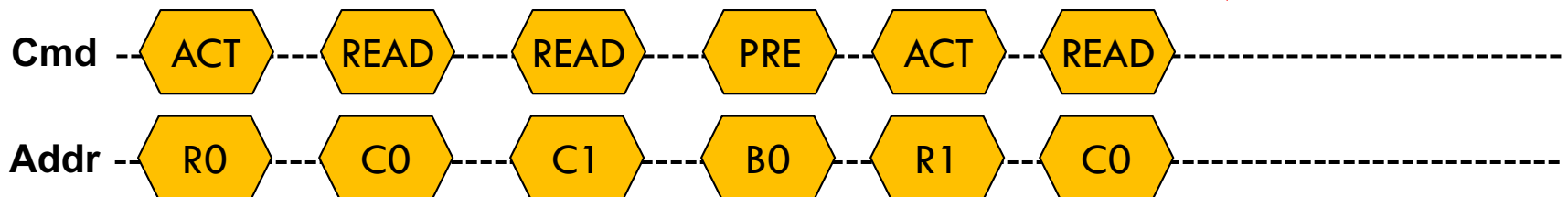
FCFS vs. FR-FCFS

□ READ(B0,R0,C0) READ(B0,R1,C0) READ(B0,R0,C1)

■ FCFS



■ FR-FCFS



Row Buffer Management Policies

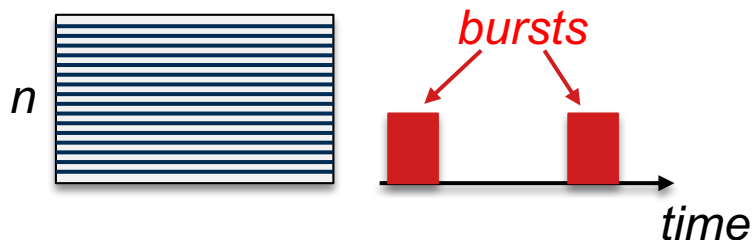
- Open-page policy
 - After access, keep page in DRAM row buffer
 - If access to different page, must close old one first
 - Good if lots of locality
- Close-page policy
 - After access, immediately close page in DRAM row buffer
 - If access to different page, old one already closed
 - Good if no locality (random access)

DRAM Refresh Management

- DRAM requires the cells' contents to be read and written periodically

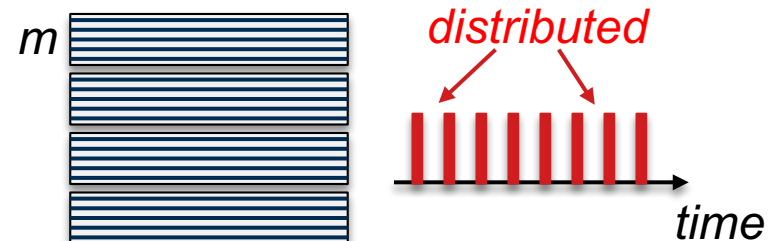
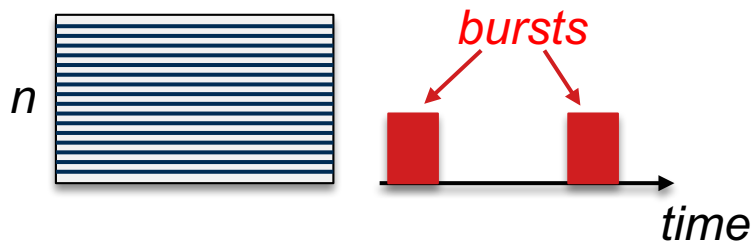
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 - ▣ **Burst refresh:** refresh all of the cells each time
 - Simple control mechanism
 - ▣ **Distributed refresh:** a group of cells are refreshed
 - Avoid blocking memory for a long time
- Recently accessed rows need not to be refreshed
 - ▣ **Smart refresh**

