A Recommended Standard of the Joint Committee on the ATC
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ATC 2070 v01.05

Advanced Transportation Controller (ATC) Standard for the Type 2070 Controller

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Advanced Transportation Controller (ATC)
Type 2070 Controller

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1 FOREWORD

The purpose of this document is to define the standard for a multi-purpose Advanced Transportation Controller (ATC) – Type 2070 Controller.

The effort to develop standards for the ATC began with the Federal Highway Administration gathering together a group of users interested in furthering the development of open architecture hardware and software to meet the future needs of Intelligent Transportation Systems. The ATC users group gained the support of the Institute of Transportation Engineers to continue their work in developing standards for the ATC. The American Association of State Highway and Transportation Officials (AASHTO) and the National Electrical Manufacturer's Association joined with ITE to create a joint effort

In July, 1999, a formal agreement was reached among NEMA, ITE and AASHTO to jointly develop, approve and maintain the ATC standards. Under the guidance of a Joint AASHTO/ITE/NEMA Committee on the ATC, a Working Group was created in order to develop a standard for the Advanced Transportation Controller. The first official meeting of this working group was in September,1999.

In preparation of this Standards Publication, input of users and other interested parties was sought and evaluated. Inquiries, comments and proposed or recommended revisions should be submitted to:

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2 INTRODUCTION

2.1 Overview

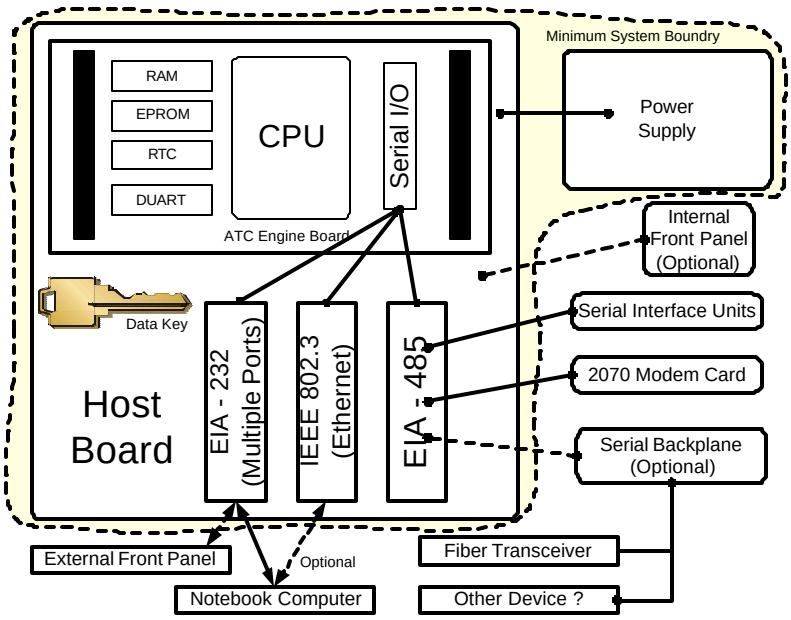
The Advanced Transportation Controller (ATC) is a general purpose field computer that is intended for continuous unattended operation in harsh environments. The Type 2070 ATC defined in this standard is intended to be the first of what may be a family of advanced transportation control devices.

This standard defines specific, interchangeable modules that are combined to form a Type 2070 ATC that is capable of running control software that might be provided from a variety of providers. These specifications, in many cases, define several module options that can be arranged in a variety of composition configurations to meet the needs of the user.

In order to effectively use this standard, the procuring AGENCY should define the composition configuration that is intended to be provided in accordance with this standard. This standard lay out sample compositions for full, NEMA, Lite, and ITS configurations.

2.2 Controllers

The Type 2070 version of the ATC is designed such that all components are fully standardized and are therefore interchangeable. The



The more general ATC standard also allows some latitude for manufacturers to customize the packaging. At this writing, the CPU, or Engine Board as we are calling it, are modular and interchangeable between manufacturers. Other components of the general ATC controller unit standard will not be required to be interchangeable between manufacturers, thus allowing maximum packaging flexibility which will allow the most cost effective design implementations where needed, as well as allowing for very small designs where needed for size restricted applications. The general ATC standard does not preclude other packaging implementations, which may be

fully modular by function. Key features and modules of the controller unit are as follows.

2.3 Controller Housing

The Type 2070 controller defines a controller housing that is intended to fit an EIA 19" rack mounted form commonly found in the Type 332 family of cabinets. A NEMA base module is defined for those NEMA TS1 and TS2 shelf mounted applications.

2.4 Power Supply

A power supply module is used to convert 120-volt power to voltages required to operate the electronics inside the Type 2070 controller unit. This power supply must meet certain minimum electrical characteristics defined herein for its intended use.

This, however, does not preclude a manufacturer or an AGENCY from requiring a specific power supply form factor so that it is consistent across a wide range of packages that may be employed by that AGENCY.

2.5 Front Panel

The Controller Front Panel contains a keyboard and display that comprise the user field interface. The Front Panel on the Type 2070 controller is optional. Communications to the controller processor may be over one of the serial ports.

The front panel might also be used as a portable input device rather than or in addition to a notebook PC. This will offer a low cost alternative and will provide a minimum functionality for those agencies that have trouble purchasing and supporting notebook PCs.

3 GENERAL ATC REQUIREMENTS

3.1 General

In CASE of CONFLICT, the individual chapter shall govern over this chapter.

All furnished equipment shall be new and unused. Vacuum or gaseous tubes and electro-mechanical devices (unless specifically called out) shall not be used.

3.1.1 Interchangeability

Assemblies and their associated devices shall be electrically and mechanically interchangeable at both the assembly and device levels:

ASSEMBLIES	*ASSOCIATED DEVICES*

Type 2070 Controller Unit	- Type 2070-1 CPU Module - Type 2070-2A & 2B Field I/O Module - Type 2070-3 Front Panel Assembly - Type 2070-4 Power Supply - Type 2070-5 VME Cage Assembly - Type 2070-6 Serial Comm Module - Type 2070-7 Serial Comm Module
Type 2070N Controller Unit	- Type 2070 Controller Unit - Type 2070-8 NEMA Module - Type 2070-2B Field I/O Module

3.1.2 Documentation

3.1.2.1 Manuals

Two copies of Manual Documentation shall be supplied for each item purchased up to 200 manuals per order. The manual shall be bound in durable covers made of either 65-pound stock paper or clear plastic. The manual shall be printed on 215.9 mm by 279.4 mm paper, with the exception that schematics, layouts, parts lists and plan details may be on 279.4 mm by 431.8 mm sheets, with each sheet neatly folded to 215.9 mm by 279.4 mm size. Manual text font shall be HELVETICA BOLD or ARIAL. Text characters shall be no more than 10 characters per 25.4 mm and 7 lines per 25.4 mm, with the exception of schematic text, which shall be no more than 18 characters per 25.4 mm and 11 lines per 25.4 mm.

3.1.2.2 Manual Contents

Each manual shall include the following sections in the order listed:

1. Table of Contents
2. Glossary
3. General Description
4. General Characteristics
5. Installation
6. Adjustments
7. Theory of Operation
   a. Systems Description (include block diagram).
   b. Detailed Description of Circuit Operation.
8. Maintenance
   a. Preventive Maintenance.
   b. Trouble Analysis.
   c. Trouble Shooting Sequence Chart.
   d. Wave Forms.
   e. Voltage Measurements.

f. Alignment Procedures.

9. Parts List (include circuit and board designation, part type and class, power rating, component manufacturer, mechanical part manufacturer, data specification sheets for special design components and original manufacturer's part number).
10. Electrical Interconnection Details & Drawings.
11. Schematic and Logic Diagram
12. Assembly Drawings and a pictorial diagram showing physical locations and identification of each component or part.
13. The date, serial numbers, model numbers and revision numbers of equipment covered by the manuals shall be printed on the front cover of the manuals.

3.1.2.3 Manual Pouches

Deleted

3.1.2.4 Draft Manual

Deleted

3.1.3 Packaging

Each item delivered shall be individually packed in its own shipping container. When loose Styrofoam is used for packing the item, the item shall be sealed in a plastic bag to prevent direct contact with the Styrofoam.

3.1.4 Delivery

Each item delivered for testing shall be complete, including manuals, and ready for testing.

3.1.5 Metals

All sharp edges and corners shall be rounded and free of any burrs.

3.1.5.1 Aluminum

Sheet shall be 1.524 mm (0.060-inch) minimum thick Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded shall be Type 6061-T6, or equal.

3.1.5.2 Stainless Steel

Sheet shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.

3.1.5.3 Cold Rolled Steel

Sheet, Rod, Bar and Extruded shall be Type 1018/1020.

3.1.5.3.1 Plating

All cold roll steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class l or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.

3.1.6 Mechanical Hardware

All bolts, nuts, washers, screws (size 8 or larger), hinges and hinge pins shall be stainless steel unless otherwise specified.

3.1.7 Electrical Isolation

Within the circuit of any device, module, or PCB, electrical isolation shall be provided between DC logic ground, equipment ground and the AC grounded conductor. They shall be electrically isolated from each other by 500 megohms, minimum, when tested at the input terminals with 500 VDC.

3.2 Components

3.2.1 General

All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:

3.2.1.1

When a component is of such special design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.

3.2.1.2

The electronic circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.

3.2.2 Electronic Components

3.2.2.1

No device shall be socket mounted unless specifically called out.

3.2.2.2

No component shall be operated above 80% of its maximum rated voltage, current or power ratings. Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.

3.2.2.3

No component shall be provided where the manufactured date is 3 years older than the contract award date. The design life of all components, operating for 24 hours a day and operating in their circuit application, shall be 10 years or longer.

3.2.2.4

Encapsulation of 2 or more discrete components into circuit modules is prohibited except for transient suppression circuits, resistor networks, diode arrays, solid- state switches, optical isolators and transistor arrays. Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance. Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.

3.2.2.5

The Contractor shall submit detailed engineering technical data on all components at the request of the AGENCY. A letter from the component manufacturer shall be submitted with the detailed engineering data when the proposed application of the component alters the technical data. The letter shall certify that the component application meets the requirements of this standard.

3.2.3 Capacitors

The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150%. Capacitor encasements shall be resistant to cracking, peeling and discoloration. All capacitors shall be insulated and shall be marked with their capacitance values and working voltages. Electrolytic capacitors shall not be used for capacitance values of less than 1.0 microfarad and shall be marked with polarity.

3.2.4 Potentiometers

Potentiometers with ratings from 1 to 2 watts shall meet Military Type RV4 requirements. Under 1 Watt potentiometers shall be used only for trimmer type function.

The potentiometer power rating shall be at least 100% greater than the maximum power requirements of the circuit.

3.2.5 Resistors

Fixed carbon film, deposited carbon, or composition insulated resistors shall conform to the performance requirements of Military Specifications MIL-R-11F or MIL-R-22684. All resistors shall be insulated and shall be marked with their resistance values. Resistance values shall be indicated by the EIA color codes, or stamped value. The value of the resistors shall not vary by more than 5% between -37 degrees C and 74 degrees C Special ventilation or heat sinking shall be provided for all 2- watt or greater resistors. They shall be insulated from the PCB.

3.2.6 Semiconductor Devices

3.2.6.1

All solid-state devices, except LED's, shall be of the silicon type.

3.2.6.2

All transistors, integrated circuits, and diodes shall be a standard type listed by EIA and clearly identifiable.

3.2.6.3

All metal oxide semiconductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.

3.2.6.4

Device pin "1" locations shall be properly marked on the PCB adjacent to the pin.

3.2.7 Transformers and Inductors

All power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination.

All transformers and inductors shall have their windings insulated, shall be protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.

3.2.8 Triacs

Each triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC shall be mounted to a heat sink with a machine screw and nut with integral lockwasher.

3.2.9 Circuit Breakers

Circuit breakers shall be listed by UL or ETL. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the ampere rating shall be visible from the front of the breaker. Contacts shall be silver alloy and enclosed in an arc quenching chamber. Overload tripping shall not be influenced by an ambient air temperature range of from -18 degrees C to 50 degrees C. The minimum Interrupting Capacity shall be 5,000 Amperes, RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity. For circuit breakers 80 amperes and above, the minimum interrupting capacity shall be 10,000 amperes, RMS. Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carlingswitch Time Delay Curve #24 or equal).

3.2.10 Fuses

All FUSEs shall be 3AG Slow Blow type and resident in a holder. Fuse size rating shall be labeled on the holder or on the panel adjacent to the holder. Fuses shall be easily accessible and removable without use of tools.

3.2.11 Switches

3.2.11.1 Logic

The switch contacts shall be rated for a minimum of one ampere resistive load at 120 VAC and shall be silver over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

3.2.11.2 Control

The switch contacts shall be rated for a minimum of five ampere resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

3.2.11.3 Power

Ratings shall be the same as CONTROL, except the contact rating shall be a minimum of ten amperes at 125 VAC.

3.2.12 Terminal Blocks

The terminal blocks shall be barrier type, rated at 20 amperes and 600 VAC RMS minimum. The terminal screws shall be 7.938 mm minimum length nickel plated brass binder head type with screw inserts of the same material. Screw size is called out under the associated file, panel or assembly.

3.2.13 Wiring, Cabling, and Harnesses

3.2.13.1

Harnesses shall be neat, firm and properly bundled with external protection. They shall be tie-wrapped and routed to minimize crosstalk and electrical interference. Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements.

3.2.13.2

Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.

3.2.13.3

Wiring shall be routed to prevent conductors from being in contact with metal edges. Wiring shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

3.2.13.4

All conductors shall conform to MIL-W-16878E/1 or better and shall have a minimum of 19 strands of copper. The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.

3.2.13.5

Conductor color identification shall be as follows:

Grounded AC circuits - gray or white
Equip. Ground - solid green or continuous green color with 1 or more yellow stripes.
DC logic ground - continuous white with a red stripe.
Ungrounded AC+ - continuous black or black with colored stripe.
DC logic ungrounded or signal - any color not specified

3.2.14 Indicators and Character Displays

All indicators and character displays shall be readily visible at a radius of up to 1.2 m (4 feet) within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 foot-candles) of white light with the light source at 45 +/-2 degrees to the front panel.

3.2.14.1

3.2.14.2 Indicators

All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted. All indicators shall be self-luminous. All indicators shall have a rated life of 100,000 hours minimum. Each LED indicator shall be white or clear when off and red when on. Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance shall be provided.

3.2.14.3 Character Displays

Liquid Crystal Displays (LCD) shall be readable at temperatures of -20 degrees C to +74 degrees C. All controller unit functions are required to operate at temperatures of –37 degrees C to +74 degrees C.

3.2.15 Connectors

3.2.15.1 General

Connectors shall be keyed to prevent improper insertion of the wrong connector where equipment damage or operator injury may result. The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).

3.2.15.2 Type T

Type T connector shall be a single row, 10 position, feed through terminal block. The terminal block shall be a barrier type with 6-32, 6.35 mm or longer, nickel plated brass binder head screws. Each terminal shall be permanently identified as to its function.

3.2.15.3 Type M

Pin and socket contacts for connectors shall be beryllium copper construction subplated with 0.00127 mm nickel and plated with 0.00076 mm gold. Pin diameter shall be 1.57 mm. All pin and socket connectors shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.

3.2.15.4 Card Edge and Two-Piece PCB

Edge connectors shall have bifurcated gold-plated contacts. The PCB receptacle connector shall meet or exceed the following:

Operating Voltage:	600 VAC (RMS)
Current Rating:	5.0 amperes
Insulation Material:	Diallyl Phthalate or Thermoplastic

Insulation Resistance:	5,000 megohms
Contact Material:	Copper alloy plated with 0.00127 mm (0.00005 inch) of nickel and 0.000381 mm (0.000015 inch) of gold
Contact Resistance:	0.006 ohm maximum

The two-piece PCB connector shall meet or exceed the DIN 41612. The PCB 22/44 Connector shall have 22 independent contacts per side, dual sided with 3.96 mm (0.156 inch) contact centers.

3.2.15.5 Wire Terminal

Each wire terminal shall be solderless with PVC insulation and a heavy duty short - locking spade type connector. All terminal connectors shall be crimped using a Controlled-Cycle type crimping tool.

3.2.15.6 Flat Cable

Each flat cable connector shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts plated with 508 nm of gold over 1270 nm of nickel; and shall have a current rating of 1 A minimum and an insulation resistance of 5 megohms minimum.

3.2.15.7 PCB Header Post

Each PCB header post shall be 1.0 mm square by 8.7 mm high; shall be mounted on 4.0 mm centers; and shall be tempered hard brass plated with 381 nm of gold over 1.270 mm of nickel.

3.2.15.8 PCB Header Socket

Each PCB header socket block shall be nylon or diallyl phthalate. Each PCB header socket contact shall be removable, but crimp-connected to its conductor. The Contractor shall list the part number of the extraction tool recommended by its manufacturer. Each PCB header socket contact shall be brass or phosphor bronze plated with 562 nm of gold over 1270 nm of nickel.

3.2.16 Surge Protection Device

Deleted

3.3 Mechanical Requirements

3.3.1 Assemblies

All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs. Assemblies shall be provided with 2 guides for each

plug-in PCB or associated device (except relays). The guides shall extend to within 19.05 mm from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis. All screw type fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.

3.3.2 PCB Design and Connectors

No components, traces, brackets or obstructions shall be within 3.175 mm of the board edge (guide edges). The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBS. Devices to prevent PC Board from backing out of their assembly connectors shall be provided. All PCB connectors mounted on a motherboard shall be mechanically secured to the chassis or frame of the unit or assembly.

3.3.3 Model and Serial Numbers

3.3.3.1

The manufacturer's model number, and circuit issue or revision number shall appear on the rear panel of all equipment supplied (where such panel exists). In addition to any assignment of model numbers by the manufacturer, the TYPE number shall be displayed on the front panel in bold type, at least 6.35 mm high.

3.3.3.2

A permanent label shall be affixed to the inside near and center floor of the Type 2070 unit chassis when viewed from the front. The label shall display the unit's serial number. The number shall be permanent and easy to read.

3.3.4 Workmanship

Workmanship shall conform to the requirements of this specification and be in accordance with the highest industry standards.

3.3.5 Tolerances

The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

Sheet Metal	+/- 1.334 mm (0.0525 inch)
PCB	+0, - 0.254 mm (0.010 inch)
Edge Guides	+/- 0.381 mm (0.015 inch)

3.4 Engineering

The equipment shall be engineered for simplicity, ease of operation and maintenance.

3.4.1 Human Engineering

PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors. PCBs shall require a force no less than 22.24 N or greater than 222.4 N for insertion or removal.

3.4.2 Design Engineering

The design shall be inherently temperature compensated to prevent abnormal operation. The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range. Personnel shall be protected from all dangerous voltages.

3.4.3 Generated Noise

No item, component or subassembly shall emit an audible noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted. No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits.

3.5 Printed Circuit Boards

3.5.1 Design, Fabrication, and Mounting

3.5.1.1

All contacts on PCBs shall be plated with a minimum thickness of 0.000763 mm gold over a minimum thickness of 0.001905 mm nickel.

3.5.1.2

PCB design shall be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.

3.5.1.3

Fabrication of PCBs shall be in compliance with Military Specification MIL-P-13949, except as follows:

3.5.1.3.1

NEMA FR-4 glass cloth base epoxy resin copper clad laminates 1.590 mm minimum thickness shall be used. Inter-component wiring shall be by laminated copper clad track

having a minimum weight of 0.556 kilogram per square meter with adequate cross section for current to be carried. All copper tracks shall be plated or soldered to provide complete coverage of all exposed copper tracks. Jumper wires to external PCB components shall be from plated-through padded holes and as short as possible.

3.5.1.3.2

In Section 3.3 of Military Specification MIL-P-13949G Grade of Pits and Dents shall be of Grade B quality (3.5.1.3) or better. Class of permissible bow or twist shall be Class C (Table V) or better. Class of permissible warp or twist shall be Class A (Table II) or better.

3.5.1.3.3

Sections 4.2 through 6.6 of Military Specification MIL-P-13949G (inclusive) shall be omitted except as referenced in previous sections of this specification.

3.5.1.4

The mounting of parts and assemblies on the PCB shall conform to Military Specification MIL-STD-275E, except as follows:

3.5.1.4.1

Semiconductor devices that dissipate more than 250 mW or cause a temperature rise of 10 degrees C or more shall be mounted with spacers, transipads or heat sinks to prevent contact with the PCB.

3.5.1.4.2

When completed, all residual flux shall be removed from the PCB.

3.5.1.4.3

The resistance between any 2 isolated, independent conductor paths shall be at least 100 megohms when a 500 VDC potential is applied.

3.5.1.4.4

All PCBs shall be coated with a moisture resistant coating.

3.5.1.4.5

Where less than 6.35 mm lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.79375 +/-0.39624 mm Thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.

3.5.1.5

Each PCB connector edge shall be chamfered at 30 degrees from board side planes. The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots shall be 1.143 +/- 0.127 mm for 2.54 mm spacing and 1.40 +/- 0.127 mm for 3.96 mm spacing.

3.5.2 Soldering

Hand soldering shall comply with Military Specification MIL-STD-2000.
Automatic flow soldering shall be a constant speed conveyor system with the conveyor speed set at optimum to minimize solder peaks or points. Temperature shall be controlled to within +/- 8 degrees C of the optimum temperature. The soldering process shall result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process. Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided. If exposure to the temperature bath is of such a time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.

3.5.3 Definitions

Definitions for the purpose of this section on PCBs shall be taken from MIL-P-55110D Section 3.3 and any current addendum.

3.6 Quality Control

3.6.1 Components

All components shall be lot sampled to assure a consistent high conformance standard to the design specification of the equipment.

3.6.2 Subassembly, Unit, or Module

Complete electrical, environmental and timing compliance testing shall be performed on each module, unit, printed circuit or subassembly. Components will be tested as a complete controller assembly. Housing, chassis, and connection terminals shall be inspected for mechanical sturdiness, and harnessing to sockets shall be electrically tested for proper wiring sequence. The equipment shall be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

3.6.3 Pre-delivery Repair

3.6.3.1

Any defects or deficiencies found by the inspection system involving mechanical structure or wiring shall be returned through the manufacturing process or special repair process for correction.

3.6.3.2

PCB flow soldering is allowed a second time if copper runs and joints are not satisfactorily coated on the first run. Under no circumstances shall a PCB be flow soldered more than twice.

3.6.3.3

Hand soldering is allowed for printed circuit repair.

3.7 Electrical, Environmental, and Testing Requirements

3.7.1 General

The requirements called out in this standard dealing with equipment evaluation are a minimum guide and shall not limit the testing and inspection to insure compliance.

3.7.2 Certification

These test procedures shall be followed by the Contractor who shall certify that they have conducted inspection and testing in accordance with this standard, for all items supplied.

3.7.3 Inspection

A visual and physical inspection shall include mechanical, dimensional and assembly conformance to all parts of this standard.

3.7.4 Environmental and Electrical

All components shall properly operate within the following limits unless otherwise noted:

Applied Line Voltage: 90 to 135 VAC, note “Power Failure / Restoration” limits
Frequency: 60 (+/-3.0) Hertz
Humidity: 5 to 95 percent
Ambient Temperature: -37 degrees C to +74 degrees C
Shock - Test per Specification MIL-STD-810E Method 516.4.
Vibration - per Specification MIL-STD-810E Method 514.4, equipment class G.

3.7.4.1

All circuits, unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 to 90 VAC at a rate of 2 (+/-0.5) volts / second.

3.7.4.2

All equipment shall be unaffected by transient voltages normally experienced on commercial power lines, as further defined herein. Where applicable, equipment purchased separately from the cabinet (which it normally is resident) will be tested for compliance in an AGENCY accepted cabinet connected to the commercial power lines.

3.7.4.3

Deleted

3.7.4.4

The equipment shall withstand (nondestructive) and operate normally when one discharge pulse of plus or minus 300 volts is synchronously added to its incoming AC power line and moved uniformly over the full wave across 360 degrees or stay at any point of Line Cycle once every second. Peak noise power shall be 5 kilowatts with a pulse rise time of 500 ns. The unit under test will be operated at 20 degrees (+/-5 degrees) C and at 120 (+/-12) VAC.

3.7.4.5

The controller unit communications modules shall be tested resident in an AGENCY-accepted controller unit which, in turn, is housed in the cabinet.

3.7.4.6

Equipment shall comply only with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment."

3.7.4.7

All equipment shall continue normal operation when subjected to the following:

3.7.4.7.1 Low Temperature Test

With the item functioning at a line voltage of 90 VAC in its intended operation, the ambient temperature shall be lowered from 20 degrees C to -37 degrees C at a rate of not more than 18 degrees C per hour. The item shall be cycled at -37 degrees C for a minimum of 5 hours and then returned to 20 degrees C at the same rate. The test shall be repeated with the line voltage at 135 VAC.

3.7.4.7.2 High Temperature Test

With the item functioning at a line voltage of 90 VAC in its intended operation, the ambient temperature shall be raised from 20 degrees C to 74 degrees C at a rate of not more than 18 degrees C per hour. The item shall be cycled at 74 degrees C for 5 hours and then returned to 20 degrees C at the same rate. The test shall be repeated with the line voltage at 135 VAC.

3.7.4.7.3

All equipment shall resume normal operation following a period of at least 5 hours at -37 degrees C and less than 10 percent humidity and at least 5 hours at 74 degrees C and 22 percent humidity, when 90VAC is applied to the incoming AC.

3.7.4.8

The relative humidity and ambient temperature values in the following table shall not be exceeded.

AMBIENT TEMPERATURE VERSUS RELATIVE HUMIDITY
AT BAROMETRIC PRESSURES (29.92 In. Hg.)

Ambient Temperature/ Dry Bulb (in degrees C)	***Relative Humidity (in percent)***	***Ambient Temperature/ Wet Bulb (in degrees C)***
-37.0 to 1.1	10	-17.2 to 42.7
1.1 to 46.0	95	42.7
48.8	70	42.7
54.4	50	42.7
60.0	38	42.7
65.4	28	42.7
71.2	21	42.7
74.0	18	42.7

3.7.4.9

All equipment shall be capable of normal operation following opening and closing of contacts (at a 50% duty cycle) in series with the required applied voltage at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.

3.7.5 Contractor's Testing Certification

3.7.5.1

A complete QC / final test report shall be supplied with each item. The test report shall indicate the name of the tester and shall be signed by a responsible manager.

3.7.5.2

The quality control procedure and test report format shall be supplied to the AGENCY for approval upon request. The quality control procedure shall include the following, in the order shown:

Acceptance testing of all supplied components.
Physical and functional testing of all modules and items.
A minimum 100-hour burn-in of all equipment.
Physical and functional testing of all modules.

4 TYPE 2070 CONTROLLER UNIT

4.1 General

4.1.1 Module Descriptions

The Controller Unit shall be composed of the Type 2070 Unit Chassis, along with other modules and assemblies. The following is a list of composition deliverables associated to a number:

NUMBER	*ITEM*	*DESCRIPTION*
1	TYPE 2070	UNIT CHASSIS
2	TYPE 2070-1A	CPU MODULE, MULTIPLE BOARD-VME
3	TYPE 2070-1B	CPU MODULE, SINGLE BOARD- SERIAL HUB
4	TYPE 2070-2A	FIELD I/O MODULE (FI/O for 170 Cab)
5	TYPE 2070-2B	FIELD I/O MODULE (ITS & NEMA Cab)
6	TYPE 2070-3A	FRONT PANEL MODULE (FP), DISPLAY A
7	TYPE 2070-3B	FRONT PANEL MODULE (FP), DISPLAY B
8	TYPE 2070-3C	FRONT PANEL MODULE (FP), BLANK
9	TYPE 2070-4A	POWER SUPPLY MODULE, 10 AMP
10	TYPE 2070-4B	POWER SUPPLY MODULE, 3.5 AMP
11	TYPE 2070-5A	VME CAGE ASSEMBLY
12	TYPE 2070-5B	MCB 1A MOUNTING ASSEMBLY
13	TYPE 2070-8	NEMA INTERFACE MODULE
14	TYPE 2070-9	2070N BACKCOVER

4.1.2 Unit Configuration

The Type 2070 Controller Unit Version defines the module composition that shall be delivered as follows:

UNIT VERSION	*COMPOSITION*	*DESCRIPTIVE*

2070 UNIT	1+2+4+6+9+11	Full unit mated to 170 cabinet family
2070N UNIT	1+2+5+6+9+11+13+14	Full unit mated to TS1 cabinet family
2070L UNIT	1+3+4+8+10	LITE Unit mated to 170 cabinet family
2070LC UNIT	1+3+5+8+10	LITE unit mated to ITS & TS2 cabinet families
2070LCN UNIT	1+3+5+8+10+13+14	LITE unit mated to TS1 cabinet Family

4.1.2.1

The communications and option modules/assemblies shall be called out separately from the unit version. The composition weight shall not exceed 11.3 kilograms.

4.1.3 Metalwork

The CHASSIS Enclosure, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Cover Plates, Power Supply Enclosure, and Front Panel shall be made of 1.524 mm minimum aluminum sheet.

4.1.4 Power Limitations

2070 UNIT module / assembly power limitations shall be as follows:

Types	*+5VDC*	*+12VDC ISO*	*+12VDC ser*	*-12 VDC ser*
MCB	750 mA	-----	-----	-----
TRANS BD	750 mA	-----	-----	-----
2070-2A FI/O	250 mA	750 mA	-----	-----
2070-2B FI/O	250 mA	500 mA	-----	-----
2070-3A&B FPA	500 mA	-----	50 mA	50 mA
2070-3C FPA	100 mA	-----	50 mA	50 mA
2070-5 VME Cage	5.0 A	-----	200 mA	200 mA
2070-6 All Comm	500 mA	-----	100 mA	100 mA
2070-7 All Comm	250 mA	-----	50 mA	50 mA

4.1.5 EIA-485 Communications Circuitry

All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 megabits per second. Isolation circuitry shall be by opto- or capacitive-coupled isolation technologies.

4.1.6 EIA-485 Line Drivers/Receivers

The EIA-485 Line Drivers/Receivers shall be socket mounted and shall not draw more than 35 mA in active state and 20 mA in inactive state. A 100-Ohm Termination Resistor shall be provided across each Differential Line Receiver Input. The MOTHERBOARD's control signals (e.g., SP1-RTS) shall be active, or asserted, when the positive terminal (e.g., SP1-RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

4.1.7 MTBF Analysis Report

Deleted

4.1.8 Sockets

Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.

4.1.9 SDLC

SP5and SP3 SDLC frame address assignments (Command/Response) are as follows:

		SP5	*SP3*
CPU 2070-1	=	“19”	“19”
FI/O 2070-2A & 8	=	“20”	Not Applicable
CPU Broadcast to all	=	“127”	“255”

All other addresses are reserved by this standard. The SDLC response frame address shall be the same address as the Command frame it receives.

4.1.10 Year 2000 Compliance

The 2070 UNIT shall comply with the Year 2000 Compliance:
"Year 2000 compliance for Systems is achieved when an application or system products (including software, microcode and microprocessors), programs, files, databases, and functionality have or create no logical or mathematical inconsistencies when dealing with dates prior to and beyond 1999. The year 2000 is recognized and processed as a leap year. The product must also operate accurately in the manner in which it was intended for date operation without requiring manual intervention."

4.2 Type 2070-1 CPU Module

4.2.1 Type 2070 – 1A Configuration

The TYPE 2070-1A CPU shall consist of the Main Controller Board, Transition Board, Board Interface Harness, and CPU Module Software.

4.2.2 Type 2070 – 1B Configuration

The TYPE 2070-1B CPU shall be a single board module meeting the 2X WIDE board requirements. The module shall be furnished normally resident in MOTHERBOARD Slot A5. The module shall meet all the requirements listed under this section and Chapter Details 4.7 except for the following:

4.2.2.1

The VME software and hardware bus requirements shall not apply nor do the MCB and Board Interface Harness physical requirements.

4.2.2.2

A Dual SCC Device (asynch / synch) and associated circuitry shall be furnished to provide two additional system serial ports. The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1. The Dual SCC2 shall be assigned as System Serial Port SP8. The SP8 and associated circuitry shall interface with the MC68360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel. The SP8 shall meet all SP2 Port requirements including EIA 485 Drivers / receivers and synchronous bps rate of 614 Kbps. An internal LOGIC Switch shall be provided to disconnect SP8 RTS, CTS and DCD (Pins 5, 6,7,18,19 and 20) lines from C13S connector.

4.2.2.3

The 68360 SCC1 shall be reassigned to ETHERNET (ENET) Network meeting ETHERNET 10 MBPS IEEE 802.3 (TP) 10 BASE T Standard Requirements, both hardware and software. The four network lines shall be used to route ETHERNET across the MOTHERBOARD to the "A" Connectors. DC Grounding plane around the network connectors and lines shall be provided. Network Lines shall be assigned as: Network 1 = ENET TX+, Network 2 = ENET TX-, Network 3= ENET RX+, and Network 4 = ENET RX-. In addition, the conditioned ETHERNET shall be brought out on RJ 45 C14S Connector mounted on the CPU-1B Front Panel. Four LEDs labeled "TX, RX, TX Collision and TX Status" shall be mounted on the front panel signifying ETHERNET operational conditions.

4.2.2.4

The 2070-1B CPU shall not draw more than 1.25 Amperes of +5VDC and 500 mA of ISO+12 VDC.

4.2.3 Main Controller Board (MCB)

4.2.3.1 General

The MCB shall be a 3U VME bus compliant board and contain a system controller, an A24-D16 interface, a Master & Slave bus interface, a Multilevel VMEbus Arbiter, a FAIR VMEbus Requester, a system clock driver, and BTO (64).

4.2.3.2 Controller

The CONTROLLER Device shall be a Motorola MC68360 or equal, clocked at 24.576 MHz minimum. The Fast IRQ Service System is reserved for AGENCY use only. The Interrupts shall be configured as follows:

Level 7 - VMEbus IRQ7, ACFAIL
Level 6 - VMEbus IRQ6
Level 5 - VMEbus IRQ5, CPU Module Counters / Timers, LINESYNC (auto vectored), Serial Interface Interrupts
Level 4 - VMEbus IRQ4
Level 3 - VMEbus IRQ3
Level 2 - VMEbus IRQ2
Level 1 - VMEbus IRQ1

4.2.3.3 Memory Address Organization

8000 0000 - 80FF FFFF	STANDARD
9000 0000 - 9000 FFFF	SHORT

4.2.3.3.1

16 megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's RBF Manager, or approved equivalent. The address of each memory block shall be specified by the Contractor and provided with the documentation.

4.2.3.3.2

When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state; and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power. An on-board circuit shall sense the +5 VDC Standby Power and shift to an On-board CPU Power Source. The CPU On-board Power shall be capable of holding the SRAM and TOD Clock up for 30 days. When the incoming +5 VDC rises to within its operating

level, the appropriate MCB Circuitry shall shift from standby power to incoming +5 VDC.

4.2.3.4 RAM Memory

A minimum of 4 MB of DRAM, organized in 32-bit words, shall be provided. A minimum of 512 KB of SRAM, organized in 16- or 32-bit words, shall be provided. The SRAM shall draw no more than 50 µA at +5 VDC in Standby Mode. The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device shall not exceed 80 ns and shall be less as required to fulfill zero wait state RAM device write access under all operational conditions.

4.2.3.5 FLASH Memory

A minimum of 4 MB of FLASH Memory, organized in 16- or 32-bit words, shall be provided. The MCB shall be equipped with all necessary circuitry for writing to the FLASH Memory under program control. No more than 1 MB of FLASH Memory shall be used for Boot Image (List) and a minimum of 3 MB shall be available for AGENCY use.

4.2.3.6 Time-of-Day Clock

A software settable hardware Time-of-Day (TOD) clock shall be provided. The Time-of-Day Clock shall be maintained to within $\pm$ 0.005% at 20°C (68°F) and to within $\pm$ 0.02% over the specified operating temperature range as compared to Coordinated Universal Time (WWV) standard for a period of thirty days during periods when AC power is not applied. The clock shall be aligned to a minimum fractional second resolution of 10 ms and shall track seconds, minutes, hours, day of month, month, and year.

4.2.3.7 CPU Reset

A software-driven CPU RESET signal (Active LOW) shall be provided to reset other controller systems. The signal output shall be driver capable of sinking 30 mA at 30 VDC. Execution of the program module "CPURESET" in the boot image shall assert the CPU RESET signal once.

4.2.3.8 CPU Activity Indicator

An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU Activity LED INDICATOR.

4.2.3.9 Tick Timer

The OS-9 Operating System TICK Timer shall be derived from each transition of LINESYNC with a tick rate of 120 ticks per second.

4.2.4 Transition Board

A TRANSITION Board (TB) shall be provided to transfer serial communication and control signals between the MCB and the Interface Master-board. Said signal and communication lines shall be driven/received off and on the module compliant to EIA-485. The Transition Board shall provide a 1 K-Ohm pull-up resistor for the A2 & A3 installed lines. If the DC Ground is not present (slot not occupied) at the CPU EIA-485 line drivers/receivers, the drivers/receivers shall be disabled (inactive).

4.2.5 Shielded Interface Harness

A SHIELDED INTERFACE HARNESS shall be provided. It shall include MCB and Transition Board connectors with strain relief, lock latch, mating connectors, and harness conductors. A minimum of 25 mm of slack shall be provided. No power shall be routed through the harness. The harness shall be 100% covered by an aluminum mylar foil and an extruded black 0.8 mm PVC jacket or equal.

4.2.6 Data Key

A DATAKEY Receptacle (KC4210, KC4210PCB or equal) with Key (DK1000or equal) resident shall be provided and mounted on the CPU module front panel (or the Transition Board of Type 1A). The Black DATAKEY shall be tested, interrogated and all 128 addresses read using Software Interface. Power shall not be applied to the receptacle if the key is not present.

4.2.7 CPU Module Software

The following shall be supplied:

1. Operating System
2. Drivers and Descriptors
3. Application Kernel
4. Error Handler
5. Validation Suite
6. Deliverables

4.2.7.1 Operating System

The CPU Module shall be supplied with Microware Embedded OS-9 Version 3.03 or later software and, in addition, the following:

1. Embedded OS-9 Real Time Kernel
2. Sequential Character File Manager (SCFMAN)
3. Sequential Protocol File Manager (SPFMAN)
4. Pipe File Manager (PIPEMAN)
5. Random Block File Manager (RBFMAN)
6. C Input Output Library (CIO)

Boot Image shall include the following utility modules:

Break	Date	Deiniz	Devs	Free	Copy
Dir	Tmode	Edt	List	Load	Deldir
Dump	Del	Ident	Iniz	Irqs	Events
Echo	Kill	Dcheck	Cio	Link	Kermit
Lmm	Mdir	Mfree	Pd	Makdir	Save
Attr	Rename	Procs	Unlink	Sleep	Xmode
Shell	Build	Setime			

4.2.7.2 Drivers and Descriptors

4.2.7.2.1

Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.

4.2.7.2.2

Drivers shall be provided to access the FLASH, SRAM, and DRAM memories through RBFMAN, or approved equivalent. The following RBFMAN descriptors shall apply:

/d0	Floppy Diskette Drive	Reserved name; no driver required
/f0	FLASH Drive	Accessed as RAM disk & OS-9 /dd default Device
/h0	Hard Disk Drive	Reserved name; no drive required
/r0	SRAM Drive	Accessed as RAM disk
/r1		Reserved; no driver required
/r2	Temporary DRAM Drive	Allows 1 MB of DRAM, accessed as RAM disk; not initialized at boot time

4.2.7.2.3

A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Access to the MC68360 internal timers shall be provided through the following device descriptors:

4.2.7.2.3.1

Descriptor names for each timer:

timer1 = access to MC68360's internal timer #1
timer2 = access to MC68360's internal timer #2
timer3 = access to MC68360's internal timer #3
timer4 = access to MC68360's internal timer #4
timer12 = access to MC68360's internal timer #1 & #2 (cascaded)

timer34 = access to MC68360's internal timer #3 & #4 (cascaded)

4.2.7.2.3.2 Timer descriptor option structure

The driver shall change appropriate functions only and ignore values that do not apply to a particular timer function. The data structures are as follows:

```
struct TER /* timer event register */
{
   u_int16 reserveTER      :14;  /* reserved                */
   u_int16 timerREF        :1;   /* output Reference Event  */
   u_int16 timerCAP        :1;   /* Capture event           */
};

struct TMR /* timer mode register */
{
   unsigned timerPS     :8;     /* prescale                */
   unsigned timerCE     :2;     /* capture edge/enable interrupts */
   unsigned timerOM     :1;     /* output mode             */
   unsigned timerORI    :1;     /* output reference enable */
   unsigned timerFRR    :1;     /* free run or restart     */
   unsigned timerICLK   :2;     /* input clock source      */
   unsigned timerGE     :1;     /* gate enable             */
};

struct TGCR /* timer global configuration register */
{
   unsigned reserveTGCR :12;    /* reserved                */
   unsigned timerCAS_GM :1;     /* cascade timers / Gate mode */
   unsigned timerFRZ    :1;     /* freeze timer            */
   unsigned timerSTP    :1;     /* stop timer              */
   unsigned timerRST    :1;     /* reset timer             */
};

typedef struct
{
   union
   {
      struct TGCR TGCR;     /* timer global configuration register */
      unsigned short tgcr;
   } uTGCR;

   union
   {
      struct TMR  TMR;      /* timer mode register     */
      unsigned short tmr;
```

```
    } uTMR;

    u_int32  timerTRR;      /* timer reference register */
    u_int32  timerTCR;      /* timer capture register */

    union
    {
       struct TER TER;      /* timer event register  */
       unsigned short ter;
    } uTER;

} TTimer_opts;
```

4.2.7.2.3.3

Standard OS-9 System Calls for the timers:

```
error_code _os_open(char *timer_desc_name, u_int32 mode, path_id *path);
error_code _os_close(path_id path);
error_code _os_gs_popt(path_id path, u_int32 *sizeof(TTimer_opts), void
        *timer_opts);
error_code _os_ss_popt(path_id path, u_ int32 *sizeof(TTimer_opts), void
        *timer_opts);
error_code _os_write(path_id path, void *timer_value, u_int32
        *sizeof(timer_value));
error_code _os_read(path_id path, void *timer_value, u_int32
        *sizeof(timer_value));
error_code _os_ss_sendsig(path_id path, signal_code timer_sig);
error_code _os_ss_relea(path_id path);
```

4.2.7.2.4

The OS-9 System Calls shall provide access to the CPU Datakey and its control through the following descriptor name and OS-9 functions

Descriptor name:

datakey = CPU Datakey

Function Calls:

```
error_code_os_open(char*datakey_desc_name, path_id*path);
        error_code=E$NotRdy if CPU Datakey is not installed
error_code_os_read(path_id_path, void*control,128);
        error_code=E$NotRdy if CPU Datakey is not inserted
error_code_os_close(path_id path);
```

4.2.7.2.5

An Async-Communications Serial Device Driver (SDD) shall be provided to accommodate a communications network (EIA 232). The SDD shall maintain a Transmit Buffer (1536 bytes minimum) and a Receive Buffer (1536 bytes minimum).

The SDD shall provide six Flow Control Modes (FCM) as described below.

FCM # Description

0) **None**: This shall be the default SDD FCM. The SDD shall continually assert the CTS and DCD signals internally. The SDD shall be capable of receiving data at all times. Upon a write command, the SDD shall assert RTS, transmit the data, and de-asserts RTS when data transmission is completed (Auto RTS Turn-Off Extension parameter shall NOT delay RTS being de-asserted). When a user program issues the first RTS related command, the SDD shall switch to Manual FCM.

1) **Manual**: The SDD shall transmit and receive data regardless of RTS, CTS, and DCD states. The user program shall have absolute control of the RTS state. The SDD shall NOT assert or de-assert RTS. The CTS and DCD states are set external to the SDD. The user program may query for CTS and DCD states.

2) **Auto-CTS**:The SDD shall continually assert the DCD signal internally. The SDD shall be capable of receiving data at all times. The user program has absolute control of the RTS state. The SDD does not assert or de-assert RTS. The CTS state is set external to the SDD. The SDD shall only transmit data when CTS is asserted.

3) **Auto-RTS**: The SDD shall continually assert the CTS and DCD signals internally. The SDD shall be capable of receiving data at all times. Upon a write command, the SDD shall assert RTS, transmit the data, and de-asserts RTS when data transmission is completed. Auto RTS Turn-Off Extension parameter shall delay RTS being de-asserted after last character.

   If the user program asserts RTS, RTS remains asserted until the user program de-asserts RTS. If user program de-asserts RTS before the Transmit Buffer is empty, the SDD shall hold RTS asserted until the Transmit Buffer is empty.

4) **Fully Automatic**: The SDD shall receive data when DCD is asserted. Upon a write command, the SDD shall assert RTS, wait for CTS to be asserted before transmiting data, and de-asserts RTS when data transmission is completed. Auto RTS Turn-Off Extension parameter shall delay RTS being de-asserted after last character.

   If the user program asserts RTS, RTS remains asserted until the user program de-asserts RTS. If user program de-asserts RTS before the

Transmit Buffer is empty, the SDD shall hold RTS asserted until the Transmit Buffer is empty.

5) **Dynamic**: The SDD shall continually assert the DCD signal internally. The SDD shall be capable of receiving data at all times. The SDD shall transmit data when CTS is asserted. The SDD shall assert RTS when the number of characters in the SDD Receive Buffer is below the Low Watermark parameter level and shall de-asserts RTS when the number of characters in the SDD Receive Buffer is above the High Watermark parameter level.

The serial device driver shall be able to accept user configuration commands to configure the device driver via OS9_os_ss_size() function call and to accept user request commands for status of serial port from the device driver via OS9_os_gs_size() function call.

The single 32-bit variable passed by_os_ss_size() is defined as follow:

a) Flow Control Code is SS_OFC (0x23):

Bits	*Description*
31-24	Auto RTS turn-off extension count in number of characters (range=0-255 default=0).
15	Auto RTS turn-off extension timing (default=0, 0=bps, 1=equivalent 1200 bps).
14-13	14-13 Reserve for Future Use (default=0).
12	Inhibit Change of SCC MRBLR for opened path (default =0; 0=NO; 1=inhibit).
11	Inhibit SCC TODR for opened path (default=0; 0=NO; 1=inhibit).
10-8	Flow Control Mode Number (FCM#) (range=0-5).
7-0	Flow Control Code (FCC) =0x23

Note: The RTS turn-off extension can represent a bps rate independent time value rather a number of character times, (higher bps rates are normalized to equivalent 1200 bps characters) when selected by bit 15=1. Thus, a value of 4 represents the time of four characters at 1200 bps even when the actual rate is 9600. If bit 15=0, then an extension value = 4 represents 4 characters, which at a bps rate of 9600 would extend the RTS by approximately 3.3 ms.

b) Flow Control Code is SS_IFC (0x22):

Bits	*Description*
31-22	Flow Control Mode 5 high water mark value (range=1-1023; default=512).
21-12	Flow Control Mode 5 low water mark value (range=1-1023; default=256).
11	Inhibit DCD activating control (default=0; 0=off; 1=on).
10	DCD flow control is active (default=0; 0=NO; 1=YES, changed by FCM#).
9-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC) = 0X22.

Note: The inhibit DCD selection has priority over the DCD ON request in the same access. Therefore, sending 0x00000822 or 0x00000C22 results in DCD inhibit and DCD Flow Control inactive for all Flow Modes. A new flow control mode number shall set DCD function to that required in the new mode unless DCD is inhibit is ON.

c) Flow Control Code is SS_Ssig (0x1a):

Bits	*Description*
31-16	A signal number to be sent to calling process when the state of a pin is changed.
15-14	Reserved for Future Use (default=0).
13	Ring is asserted (capable hardware only).
12	CTS is de-asserted.
11	CTS is asserted.
10-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC) = 0x1a.

d) Flow Control Code is SS_DCmd (0x0d):

Bits	Description
31-15	Reserved for Future Use (default=0).
14	De-assert DTR (capable hardware only).
13	Assert DTR (capable hardware only).
12	De-assert RTS (duplicated function with_os_ss_DsRTS();).
11	Assert RTS (duplicated function with_os_ss_EnRTS();).
10-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC)=0x0d.

The single 32-bit variable returned by_os_gs_size() is defined as follow:

Bits	*Description*
31-16	Current unfilled transmit buffer character count of the serial device driver.
15-11	Reserved for Future Use (default=0).
10-8	Current Flow Control Mode Number (FCM#).
7	Reserved for Future Used (default=0).
6	Overrun error – 0=no error; 1=error since the last query.
5	Frame error – 0=no error; 1=error since the last query.
4	Parity error – 0=no error; 1=error since the last query.
3	Ring Indicator input state – 0=de-asserted; 1=asserted (capable hardware only).
2	DSR input state – 0=de-asserted; 1=asserted (capable hardware only).
1	DCD input state – 0=de-asserted; 1=asserted.
0	CTS input state – 0=de-asserted; 1=asserted.

4.2.7.2.6

The device shall provide four input buffering modes as follows:

1.Line - characters are buffered up to and including a programmable termination character.
2. Fixed - a fixed specific number of characters is buffered by the driver (1 @ 1200bps, 2 @ 2400bps, 4 @ 4800 bps, 8 @ 9600 bps, and 16 @ 19200 bps & above)
3.Timed- characters are buffered until a programmable inter-character time out occurs.
4. Raw – characters are unbuffered and delivered to the task as received.

4.2.7.2.7

Line, Fixed, and Timed Modes shall be capable of being used together. Raw mode shall disable all other buffering modes.

4.2.7.2.8

Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names shall be as follows:

led	=	access to CPU Activity LED Indicator
dstclock	=	access to Daylight Savings Time Clock correction

The standard OS-9 SCFMAN library calls and their functions are as follows:

```
error_code  _os_open (char *desc_name, path_id *path);  //open descriptor for command
error_code  _os_close (path_id path);                   //close descriptor
error_code  _os_write (path_id path, void *value, 1);   //set value or function
        *value = 1, turn led on or turn DLSclock feature on (default)
        *value = 0, turn led off or turn DLSclock feature off
error_code  _os_read (path_id path, void *value, 1);    //get current state
```

4.2.7.2.9 Time-of-Day (TOD) Clock

The OS-9 operating system's TOD Clock shall be driven by the LINESYNC derived OS-9 Operating System TICK Timer. The device shall provide the following features to support the TOD operation and synchronization.

4.2.7.2.9.1

Leap Year and Daylight Savings Time (DST) Adjustments - The OS-9 System clock / calendar shall automatically be adjusted to account for DST and leap years. A SCFMAN driver shall be provided to enable/disable the automatic DST adjustment.

4.2.7.2.9.2

Setting Hardware Clock from OS-9 System Clock - A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be "ClockUpdate." Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.

4.2.7.2.9.3

Setting OS-9 System Clock from Hardware Clock - At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall by synchronized to a minimum of 10 ms resolution.

4.2.7.2.9.4

The FLASH RAM drive (/f0) shall be protected from corruption due to power failure during a write operation. The current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy. A user write operation shall restore the valid backup sector copy first. Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds. No more that 150 KB of SRAM shall be dedicated to this purpose. A large file being written, but truncated due to power fail, shall not be restored intact.

4.2.7.3 Application Kernel

4.2.7.3.1

The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The initialization routines shall configure the serial port protocols as follows:

SP1 & 2	1.2 Kbps, 8-bit word, 1 stop, no parity, no pause, no echo
SP 3S	153.6 Kbps
SP4	9.6 Kbps, 8-bit word, 1 stop, no parity, no pause, XDR off, xoff
SP 5S	614.4 Kbps
SP 6	38.4 Kbps, 8-bit word, 1 stop and no parity

4.2.7.3.2

Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 1.3 seconds.

4.2.7.3.3

A Trap Library routine, "Warmboot," shall be provided, which upon execution shall first shut down the OS-9 operating system, then jump to the start of the initialization routines executed on SYSRESET and proceed.

4.2.7.3.4

After initialization (boot up from SYSRESET), the program shall fork to the defined module in FLASH memory named OPEXEC preceded by a full path. If OPEXEC is not found or fails the program shall fork a shell. If OPEXEC is forked successfully, the program shall exit.

4.2.7.3.5

A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. A Short Out results in resumption of Application Software without an operating system reboot. The Contractor shall provide a documented method for the Application Software to recover from Level 7 IRQ (ACFAIL) without a SYSRESET. A Long Out is defined as ACFAIL transition to LOW followed by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

4.2.7.4 Error Handler

4.2.7.4.1

Error handling routine to cope with initialization and power-up test anomalies shall be provided. Errors that occur during initialization and/or during power-up test shall produce a report.

4.2.7.4.2

The Error Handler shall respond to the following conditions and generate an Error Report (saved in Memory):

1. Timer initialization error
2. Timer power up test error
3. Serial communication port initialization error
4. Serial communication port power up test error
5. Peripheral component initialization error

4.2.7.4.3

The Error Handler error report shall contain, at a minimum, component identification and an error code to identify the form of the error. The error report shall be a file accessible through the Random Block File Manager and named "ErrorReport."

4.2.7.5 Validation Suite

4.2.7.5.1

A validation suite of software and associated documentation shall be provided. It shall include diagnostic programs necessary to test 2070 Controller Unit functions. The diagnostic programs shall demonstrate that all software and hardware functions operate in conformance to specified functionality. It shall provide a working example of how to program functions

4.2.7.5.2

Validation suite software and associated documentation shall be segmented into individual test sequences. It shall be possible to separate out any one or group of these sequences and, with the addition of a general header file, execute it in isolation or in combination with application software.

4.2.7.5.3

When factory boot code is operating without the User “Opexec” started, the Validation Suite shall be invoked from the front panel keypad, either as a execution in a continuous loop or by individual test selections.

4.2.7.5.4

The validation suite shall execute as a task of the OS-9 Shell Utilities and Commands module. Execution from the shell shall be by typing "Valsuite" from the prompt. If the User Program has been executed, the VALSUITE shall not execute any of its tests due to resource conflicts. It shall be possible to execute the following additional CPU Module specific commands while in the OS-9 Shell Utility:

1. Get/Set the hardware time of day clock
2. Set OS-9 clock from hardware clock
3. Read/write all I/O registers internal to the MC 68360
4. Get/Set all programmable controls on serial ports
5. Verify that the 120 Hz interrupt is functioning
6. Set, configure, and read timers
7. Observe time-out interrupts

4.2.7.5.5

The OS-9 Shell Utility shall communicate with the user through the SP4 Port. When invoked, a low-priority task shall be executed for each SP port 1 and 2. Each task shall be configurable to use a different combination of input buffering options. The task shall open the port, configure it, and then enter a processing loop. In the loop, it shall wait for input and echo any input to the output. If no input is received for one second, an ASCII text string shall be sent out on the port. This text string shall be of the form *"port P hh:mm:ss."* P is the port number and hh:mm:ss is the current OS-9 time stamp. The text shall be terminated with a carriage return followed by a line feed character.

4.2.7.6 Deliverables

4.2.7.6.1

A software package resident on the FLASH Memory shall be provided, including the Embedded OS-9 kernels, platform drivers, and a validation suite.

4.2.7.6.2

Software shall be delivered in the following forms:

1. Fully commented source code of contractor developed validation suite software (OS-9 drivers and user application program not required)
2. Microware Ultra-C Version 1.1 compatible linkable object code
3. Memory map listing

4.2.7.6.3

Specific hardware memory addresses shall be specified and provided in a supplied INCLUDE FILE as defined constants. The INCLUDE FILE shall meet all applicable software delivery requirements.

4.2.7.6.4

Timer usage by drivers and their uninterrupted execution latencies, error values returned by driver calls, error codes, and a format of the error report file shall be documented.

4.2.7.6.5

Software to initialize and perform a power-up self-test of the CPU Module prior to the initialization of the OS-9 operating system shall be provided. All software components detailed in this specification or otherwise, and requiring initialization, shall be identified and the required initialization and nature of the test, documented. In addition, software provided to perform initialization and/or test shall be documented.

4.2.7.6.6

OS-9 compliant header files shall be provided with all Driver Modules.

4.3 Type 2070-2 Field I/O Module (FI/O)

4.3.1 Type 2070-2A Module

The TYPE 2070-2A MODULE shall consist of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle switch); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required resident software.

4.3.2 Type 2070-2B Module

The TYPE 2070-2B MODULE shall consist of the Serial Communication Circuitry, VDC Power Supply, and Module Connector C12S mounted on the module front plate only.

4.3.3 Field Controller Unit (FCU)

The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware.

4.3.4 Parallel I/O Ports

4.3.4.1

The I/O Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the Isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground.

4.3.4.2

The I/O Ports shall provide 64 bits of output.

Inputs shall have the following characteristics:

1. A voltage between 0 and 4 volts shall be considered the **Low** (True/Operate) state.
2. A voltage greater than 8 volts shall be considered the **High** (False) state.

3. The transition from the **Low** state to **High** state (and vice versa) shall occur between 4 and 8 volts.

Outputs shall have the following characteristics:

1. The **Low** (True/Operate) voltage shall be between 0 and 3 volts.
2. Current sinking capability in the **Low** state shall be at least 100 milliamperes.
3. With an external impedance of 100K ohms or greater, the transition from 4 to 16 volts (and vice versa) shall be accomplished within 0.1 millisecond.
4. The **High** state impedance shall exceed 1 megohms to 12 volts DC.

4.3.4.3

Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state shall be open (logic 0). It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

4.3.5 Other Module Circuit Functions

4.3.5.1

A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

4.3.5.2

An External WDT "Muzzle" Jumper shall be provided on the board. With the jumper in and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 – Monitor Watchdog Timer Input) every 100 ms for 3.5 seconds or due to CPU Command. When the jumper is missing (open), the feature shall not apply. This feature is required to operate with the Type 210 Monitor Unit only.

4.3.5.3

A WATCHDOG Circuit shall be provided. It shall be enabled by the FIELD I/O software at Power Up with a value of 100 ms. Its enabled state shall be machine readable and reported in the FI/O status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FI/O. Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

4.3.5.4 One KHz Reference

A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

4.3.5.5

A 32-bit MILLISECOND COUNTER (MC) shall be provided for "timestamping." Each 1 KHz reference interrupt shall increment the MC.

4.3.5.6

At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the "E" Bit and a subsequent set output command is processed.

4.3.5.7

A LOGIC Switch shall be provided resident on the module board. The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of SP3. A LED shall be provided on the module front panel labeled "SP3 ON". If LED light ON, SP3 is active and available at C12S.

4.3.6 Serial Communications/Logic Circuitry

4.3.6.1

System Serial Port 5 (SP5) EIA-485 signal lines shall enter the I/O Module and be split into two multi-drop isolated ports. One shall be routed to the FCU and the other converted to EIA-485, then routed to Connector C12S.

4.3.6.2

System Serial Port 3 (SP3) EIA-485 signal lines shall enter the I/O module and be isolated, converted back to EIA-485 and then routed to connector C12S.

4.3.6.3

LINE SYNC and POWER DOWN lines shall be split and isolated, one routed to the FCU for shut down functions and the other changed to EIA-485; then routed to connector C12S for external module use.

4.3.6.4

CPU RESET and POWER UP (SYSRESET) lines shall be isolated and "OR'd" to form NRESET. NRESET shall be used to reset FCU and other module devices. NRESET shall also be converted to EIA-485 then routed to connector C12S.

4.3.6.5

If the 2070 module is a –2B, then routing to FCU doesn't apply.

4.3.6.6

Isolation is between internal +5 VDC / Ground #1 and +12 VDC ISO / VDC Ground #2. +12 VDC ISO is for board power and external logic.

4.3.7 Buffers

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer. The entry types are depicted as follows:

Input Transition Entry

Description	***msb***							***lsb***	***Byte Number***
Transition Entry Identifier	S	Input Number							1
MC Timestamp NLSB	x	x	x	x	x	x	x	x	2
MC Timestamp LSB	x	x	x	x	x	x	x	x	3

Millisecond Counter Rollover Entry

Description	***msb***							***lsb***	***Byte Number***
Rollover Entry Identifier	1	1	1	1	1	1	1	1	1
MC Timestamp MSB	x	x	x	x	x	x	x	x	2
MC Timestamp NMSB	x	x	x	x	x	x	x	x	3

4.3.8 I/O Functions

4.3.8.1 Inputs

Input scanning shall begin at I0 (bit 0) and proceed to the highest input, ascending from lsb to msb. Each complete input scan shall finish within 100 µs. Once sampled, the logic state of an input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 µs. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and MC timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 µs of the completion of the input scan.

4.3.8.2 Data Filtering

If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering	Enabled
On and off filter values shall be set to	5
Transition monitoring	Disabled (MC Timestamps are not logged)

4.3.8.3 Outputs

Simultaneous assertion of all outputs shall occur within 100 µs. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the FI/O status byte shall be updated to reflect the loss of communication from the CPU Module.

4.3.8.4 Standard Function

Each output shall be controlled by the data and control bits in the CPU Module-FI/O frame protocol as follows:

Output Bit Translation

Case	*Output Data Bit*	*Output Control Bit*	*Function*
A	0	0	Output in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state.

4.3.8.4.1

In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 µs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs shall not change state unless configured to do so.

4.3.8.5 Interrupts

All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 KHz reference once per ms. An MC timestamp rollover flag set by MC rollover shall be cleared only on command. LINESYNC Interrupt - This interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds ($\geq$60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer ($\geq$500 consecutive millisecond interrupts).

4.3.8.6 Communication Service Routine

A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically:

For Transmission:

Generate the opening and closing flags

Generate the CRC value
Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU
Provide zero bit insertion

For Receiving:

Detect the opening and closing flags
Provide address comparison, generating an interrupt for messages addressed to the I/O Module, and ignoring messages not addressed to the I/O Module
Strip out inserted zeros
Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
Generate an interrupt if an abort sequence is received

4.3.8.7 Communication Processing

The task shall be to process the command messages received from the CPU Module, prepare, and start response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. The time from the receipt of message to the completion of the commanded task shall not exceed 70ms.

4.3.8.8 Input Processing

This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

4.3.9 Data Communications Protocols

Protocols - All communication with the CPU Module shall be SDLC-compatible command-response protocol, support 0 bit stuffing, and operate at a data rate of 614.4 Kbps. The CPU Module shall always initiate the communication and should the command frame be incomplete or in error, no FI/O response shall be transmitted. The amount of bytes of a command or response is dependent upon the I/O Module identification.

4.3.9.1.1

The frame type shall be determined by the value of the first byte of the message. The command frames type values 112-127 and associated response frame type values 240-255 are allocated to the Contractor diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Frame Types

Module Command	*I/0 Module Response*	*Description*	*Minimum Message Time*	*Maximum Message Time*
0-43	128-171	Reserved for NEMA TS-2		
49	177	Request Module Status	250 µs	275 us
50	178	MILLISECOND CTR. Mgmt.	222.5 µs	237.5 us
51	179	Configure Inputs	344.5 µs	6.8750 ms
52	180	Poll Raw Input Data	317.5 µs	320 µs
53	181	Poll Filtered Input Data	317.5 µs	320 µs
54	182	Poll Input Transition Buffer	300 µs	10.25 ms
55	183	Command Outputs	405 µs	410 µs
56	184	Config. Input Tracking Functions	340 µs	10.25 ms
57	185	Config. Complex Output Functions	340 µs	6.875 ms
58	186	Configure Watchdog	222.5 µs	222.5 µs
59	187	Controller Identification	222.5 µs	222.5 µs
60	188	I/O Module Identification	222.5 µs	222.5 µs
61-62	189-190	Reserved (note below)		
63	191	Poll variable length raw input	317.5 us	320 us
64	192	Variable length command outputs	405 us	410 us

4.3.9.1.2

Messages 61 / 189 and 62 / 190 are reserved for ITS Cabinet Frame Types. Message 63 / Message 191 shall be the same as Message 52 / 180 except Byte 2 of Message 180 response shall denote the following number of inputs bytes. Message 64 / 192 shall be the same as Message 55 / 183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes along with the following output data.

4.3.9.2 Request Module Status

The Command shall be used to request FI/O status information response. Command/response frames are as follows:

Request Module Status Command

Description	*msb*							*lsb*	*Byte Number*
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response

Description	*msb*							*lsb*	*Byte Number*
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3

SCC Transmit Error Count	Transmit Error Count	Byte 4
MC Timestamp MSB	MC Timestamp MSB	Byte 5
MC Timestamp NMSB	MC Timestamp NMSB	Byte 6
MC Timestamp NLSB	MC Timestamp NLSB	Byte 7
MC Timestamp LSB	MC Timestamp LSB	Byte 8

4.3.9.2.1

The response status bits are defined as follows:

P - Indicates FI/O hardware reset
E - Indicates a communications loss of greater than 2 seconds
K - Indicates the Datakey has failed or is not present
R - Indicates that the EIA-485 receive error count byte has rolled over
T - Indicates that the EIA-485 transmit error count byte has rolled over
M - Indicates an error with the MC interrupt
L - Indicates an error in the LINESYNC
W - Indicates that the FI/O has been reset by the Watchdog

4.3.9.2.2

The FI/O status byte shall be updated (set to '1') to reflect the faults noted in clause 4.3.9.2.1. Each status bit shall only be reset (set to '0') when the corresponding bit of the Request Module Status Command is a '1'. The Request Module Status Response shall report the current status (subsequent to reset and sampling).

4.3.9.2.3

The FI/O shall count the number of errored frames the FI/O Communications Processor reports. Separate counts shall be maintained for transmit and received frames. When a individual count rolls over (255-0), the corresponding roll-over flag shall be set.

4.3.9.2.4

FI/O modules with Datakey: On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key. If absent, Status Bit “K” shall be set to '1' and no interrogation shall take place. If an error occurs during the interrogation, Status Bit “K” shall be set to '1'. FI/O modules without Datakey: Status Bit "K" shall always be set to '1'

4.3.9.2.5

The MC timestamp value shall be sampled just prior to the Request Module Status Response.

4.3.9.3 MC Management

MC MANAGEMENT frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

Millisecond Counter Management Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1
New MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 2
New MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3
New MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 4
New MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 5

Millisecond Counter Management Response

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

4.3.9.4 Configure Inputs

The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1
Number of Items (n)	n	n	n	n	n	n	n	n	Byte 2
Item # - Byte 1	E	Input Number							Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)								Byte 3(I-1)+4
Item # - Byte 3	Trailing edge filter (r)								Byte 3(I-1)+5

Configure Inputs Response

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

Block field definitions shall be as follows:

E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input

e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)

r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)

S - return status S = '0' on completion or '1' on input error out of range

4.3.9.5 Poll Raw Input Data

The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes (2B) of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1

Poll Raw Input Data Response (2070-2A)

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x	Bytes 3 to 9
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 10
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 11
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 12
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 13

Poll Raw Input Data Response (2070-8)

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

4.3.9.6 Poll Filtered Input Data

The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes (2B) of information indicating the current filtered status of the inputs. Raw input data shall be

provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 53)	0	0	1	1	0	1	0	1	Byte 1

Poll Filter Input Data Response (2070-2A)

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x	Bytes 3 to 9
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 10
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 11
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 12
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 13

Poll Filter Input Data Response (2070-8)

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

4.3.9.7 Poll Input Transition Buffer

The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 54)	0	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2

Poll Input Transition Buffer Response

Description	***msb***							***lsb***	***Byte Number***

(Type Number = 182)	1	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2
Number of Entries	x	x	x	x	x	x	x	x	Byte 3
Item #	S	Input Number							Byte 3(I-1)+4
Item # MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+5
Item # MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G	Byte 3(I-1)+7
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+8
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+9
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+10
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+11

4.3.9.7.1

Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. The FI/O shall set the 'F' bit to '1' when attempting to record a transition and the Transition Buffer is full. While the Transition Buffer is full, all subsequent entries shall be discarded. Bit definitions are as follows:

S - Indicates the state of the input after the transition
C - Indicates the 255 transition entries limit has been exceeded
F - Indicates the transition buffer limit has been exceeded
G - Indicates the requested block number is out of monotonic increment sequence
E - Same block number requested, E is set in response

4.3.9.7.2

The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

4.3.9.7.3

The Timestamp shall equal the MC value at the time the Poll Input Transition Buffer Response is generated.

4.3.9.8 Set Outputs

The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set. Loss of LINESYNC reference shall also be indicated in system status information. The output bytes depend upon field I/O module. These command and response frames are as follows:

Set Outputs Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	x	x	x	x	x	x	x	x	Byte 2
Outputs O8 to O103 Data	x	x	x	x	x	x	x	x	Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	x	x	x	x	x	x	x	x	Byte 15
Outputs O8 to O103 Control	x	x	x	x	x	x	x	x	Bytes 16 to 27

Set Outputs Response

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 183)	1	0	1	1	0	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E	Byte 2

4.3.9.9 Configure Input Tracking Functions

The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to '1' and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 56)	0	0	1	1	1	0	0	0	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	E	Output Number							Byte 2(I-1)+3
Item # - Byte 2	I	Input Number							Byte 2(I-1)+4

Configure Input Tracking Functions Response

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 184)	1	0	1	1	1	0	0	0	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3

MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 4
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 5
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 6

4.3.9.9.1

Definitions are as follows:

E '1' - Enable input tracking functions for this output
'0' - Disable input tracking functions for this output
I '1' - The output is OFF when input is ON, ON when input OFF
'0' - The output is ON when input is ON, OFF when input is OFF
V '1' - The max. number of 8 configurable outputs has been exceeded
'0' - No error
Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

4.3.9.9.2

The Timestamp shall equal the MC value at the time the Configure Input Tracking Functions Response is generated.

4.3.9.9.3

Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

4.3.9.9.4

The "Number of Items" field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message "V" bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function, or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

4.3.9.10 Configure Complex Output Functions

The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function

command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

Configure Complex Output Functions Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 57)	0	0	1	1	1	0	0	1	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	0	Output Number							Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)								Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)								Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)								Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)								Byte 7(I-1)+7
Item # - Byte 6	0	Input Number							Byte 7(I-1)+8
Item # - Byte 7	P	W	G	E	J	F	R	L	Byte 7(I-1)+9

Configure Complex Output Functions Response

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 185)	1	0	1	1	1	0	0	1	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
MC Timestamp (MSB)	x	x	x	x	x	x	x	x	Byte 3
MC Timestamp (NMSB)	x	x	x	x	x	x	x	x	Byte 4
MC Timestamp (NLSB)	x	x	x	x	x	x	x	x	Byte 5
MC Timestamp (LSB)	x	x	x	x	x	x	x	x	Byte 6

4.3.9.10.1

Number of items - The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.

Output Number - 7-bit output number identifying outputs

F '1' - The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.
'0' - The trigger or gate shall be derived from the raw input.

R '1' - For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered

immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.

'0' - For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.

Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.

Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.

Input Number - 7-bit input number identifying inputs.

P	'1'	-	The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.
	'0'	-	The output is configured for continuous oscillation.
W	'1'	-	It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.
	'0'	-	Operation shall begin within 2 ms of the command receipt.
G	'1'	-	Operation shall be gated active by the specified input.
	'0'	-	Gating is inactive.
L	'1'	-	The LINESYNC based clock shall be used for the time ticks.
	'0'	-	The MC shall be used for the time ticks.
V	'1'	-	Indicates maximum number of configurable outputs is exceeded.
	'0'	-	No error

The bit fields of the command frame are defined as follows:

E	'1'	-	enable complex output function for this output
	'0'	-	disable complex output function for this output
J	'1'	-	During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.
	'0'	-	During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.

The Timestamp shall equal the MC value at the time the Configure Complex Output Functions Response is generated.

4.3.9.10.2

Controlling input signals shall be sampled at least once per millisecond.

4.3.9.10.3

The "Number of Items" field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message "V" bit shall be set to 1. If an invalid output or input number (the "G" or "W" bits being set to 1) is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The "G" bit (gating) set to 1 takes precedence over the "W" bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the "W" bit in the command message. If a Complex Output is configured with the "G" bit set to 1 (gating) and the "P" bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscillation should cease (output inactive). For a single pulse operation ("G" bit set to 1), after the secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

4.3.9.11 Configure Watchdog

The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

Configure Watchdog Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1
Timeout Value	x	x	x	x	x	x	x	x	Byte 2

Configure Watchdog Response

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	Y	Byte 2

4.3.9.11.1

The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

4.3.9.11.2

On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the “Y” bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

4.3.9.12 Controller Identification

This is a legacy message command / response for FI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey See previous sections on Request Module Status for FI/O Status Bit ‘K’ definition. If “K” bit set, only the first two bytes shall be returned. The Command and Response frames are as follows:

Controller Identification Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number= 59)	0	0	1	1	1	0	1	1	Byte 1

Controller Identification Response

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 187)	1	0	1	1	1	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	K	Byte 2
Datakey	x	x	x	x	x	x	x	x	Bytes 3 to 130

4.3.9.13 Module Identification

The I/O Module Identification Command frame shall be used to request the FI/O Identification value. A response of "1" shall be returned by 2070-2A, "2" by 2070-8, "3" is reserved for NEMA TS 2 Type 1 FI/O and "32 to 40" are reserved for ITS Cabinets. The command and response frames are shown as follows:

I/O Module Identification Command

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1

I/O Module Identification Response

Description	***msb***							***lsb***	***Byte Number***
(Type Number = 188)	1	0	1	1	1	1	0	0	Byte 1

FI/O I D byte	x	x	x	x	x	x	x	x	Byte 2

4.4 Type 2070-3 Front Panel Assembly

4.4.1 General

The Type 2070-3 Front Panel Assembly (FPA) shall be delivered with one of the three options as defined in this clause. All options shall consist of a panel with Latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connector(s), CPU active LED indicator, and FP Harness Interface. The options shall include the additional features, as follows:

OPTION 3A -FPA controller, two keyboards, AUX switch, alarm bell and Display A
OPTION 3B- FPA controller, two keyboards, AUX switch, alarm bell and Display B
OPTION 3C-System Serial Port 6 Lines, isolated and vectored to Connector C60S.

4.4.2 Keyboards

Two KEYBOARDS shall be provided, one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 50 and 100 grams and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure.

4.4.3 CPU Active Indicator

The cathode of the CPU ACTIVE LED INDICATOR shall be electrically connected to the CPU Activity LED signal and shall be pulled up to +5 VDC.

4.4.4 Display

The DISPLAY shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A shall have 4 lines of 40 characters each with a minimum character dimensions of 5.00 mm wide by 10.44 mm high and an electro - luminescent (EL) backlight. Display B shall have 8 lines of 40 characters each with minimum dimensions of 2.65 mm wide by 4.24 mm high and either LED or EL backlight.

4.4.4.1

Each character shall be composed of a 5 x 7 dot matrix with a underline row or a 5 x 8 dot matrix. The viewing angle of the LCD shall be optimized for direct (90^{o}) viewing, +/-35^{o} vertical, +/-45^{o} horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

4.4.4.2

The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.

4.4.4.3

Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.

4.4.5 FPA Controller

The FPA CONTROLLER shall function as the Front Panel Device controller interfacing with the CPU Module.

4.4.5.1

A FPA RESET Switch shall be provided on the Assembly PCB. The momentary CONTROL switch shall be logic OR'd with the CPU RESET Line, producing a FPA RESET Output. Upon FPA RESET being active or receipt of a valid Soft Reset display command, the following shall occur:

1. Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.
2. Each special character shall be set to ASCII SPC (space).
3. The tab stops shall be set to columns 9, 17, 25, and 33.
4. The backlight timeout value shall be set to 6 (60 seconds).
5. The backlight shall be extinguished.
6. The display shall be cleared (all ASCII SPC).
7. The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware RESET BUTTON IS PUSHED. The string is " ESC [PU", hex value "1B 5B 50 55".

4.4.5.2

When a keypress is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

4.4.5.3

Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

4.4.5.4

When the AUX Switch is toggled, the appropriate AUX Switch code shall be transmitted to the CPU.

4.4.5.5

The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication protocol on Page 9-7-12. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic '1' shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

4.4.5.6

Character overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

4.4.5.7

Auto-wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

4.4.5.8

Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

4.4.5.9

Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60 % ON / 40 % OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

4.4.5.10

Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

4.4.5.11

Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

4.4.5.12

The display shall have a buffer. The screen shall be refreshed from the buffer at a rate of no less than 20 times per second.

4.4.5.13

The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

4.4.5.14

The Command Codes shall use the following conventions:

1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:

   Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.
   P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)
   Px: Display column number (1-40), using one ASCII character per digit without leading zero.
   Py: Display line (1-4) one ASCII character
   ...: Continue the list in the same fashion

   Values of 'h' (0x68) and 'l' (0x6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.

3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 0x00 to 0x7F (7 bits).

4.4.5.15

The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.

4.4.5.16

C50 ENABLE function when grounded by pins 1 and 5, shall be brought to Connectors A1, pin B21 for the purpose of disabling the module channel 2, (SP4).

4.4.6 Electronic Bell

The Front Panel shall include an electronic bell to signal receipt of (0x07). The bell shall sound at 2,000 Hz, with a minimum output rating of 85 dB upon receipt of (0x07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

4.5 Type 2070-4 Power Supply Module

4.5.1 General

The Type 2070-4 Power Supply Module shall be independent, self contained Module, vented, and cooled by convection only. The Module shall slide into the unit's power

supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices.

4.5.1.1

The Type 2070-4B Module shall meet the same requirements as the 2070-4A except for 3.5 Amperes of +5 VDC and the +5 VDC STANDBY Power.

4.5.2 Module Front

An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.

4.5.3 Input Protection

Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 µH inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arrestors shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arrestors).

4.5.4 +5VDC Standby Power

+5 VDC STANDBY POWER shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry, hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 µA at a range of +5 VDC to +2 VDC for over 600 minutes.

4.5.5 Monitor Circuitry

MONITOR CIRCUITRY shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

4.5.5.1

The ACFAIL/POWER DOWN Output Lines shall go LOW (ground true) immediately upon Power Failure. The Lines shall transition to HIGH at Power Restoration. The Lines shall be driven separately. The SYSRESET/POWERUP Output Lines shall transition to LOW 525 +/-25 ms after ACFAIL/POWER DOWN transition to LOW. The Lines shall transition to HIGH 225 +/-25 ms after Power Restoration and the supply is fully recovered. The Lines shall be driven separately.

4.5.5.2

The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

4.5.5.3

The 60 Hz Square Wave LINESYNC signal shall be generated by a crystal oscillator, which shall be synchronized to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ±1% duty cycle. The output shall have drive sink capability of 16 mA. A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC. The monitor circuit shall compensate for missing pulses and line noise during normal operation.

4.5.5.4

The LINESYNC shall continue until SYSRESET transitions LOW and begin when SYSRESET transitions HIGH.

4.5.6 Power Supply Requirements

Voltage	***Tolerances***	***I Minimum***	***I Maximum***
+5 VDC	+4.875 to +5.125 VDC	1.0 AMP	10.0 AMP - MODULE 2070-4A 3.5 AMP – MODULE 2070-4B
+12 VDC Serial	+11. 4 to +12. 6 VDC	0.1 AMP	0.5 AMP
-12 VDC Serial	-11. 4 to –12. 6 VDC	0.1 AMP	0.5 AMP
+12 VDC	+11. 4 to +12. 6 VDC	0.1 AMP	1.0 AMP

4.5.6.1 Line Regulation

Line Regulation shall meet the table tolerance values for voltage range of 90 to 135 VAC, the maximum/minimum loads called out in the table and including ripple noise.

4.5.6.2 Load Regulation

Load Regulation shall meet the table tolerance values for voltage range of 90 to 135 VAC, the maximum/minimum loads called out in the table and including ripple noise.

4.5.6.3 Efficiency

70 % minimum.

4.5.6.4 Ripple & noise

Less than 0.2% rms, 1% peak to peak or 50 mV, whichever is greater.

4.5.6.5 Voltage Overshoot

No greater than 5 %, all outputs.

4.5.6.6 Overvoltage Protection

130% Vout for all outputs.

4.5.6.7 Overload & Short Circuit Protection

Power foldback point 120% of max rated power

Circuit Protection

Automatic recovery upon removal of fault.

4.5.6.8 Inrush Current

Cold Start Inrush shall be less than 25A at 115VAC.

4.5.6.9 Transient response

Output voltage back to within 1% in less than 500 µs on a 50% Load change. Peak transient not to exceed 5%.

4.5.6.10 Holdup Time

The power supply shall supply 30 watts minimum for 550 ms after ACFAIL going LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period.

4.5.6.11 Remote Sense

+5 VDC compensates 250 mV total line drop. Open sense load protection required.

4.6 Unit Chassis and Type 2070-5 VME Cage Assembly

4.6.1 General

4.6.1.1

The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s).

4.6.1.2

All external screws shall be countersunk and shall be Phillips flat head stainless steel type.

4.6.1.3

The housing shall be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide.

4.6.1.4

The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

4.6.2 Serial Motherboard

SERIAL MOTHERBOARD shall function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one layer plane assigned to DC Ground.

4.6.2.1

A wiring harness PS2 shall be provided between the Type 2070-4 Power Supply and the MOTHERBOARD PCB (provide strain relief). Test points shall be provided on the FPA side of the MOTHERBOARD for PS2 lines.

4.6.2.2

A wiring harness FP shall be provided, linking the MOTHERBOARD with the FPA.

4.6.3 Type 2070-5 VME Cage Assembly

TYPE 2070-5 VME CAGE ASSEMBLY shall consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness. The VME Cage shall conform to VME Standard IEEE P1014/D12 for 3U Cage. All slot/connectors shall be A24:D16 Interface.

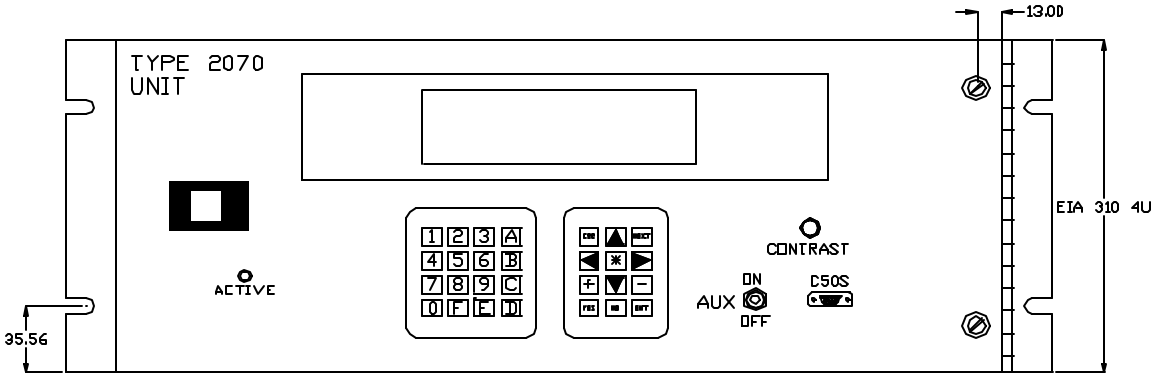
4.6.4 Type 2070-1A CPU Main Controller Board

The Type 2070 – 1A CPU Main Controller Board shall either be affixed to the Transition Board via at least four stand-off devices or mounted in a one slot VME board assembly (removable). A PS1L Harness shall be supplied with one end mating to the PS1 power supply connector and the other end mated to the MCB DIN Connector. The VME bus lines shall be terminated by a 100-Ohm resistor per line.

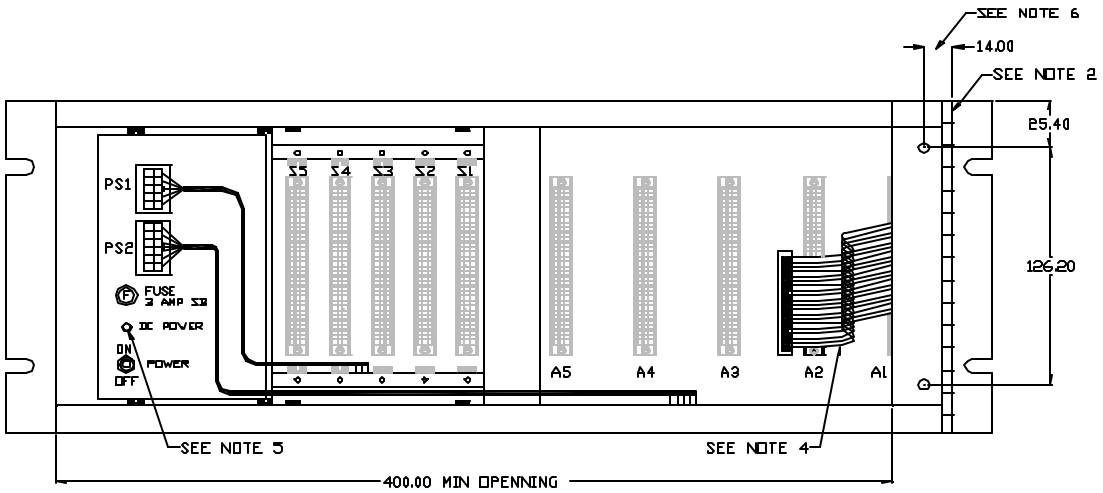
4.7 Chapter Details

TABLE OF CONTENTS

Section Notes:
All dimensions are in millimeters.



FRONT PANEL INSTALLED



FRONT PANEL REMOVED

NOTES (THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA-310B Rack using 4U open end mounting slots.

2. Continuous stainless steel hinge (4 mm maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.

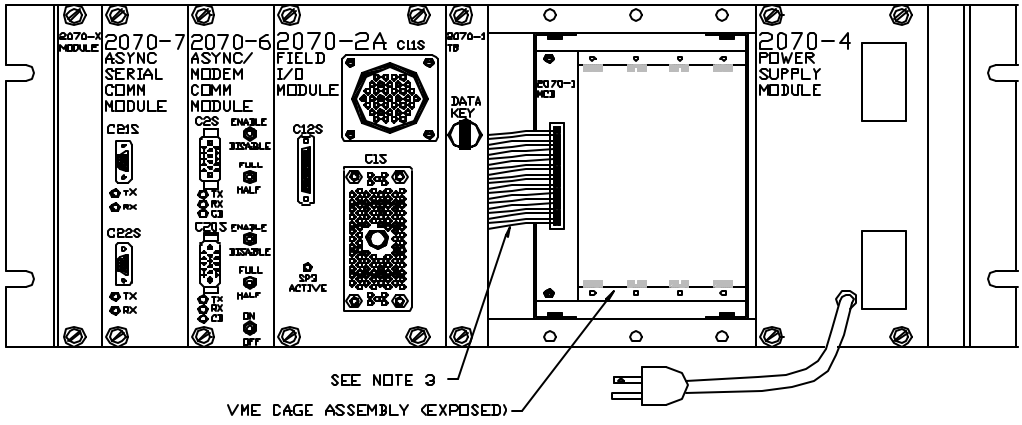
3. Actual location of ACTIVE light and contrast control shall be limited to ACTIVE light on the left side of the panel and the contrast control on the right side. They shall be located greater than 25.4 mm from other devices, connector or latch.

4. The length of the Front Panel Harness shall be no less than 284 mm.

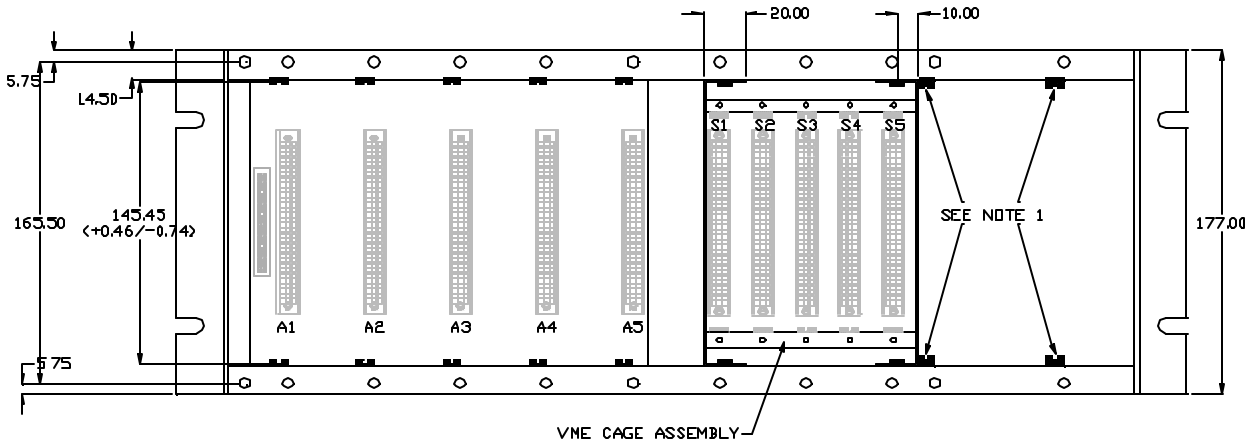
5. A LED indicator for each DC voltage shall be provided.

6. With the hinge installed, the distance between the TSD hole center and the CHASSIS Right Side (inside panel) shall be 14.00 mm.

	TITLE: TYPE 2070 CHASSIS FRONT VIEW	
	NO SCALE	
	NOV 19, 1999	4-7-1



REAR VIEW, LOADED



REAR VIEW, UNLOADED

NOTES (THIS DETAIL)

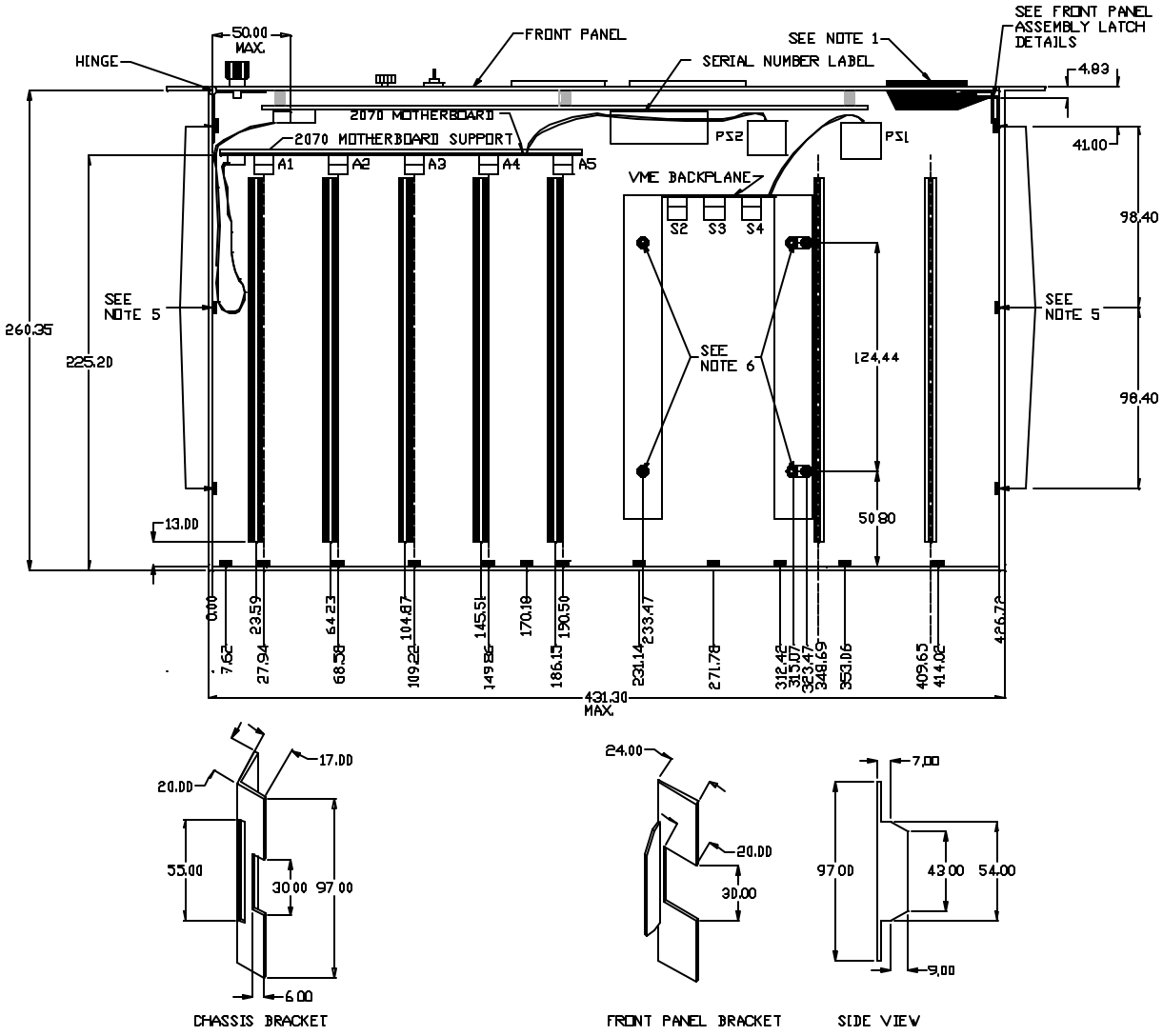
1. Four permanently attached 203.2 mm long Card Guides SAE 1800F (OR EQUAL) beginning 13 mm from the backplane mounting surface.

2. TB - TRANSITION BOARD
   MCB - MAIN CONTROLLER BOARD

3. Maximum length of harness shall be 101.60 mm, and shall not protrude beyond the back of the 2070 unit.

4. The VME Cage Assembly Openning shall be delivered covered by a blank panel. Matching M3 PEM fasteners shall be provided on the back plane surface for panel mounting.

	TYPE 2070 CHASSIS REAR VIEW	
	NO SCALE	
	NOV 19, 1999	4-7-2

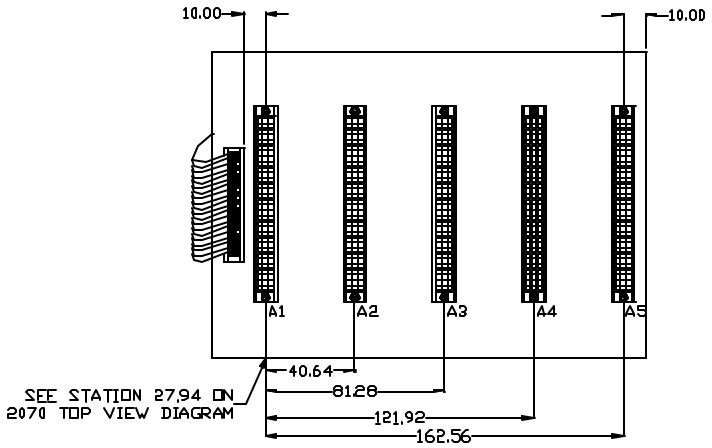


FRONT PANEL ASSEMBLY LATCH DETAILS

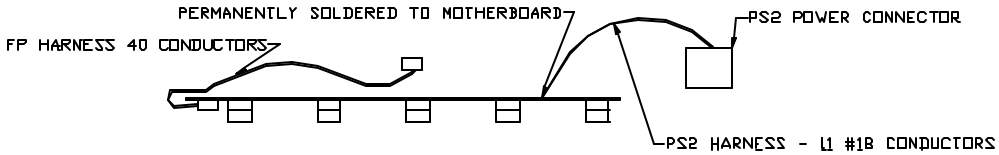
NOTES (THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided. The member shall vertically support the Front Panel Assembly in two other points besides the Latch.
2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin 13 mm from the Backplane surface.
3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.
4. All harnesses shall have a minimum slack of 25 mm when connected.
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSO #3 Thumbscrew Devices on the Type 2070-8 Module Fastener centers shall be 6.35 mm above unit baseline
6. Eight 6-32 Philips head screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.
7. The 2070 chassis top & bottom sections shall be constructed with a continuous 15.77 mm folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed 18 mm as measured from the front surface of the front panel.

	TITLE: TYPE 2070 CHASSIS TOP VIEW	
	NO SCALE	
	JANUARY 26, 2001	4-7-3



FRONT VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4-TXD+	2	SP4-TXD-
3	SP4-RXD+	4	SP4-RXD-
5	SP6-TXD+	6	SP6-TXD-
7	SP6-RXD+	8	SP6-RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DC GROUND #1	22	DC GROUND #1
23	+12 VDC SERIAL	24	-12 VDC SERIAL
25	DC GROUND #1	26	DC GROUND #1
27	CPU LED	28	DC GROUND #1
29	CPURESET	30	DC GROUND #1
31	DC GROUND #1	32	C50 ENABLE
33	DC GROUND #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC - ISOLATED
7	DC GROUND #2 (+12 VDC ONLY)
8	POWER DOWN
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

NOTES (THIS DETAIL)

1. The Motherboard shall be a 3.175 mm minimum thickness pcb mechanically mounted in a vertical position.

2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).

3. The location of the FP Harness on either side of the motherboard is allowed. The FP Harness shall either be directly soldered to the motherboard or a header used.

TITLE:

TYPE 2070 CHASSIS MOTHERBOARD

	NO SCALE	
	NOV 19, 1999	4-7-4

A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXCO+	SP5RXD+
6	SP3RTS-	SP3TXCO-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXCO+
20	NA	NA	SP3TXCO-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	DCG #1	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXCO+	SP5RXD+
6	SP1RTS-	SP1TXCO-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXCO+	SP3CTS+
16	SP2RTS-	SP2TXCO-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXCO+
20	SP2DCD-	SP2RXC-	SP3TXCO-
21	DCG #1	(SEE NOTE 4)	SP3TXCI+
22	NETWK1	(SEE NOTE 4)	SP3TXCI-
23	NETWK2	(SEE NOTE 4)	SP3RXC+
24	DCG #1	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

NOTES (THIS DETAIL)

1. Functions are referenced to the CPU.
2. DC GND #1 for +5VDC and +12VDC Serial. DC GND #2 for +12VDC ISO.
3. A1 Connector is the furthest A Connector to the left when viewed from the unit back. All A Connectors are pin assigned the same.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".

   Connector A2, pin B23 shall read "A2 Installed".

   Connector A3, pin B23 shall read "A3 Installed".

   Connector A4, pin B23 shall read "NA".

   Connector A5, pin B21 shall read "A2 Installed".

   Connector A5, pin B22 shall read "DCG #1".

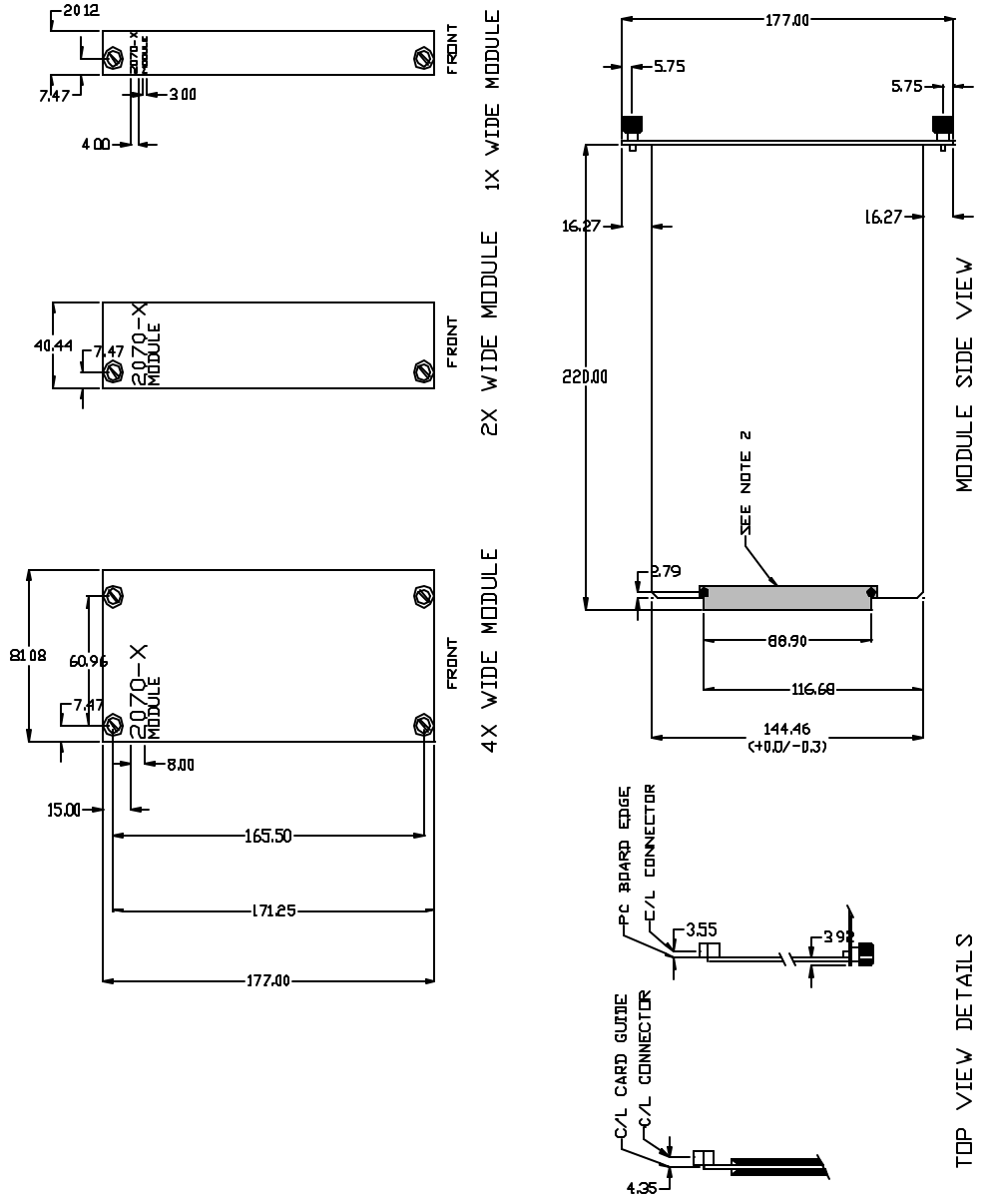
   Connector A5, pin B23 shall read "A3 Installed".
5. Pin A24 (DCG #1) is reserved for network protection only, ie., "Ethernet Shield".
6. Connector A2 installed, enables SP1 and SP2.
7. Connector A3 installed, enables SP5.
8. SP3 and SP6 are always enabled.
9. C50 enabled, disconnects SP4 on connector A1.

TITLE:
Motherboard A Connector Pin Assignment

NO SCALE

NOV 19, 1999

4-7-5



NOTES (THIS DETAIL)

1. All Thumbscrew devices on modules described in this drawing shall be TD#3 OR EQUAL

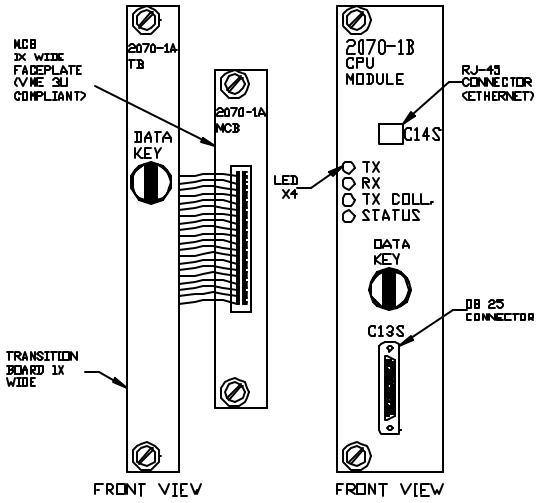
2. 96 pin DIN connector ELCO # 00 8272 96 000 013 OR EQUAL.

	TITLE: TYPE 2070 SYSTEM PCB MODULES, GENERAL	
	NO SCALE	
	NOV 19, 1999	4-7-6

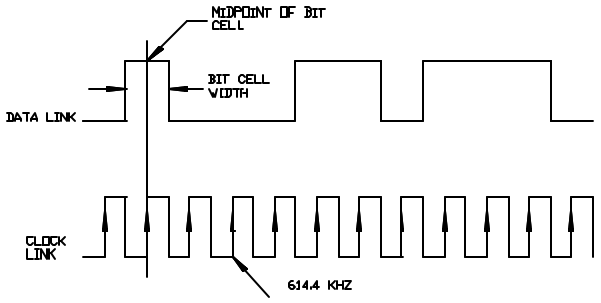
SERIAL PORT REQUIREMENTS

A2 TO A5 CONNECTOR PIN OUT			
LOGICAL PORT	68360 PORT	RATE KBITS	PROTOCOL
SP1	SEE NOTE 4	(1)	ASYNC
SP1S	SEE NOTE 4	(2)	SYNC, HDLC, SDLC
SP2	SCC2	(1)	ASYNC
SP2S	SCC2	(2)	SYNC, HDLC, SDLC
SP3	SCC4	(1)	ASYNC
SP3S	SCC4	153.6, 614.4*	SYNC, HDLC, SDLC
SP4	SMC2	(1)	ASYNC
SP5	SCC3	(1)	ASYNC
SP5S	SCC3	153.6, 614.4*	SYNC, HDLC, SDLC
SP6	SMC1	(1), 38.4*	ASYNC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



CPU FACE PANELS



SDLC TIMING

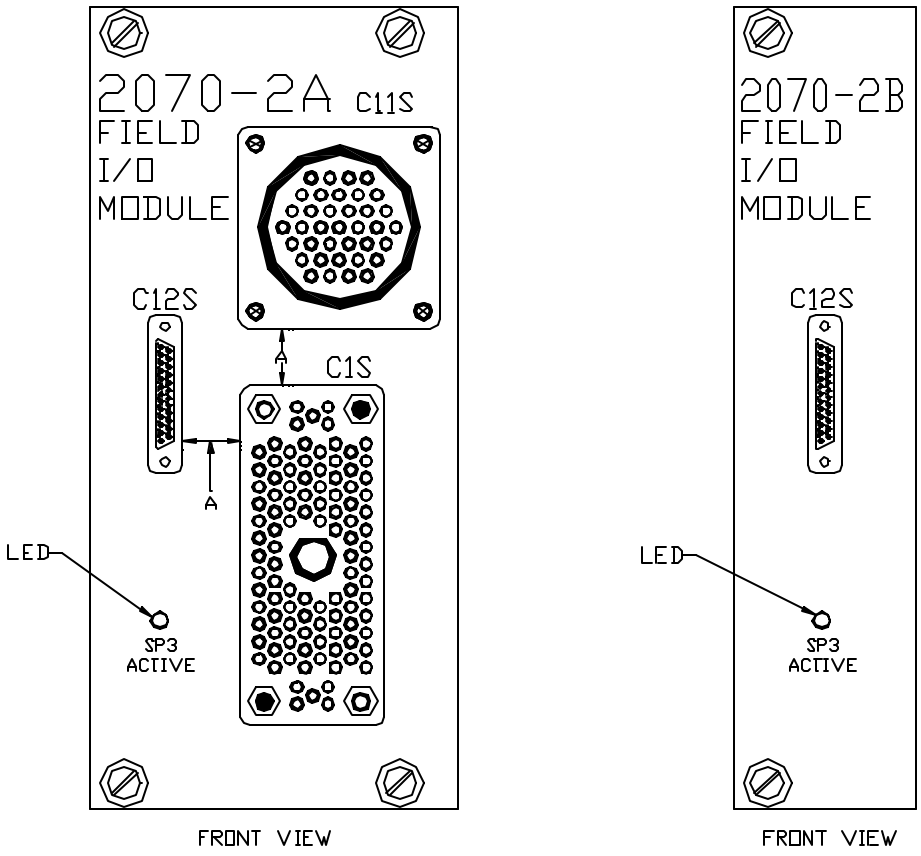
C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS + **	18	SP8 RTS - **
6	SP8 CTS + **	19	SP8 CTS - **
7	SP8 DCD + **	20	SP8 DCD - **
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

C14S PIN ASSIGNMENT (ETHERNET)			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES (THIS DETAIL)

1. (1) BPS Rates 1.2* 2.4, 4.8, 9.6, 19.2, 38.4
2. (2) BPS Rates 19.2*, 38.4, 57.6, 76.8, 153.6
3. * Default BPS Rate for indicated Port.
   Async Defaults are 8-N-1
   ** Disconnected by internal switch.
4. SP1 OF THE 2070-1A is 68360 SCC1. SP1 OF THE 2070-1B is Dual SCC1 with 68360 SCC1 assigned to ETHERNET.
5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.

TITLE: TYPE 2070-1 CPU MODULES AND SERIAL PORT/SDLC PROTOCOL		
	NO SCALE	
	JANUARY 26, 2001	4-7-7



FIELD I/O FACE PANELS

NOTES (THIS DETAIL)

1. 2070-2A Faceplate shall be 4X wide. 2070-2B Faceplate shall be 2X wide. (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)

2. Dark Circles in the C1S Connector denote guide pin locations and open circles denote guide socket locations.

3. Dimension "A" shall be a minimum of 12.7 mm.

4. C1S - M104 Type
   C11S - 37-Pin Circular Plastic Type
   C12S - 25-Pin DB Socket Type

5. C12S Pin 12 +5 VDC is derived from the +12 VDC power supply.

C12S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX5 DATA +	14	TX5 DATA -
2	RX5 DATA +	15	RX5 DATA -
3	TX5 CLOCK +	16	TX5 CLOCK -
4	RX5 CLOCK +	17	RX5 CLOCK -
5	TX3 DATA +	18	TX3 DATA -
6	RX3 DATA +	19	RX3 DATA -
7	TX3 CLOCK +	20	TX3 CLOCK -
8	RX3 CLOCK +	21	RX3 CLOCK -
9	LINE SYNC +	22	LINE SYNC -
10	NRESET +	23	NRESET -
11	POWER DOWN +	24	POWER DOWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

TITLE:

TYPE 2070-2
FIELD I/O MODULES

	NO SCALE	
	NOV 19, 1999	4-7-8

C1S PIN ASSIGNMENT

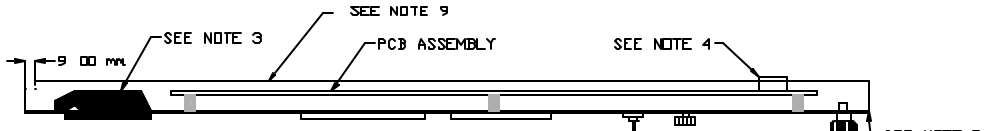
PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION	
	NAME	PORT		NAME	PORT		NAME	PORT		NAME	PORT
1	DC GROUND		27	O24	O4-1	53	I14	I2-7	79	I44	I6-5
2	O0	O1-1	28	O25	O4-2	54	I15	I2-8	80	I45	I6-6
3	O1	O1-2	29	O26	O4-3	55	I16	I3-1	81	I46	I6-7
4	O2	O1-3	30	O27	O4-4	56	I17	I3-2	82	I47	I6-8
5	O3	O1-4	31	O28	O4-5	57	I18	I3-3	83	O40	O6-1
6	O4	O1-5	32	O29	O4-6	58	I19	I3-4	84	O41	O6-2
7	O5	O1-6	33	O30	O4-7	59	I20	I3-5	85	O42	O6-3
8	O6	O1-7	34	O31	O4-8	60	I21	I3-6	86	O43	O6-4
9	O7	O1-8	35	O32	O5-1	61	I22	I3-7	87	O44	O6-5
10	O8	O2-1	36	O33	O5-2	62	I23	I3-8	88	O45	O6-6
11	O9	O2-2	37	O34	O5-3	63	I28	I4-5	89	O46	O6-7
12	O10	O2-3	38	O35	O5-4	64	I29	I4-6	90	O47	O6-8
13	O11	O2-4	39	I0	I1-1	65	I30	I4-7	91	O48	O7-1
14	DC GROUND		40	I1	I1-2	66	I31	I4-8	92	DC GROUND	
15	O12	O2-5	41	I2	I1-3	67	I32	I5-1	93	O49	O7-2
16	O13	O2-6	42	I3	I1-4	68	I33	I5-2	94	O50	O7-3
17	O14	O2-7	43	I4	I1-5	69	I34	I5-3	95	O51	O7-4
18	O15	O2-8	44	I5	I1-6	70	I35	I5-4	96	O52	O7-5
19	O16	O3-1	45	I6	I1-7	71	I36	I5-5	97	O53	O7-6
20	O17	O3-2	46	I7	I1-8	72	I37	I5-6	98	O54	O7-7
21	O18	O3-3	47	I8	I2-1	73	I38	I5-7	99	O55	O7-8
22	O19	O3-4	48	I9	I2-2	74	I39	I5-8	100	O36	O5-5
23	O20	O3-5	49	I10	I2-3	75	I40	I6-1	101	O37	O5-6
24	O21	O3-6	50	I11	I2-4	76	I41	I6-2	102	O38 *	O5-7
25	O22	O3-7	51	I12	I2-5	77	I42	I6-3	103	O39 **	O5-8
26	O23	O3-8	52	I13	I2-6	78	I43	I6-4	104	DC GROUND	

NOTE: * Special application FIO Module DET RESET
** Special application FIO Module WDT

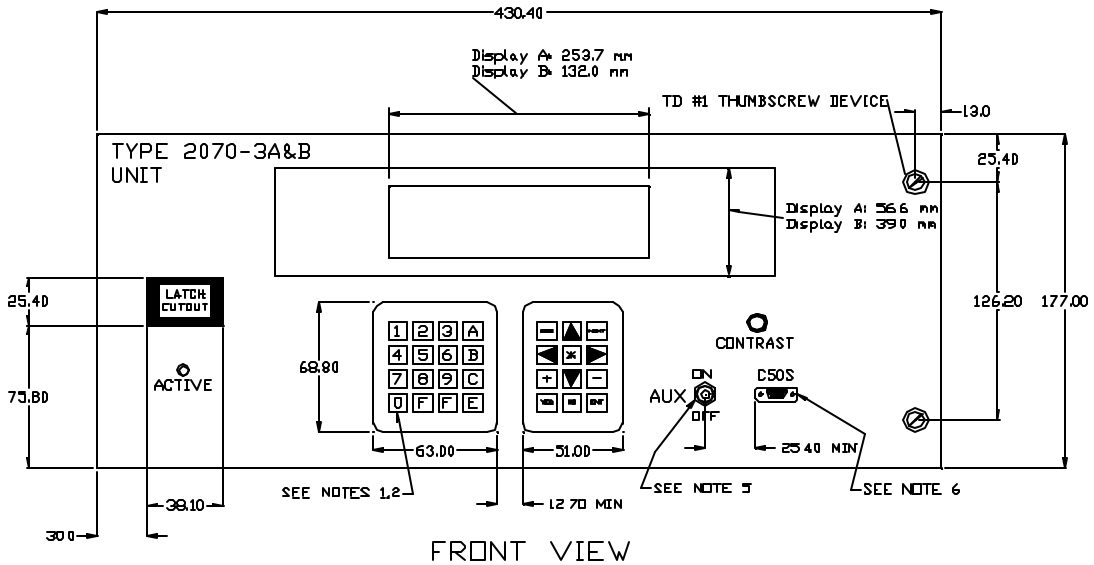
C11S PIN ASSIGNMENT

PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION	
	NAME	PORT		NAME	PORT		NAME	PORT		NAME	PORT
1	O56	O8-1	11	I25	I4-2	21	I54	I7-7	31	DC GROUND	
2	O57	O8-2	12	I26	I4-3	22	I55	I7-8	32	NA	- - -
3	O58	O8-3	13	I27	I4-4	23	I56	I8-1	33	NA	- - -
4	O59	O8-4	14	DC GROUND		24	I57	I8-2	34	NA	- - -
5	O60	O8-5	15	I48	I7-1	25	I58	I8-3	35	NA	- - -
6	O61	O8-6	16	I49	I7-2	26	I59	I8-4	36	NA	- - -
7	O62	O8-7	17	I50	I7-3	27	I60	I8-5	37	DC GROUND	
8	O63	O8-8	18	I51	I7-4	28	I61	I8-6			
9	DC GROUND		19	I52	I7-5	29	I62	I8-7			
10	I24	I4-1	20	I53	I7-6	30	I63	I8-8			

	TITLE: TYPE 2070-2A FIELD I/O MODULE C1 & C11 CONNECTORS	
	NO SCALE	
	JANUARY 26, 2001	4-7-9



TOP VIEW



FRONT VIEW

NOTES (THIS DETAIL)

1. Key size shall be 7.62 X 7.62.
2. Key center to center spacing shall be 12.70 mm.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. 40 contact FP harness pin header connector. It shall be compatible to the FP harness in type and pin assignments. The center of the FP Harness Pin Header shall be vertically positioned between 85 and 95 MM as measured from the top of the FPA
5. Two position CONTROL switch mounted vertically.
6. 'C50S' connector shall be a DB-9 socket contact connector.
7. Fron panel sheet metal thickness shall be 1.52 ±0.13.
8. All FPA devices shall be located as shown.
9. The FPA shall be provided with a continuous top and bottom 17 mm lip bent 90 degrees to the front plate and shall extend the full length of the FPA.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 - ENABLE
2	SP4 RX
3	SP4 TX
4	NA
5	DC GROUND #1
6	NA
7	NA
8	NA
9	NA

C60S CONNECTOR PINOUTS	
PIN	FUNCTION
1	NA
2	SP6 RX
3	SP6 TX
4	NA
5	DC GROUND #1
6	NA
7	CPU RESET
8	NA
9	CPU LED

TITLE:

TYPE 2070-3A&B FRONT PANEL ASSEMBLY

	NOV 19, 1999	4-7-10

TYPE 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

TYPE 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	OD

	TITLE: TYPE 2070-3 FRONT PANEL ASSEMBLY KEY CODES	
	NO SCALE	
	NOV 19, 1999	4-7-11

CONFIGURATION COMMAND CODES

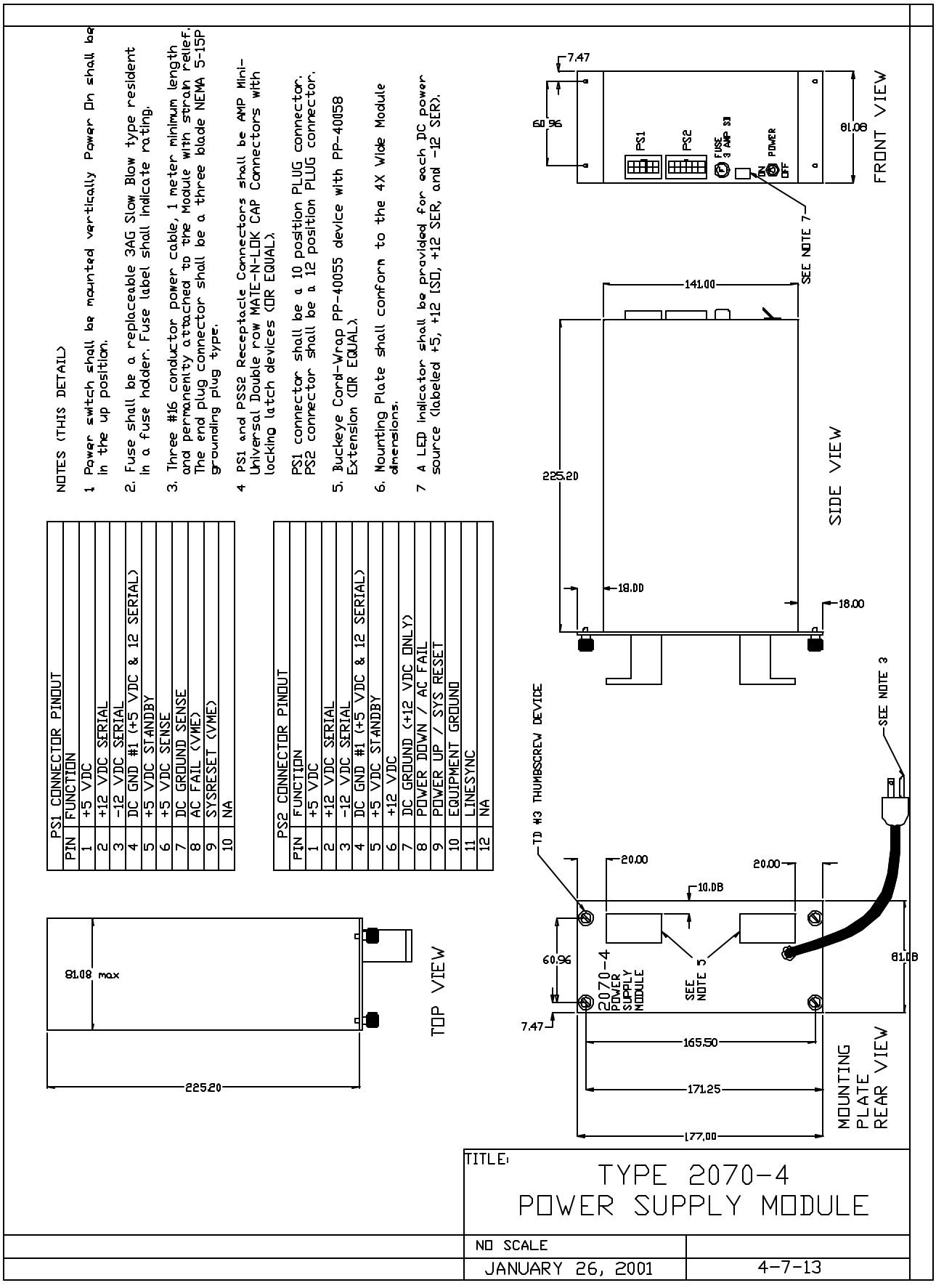
ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn..f	1B 50 P1 5B Pn 3B..Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 3 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 3 l	1B 3B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on (Note 2)
ESC [27 l	1B 5B 32 37 6C	Reverse video off (Note 2)
ESC [24 h	1B 5B 32 34 68	Underline on (Note 2)
ESC [24 l	1B 5B 32 34 6C	Underline off (Note 2)
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Clear tab stop Pn = 0,1,2 at cursor = 3 all tab stops
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

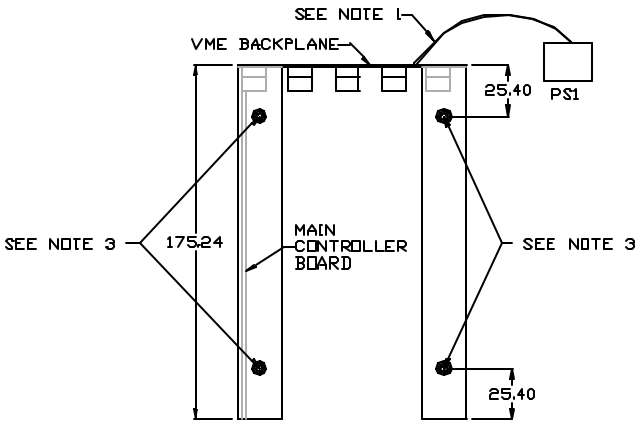
NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A.
Reverse Video is NOT required for Option 3B. Command codes shall be available for option 3C (C60).

INQUIRY COMMAND-RESPONSE CODES

COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [9 n	1B 5B 42 6E	ESC [P1,P2,...P6 R	1B 5B P1 3B P2 3B P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

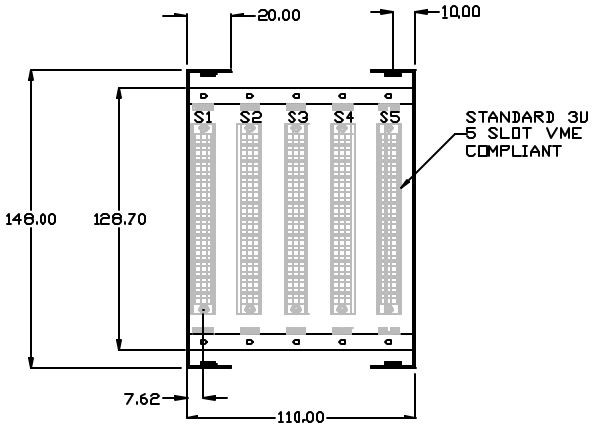
TITLE: TYPE 2070-3 FRONT PANEL ASSEMBLY KEY CODES		
	NO SCALE	
	NOV 19, 1999	4-7-12


NOTES (THIS DETAIL)
1 Power switch shall be mounted vertically. Power On shall be in the up position.
2. Fuse shall be a replaceable 3AG Slow Blow type resident in a fuse holder. Fuse label shall indicate rating.
3. Three #16 conductor power cable, 1 meter minimum length and permanently attached to the Module with strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug type.
4 PS1 and PS2 Receptacle Connectors shall be AMP Mini-Universal Double row MATE-N-LOK CAP Connectors with locking latch devices (OR EQUAL).
PS1 connector shall be a 10 position PLUG connector.
PS2 connector shall be a 12 position PLUG connector.
5. Buckeye Cord-Wrap PP-40055 device with PP-40058 Extension (OR EQUAL).
6. Mounting Plate shall conform to the 4X Wide Module dimensions.
7 A LED indicator shall be provided for each DC power source (labeled +5, +12 ISO, +12 SER, and -12 SER).
PS1 CONNECTOR PINOUT
PIN FUNCTION
1 +5 VDC
2 +12 VDC SERIAL
3 -12 VDC SERIAL
4 DC GND #1 (+5 VDC & 12 SERIAL)
5 +5 VDC STANDBY
6 +5 VDC SENSE
7 DC GROUND SENSE
8 AC FAIL (VME)
9 SYSRESET (VME)
10 NA
PS2 CONNECTOR PINOUT
PIN FUNCTION
1 +5 VDC
2 +12 VDC SERIAL
3 -12 VDC SERIAL
4 DC GND #1 (+5 VDC & 12 SERIAL)
5 +5 VDC STANDBY
6 +12 VDC
7 DC GROUND (+12 VDC ONLY)
8 POWER DOWN / AC FAIL
9 POWER UP / SYS RESET
10 EQUIPMENT GROUND
11 LINESYNC
12 NA
81.08 max
225.20
TOP VIEW
7.47
60.96
PS1
PS2
FUSE 3 AMP 3
POWER
ON
OFF
81.08
FRONT VIEW
SEE NOTE 7
141.00
225.20
18.00
18.00
SIDE VIEW
SEE NOTE 3
TO #3 THUMBSCREW DEVICE
20.00
20.00
10.08
60.96
2070-4 POWER SUPPLY MODULE
SEE NOTE 5
81.08
7.47
165.50
171.25
177.00
MOUNTING PLATE REAR VIEW
TITLE:
TYPE 2070-4
POWER SUPPLY MODULE
NO SCALE
JANUARY 26, 2001
4-7-13



TOP VIEW

PS1 CONNECTOR PIN ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA



FRONT VIEW

NOTES (THIS DETAIL)

1. PS1 Harness interfaces between the Type 2070-4 Power Supply Module and the 2070-5 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, FASTON or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.

2. The plate shall cover the open area and attach to the Chassis Backplane mounting surface via screws meeting the Chapter 1 external screw requirements. The screws shall mate with the PEM nuts as specified in the Type 2070 Chassis Top View Detail.

3. 6-32 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 Phillips screws on the top and bottom of the Type 2070 chassis.

TITLE: TYPE 2070-5 VME CAGE ASSEMBLY		
	NO SCALE	
	NOV 19, 1999	4-7-14

5 TYPE 2070 PERIPHERAL EQUIPMENT AND NEMA MODULE

GENERAL NOTES:

1. The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA-232 control lines (TX, RX, RTS, CTS, and DCD) when a ground true state is present at Connector A1, Pin B21 (C50 Enable). The disable lines shall be pulled up on this module

2. Line drivers/receivers shall be socket mounted.

3. Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each modules's circuit shall be capable of reliably passing a minimum of 1.0 Mbps.

4. The Comm modules shall be "Hot" swappable without damage to circuitry or operations.

5.1 Type 2070-6 A & B Async/Modem Serial Comm Modules

5.1.1 Power Requirements

A fused isolated +5 VDC with a minimum of 100 mA power supply shall be provided for external use.

5.1.2 Circuitry

Two circuits, designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and C2S Connector and CIRCUIT #2 to SP2 [or SP4] and C20S Connector).

5.1.2.1

The Circuits shall convert the 2070 UNIT Motherboard SP EIA-485 signals to/from board TTL level signals, isolate and drive the converted EIA-232 Signals interfacing with their associated MODEM and external connector.

5.1.3 Modem Requirements

Each CIRCUIT shall have a MODEM with the following requirements:

1. Data Rate: Baud modulation of 300 to 1200 for Module 2070-6A and 0 to 9600 for Module 2070-6B.

2. Modulation: Phase coherent frequency shift keying (FSK).
3. Data Format: Asynchronous, serial by bit.
4. Line & Signal Requirements: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive):2070-6A - 1.2 KHz MARK and 2.2 KHz SPACE, ±1% tolerance. 2070-6B - 11.2 KHz MARK and 17.6 KHz SPACE, ±1% tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz & .4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.
5. Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A & 14.7 KHz for 2070-6B) continuous or switch selectable.
6. Receiver Input Sensitivity: 0 to -40 dB.
7. Receiver Bandpass Filter: Shall meet the error rate requirement specified below and shall provide 20 dB/octave, minimum active attenuation for all frequencies outside the operating band.
8. Clear-to-Send (CTS) Delay: 11 ±3 ms.
9. Receive Line Signal Detect Time: 8 ±2 ms mark frequency.
10. Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).
11. Soft Carrier Turn Off Time: 10 ±2 ms (0.9 KHz for 2070-6A and 7.8 KHz for 2070-6B). When the RTS is unasserted , the carrier shall turn off or go to soft carrier frequency.
12. Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.
13. Error Rate: Shall not exceed 1 bit in 100 Kbits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hz band.
14. Transmit Noise: Less than -50 dB across 600-ohms resistive load within the frequency spectrum of 300 to 3,000 Hz at maximum output.
15. Modem interface: EIA-232 Standards.

5.1.4 Logic Switches

Two LOGIC switches per circuit shall be provided (faceplate mounted).

5.1.4.1

One shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

5.1.4.2

A MODEM Enable switch shall be provided that when in the UP Position shall enable MODEM and disable MODEM in the DOWN Position.

5.1.5 Control Switch

A CONTROL switch shall be provided on the module front panel to turn ON (Up) / OFF (Down) all module power.

5.2 Type 2070-7A & 7B Async Serial Comm Module

5.2.1 Circuitry

Two circuits, designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and Connector C21S and CIRCUIT #2 to SP2 [or SP4] and Connector C22S).

5.2.2 2070 -7A

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Connectors shall be DB-9S type.

5.2.3 2070 - 7B

Each circuit EIA -485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground shall be board terminated to matching drivers/receivers; isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors. Connectors shall be DB-15S type.

5.2.4 Indicators

Each circuit signal TX and RX line shall have an LED Indicator mounted on the front plate and labeled to function.

5.3 Reserved for Future Use

This section is reserved for future communication module requirements.

5.4 Type 2070N Controller Unit

5.4.1 General

5.4.1.1

The Type 2070-8 NEMA Interface Module Chassis and 2070N Back Cover shall be made of 1.524 mm minimum aluminum sheet and treated with clear chromate. All

external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel. The matching nuts shall be permanently captive on the mating surfaces.

5.4.1.2

Deleted

5.4.2 Type 2070-8 NEMA Interface Module

5.4.2.1

The Module shall consist of the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors.

5.4.2.2

The Module Front Panel shall be furnished with the following:

1. ON/OFF POWER Switch mounted vertically with ON in the UP position.
2. LED DC Power Indicator. The indicator shall indicate that the required + 5 VDC is within 5% and the +24 VDC is within 8%.
3. Incoming VAC fuse protection.
4. Two DB-25S COMM connectors labeled "EX1" & "EX2."
5. Four NEMA Connectors A, B, C, & D-style.

5.4.2.3

A MODULE POWER SUPPLY shall be provided and located on the right side of the module as viewed from the front. The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control. The supply shall meet the following requirements:

5.4.2.3.1

See previous specifications for INPUT PROTECTION in previous chapter.

5.4.2.3.2

See previous specifications for POWER SUPPLY REQUIREMENTS in previous chapter excepting Voltage/Current Table.

5.4.2.3.3

DC Voltage tolerances shall be ±3 %.

5.4.2.4

The supplied incoming AC Power shall be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral). External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN."

5.4.2.5

AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.

5.4.2.6

A MODULE PC Boards shall be mounted vertically.

5.4.2.7

Power Down, NRESET, and LINESYNC shall be routed to the module via C12 Connector. The state of the module output ports at the time of Power Down transition to LOW State and until NRESET goes HIGH shall be an open circuit.

5.4.2.8

The Type 2070-8 NEMA Interface Module shall meet all requirements under previous sections on Parallel I/O Ports with the following exceptions:

5.4.2.8.1 Parallel Ports

118 Bits of Input and 102 bits of Output shall be provided. Previous sections on Parallel I/O Ports applies except the voltage is +24 in lieu of +12 and for inputs the Logic "0" occurs when the input voltage exceeds 16.0 VDC.

5.4.2.8.2 Serial Communications Circuitry

The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. All signal lines shall be isolated. HAR 1 Harness shall be 17 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to the Controller interface, the EIA-485 Signal lines shall be routed to EX1 Connector. All necessary driver/receiver and isolation circuitry shall be provided.

5.4.2.9

An EIA-232 Serial Port shall be provided with rate selection by jumper of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 Kbps asynchronous and shall be connected at EX1 Connector.

5.4.2.10

A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Type 2070-6 Serial COMM Module in the 2070 UNIT. This provides two Modems or EIA-232 Interfaces with the 2070 UNIT and the outside world.

5.4.2.11 Fault and Voltage Monitor Circuitry

NEMA TS1 and TS2 Controller FAULT and VOLTAGE MONITOR functions (outputs to cabinet monitor) shall be provided.

5.4.2.11.1

Two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (FAULT MONITOR) and gate 2 output shall be connected to Connector A, Pin C. Any FALSE state input shall cause a gate output FALSE (+24VDC) state.

5.4.2.11.2

The FCU Port 10, Bit 7 output shall normally change its state every 100 ms. A MODULE Watchdog (WDT) circuit shall monitor the output. No state change for 2 ±0.1 seconds shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the WDT output shall return to TRUE (0 VDC) state.

5.4.2.11.3

The module shall have a +5 VDC monitoring circuit which monitors the module's +5 VDC (±0.25). If the voltage exceeds the limits, the circuit output shall generate a FALSE output (input to gates 1 and 2). Normal operation shall return the output state to TRUE state.

5.4.2.11.4

The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).

5.4.2.11.5

CPU Port 5 SET OUTPUT COMMAND Message OUTPUTs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state "1" shall be FCU output FALSE.

5.4.2.11.6

CPU / FCU operation at POWER UP shall be as follows:

1. FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.
2. CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and responses to CPU with "E" bit set.
3. Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to "0" will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.
4. If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.
5. This is operational and preceded User Software.

5.4.2.11.7

A CPU / FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm Loss Flag. FM and VM outputs shall be in FALSE state.

5.4.3 Type 2070N Back Cover

The 2070N Back Cover shall be provided to protect the interface harnesses. The Back Cover shall be delivered attached to the 2070 ATMS Controller Unit and 2070-8 NEMA Interface Module per Section 5.

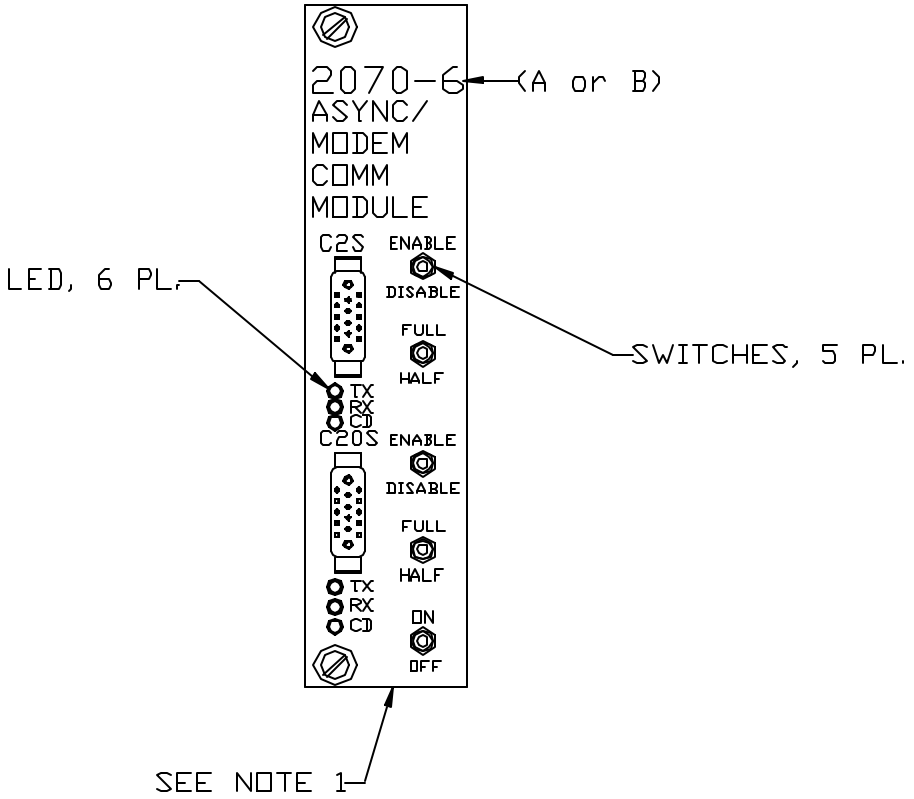
5.5 Chapter Details

TABLE OF CONTENTS

Section Notes:

All dimensions are in millimeters.

Module sheet metal tolerance shall be 0.38 mm or less.



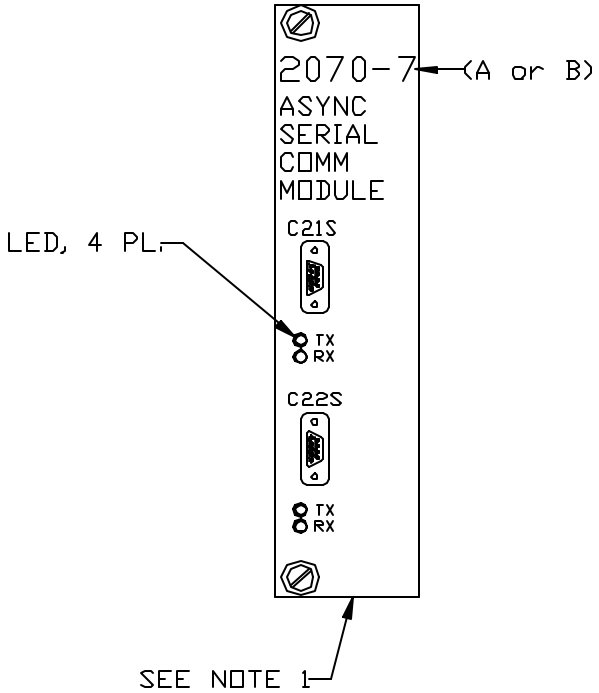
C2 & C20 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	DATA IN
C	AUDIO OUT	L	DATA OUT
D	ISO +5 VDC	M	CTS
E	AUDIO OUT	N	ISO DC GND
F	NA	P	NA
H	CD	R	NA

NOTES (THIS DETAIL)

1. 2X Faceplate (See System PCB Module, General Details).

2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.

TITLE: TYPE 2070-6A, 6B ASYNC/MODEM SERIAL COMM MODULE	
NO SCALE	
NOV 19, 1999	5-5-1



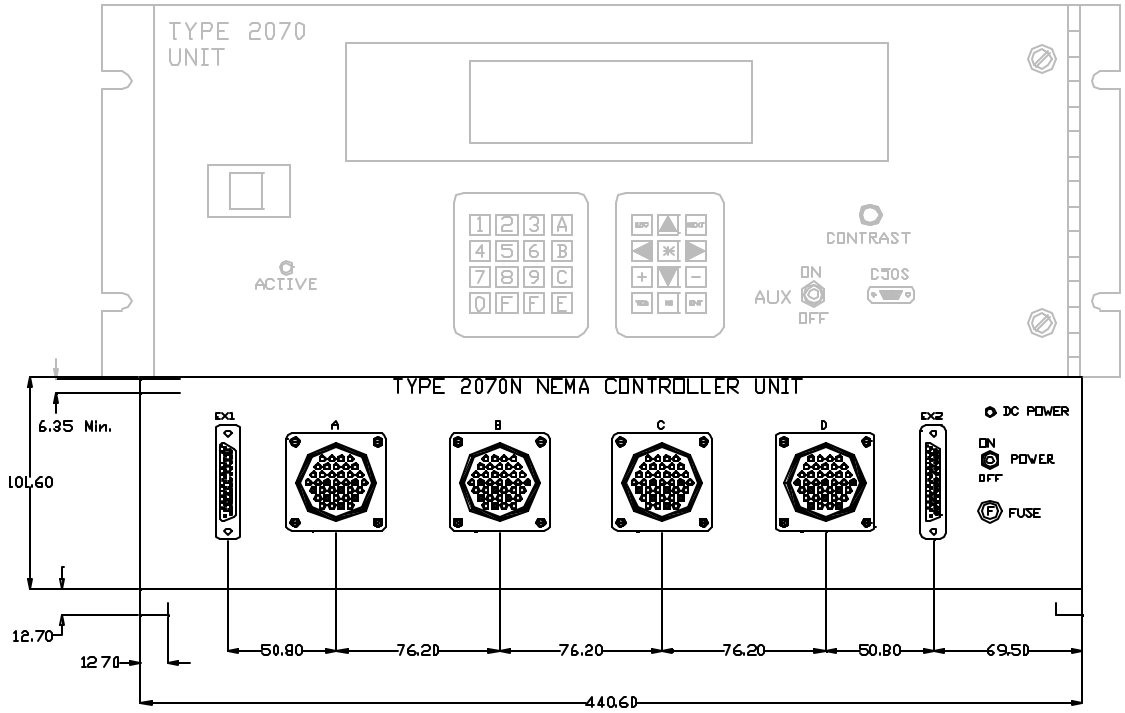
2070-7A (DB-9S)	
C21 & C22 CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	ISO DC GND
6	NA
7	RTS
8	CTS
9	NA

2070-7B (DB-15S)			
C21 & C22 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA +	9	TX DATA -
2	ISO DC GND	10	ISO DC GND
3	TX CLOCK +	11	TX CLOCK -
4	ISO DC GND	12	ISO DC GND
5	RX DATA +	13	RX DATA -
6	ISO DC GND	14	ISO DC GND
7	RX CLOCK +	15	RX CLOCK -
8	NA		

NOTES (THIS DETAIL)

1. 2X Faceplate (See System PCB Module, General Details).

TITLE: TYPE 2070-7A, 7B SERIAL COMM MODULE		
	NO SCALE	
	NOV 19, 1999	5-5-2



NOTES (THIS DETAIL)

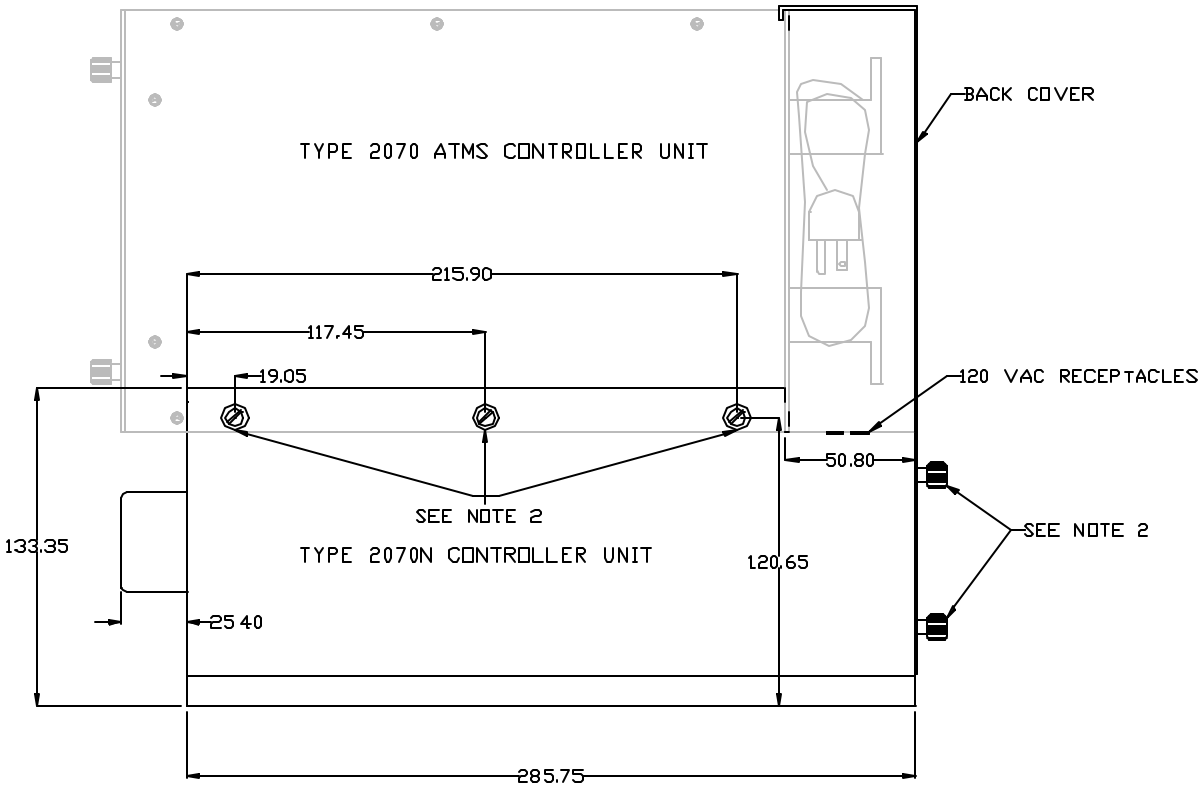
1. The Type 2070 Controller Unit is shown only for refernce.

2. The bottom supports shall be double flanged.

3. A = Connector A (MS-3112-22-55P Type)
   B = Connector B (MS-3112-22-55S Type)
   C = Connector C (MS-3112-24-61S Type)
   D = Connector D (MS-3112-24-61P Type)
   EX1 = Connector EX1 (DB-25S Type)
   EX2 = Connector EX2 (DB-25S Type)

4. 2.286 mm wide spacers shall be provided between the inside wall of the 2070-8 Module and the 2070 unit (each side).

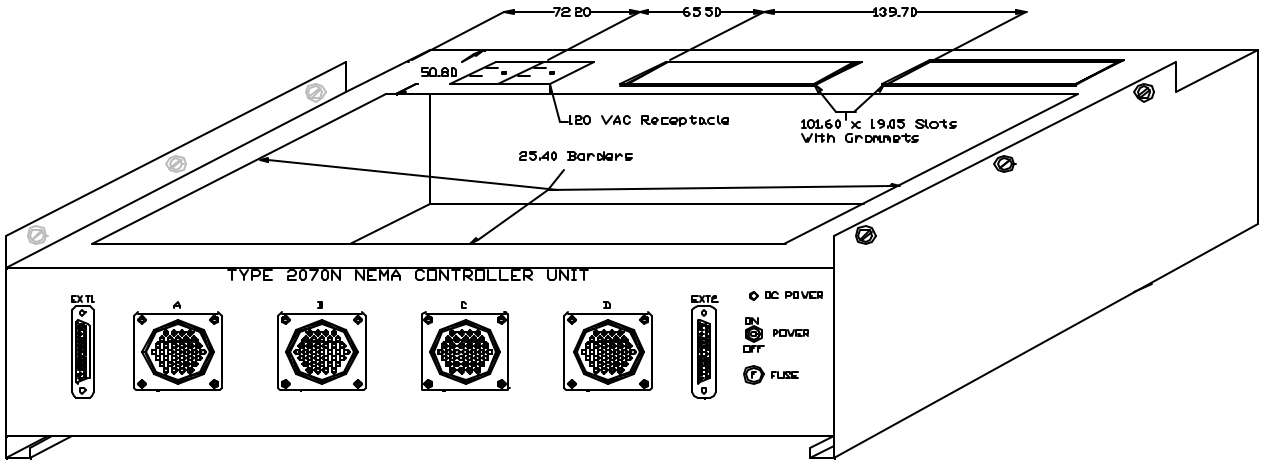
	TITLE: 2070N CONTROLLER UNIT FRONT VIEW	
	NO SCALE	
	NOV 19, 1999	5-5-3



NOTES (THIS DETAIL)

1. The Type 2070 Controller Unit is shown only for reference.
2. TDS #3 Thumbscrew Devices. Module shall provide mating nuts permanently mounted on the module.

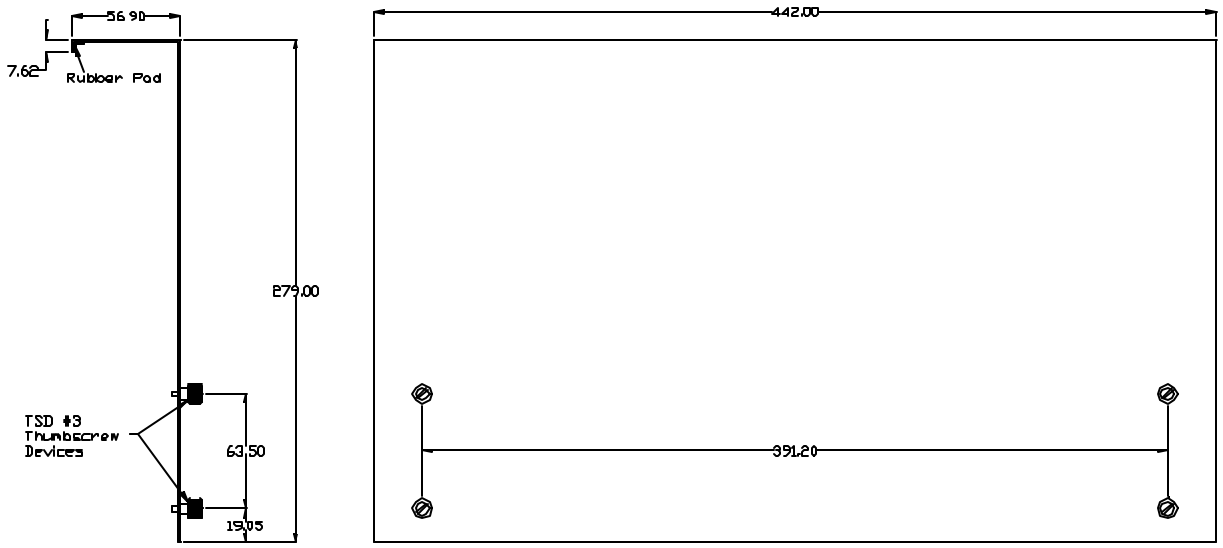
	TITLE: 2070N CONTROLLER UNIT SIDE VIEW	
	NO SCALE	
	NOV 19, 1999	5-5-4



NOTES (THIS DETAIL)

1. The module housing bottom shall be slot vented. The top shall be open.

	TITLE: 2070N CONTROLLER UNIT ISOMETRIC VIEW	
	NO SCALE	
	NOV 19, 1999	5-5-5



SIDE VIEW

REAR VIEW

NOTES (THIS DETAIL)

1. The overhang lip shall be notched 19.05 mm on each side.

	TITLE: 2070N CONTROLLER UNIT BACK COVER	
	NO SCALE	
	NOV 19, 1999	5-5-6

	CONNECTOR A			CONNECTOR B		
PIN	FUNCTION	I/O	PORT-BIT	FUNCTION	I/O	PORT-BIT
A	Fault Monitor	---	---	Phase 1 Next	Out	8-1
B	+24 VDC External	---	---	Reserved	In	9-5
C	Voltage Monitor	---	---	Phase 2 Next	Out	8-2
D	Phase 1 Red	Out	1-1	Phase 3 Green	Out	3-3
E	Phase 1 Don't Walk	Out	4-1	Phase 3 Yellow	Out	2-3
F	Phase 2 Red	Out	1-2	Phase 3 Red	Out	1-3
G	Phase 2 Don't Walk	Out	4-2	Phase 4 Red	Out	1-4
H	Phase 2 Ped Clear	Out	5-2	Phase 4 Ped Clear	Out	5-4
J	Phase 2 Walk	Out	6-2	Phase 4 Don't Walk	Out	4-4
K	Phase 2 Vehicle Detector	In	1-2	Phase 4 Check	Out	7-4
L	Phase 2 Pedestrian Detector	In	2-2	Phase 4 Vehicle Detector	In	1-4
M	Phase 2 Hold	In	3-2	Phase 4 Pedestrian Detector	In	2-4
N	Stop Timing (Ring 1)	In	6-2	Phase 3 Vehicle Detector	In	1-3
P	Inh Max Term (Ring 1)	In	6-3	Phase 3 Pedestrian Detector	In	2-3
R	External Start	In	8-1	Phase 3 Omit	In	5-3
S	Interval Advance	In	8-2	Phase 2 Omit	In	5-2
T	Indicator Lamp Control	In	8-3	Phase 5 Ped Omit	In	4-5
U	AC Neutral	---	---	Phase 1 Omit	In	5-1
V	Chassis Ground	---	---	Ped Recycle (Ring 2)	In	7-5
W	2070N DC Ground	---	---	Reserved	In	9-6
X	Flashing Logic Out	Out	11-7	Reserved	In	9-7
Y	Coded Status Bit C (Ring 1)	Out	12-3	Phase 3 Walk	Out	6-3
Z	Phase 1 Yellow	Out	2-1	Phase 3 Ped Clear	Out	5-3
a	Phase 1 Ped Clear	Out	5-1	Phase 3 Don't Walk	Out	4-3
b	Phase 2 Yellow	Out	2-2	Phase 4 Green	Out	3-4
c	Phase 2 Green	Out	3-2	Phase 4 Yellow	Out	2-4
d	Phase 2 Check	Out	7-2	Phase 4 Walk	Out	6-4
e	Phase 2 On	Out	9-2	Phase 4 On	Out	9-4
f	Phase 1 Vehicle Detector	In	1-1	Phase 4 Next	Out	8-4
g	Phase 1 Pedestrian Detector	In	2-1	Phase 4 Omit	In	5-4
h	Phase 1 Hold	In	3-1	Phase 4 Hold	In	3-4
i	Force Off (Ring 1)	In	6-1	Phase 3 Hold	In	3-3
j	Min Recall All Phases	In	8-4	Phase 3 Ped Omit	In	4-3
k	Manual Control Enable	In	8-5	Phase 6 Ped Omit	In	4-6
m	Call To Non-Actuated I	In	6-8	Phase 7 Ped Omit	In	4-7
n	Test Input A	In	9-1	Phase 8 Ped Omit	In	4-8
p	AC Power	---	---	Overlap A Yellow	Out	10-2
q	I/O Mode Bit A	In	8-6	Overlap A Red	Out	10-3
r	Coded Status Bit B (Ring 1)	Out	12-2	Phase 3 Check	Out	7-3
s	Phase 1 Green	Out	3-1	Phase 3 On	Out	9-3
t	Phase 1 Walk	Out	6-1	Phase 3 Next	Out	8-3
u	Phase 1 Check	Out	7-1	Overlap D Red	Out	11-6
v	Phase 2 Ped Omit	In	4-2	Reserved	In	9-8
w	Omit All-Red Clear (Phase 1)	In	6-7	Overlap D Green	Out	11-4
x	Red Rest Mode (Ring 1)	In	6-4	Phase 4 Ped Omit	In	4-4
y	I/O Mode Bit B	In	8-7	Not Assigned	---	---
z	Call To Non-Actuated II	In	7-8	Max II Selection (Ring 2)	In	7-6
AA	Test Input B	In	9-2	Overlap A Green	Out	10-1
BB	Walk Rest Modifier	In	9-4	Overlap B Yellow	Out	10-5
CC	Coded Status Bit A (Ring 1)	Out	12-1	Overlap B Red	Out	10-6
DD	Phase 1 On	Out	9-1	Overlap C Red	Out	11-3
EE	Phase 1 Ped Omit	In	4-1	Overlap D Yellow	Out	11-5
FF	Pedestrian Recycle (Ring 1)	In	6-5	Overlap C Green	Out	11-1
GG	Max II Selection (Ring 1)	In	6-6	Overlap B Green	Out	10-4
HH	I/O Mode Bit C	In	8-8	Overlap C Yellow	Out	11-2

TITLE:
NEMA INTERFACE I/O PORT CONNECTORS A & B

NO SCALE

NOV 19, 1999

5-5-7

	CONNECTOR C			CONNECTOR D		
PIN	FUNCTION	I/O	PORT-BIT	FUNCTION	I/O	PORT-BIT
A	Coded Status Bit A (Ring 2)	Out	12-4	Detector 9	In	10-1
B	Coded Status Bit B (Ring 2)	Out	12-5	Detector 10	In	10-2
C	Phase 8 Don't Walk	Out	4-8	Detector 11	In	10-3
D	Phase 8 Red	Out	1-8	Detector 12	In	10-4
E	Phase 7 Yellow	Out	2-7	Detector 13	In	10-5
F	Phase 7 Red	Out	1-7	Detector 14	In	10-6
G	Phase 6 Red	Out	1-6	Detector 15	In	10-7
H	Phase 3 Red	Out	1-3	Detector 16	In	10-8
J	Phase 5 Yellow	Out	2-5	Detector 17	In	11-1
K	Phase 5 Ped Clear	Out	5-5	Detector 18	In	11-2
L	Phase 5 Don't Walk	Out	4-5	Detector 19	In	11-3
M	Phase 5 Next	Out	8-5	Detector 20	In	11-4
N	Phase 3 On	Out	9-3	Detector 21	In	11-5
P	Phase 5 Vehicle Detector	In	1-5	Detector 22	In	11-6
R	Phase 5 Pedestrian Detector	In	2-5	Detector 23	In	11-7
S	Phase 6 Vehicle Detector	In	1-6	Detector 24	In	11-8
T	Phase 6 Pedestrian Detector	In	2-6	Clock Update	In	12-1
U	Phase 7 Pedestrian Detector	In	2-7	Hardware Control	In	12-2
V	Phase 7 Vehicle Detector	In	1-7	Cycle Advance	In	12-3
W	Phase 8 Pedestrian Detector	In	2-8	Max 3 Selection	In	12-4
X	Phase 8 Hold	In	3-8	Max 4 Selection	In	12-5
Y	Force Off (Ring 2)	In	7-1	Free	In	12-6
Z	Stop Timing (Ring 2)	In	7-2	Not Assigned	In	12-7
a	Inhibit Max Timing (Ring 2)	In	7-3	Not Assigned	In	12-8
b	Test Input C	In	9-3	Alarm 1	In	13-1
c	Coded Status Bit C (Ring 2)	Out	12-6	Alarm 2	In	13-2
d	Phase 8 Walk	Out	6-8	Alarm 3	In	13-3
e	Phase 8 Yellow	Out	2-8	Alarm 4	In	13-4
f	Phase 7 Green	Out	3-7	Alarm 5	In	13-5
g	Phase 6 Green	Out	3-6	Flash In	In	13-6
h	Phase 6 Yellow	Out	2-6	Conflict Monitor Status	In	13-7
i	Phase 5 Green	Out	3-5	Door Ajar	In	13-8
j	Phase 5 Walk	Out	6-5	Special Function 1	In	14-1
k	Phase 5 Check	Out	7-5	Special Function 2	In	14-2
m	Phase 3 Hold	In	3-3	Special Function 3	In	14-3
n	Phase 5 Omit	In	5-5	Special Function 4	In	14-4
p	Phase 6 Hold	In	3-6	Special Function 5	In	14-5
q	Phase 6 Omit	In	5-6	Special Function 6	In	14-6
r	Phase 7 Omit	In	5-7	Special Function 7	In	14-7
s	Phase 8 Omit	In	5-8	Special Function 8	In	14-8
t	Phase 8 Vehicle Detector	In	1-8	Preempt 1 In	In	15-1
u	Red Rest Mode (Ring 2)	In	7-4	Preempt 2 In	In	15-2
v	Omit All Red (Ring 2)	In	7-7	Preempt 3 In	In	15-3
w	Phase 8 Ped Clear	Out	5-8	Preempt 4 In	In	15-4
x	Phase 8 Green	Out	3-8	Preempt 5 In	In	15-5
y	Phase 7 Don't Walk	Out	4-7	Preempt 6 In	In	15-6
z	Phase 6 Don't Walk	Out	4-6	Alarm 1 Out	Out	12-7
AA	Phase 6 Ped Clear	Out	5-6	Alarm 2 Out	Out	12-8
BB	Phase 6 Check	Out	7-6	Special Function 1 Out	Out	13-1
CC	Phase 6 On	Out	9-6	Special Function 2 Out	Out	13-2
DD	Phase 6 Next	Out	8-6	Special Function 3 Out	Out	13-3
EE	Phase 7 Hold	In	3-7	Special Function 4 Out	Out	13-4
FF	Phase 8 Check	Out	7-8	Special Function 5 Out	Out	13-5
GG	Phase 8 On	Out	9-8	Special Function 6 Out	Out	13-6
HH	Phase 8 Next	Out	8-8	Special Function 7 Out	Out	13-7
JJ	Phase 7 Walk	Out	6-7	Special Function 8 Out	Out	13-8
KK	Phase 7 Ped Clear	Out	5-7	Not Assigned	---	---
LL	Phase 6 Walk	Out	6-6	Detector Reset	Out	11-8
MM	Phase 7 Check	Out	7-7	Not Assigned	---	---
NN	Phase 7 On	Out	9-7	+24 VDC	---	---
PP	Phase 7 Next	Out	8-7	2070N DC Gnd	---	---

TITLE:
NEMA INTERFACE I/O PORT CONNECTORS C & D

NO SCALE

NOV 19, 1999

5-5-8

EX1 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD FCU
3	RXD FCU
4	RTS FCU
5	CTS FCU
6	NA
7	2070-8 DC GND
8	DCD FCU
9	2070-8 DC GND
10	485 TX Data+
11	485 TX Data-
12	485 TX Clock+
13	485 TX Clock-
14	2070-8 DC GND
15	485 RX Data+
16	485 RX Data-
17	2070-8 DC GND
18	485 RX Clock+
19	485 RX Clock-
20	NA
21	NA
22	NA
23	NA
24	NA
25	NA

EX2 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD 1
3	RXD 1
4	RTS 1
5	CTS 1
6	NA
7	DC GND #1
8	DCD 1
9	AUDIO IN 1
10	AUDIO IN 1
11	AUDIO OUT 1
12	AUDIO OUT 1
13	NA
14	EQ GND
15	TXD 2
16	RXD 2
17	RTS 2
18	CTS 2
19	NA
20	DC GND #1
21	DCD 2
22	AUDIO IN 2
23	AUDIO IN 2
24	AUDIO OUT 2
25	AUDIO OUT 2

TITLE: 2070-8 NEMA MODULE EX1 & EX2 CONNECTOR PINOUTS

NO SCALE

NOV 19, 1999

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6 GLOSSARY

6.1.1 Terms and Abbreviations

Wherever the following terms or abbreviations are used, the intent and meaning shall be interpreted as follows:

A	-	Ampere
AC	-	Alternating Current
AC+	-	120 Volts AC, 60 hertz ungrounded power source
AC-	-	120 Volts AC, 60 hertz grounded return to the power source
AGENCY	-	The AGENCY director, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them.
ANSI	-	American National Standard Institute
ASCII	-	American Standard Code for Information Interchange
Assembly	-	A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules
ASTM	-	American Society for Testing and Materials
AWG	-	American Wire Gage
C	-	Celsius
C Language	-	The ANSI C Programming Language
Cabinet	-	An outdoor enclosure generally housing the controller unit and associated equipment
Certificate of Compliance	-	A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications

Channel	-	An information path from a discrete input to a discrete output.
Component	-	Any electrical or electronic device
Contractor	-	The person or persons, manufacturer, firm, partnership, corporation, vendor or combination thereof, who have entered into a contract with the AGENCY, as party (s) of the second part or legal representative
Controller Unit	-	That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly
CPU	-	Central Processing Unit
CTS	-	Clear To Send
DAT Program	-	The AGENCY's Diagnostic and Acceptance Test Program
dB	-	Decibel
dBa	-	Decibels above reference noise, adjusted
DC	-	Direct Current
DCD	-	Data Carrier Detect (Receive Line Signal Detector)
DIN	-	Deutsche Industrie Norm
DRAM	-	Dynamic random access memory. Random access means that the processor can access any part of the memory or data storage space directly rather than having to proceed sequentially from some starting place. DRAM is dynamic in that it needs to have its storage cells refreshed or given a new electronic charge every few milliseconds.
EG	-	Equipment Ground
EIA	-	Electronic Industries Association
EMI	-	Electro Magnetic Interference
EPROM	-	Ultraviolet Erasable, Programmable, Read Only Memory Device

EEPROM	-	Electrically Erasable, Programmable, Read Only Memory Device
Equal	-	Connectors: comply to physical dimensions, contact material, plating and method of connection. Devices: comply to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device
ETL	-	Electrical Testing Laboratories, Inc.
Firmware	-	A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM
FLASH	-	A +5 VDC powered IC Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features
FPA	-	Front Panel Assembly
HEX	-	Hexadecimal
Hz	-	Hertz
IC	-	Integrated Circuit
I.D.	-	Identification
IEEE	-	Institute of Electrical and Electronics Engineers
ISO	-	Isolated
Jumper	-	A means of connecting/disconnecting two or more conductive by soldering/desoldering a conductive wire or by PCB post jumper
KB	-	Kilobytes
Keyed	-	Means by which like connectors can be physically altered to prevent improper insertion.
Laboratory	-	The established laboratory of the AGENCY or other laboratories authorized by the AGENCY to test materials involved in the contract

LCD	-	Liquid Crystal Display
LED	-	Light Emitting Diode
LOGIC	-	Negative Logic Convention (Ground True) State
LSB	-	Least Significant Byte
lsb	-	Least Significant Bit
MB	-	MegaByte
MSB	-	Most Significant Byte
msb	-	Most Significant Bit
m	-	Milli
MCU/MPU/ IMP	-	Micro Controller Unit, Microprocessor Unit, or Integrated Multiprotocol Processor
MIL	-	Military Specifications
MODEM	-	Modulation/Demodulation Unit
Module	-	A functional unit that plugs into an assembly
Motherboard	-	A printed circuit connector interface board with no active or passive components
MOS	-	Metal-Oxide Semiconductor
MOV	-	Metal-Oxide Varistor
MS	-	Military Standards
N	-	Newton: SI unit of force
N.C.	-	Normally closed contact
N.O.	-	Normally open contact
NA	-	Presently Not Assigned. Cannot be used by the contractor for other purposes
NEMA	-	National Electrical Manufacturer's Association

NETA	-	National Electrical Testing Association, Inc.
n	-	nano
NLSB	-	Next Least Significant Byte
nlsb	-	Next Least Significant Bit
NMSB	-	Next Most Significant Byte
nmsb	-	Next Most Significant Bit
PCB	-	Printed Circuit Board
PDA	-	Power Distribution Assembly
PLA/PAL	-	Programmable Array Logic Device
Power Failure	-	A Power Failure is said to have occurred when the incoming line voltage falls below 92 +/- 2 VAC for 50 ms. See Power Conditions.
Power Restoration	-	Power is said to be restored when the incoming line voltage equals or exceeds 97 +/- 2 VAC for 50 ms. See Power Conditions.
Power Conditions	-	16.7 ms (one 60 Hz cycle) reaction period is allowed to be included in the 50 ms timing or added to (67 ms duration). The hysteresis between power failure and power restoration voltage settings shall be a min. of 5 VAC with a threshold drift of no more than 0.2 VAC.
ppm	-	Parts per million
PWM	-	Pulse Width Modulation
RAM	-	Random Access Memory
RF	-	Radio Frequency
RMS	-	Root-Mean-Square
ROM	-	Read Only Memory Device

RTS	-	Request to Send
R/W	-	Controller Unit Read/Write Control Line
RxD	-	Received Data
SCI	-	Serial Communications Interface
SDLC	-	Synchronous Data Link Control
S	-	Logic State
s	-	second
Second Sourced	-	Produced by more than one manufacturer
SRAM	-	Static Random Access Memory Device
SW	-	Switch
TB	-	Terminal Block
TOD	-	Time Of Day Clock
Triac	-	Silicon-Controlled Rectifier which controls power bilaterally in an AC switching circuit
TTL	-	Transistor-Transistor Logic
Thumb Screw Device	-	(TSD) A retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish. (TSD No.2 shall be flat black.) TSD No.1 - 8-32 SOUTHCO #47-62-301-20 or equal. TSD No.2 - 8-32 SOUTHCO #47-62-301-60 or equal. TSD No.3 - M3 SOUTHCO #47-82-101-10 or equal.
TxD	-	Transmitted Data
u	-	Micro
UL	-	Underwriter's Laboratories, Inc.
VAC	-	Voltage Alternating Current (root mean square)

VDC	-	Voltage Direct Current
VME	-	Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2
x	-	Number Value
XX	-	Manufacturer's Option
WDT	-	Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts