Introduction

The HIP4081A is a member of the HIP408x family of High Frequency H-Bridge Driver ICs. A simplified application diagram of the HIP4081A IC is shown in Figure 1. The HIP408x family of H-Bridge driver ICs provide the ability to operate from 10VDC to 80VDC busses for driving H-Bridges, whose switch elements are comprised of power N-Channel MOSFETs. The HIP408x family, packaged in both 20 pin DIP and 20 pin SOIC DIPs, provide peak gate current drive of 2.5A. The HIP4081A includes undervoltage protection, which sends a continuous gate turn-off pulse to all gate outputs when the V_{DD} voltage falls below a nominal 8.25V. The startup sequence of the HIP4081A is initiated when the V_{DD} voltage returns above a nominal 8.75V. Of course, the DIS pin must be in the low state for the IC to be enabled. The startup sequence turns on both low side outputs, ALO and BLO, so that the bootstrap capacitors for both sides of the H-bridge can be fully charged. During this time the AHO and BHO gate outputs are held low continuously to insure that no shoot-through can occur during the nominal 400ns boot-strap refresh period. At the end of the boot strap refresh period the outputs respond normally to the state of the input control signals.

A combination of bootstrap and charge-pumping techniques is used to power the circuitry which drives the upper halves of the H-Bridge. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to "maintain" bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin "float" along with the source terminals of the upper power switches, the design of this family provides voltage capability for the upper bias supply terminals to 95VDC.

The HIP4081A can drive lamp loads for automotive and industrial applications as shown in Figure 2. When inductive loads are switched, flyback diodes must be placed around the loads to protect the MOSFET switches.

Many applications utilize the full bridge topology. These are voice coil motor drives, stepper and DC brush motors, audio amplifiers and even power supply inverters used in uninterruptable power supplies, just to name a few. The HIP408x family of devices is fabricated using a proprietary Intersil IC process which allows this family to switch at frequencies over 250kHz. Therefore the HIP408x family is ideal for use in various high frequency converter applications, such as motor drives, switching power amplifiers, and high-performance DC/DC converters. A typical application is shown in Figure 5.
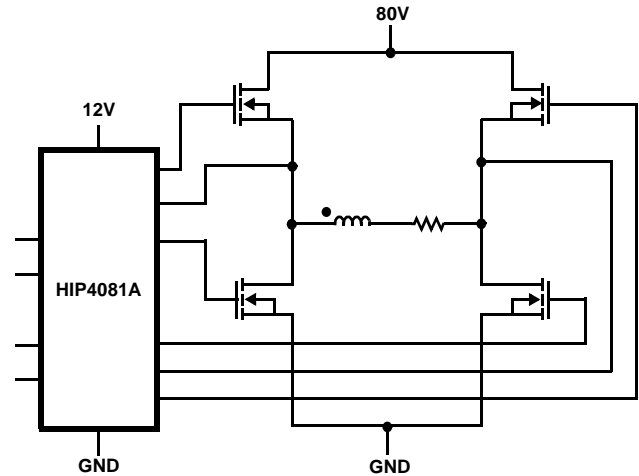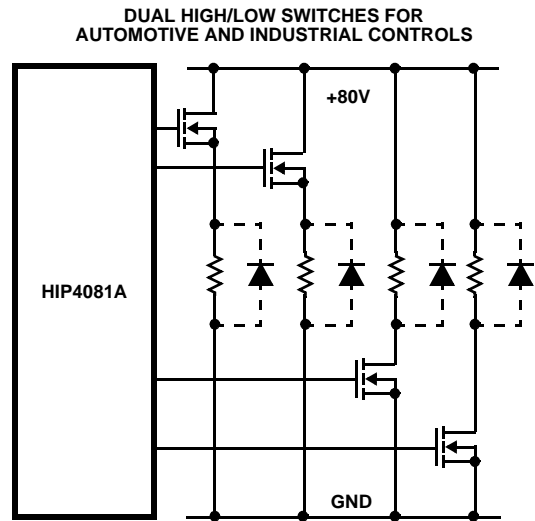

FIGURE 1. HIP4081A SIMPLIFIED APPLICATION DIAGRAM

DUAL HIGH/LOW SWITCHES FOR AUTOMOTIVE AND INDUSTRIAL CONTROLS

FIGURE 2. HIP4081A AS LAMP SWITCH DRIVER

To provide accurate dead-time control for shoot-through avoidance and duty-cycle maximization, two resistors tied to pins HDEL and LDEL provide precise delay matching of upper and lower propagation delays, which are typically only 55ns. The HIP4081A H-Bridge driver has enough voltage margin to meet all SELV (UL classification for operation at £ 42.0V) applications and most Automotive applications where "load dump" capability over 65V is required. This capability makes the HIP408x family a more cost-effective solution for driving N-Channel power MOSFETs than either discrete solutions or other solutions relying on transformer- or opto-coupling gate-drive techniques.

The biggest difference between the HIP4080A and the HIP4081A is that the HIP4081A allows separate and individual control of the 4 MOSFET gates, whereas the HIP4080A does not. Also the HIP4081A does not include an internal comparator which can create a PWM signal directly within the HIP4080A.

Description of the HIP4081A

The block diagram of the HIP4081A relating to driving the A-side of the H-Bridge is shown in Figure 4. The blocks associated with each half of the H-Bridge are identical, so the B-side is not shown for simplicity.

The V_{CC} and V_{DD} terminals on the HIP4081A should be tied together. They were separated within the HIP4081A IC to avoid possible ground loops internal to the IC. Tying them together and providing a decoupling capacitor from the common tie-point to V_{SS} greatly improves noise immunity.

Input Logic

The HIP4081A has 4 inputs, ALI, BLI, AHI and BHI, which control the gate outputs of the H-Bridge. The DIS, "Disable," pin disables gate drive to all H-Bridge MOSFETs regardless of the command states of the input pins above. The state of the bias voltage, V_{DD}, also can disable all gate drive as discussed in the introduction. With external pull-ups on the high input terminals, AHI and BHI, the bridge can be totally controlled using only the lower input control pins, ALI and BLI, which can greatly simplify the external control circuitry needed to control the HIP4081A. As Table 1 suggests, the lower inputs ALI and BLI dominate the upper inputs. That is, when one of the lower inputs is high, it doesn't matter what the level of the upper input is, because the lower will turn on and the upper will remain off.

TABLE 1. INPUT LOGIC TRUTH TABLE

INPUT				OUTPUT	
ALI, BLI	AHI, BHI	U/V	DIS	ALO, BLO	AHO, BHO
X	X	X	1	0	0
1	X	0	0	1	0
0	1	0	0	0	1
0	0	0	0	0	0
X	X	1	X	0	0

NOTE: X signifies that input can be either a "1" or "0".

The input sensitivity of the DIS input pin is best described as "enhanced TTL" levels. Inputs which fall below 1.0V or rise above 2.5V are recognized, respectively, as low level or high level inputs.

Propagation Delay Control

Propagation delay control is a major feature of the HIP4081A. Two identical sub-circuits within the IC delay the commutation of the power MOSFET gate turn-on signals for both A and B sides of the H-Bridge. The gate turn-off signals are not delayed. Propagation delays related to the level-translation function (see section on Level-Translation) cause both upper on/off propagation delays to naturally be longer than the lower on/off propagation delays. Four delay trim sub-circuits are incorporated to better match the H-bridge delays, two for upper delay control and two for lower gate control.

Users can tailor the low side to high side commutation delay times by placing a resistor from the HDEL pin to the V_{SS} pin. Similarly, a resistor connected from LDEL to V_{SS} controls the high side to low side commutation delay times of the lower power switches. The HDEL resistor controls both upper commutation delays and the LDEL resistor controls the lower commutation delays. Each of the resistors sets a current which is inversely proportional to the created delay. The delay is added to the falling edge of the "off" pulse associated with the MOSFET which is being commutated off. When the delay is complete, the "on" pulse is initiated. This has the effect of "delaying" the commanded on pulse by the amount set by the delay, thereby creating dead-time.

Proper choice of resistor values connected from HDEL and LDEL to V_{SS} provides a means for matching the commutation dead times whether commutating high to low or low to high. Values for the resistors ranging from 10kW to 200kW are recommended. Figure 3 shows the dead-time delays obtainable as a function of the resistor values used.
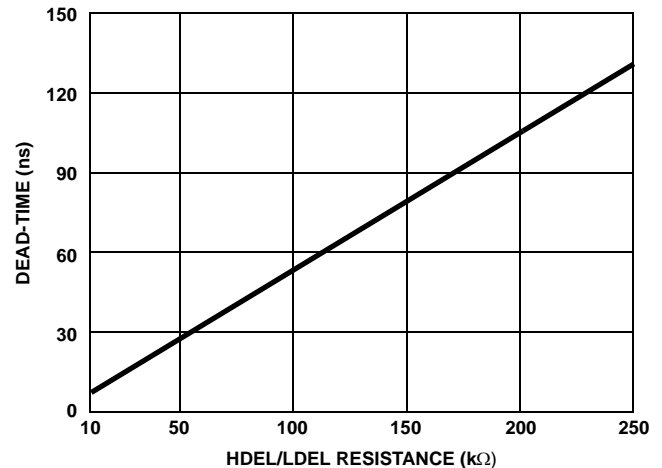

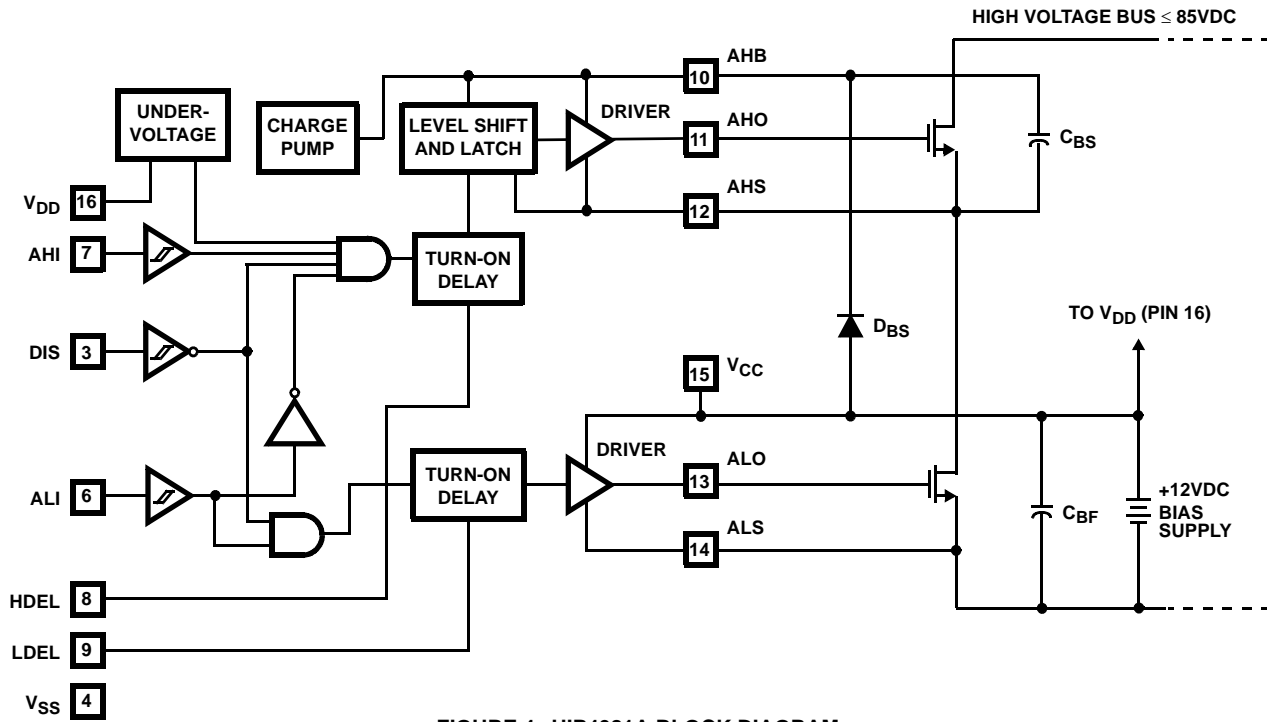**FIGURE 3. MINIMUM DEAD-TIME vs DEL RESISTANCE**

HIGH VOLTAGE BUS ≤ 85VDC

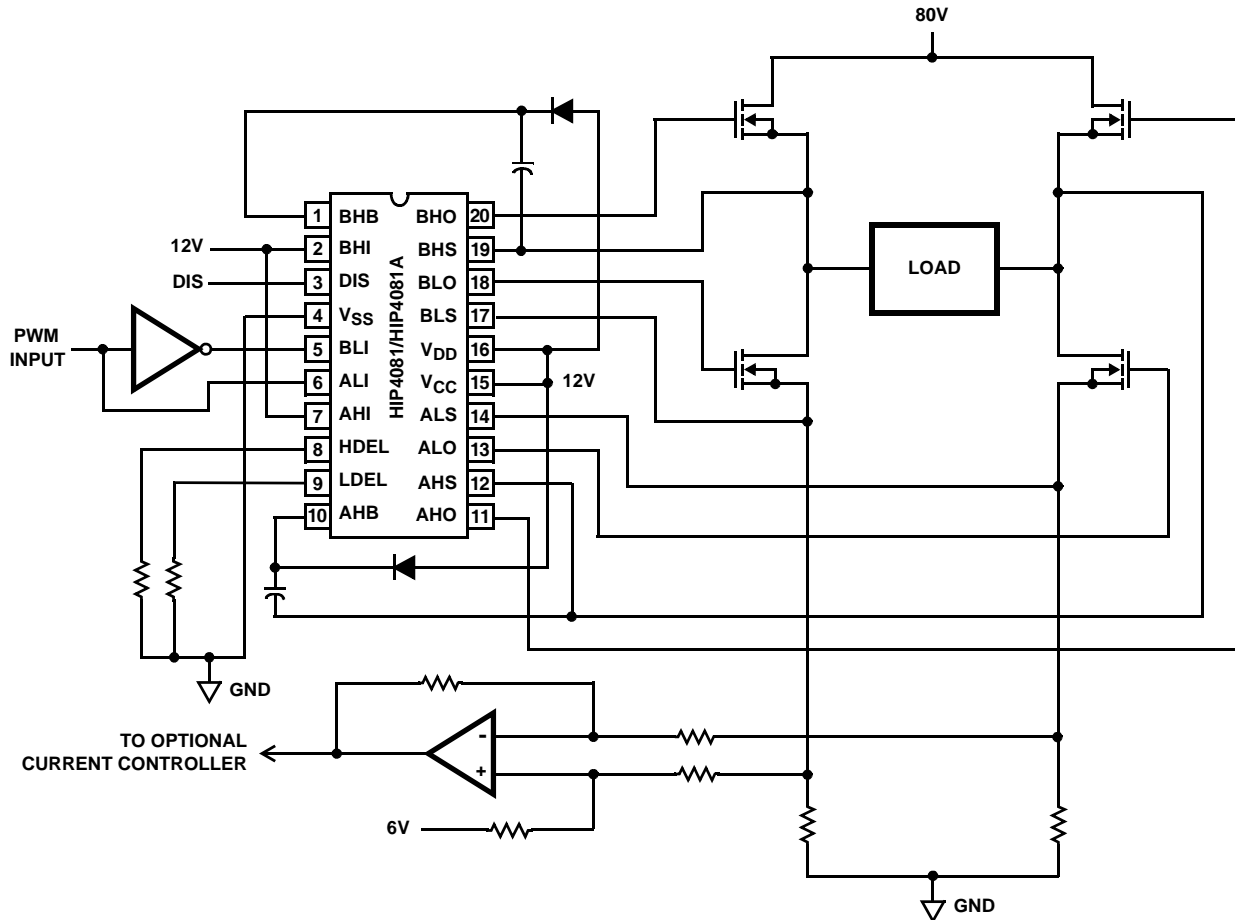
FIGURE 4. HIP4081A BLOCK DIAGRAM

FIGURE 5. TYPICAL APPLICATION (PWM MODE SWITCHING)

Level-Translation

The lower power MOSFET gate drive signals from the propagation delay and control circuits go to amplification circuits which are described in more detail under the section "Driver Circuits". The upper power MOSFET gate drive signals are directed first to the Level-Translation circuits before going to the upper power MOSFET "Driver Circuits".

The Level-Translation circuit communicate "on" and "off" pulses from the Propagation Delay subcircuit to the upper logic and gate drive sub-circuits which "float" at the potential of the upper power MOSFET source connections. This voltage can be as much as 85V when the bias supply voltage is only 10V (the sum of the bias supply voltage and bus voltages must not exceed 95VDC).

In order to minimize power dissipation in the level-shifter circuit, it is important to minimize the width of the pulses translated because the power dissipation is proportional to the product of switching frequency and pulse energy in joules. The pulse energy in turn is equal to the product of the bus voltage magnitude, translation pulse current and translation pulse duration. To provide a reliable, noise free pulse requires a nominal current pulse magnitude of approximately 3mA. The translated pulses are then "latched" to maintain the "on" or "off" state until another level-translation pulse comes along to set the latch to the opposite state. Very reliable operation can be obtained with pulse widths of approximately 80ns. At a switching frequency of even 1.0MHz, with an 80VDC bus potential, the power developed by the level-translation circuit will be less than 0.08W.

Charge Pump Circuits

There are two charge pump circuits in the HIP4081A, one for each of the two upper logic and driver circuits. Each charge pump uses a switched capacitor doubler to provide about 30µA to 50µA of gate load current. The sourcing current charging capability drops off as the floating supply voltage increases. Eventually the gate voltage approaches the level set by an internal zener clamp, which prevents the voltage from exceeding about 15V, the safe gate voltage rating of most commonly available MOSFETs.

Driver Circuits

Each of the four output drivers are comprised of bipolar high speed NPN transistors for both sourcing and sinking gate charge to and from the MOSFET switches. In addition, the sink driver incorporates a parallel-connected N-Channel MOSFET to enable the gate of the power switch gate-source voltage to be brought completely to 0V.

The propagation delays through the gate driver sub-circuits while driving 500pF loads is typically less than 10ns. Nevertheless, the gate driver design nearly eliminates all gate driver shoot-through which significantly reduces IC power dissipation.

Application Considerations

To successfully apply the HIP4081A the designer should address the following concerns:

* General Bias Supply Design Issues

* Upper Bias Supply Circuit Design

* Bootstrap Bias Supply Circuit Design

General Bias Supply Design Issues

The bias supply design is simple. The designer must first establish the desired gate voltage for turning on the power switches. For most power MOSFETs, increasing the gate-source voltage beyond 10V yields little reduction in switch drain-source voltage drop.

Overcharging the power switch's gate-source capacitance also delays turn-off, increases MOSFET gate switching losses and increases the power dissipation of the HIP4081A. Overcharging the MOSFET gate-source capacitance also can lead to "shoot-through" (both upper and lower MOSFETs in a single bridge leg find themselves conducting simultaneously), thereby shorting out the high voltage DC. Bias supply voltages close to 12V are optimum for V_{DD} and V_{CC}, although the HIP4081A will operate up to 15V.

Lower Bias Supply Design

Since most applications use identical MOSFETs for both upper and lower power switches, the bias supply requirements with respect to driving the MOSFET gates will also be identical. In case switching frequencies for driving upper and lower MOSFETs differ, two sets of calculations must be done; one for the upper switches and one for the lower switches. The bias current budget for upper and lower switches will be the sum of each calculation.

Always keep in mind that the lower bias supply must supply current to the upper gate drive and logic circuits as well as the lower gate drive circuits and logic circuits. This is due to the fact that the low side bias supplies (V_{CC}/V_{DD}) charge the bootstrap capacitors and the charge pumps, which maintain voltage across the upper power switch's gate-source terminals.

Good layout practice and capacitor bypassing technique avoids transient voltage dips of the bias power supply to the HIP4081A. Always place a low ESR (equivalent series resistance) ceramic capacitor adjacent to the IC, connected between the bias terminals V_{CC} and V_{DD} and the common terminal, V_{SS} of the IC. A value in the range of 0.22µF and 0.5µF is usually sufficient.

Minimize the effects of Miller feedback by keeping the source and gate return leads from the MOSFETs to the HIP4081A short. This also reduces ringing, by minimizing the length and the inductance of these connections. Another way to minimize inductance in the gate charge/discharge path, in addition to minimizing path length, is to run the outbound gate lead directly "over" the source return lead. Sometimes the source

return leads can be made into a small "ground plane" on the back side of the PC board making it possible to run the outbound gate lead "on top" of the board. This minimizes the "enclosed area" of the loop, thus minimizing inductance in this loop. It also adds some capacitance between gate and source which shunts out some of the Miller feedback effect.

Upper Bias Supply Circuit Design

Before discussing bootstrap circuit design in detail, it is worth mentioning that it is possible to operate the HIP4081A without a bootstrap circuit altogether. Even the bootstrap capacitor, which functions to supply a reservoir of charge for rapidly turning on the MOSFETs is optional in some cases. In situations where very slow turn-on of the MOSFETs is tolerable, one may consider omitting some or all bootstrap components. Applications such as driving relays or lamp loads, where the MOSFETs are switched infrequently and switching losses are low, may provide opportunities for boot strapless operation. Generally, loads with lots of resistance and inductance are possible candidates.

Operating the HIP4081A without a bootstrap diode and/or capacitor will severely slow gate turn-on. Without a bootstrap capacitor, gate current only comes from the internal charge pump. The peak charge pump current is only about 30mA to 50mA. The gate voltage waveform, when operating without a bootstrap capacitor, will appear similar to the dotted line shown in Figure 6.

If a bootstrap capacitor value approximately equal to the equivalent MOSFET gate capacitance is used, the upper bias supply (labeled "bootstrap voltage" in Figure 6) will drop approximately in half when the gate is turned on. The larger the bootstrap capacitance used, the smaller is the instantaneous drop in bootstrap supply voltage when an upper MOSFET is turned on.
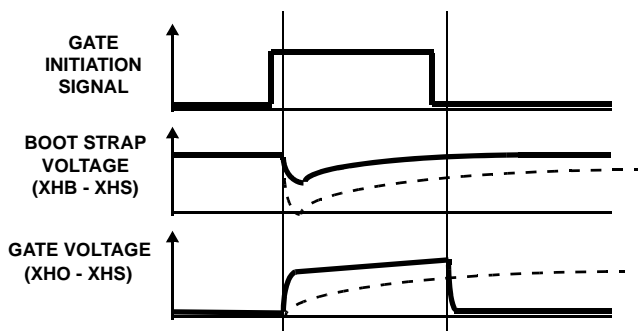

FIGURE 6.

Although not recommended, one may employ a bootstrap capacitor without a bootstrap diode. In this case the charge pump is used to charge up a capacitor whose value should be much larger than the equivalent gate-source capacitance of the driven MOSFET. A value of bootstrap capacitance about 10 times greater than the equivalent MOSFET gate-source capacitance is usually sufficient. Provided that sufficient time elapses before turning on the MOSFET again,

the bootstrap capacitor will have a chance to recharge to the voltage value that the bootstrap capacitor had prior to turning on the MOSFET. Assuming 2W of series resistance is in the bootstrap change path, an output frequency of up to $\dfrac{1}{5 \times 2\Omega \times C_{BS}}$ should allow sufficient refresh time.

A bootstrap capacitor 10 times larger than the equivalent gate-source capacitance of the driven MOSFET prevents the drop in bootstrap supply voltage from exceeding 10% of the bias supply voltage during turn-on of the MOSFET. When operating without the bootstrap diode the time required to replenish the charge on the bootstrap capacitor will be the same time as it would take to charge up the equivalent gate capacitance from 0V. This is because the charge lost on the bootstrap capacitor is exactly equal to the charge transferred to the gate capacitance during turn-on. Note that the very first time that the bootstrap capacitor is charged up, it takes much longer to do so, since the capacitor must be charged from 0V. With a bootstrap diode, the initial charging of the bootstrap supply is almost instantaneous, since the charge required comes from the low-side bias supply. Therefore, before any upper MOSFETs can initially be gated, time must be allowed for the upper bootstrap supply to reach full voltage. Without a bootstrap diode, this initial "charge" time can be excessive.

If the switching cycle is assumed to begin when an upper MOSFET is gated on, then the bootstrap capacitor will undergo a charge withdrawal when the source driver connects it to the equivalent gate-source capacitance of the MOSFET. After this initial "dump" of charge, the quiescent current drain experienced by the bootstrap supply is infinitesimal. In fact, the quiescent supply current is more than offset by the charge pump current.

The charge pump continuously supplies current to the bootstrap supply and eventually would charge the bootstrap capacitor and the MOSFET gate capacitance back to its initial value prior to the beginning of the switching cycle. The problem is that "eventually" may not be fast enough when the switching frequency is greater than a few hundred Hz.

Bootstrap Bias Supply Circuit Design

For high frequency applications all bootstrap components, both diodes and capacitors, are required. Therefore, one must be familiar with bootstrap capacitor sizing and proper choice of bootstrap diode.

Just after the switch cycle begins and the charge transfer from the bootstrap capacitor to the gate capacitance is complete, the voltage on the bootstrap capacitor is the lowest that it will ever be during the switch cycle. The charge lost on the bootstrap capacitor will be very nearly equal to the charge transferred to the equivalent gate-source capacitance of the MOSFET as shown in Equation 1.

$$Q_G = (V_{BS1} - V_{BS2}) \times C_{BS} \qquad \text{(EQ. 1)}$$

where:

V$_{BS1}$ = Bootstrap capacitor voltage just after refresh

V$_{BS2}$ = Bootstrap voltage immediately after upper turn-on

C$_{BS}$ = Bootstrap Capacitance

Q$_G$ = Gate charge transferred during turn-on

Were it not for the internal charge pump, the voltage on the bootstrap capacitor and the gate capacitor (because an upper MOSFET is now turned on) would eventually drain down to zero due to bootstrap diode leakage current and the very small supply current associated with the level-shifters and upper gate driver sub-circuits.

In PWM switch-mode, the switching frequency is equal to the reciprocal of the period between successive turn-on (or turn-off) pulses. Between any two turn-on gate pulses exists one turn-off pulse. Each time a turn-off pulse is issued to an upper MOSFET, the bootstrap capacitor of that MOSFET begins its "refresh" cycle. A refresh cycle ends when the upper MOSFET is turned on again, which varies depending on the PWM frequency and duty cycle. As the duty cycle approaches 100%, the available "off-time", t$_{OFF}$ approaches zero. Equation 2 shows the relationship between t$_{OFF}$, f$_{PWM}$ and the duty cycle.

$$t_{OFF} = (1 - DC)/f_{PWM} \qquad \text{(EQ. 2)}$$

As soon as the upper MOSFET is turned off, the voltage on the phase terminal (the source terminal of the upper MOSFET) begins its descent toward the negative rail of the high voltage bus. When the phase terminal voltage becomes less than the V$_{CC}$ voltage, refreshing (charging) of the bootstrap capacitor begins. As long as the phase voltage is below V$_{CC}$ refreshing continues until the bootstrap and V$_{CC}$ voltages are equal.

The off-time of the upper MOSFET is dependent on the gate control input signals, but it can never be shorter than the dead-time delay setting, which is set by the resistors connecting HDEL and LDEL to V$_{SS}$. If the bootstrap capacitor is not fully charged by the time the upper MOSFET turns on again, incomplete refreshing occurs. The designer must insure that the dead-time setting be consistent with the size of the bootstrap capacitor in order to guarantee

complete refreshing. Figure 7 illustrates the circuit path for refreshing the bootstrap capacitor.
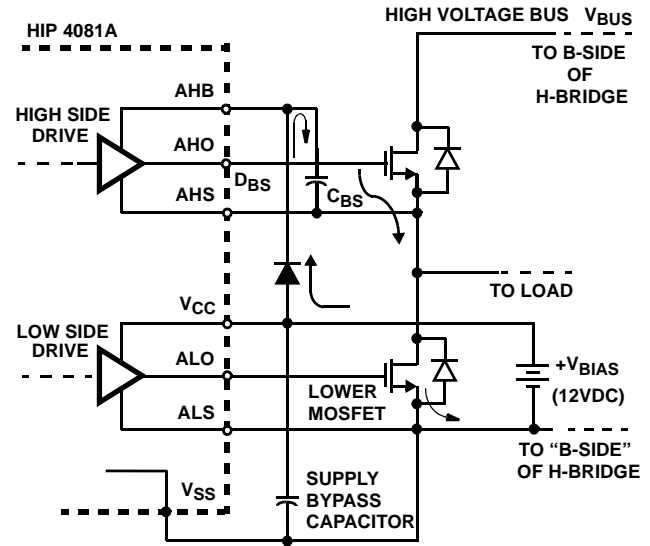
NOTE: Only "A-side" of H-Bridge Is shown for simplicity. Arrows show bootstrap charging path.

FIGURE 7. BOOTSTRAP CAPACITOR CHARGING PATH

The bootstrap charging and discharging paths should be kept short, minimizing the inductance of these loops as mentioned in the section, "Lower Bias Supply Design".

Bootstrap Circuit Design - An Example

Equation 1 describes the relationship between the gate charge transferred to the MOSFET upon turn-on, the size of the bootstrap capacitor and the change in voltage across the bootstrap capacitor which occurs as a result of turn-on charge transfer.

The effects of reverse leakage current associated with the bootstrap diode and the bias current associated with the upper gate drive circuits also affect bootstrap capacitor sizing. At the instant that the upper MOSFET turns on and its source voltage begins to rapidly rise, the bootstrap diode becomes rapidly reverse biased resulting in a reverse recovery charge which further depletes the charge on the bootstrap capacitor. To completely model the total charge transferred during turn-on of the upper MOSFETs, these effects must be accounted for, as shown in Equation 3.

$$C_{BS} = \frac{Q_G + Q_{RR} + \dfrac{(I_{DR} + I_{QBS})}{f_{PWM}}}{V_{BS1} - V_{BS2}} \qquad \text{(EQ. 3)}$$

where:

I$_{DR}$ = Bootstrap diode reverse leakage current

I$_{QBS}$ = Upper supply quiescent current

Q$_{RR}$ = Bootstrap diode reverse recovered charge

Q_G = Turn-on gate charge transferred

f_{PWM} = PWM operating frequency

V_{BS1} = Bootstrap capacitor voltage just after refresh

V_{BS2} = Bootstrap capacitor voltage just after upper turn on

C_{BS} = Bootstrap capacitance

From a practical standpoint, the bootstrap diode reverse leakage and the upper supply quiescent current are negligible, particularly since the HIP4081A's internal charge pump continuously sources a minimum of about 30mA. This current more than offsets the leakage and supply current components, which are fixed and not a function of the switching frequency. The higher the switching frequency, the lower is the charge effect contributed by these components and their effect on bootstrap capacitor sizing is negligible, as shown in Equation 3. Supply current due to the bootstrap diode recovery charge component increases with switching frequency and generally is not negligible. Hence the need to use a fast recovery diode. Diode recovery charge information can usually be found in most vendor data sheets.

For example, if we choose a Intersil IRF520R power MOSFET, the data book states a gate charge, Qg, of 12nC typical and 18nC maximum, both at V_{DS} = 12V. Using the maximum value of 18nC the maximum charge we should have to transfer will be less than 18nC.

Suppose a General Instrument UF4002, 100V, fast recovery, 1A, miniature plastic rectifier is used. The data sheet gives a reverse recovery time of 25ns. Since the recovery current waveform is approximately triangular, the recovery charge can be approximated by taking the product of half the peak reverse current magnitude (1A peak) and the recovery time duration (25ns). In this case the recovery charge should be 12.5nC.

Since the internal charge pump offsets any possible diode leakage and upper drive circuit bias currents, these sources of discharge current for the bootstrap capacitor will be ignored. The bootstrap capacitance required for the example above can be calculated as shown in Equation 4, using Equation 2.

$$C_{BS} = \frac{18nC + 12.5nC}{12.0 - 11.0} \qquad \text{(EQ. 4)}$$

Therefore a bootstrap capacitance of 0.033mF will result in less than a 1.0V droop in the voltage across the bootstrap capacitor during the turn-on period of either of the upper MOSFETs. If typical values of gate charge and bootstrap diode recovered charge are used rather than the maximum value, the voltage droop on the bootstrap supply will be only about 0.5V.

Special Gate Drive Considerations

The dead-time adjustment range provided for in the HIP4081A and HIP4080A parts is usually long enough for driving small to medium size MOSFETs. Often when driving larger MOSFETs, such as RFP25N06 and above, it may be necessary to extend the dead-time adjustment available through adjustment of the RDEL resistors by adding a Schottky diode in parallel with an appropriately sized gate resistor. The gate resistor slows down the turn-on rate of the MOSFET, while the other MOSFET in each of the bridge legs can rapidly turn off through the Schottky diode.

A Schottky diode is recommended in order to keep the drop across it to a minimum which also aids in holding off a MOSFET in the process of turning off during the time that the Miller Effect is trying to turn it back on.

An added protection feature to keep the AHS and BHS pins from flying below ground (VSS) potential when an upper MOSFET turns off is achieved by adding a series resistor between the upper MOSFET source terminals and the AHS and BHS terminals of the driver, respectively. The value of this resistor can usually be in the order of several ohms. Using it, however, provides a means to tailor the turn-off time of the upper MOSFETs in an effort to control how hard the source drives down (and often past) the VSS potential. It is desirable in order to protect the HIP4081A driver that the extent of the undershoot of VSS does not exceed about 4V. Often, the source return resistor recommended above is sufficient to limit the current pulled out of the HIP4081A when the source of the upper MOSFET flys below VSS for a small period of time during the turn-off transient of the upper MOSFETs. Sometimes it is necessary in addition to adding the source return resistor to also add another diode, cathode to AHS and BHS, and anode(s) to VSS close to the VSS terminal of the HIP4081A.

Power Dissipation and Thermal Design

One way to model the power dissipated in the HIP4081A is by lumping the losses into static losses and dynamic (switching) losses. The static losses are due to bias current losses for the upper and lower sections of the IC and include the sum of the I_{CC} and I_{DD} currents when the IC is not switching. The quiescent current is approximately 9mA. Therefore with a 12V bias supply, the static power dissipation in the IC is slightly over 100mW.

The dynamic losses associated with switching the power MOSFETs are much more significant and can be divided into the following categories:

• Low Voltage Gate Drive (charge transfer)

• High Voltage Level-shifter (V-I) losses

• High Voltage Level-shifter (charge transfer)

In practice, the high voltage level-shifter and charge transfer losses are small compared to the gate drive charge transfer losses.

The more significant low voltage gate drive charge transfer losses are caused by the movement of charge in and out of

the equivalent gate-source capacitor of each of the 4 MOSFETs comprising the H-Bridge. The loss is a function of PWM (switching) frequency, the applied bias voltage, the equivalent gate-source capacitance and a minute amount of CMOS gate charge internal to the HIP4081A. The low voltage charge transfer losses are given by Equation 5.

$$P_{SWLO} = f_{PWM} \times (Q_G + Q_{IC}) \times V_{BIAS} \qquad \text{(EQ. 5)}$$

The high voltage level-shifter power dissipation is much more difficult to evaluate, although the equation which defines it is simple as shown in Equation 6. The difficulty arises from the fact that the level-shift current pulses, I_{ON} and I_{OFF}, are not perfectly in phase with the voltage at the upper MOSFET source terminals, V_{SHIFT} due to propagation delays within the IC. These time-dependent source voltages (or "phase" voltages) are further dependent on the gate capacitance of the driven MOSFETs and the type of load (resistive, capacitive or inductive) which determines how rapidly the MOSFETs turn on. For example, the level-shifter I_{ON} and I_{OFF} pulses may come and go and be latched by the upper logic circuits before the phase voltage even moves. As a result, little level-shift power dissipation may result from the I_{ON} pulse, whereas the I_{OFF} pulse may have a significant power dissipation associated with it, since the phase voltage generally remains high throughout the duration of the I_{OFF} pulse.

$$P_{SHIFT} = \frac{I}{T} \int_0^T (I_{ON}(t) + I_{OFF}(t)) \times V_{SHIFT}(t) \times dt \qquad \text{(EQ. 6)}$$

Lastly, there is power dissipated within the IC due to charge transfer in and out of the capacitance between the upper driver circuits and V_{SS}. Since it is a charge transfer phenomena, it closely resembles the form of Equation 5, except that the capacitance is much smaller than the equivalent gate-source capacitances associated with power MOSFETs. On the other hand, the voltages associated with the level-shifting function are much higher than the voltage changes experienced at the gate of the MOSFETs. The relationship is shown in Equation 7.

$$P_{TUB} = C_{TUB} \times V_{SHIFT}^2 \times f_{PWM} \qquad \text{(EQ. 7)}$$

The power associated with each of the two high voltage tubs in the HIP4081A derived from Equation 7 is quite small, due to the extremely small capacitance associated with these tubs. A "tub" is the isolation area which surrounds and isolates the high side circuits from the ground referenced circuits of the IC. The important point for users is that the power dissipated is linearly related to switching frequency and the square of the applied bus voltage.

The tub capacitance in Equation 7 varies with applied voltage, V_{SHIFT}, making its solution difficult, and the phase shift of the I_{ON} and I_{OFF} pulses with respect to the phase voltage, V_{SHIFT}, in Equation 6 are difficult to measure. Even the Q_{IC} in Equation 5 is not easy to measure. Hence the use

of Equation 5 through Equation 7 to calculate total power dissipation is at best difficult. The equations do, however, allow users to understand the significance that MOSFET choice, switching frequency and bus voltage play in determining power dissipation. This knowledge can lead to corrective action when power dissipation becomes excessive.

Fortunately, there is an easy method which can be used to measure the components of power dissipation rather than calculating them, except for the tiny "tub capacitance" component.

Power Dissipation, the Easy Way

The average power dissipation associated with the IC and the gate of the connected MOSFETs can easily be measured using a signal generator, an averaging millimeter and a voltmeter.

Low Voltage Power Dissipation

Two sets of measurements are required. The first set uses the circuit of Figure 8 and evaluates all of the low voltage power dissipation components. These components include the MOSFET gate charge and internal CMOS charge transfer losses shown in Equation 5 as well as the quiescent bias current losses associated with the IC. The losses are calculated very simply by calculating the product of the bias voltage and current measurements as performed using the circuit shown in Figure 9. For measurement purposes, the phase terminals (AHS and BHS) for both A and B phases are both tied to the chip common, V_{SS} terminal, along with the lower source terminals, ALS and BLS. Capacitors equal to the equivalent gate-source capacitance of the MOSFETs are connected from each gate terminal to V_{SS}. The value of the capacitance chosen comes from the MOSFET manufacturers data sheet. Notice that the MOSFET data sheet usually gives the value in units of charge (usually nano-coulombs) for different drain-source voltages. Choose the drain-source voltage closest to the particular dc bus voltage of interest.

Simply substituting the actual MOSFETs for the capacitors, C_L, doesn't yield the correct average current because the Miller capacitance will not be accounted for. This is because the drains don't switch using the test circuit shown in Figure 8. Also the gate capacitance of the devices you are

using may not represent the maximum values which only the data sheet will provide.
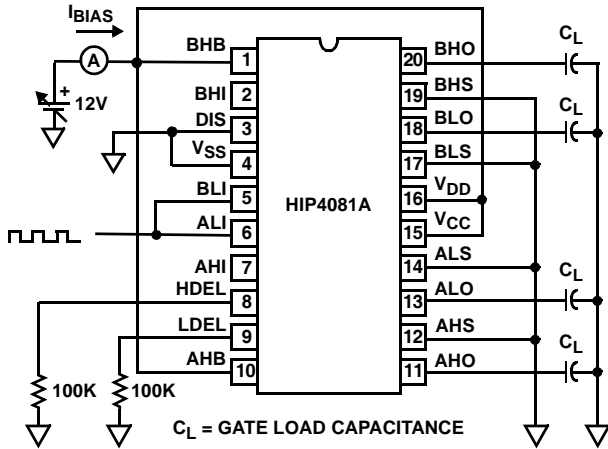

FIGURE 8. LOW VOLTAGE POWER DISSIPATION TEST CIRCUIT

The low voltage charge transfer switching currents are shown in Figure 9. Figure 9 does not include the quiescent bias current component, which is the bias current which flows in the IC when switching is disabled. The quiescent bias current component is approximately 10mA. Therefore the quiescent power loss at 12V would be 120mW. Note that the bias current at a given switching frequency grows almost proportionally to the load capacitance, and the current is directly proportional to switching frequency, as previously suggested by Equation 5.

High Voltage Power Dissipation

The high voltage power dissipation component is largely comprised of the high voltage level-shifter component as described by Equation 6. All of the difficulties associated with the time variance of the I_{ON} and I_{OFF} pulses and the level shift voltage, V_{SHIFT}, under the integrand in Equation 6 are avoided. For completeness, the total loss must include a small leakage current component, although the latter is usually smaller compared to the level-shifter component. The high voltage power loss calculation is the product of the high voltage bus voltage level, V_{BUS}, and the average high voltage bus current, I_{BUS}, as measured by the circuit shown in Figure 10. Averaging meters should be used to make the measurements.
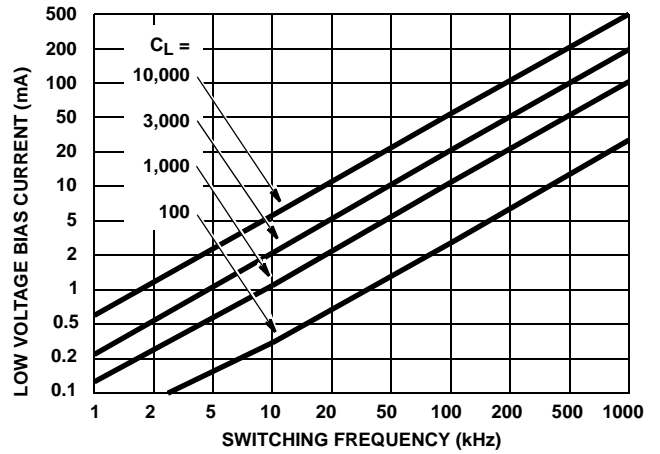

FIGURE 9. LOW VOLTAGE BIAS CURRENT vs FREQUENCY AND LOAD CAPACITANCE

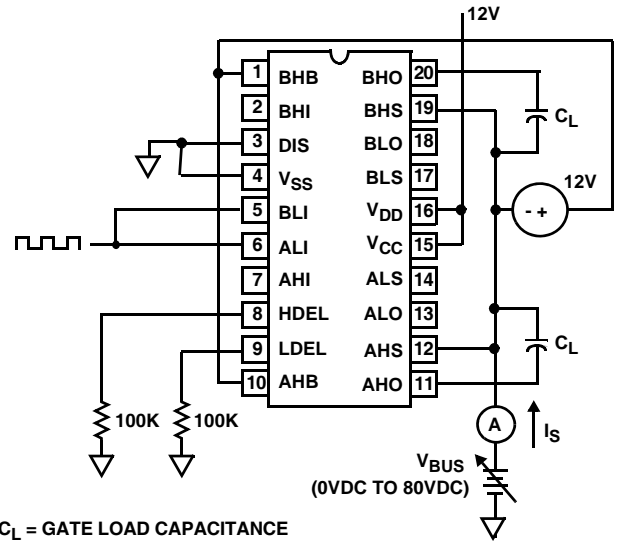

C_L = GATE LOAD CAPACITANCE

FIGURE 10. HIGH VOLTAGE LEVEL-SHIFT CURRENT TEST CIRCUIT

Figure 11 shows that the high voltage level-shift current varies directly with switching frequency. This result should not be surprising, since Equation 6 can be rearranged to show the current as a function of frequency, which is the reciprocal of the switching period, 1/T. Notice that the current increases somewhat with applied bus voltage. This is due to the finite output resistance of the level-shift transistors in the IC.
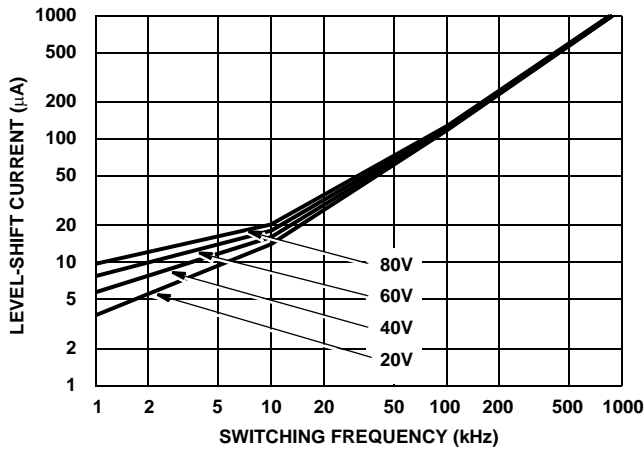
FIGURE 11. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs
FREQUENCY AND BUS VOLTAGE

TABLE 2. LAYOUT PROBLEMS AND EFFECTS

PROBLEM	EFFECT
Bootstrap circuit path too long	Inductance may cause voltage on bootstrap capacitor to ring, slowing down refresh and/or causing an overvoltage on the bootstrap bias supply.
Lack of tight power circuit layout (long circuit path between upper/lower power switches)	Can cause ringing on the phase lead(s) causing BHS and AHS to ring excessively below the V_{SS} terminal causing excessive charge extraction from the substrate and possible malfunction of the IC.
Excessive gate lead lengths	Can cause gate voltage ringing and subsequent modulation of the drain current and impairs the effectiveness of the sink driver from minimizing the miller effect when an opposing switch is being rapidly turned on.

Layout Problems and Effects

In fast switching, high frequency systems, proper PC board layout is crucial. To consider PCB layout. The HIP4081A pinout configuration encourages tight layout by placing the gate drive output terminals strategically along the right side of the chip (pin 1 is in the upper left-hand corner). This provides for short gate and source return leads connecting the IC with the power MOSFETs.

Always minimize the series inductance in the gate drive loop by running the gate leads to the MOSFETs over the top of the source return leads of the MOSFETs. A double-sided PCB makes this easy. The PC board separates the traces and provides a small amount of capacitance as well as reducing the loop inductance by reducing the encircled area of the gate drive loop. The result is reduced ringing which can similarly reduce drain current modulate in the MOSFET. Table 2 summarizes some layout problems which can occur and the corrective action to take.

The Bootstrap circuit path should also be kept short. This minimizes series inductance that may cause the voltage on the bootstrap capacitor to ring, slowing down refresh or causing an overvoltage on the bootstrap bias supply.

A compact power circuit layout (short circuit path between upper/lower power switches) minimizes ringing on the phase lead(s) keeping BHS and AHS voltages from ringing excessively below the V_{SS} terminal which can cause excessive charge extraction from the substrate and possible malfunction of the IC.

Quick Help Table

The quick help table has been included to help locate solutions to problems you may have in applying the HIP4081A.

TABLE 3. QUICK HELP TABLE

PROBLEM	EFFECT
Low chip bias voltages (V_{CC} and V_{DD})	May cause the IC to go into U/V trip.
High chip bias voltages (V_{CC} and V_{DD})	At V_{DD} voltages above about 12V, the charge pump limiter will begin to operate, in turn drawing heavier V_{DD} current. Above 16V, Breakdown may occur.
Bootstrap capacitor(s) too small	May cause insufficient or soft charge delivery to MOSFETs at turn-on causing MOSFET overheating. Charge pump will pump charge, but possibly not quickly enough to avoid excessive switching losses.
Bootstrap capacitor(s) too large	Dead time may need to be increased in order to allow sufficient bootstrap refresh time. The alternative is to decrease bootstrap capacitance.
R_{GATE} too small	Smaller values of R_{GATE} reduces turn-on/off times and may cause excessive EMI problems. Incorporating a series gate resistor with an anti-parallel diode can solve EMI problem and add to the dead time, reducing shoot-through tendency.
R_{GATE} too large	Increases switching losses and MOSFET heating. If anti-parallel diode mentioned above is in backwards, turn-off time is increased, but turn-on time is not, possibly causing a shoot-through fault.
Dead time too small	Reduces "refresh" time as well as dead time, with increased shoot-through tendency. Try increasing HDEL and LDEL resistors (don't exceed 250kW).
HIP4081A IC gets too hot	Reduce bus voltage, switching frequency, choose a MOSFET with lower gate capacitance or reduce bias voltage (if it is not below the U/V trip level). Shed some of the low voltage gate switching losses in the HIP4081A by placing a small amount of series resistance in the leads going to the MOSFET gates, thereby transferring some of the IC losses to the resistors.
Lower MOSFETs turn on, but upper MOSFETs don't	Check that the HEN terminal is not tied low inadvertently.

Application Demonstration PC Board

Intersil has developed a demonstration PC board to allow fast prototyping of numerous types of applications. The board can be used to aid in characterizing the HIP4081A device under actual operating conditions.

Figure 12 and Figure 13 show the silkscreen and the schematic indicating component placement, respectively, for the HIP4080A/1A demo board. Note that the board can be used to evaluate either the HIP4080A or the HIP4081A, simply by changing a few jumpers. Refer to the appropriate application note for instructions on jumper placement.

The PC board incorporates a CD4069UB to "buffer" inputs to the HIP4081A. JMPR5, resistors R27 and R28, and capacitor, C7 must be removed in order to implement the power up reset circuit described in this application note and in the HIP4081A data sheet, File Number 3659. Depending on the positions of JMPR1-4, one can operate the driver as two separate half-bridges or an H-bridge.

Consistent with good design practice, the +12V bias supply is bypassed by capacitors C6 and C5 (at the IC terminals directly). Capacitor C6 is a 4.7mF tantalum, designed to bypass the whole PCB, whereas C5 is a 0.22mF, designed to bypass the HIP4081A. The bootstrap capacitors, C3 and C4, and the high voltage bus bypass capacitors are 0.1mF, 100V ceramic. Ceramic is used here because of the low inductance required of these capacitors in the application. The bootstrap diodes are 1A, fast recovery (t_{RR} = 200ns), 100V, to minimize the charge loss from the bootstrap capacitors when the diodes become reverse-biased.

The MOSFETs supplied with the demo board is a Intersil IRF520, 100V, 9A device. Since it has a gate charge of approximately 12nC, 10W gate resistors, R21 through R24, have been employed to deliberately slow down turn-on and turn-off of these switches. Finally, R33 and R34 provide adjustment of the dead-time. These are 500kW normally set for 100kW, which will result in a dead-time of approximately 50ns. R30 and R31 provide space for optional shunt resistors (0.1W, 2W, 2%, wirewound) which can be used to provide a current-limiting signal, if desired. R30 and R31 should be replaced with wire jumpers if resistors are not used.

Finally, space has been provided for filter reactors, L1 and L2, and filter capacitors, C1 and C2, to provide filtering of PWM switching components from appearing at output terminals AO and BO. To facilitate placement of user-defined ICs, such as op amps, comparators, etc., space for 3 fourteen pin standard width ICs has been reserved at the far left side of the demo board. The output terminations of the 3 optional locations are wired to holes which can be used to mount application-specific components, easing the process for building up working amplifiers for motor controls and audio amplifiers.
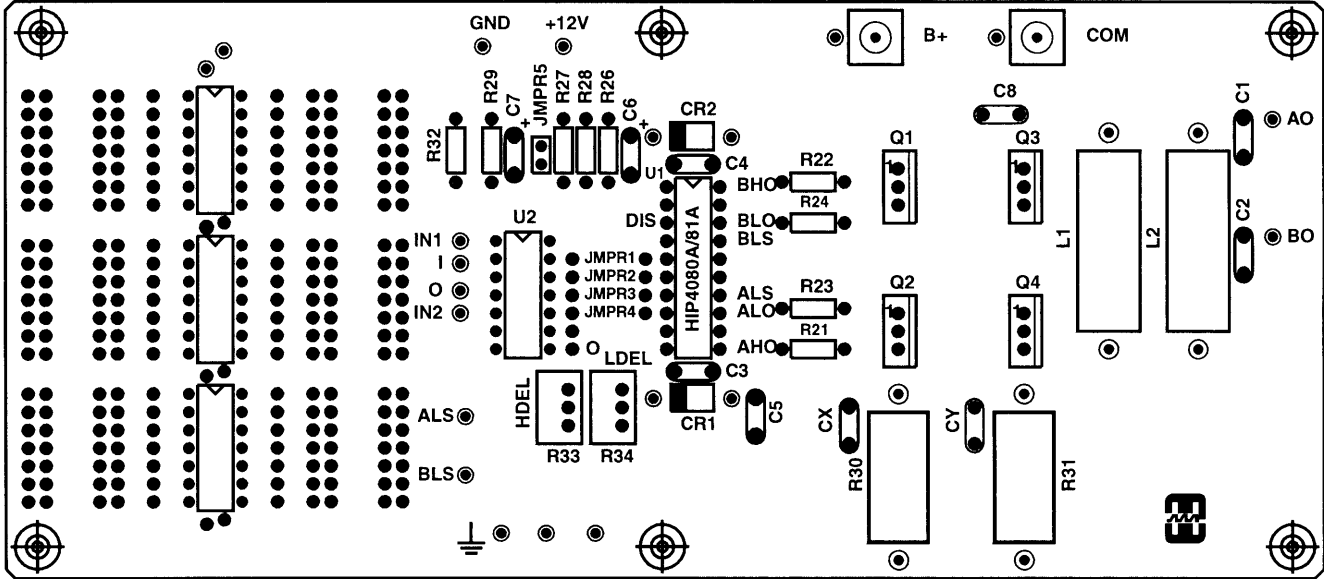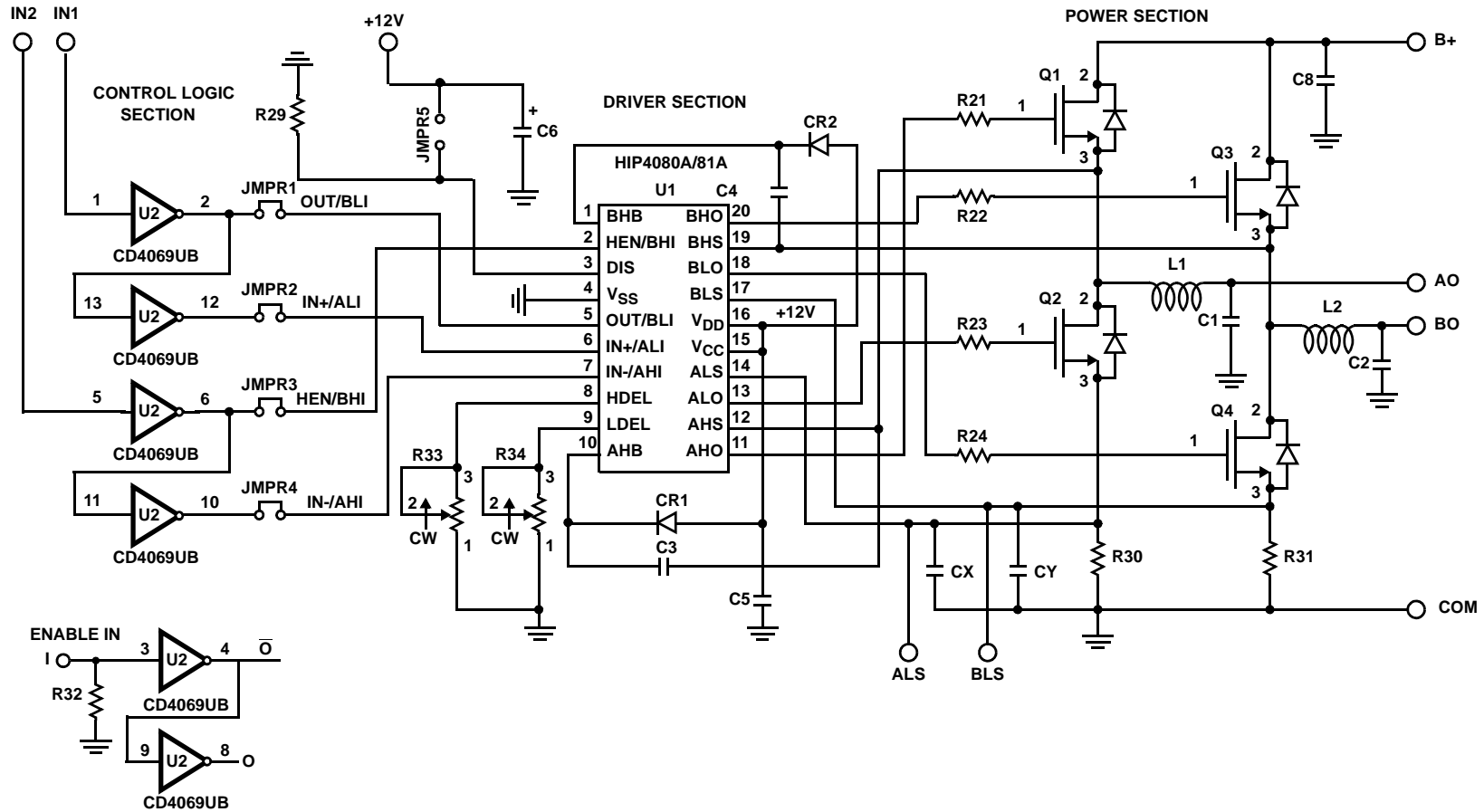
FIGURE 12. HIP4080A/81AEVALZ EVALUATION BOARD SILKSCREEN

For information regarding Intersil Corporation and its products, see www.intersil.com

intersil

IN2 IN1

+12V

POWER SECTION

B+

CONTROL LOGIC
SECTION

R29

JMPR5

C6

DRIVER SECTION

Q1

C8

R21

CR2

Q3

HIP4080A/81A

R22

L1

JMPR1 OUT/BLI

U2

CD4069UB

U1   C4

1 BHB   BHO 20

2 HEN/BHI BHS 19

3 DIS   BLO 18

4 V_SS   BLS 17

5 OUT/BLI V_DD 16 +12V

6 IN+/ALI V_CC 15

7 IN-/AHI ALS 14

8 HDEL   ALO 13

9 LDEL   AHS 12

10 AHB   AHO 11

JMPR2 IN+/ALI

U2

CD4069UB

Q2

R23

C1

AO

L2

BO

C2

JMPR3 HEN/BHI

U2

CD4069UB

JMPR4 IN-/AHI

U2

CD4069UB

R33

R34

CW   CW

CR1

C3

Q4

R24

R30   R31

COM

ENABLE IN

I

R32

3 U2 4   Ō

CD4069UB

9 U2 8   O

CD4069UB

C5

CX   CY

ALS BLS

NOTES:

1. Device CD4069UB Pin 7 = COM, Pin 14 = +12V.

2. Components L1, L2, C1, C2, CX, CY, R30, R31, not supplied. Refer to application note for description of input logic operation to determine jumper locations for JMPR1 - JMPR4.

FIGURE 13. HIP4080A/81AEVALZ EVALUATION PC BOARD SCHEMATIC