B EE 546: CMOS II

LAB REPORT: 1

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**Group: 4**

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1. **Goals:**

The goals included:

**Lab-1:**

* Safety and Cleanroom orientation
* To measure the resistivity of wafers and confirm the type of semiconductor
* CMOS Process overview and RCA Cleaning

**Lab-2**: To develop and pattern mask-1 using photolithography

**Lab-3:**

* To etch
* To remove the photoresist with 1165 solution
* To measure oxide thickness
* To perform RCA Cleaning

**Briefly, state the objective of the first lithography process (MASK #1) in your own words.**

The primary objective of the first lithography process (MASK #1) is to transfer a predefined pattern from a mask onto the substrate, (a silicon wafer). This process is crucial for creating intricate patterns and structures on the substrate surface, forming the foundation for subsequent steps in semiconductor fabrication.

**2.a Process overview:**

The laboratory process commenced with a comprehensive orientation session focusing on cleanroom and safety procedures. The orientation provided a detailed overview of the cleanroom protocols, emphasizing the importance of adherence to established guidelines. Various safety measures were clarified, and potential hazards that may arise during the fabrication process were briefed. Clear explanations of solutions and precautionary measures were provided to address these potential issues.

After the thorough cleanroom orientation, the fabrication process officially began with the crucial step of identifying the type of wafer to be used in the subsequent procedures. Following this determination, the focus shifted to obtaining key parameters such as resistivity and thickness. To measure resistivity accurately, the sheet resistance was calculated using the four-point probe method.

The resistivity is obtained by:

where = 279 +/- 25um ≈ 280um.

RCA Cleaning:

Following the resistivity measurement, the fabrication process initiates with the first RCA cleaning process. In the initial phase, the wafer is immersed in a solution composed of in a *5:1:1* ratio at **80°C** for **15** minutes. Subsequently, the wafer undergoes a rinse in DI water for 1 minute, followed by immersion in an HF: DI solution for 15 seconds, and a final rinse in DI water for 30 seconds. The second part of the RCA cleaning process involves immersing the wafer in a solution of in a 5:1:1 ratio at 80°C for 15 minutes. The wafer is then rinsed with DI water for 10 minutes. Concluding the RCA cleaning process, the wafers are dried using nitrogen and carefully stored in the vacuum oven for further processing.

Field Oxidation:

To oxidize the silicon substrate, a series of dry and wet oxidations have been performed. The oxidation starts with dry oxidation at 1000°C for 5 minutes, followed by wet oxidation at 1000°C for 40 minutes and completed by dry oxidation at 1000°C for 5 minutes.

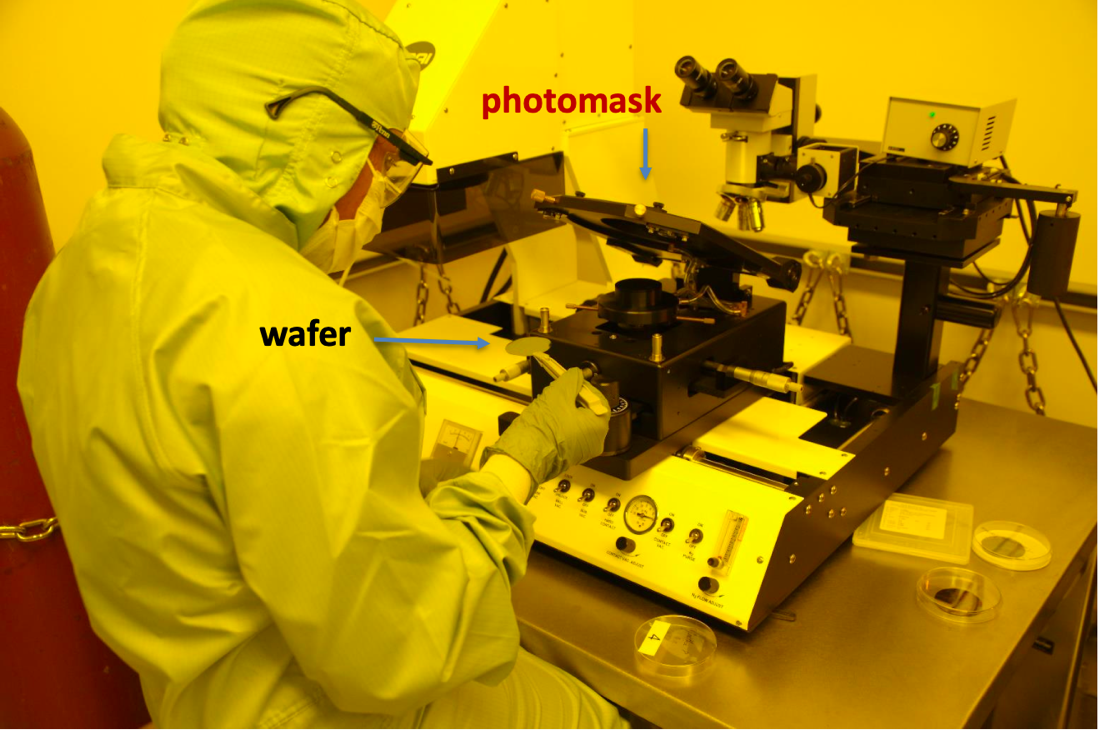
MASK #1 Photolithography:

The photolithography steps include:

1. **HMDS Coating:** In the subsequent stage of the fabrication process, 6 drops of hexamethyldisilane () (HMDS, are introduced to enhance the adhesion of the photoresist layer and converting the wafer from hydrophilic to hydrophobic. The deposition of HMDS is accomplished through the spin coating technique, a critical step in ensuring uniformity. The process involves setting the spin speed to 3500 rpm with a dwell time of 10 seconds. During the spin coating, the wafer is subjected to rotation for 10 seconds.
2. **S1813 Photoresist:** A positive photoresist, S1813, was uniformly deposited on a substrate using spin coating. The spin coating process involved applying the photoresist solution to the substrate, followed by spinning at a speed of 3500 revolutions per minute (rpm) for 30 seconds.
3. **Softbake(hotplate):** At a temperature of 115°C, the wafer underwent a soft bake process lasting for 5 minutes. During this soft bake step, the wafer was subjected to controlled heating, allowing for the removal of residual organic solvents from the photoresist layer, enhancing adhesion, and preparing the photoresist for subsequent processing steps in semiconductor fabrication.

. . 1. Softbakin

1. **UV exposure (#1 Mask):** The wafer underwent patterning through the UV exposure technique, utilizing a UV lamp with a specified power level. The exposure energy for this process was set at 60 millijoules per square centimeter (). The exposure time required to achieve this energy level was



2.Photomask aligning

1. **PR Developing:** To develop the photoresist layer, the mask is immersed in MF 319: undiluted solution for 40 seconds, followed by a thorough washing with DI water for 1 minute. If, upon inspection, the photoresist is found to be underdeveloped, it is recommended to repeat the PR development process.
2. **Hardbake (hotplate):** The wafer is hardbaked for 15 minutes to enhance the development of the photoresist pattern on the substrate. During the hot bake, the temperature is increased to 120°C, which helps in achieving uniformity in the photoresist layer and promotes the cross-linking or hardening of the exposed areas.



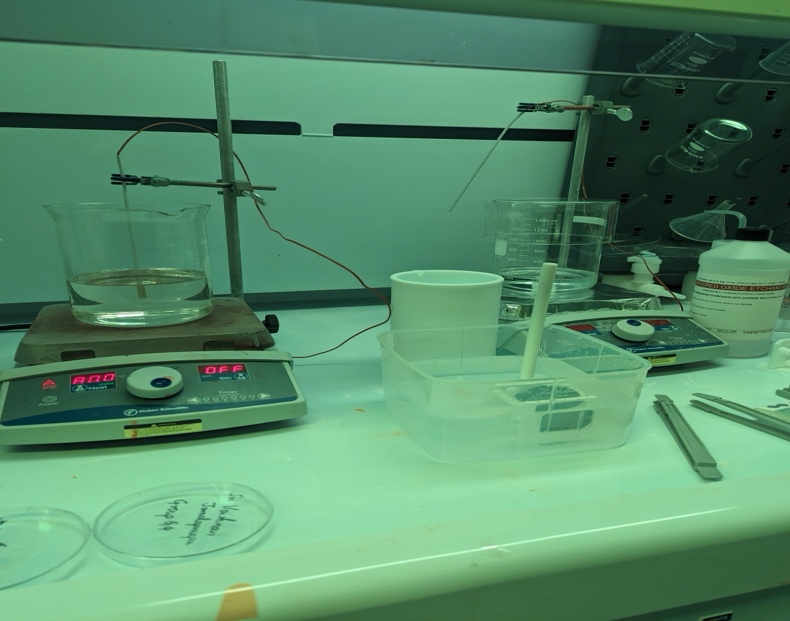
3.Underdeveloped Photoresist



4.After redepositing PR

Etching:

The process initiates with the etching of silicon dioxide () using buffered oxide etching (BOE) for a duration of 6 minutes, followed by a meticulous rinsing step lasting 1 minute. The etch rate for in this process falls within the range of 70-90 nanometers per minute. Subsequently, the wafer undergoes microscopic inspection for residuals. If oxide is detected during the inspection, additional etching is performed in 30-second intervals until complete oxide removal is achieved.



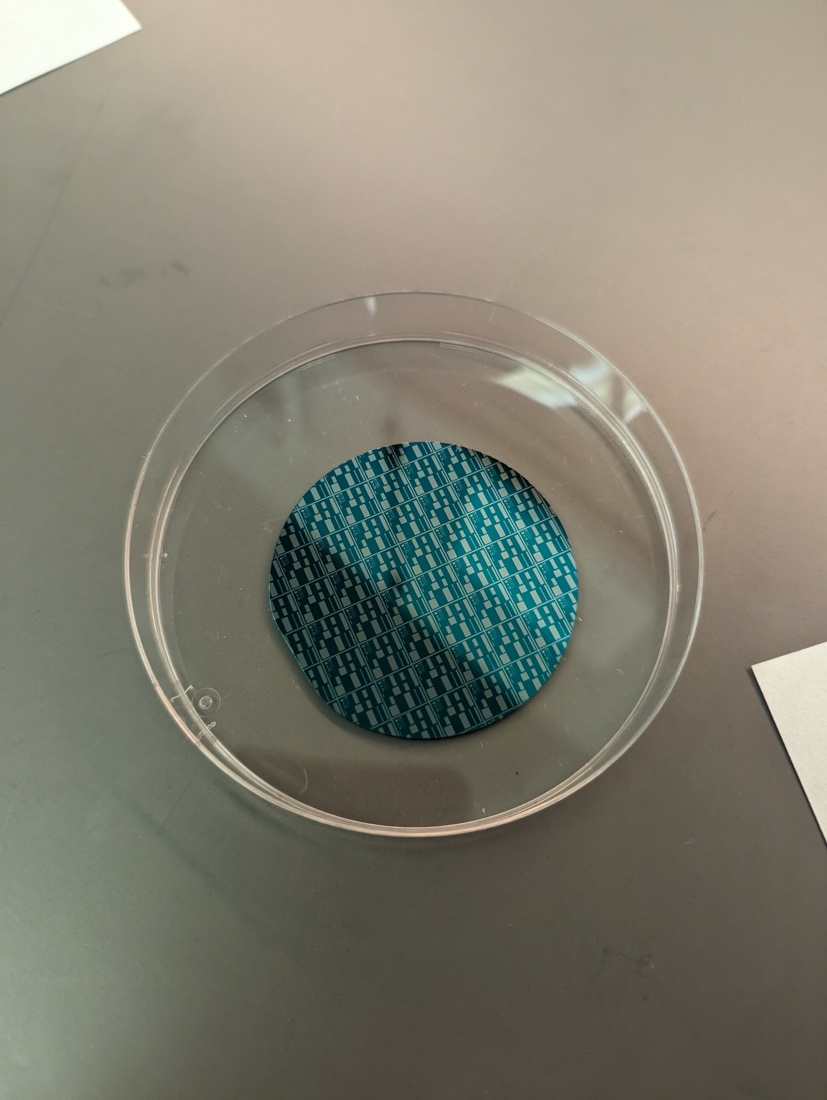
5. BOE Etching



6. Wafer after BOE etching

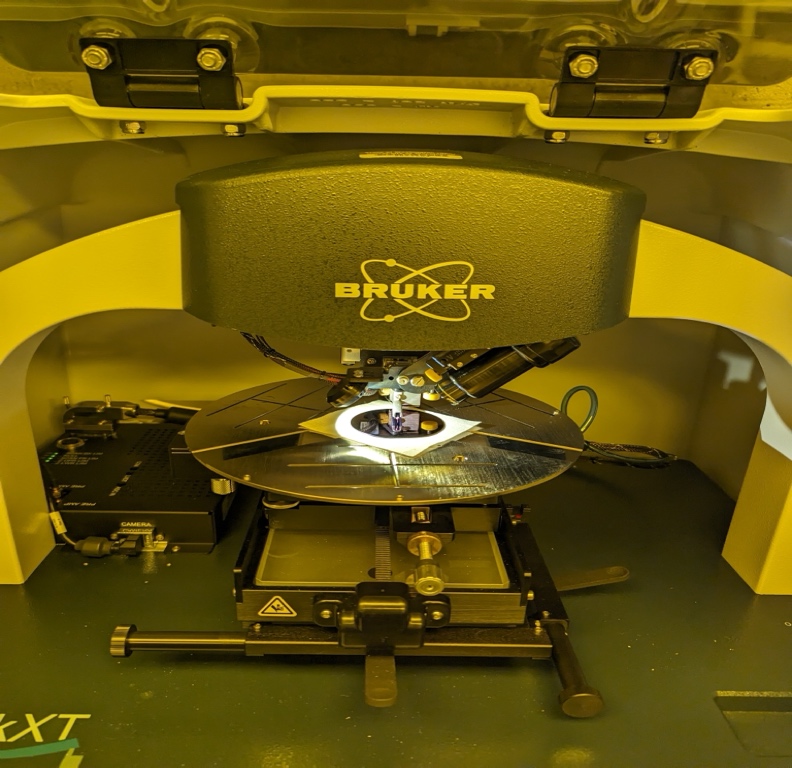
PR Removal:

Following etching, the photoresist layer is eliminated using a 1165 etchant solution for 5 mins at 80°C, after which the wafer undergoes thorough rinsing with deionized (DI) water for 1 minute. A microscopic inspection is then conducted to detect any remaining photoresist residue. If such residue is observed, a degreasing step is deemed necessary. It is crucial to note that incomplete removal of the photoresist layer is identified as the most prevalent cause of contamination in furnace tubes during subsequent processing steps. This comprehensive process ensures the effective removal of and photoresist materials, contributing to the overall cleanliness and reliability of the semiconductor fabrication process.



7. Top view of the silicon wafer

* Measuring oxide thickness: The oxide thickness is measured under a microscopic lens and the results are recorded in a graph format.



Measuring oxide thickness under a microscopic lens

* RCA Cleaning: Following these steps, the process continues with the first RCA cleaning process. The first step of RCA cleaning process is to immerse the wafer in a solution of the mixture of in 5:1:1 ratio at 80°C for 15 minutes. The next step is to rinse the wafer in DI water. Following this, the wafer is dipped in a solution of HF: DI for 30 seconds. The second part of RCA cleaning process is to immerse the wafer in a solution of in 5:1:1 ratio at 80°C for 15 minutes. The last step is to rinse the wafer with DI water for 10 minutes. To finish the RCA cleaning process, the wafer is dried using nitrogen and stored in the vacuum oven.

**2.b Experiment equipment and tools:**

1. **Four-Point Probe Setup-** to measure the resistivity of the wafer.
2. **Hot Plates-** to heat the chemical solutions to the specified temperatures during the RCA cleaning process.
3. **DI Water Bath-** torinse the wafer after each chemical treatment.
4. **Wafer Holder or Cassette-** to hold and handle the semiconductor wafers during the RCA cleaning process.
5. **Tongs or Tweezers-** Non-contaminating tools to handle wafers during the cleaning process
6. **Nitrogen Gun or Compressed Air-** to dry the wafer after rinsing.
7. **Mask Aligner-** to align the mask with the wafer and expose the photoresist to light for pattern transfer.
8. **Photomask-** A high-resolution mask containing the pattern to be transferred onto the wafer. It is typically made of quartz or glass with a chrome pattern.
9. **Photoresist Spinner-** to Coat the wafer with a thin, uniform layer of photoresist. The spinner rotates the wafer, spreading the photoresist evenly.
10. **UV Light Source-** Provides the ultraviolet (UV) light necessary for exposing the photoresist through the photomask.
11. **Hot Plate-** to pre-bake the coated wafer to remove solvents from the photoresist and enhance adhesion.
12. **Soft Bake Oven-** Performs a controlled, low-temperature baking step to further evaporate solvents from the photoresist.
13. **Mask Holder-** Holds the photomask securely in place during the alignment and exposure steps.
14. **Hard Bake Oven-** Heats the wafer to a higher temperature to cure the photoresist and make it more durable.
15. **Inspection Microscope-** to inspect and verify the pattern quality on the wafer after the photolithography process.
16. **Fume Hood or Exhaust System-** to exhaust and remove potentially hazardous fumes generated during the BOE etching process.

**3. Study and discussion:**

**a. Substrate characterization process**

1. **Type of semiconductor -** In this process, a high-quality 2-inch n-type silicon wafer is employed as the substrate. The substrate material is composed of silicon with n-type doping, specifically utilizing phosphorus as the dopant. The orientation of the silicon wafer is denoted as (100), indicating a crystal orientation along the <100> axis. It is noteworthy that the selected silicon wafers belong to the Prime grade, a classification reserved for superior quality wafers widely utilized in semiconductor device manufacturing, photolithography applications, and particle monitors.
2. **Hot point measurement-** The hot point measurement is valuable for a quick and on-the-spot assessment of semiconductor type without the need for complex testing equipment. This technique is particularly useful in educational settings when a rapid preliminary classification of the semiconductor type is required.

* First, the semiconductor sample is probed using a voltmeter or ammeter to measure its electrical characteristics.
* A heat source (soldering iron) is applied to one of the leads of the semiconductor sample, creating a localized heated region which causes carriers (electrons or holes) to be released, leading to a change in the conductivity of the probed region.
* Following the application of the soldering iron to the semiconductor sample, an increase in conductivity was observed. This observed change in conductivity serves as confirmation that the semiconductor wafer was of n-type.

1. **Resistivity measurement (4-point probe)-**

* We conducted resistivity measurements using the four-point probe method, yielding a resistance value of 0.0579 ohm.
* Subsequently, the sheet resistance was calculated by- 0.0579\*4.532=ohms per square.
* We have assumed the wafer thickness to be 0.028 cm. Finally, to ascertain the resistivity, the sheet resistance was multiplied by the known thickness of the semiconductor sample- 0.028\* = 0.0579

1. **Given that the mobility of electrons is 1800 cm2/(V-s), what is the dopant concentration?**

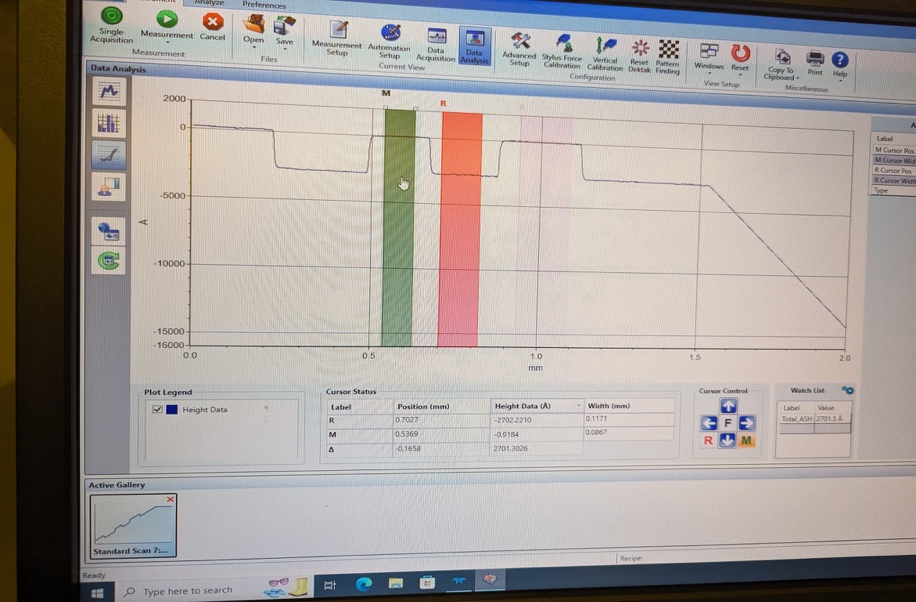
**b. Oxidation process**

1. **Theory of oxidation:** In semiconductor fabrication, oxidation involves the growth of a thin layer of silicon dioxide () on a silicon wafer**.** This process is crucial for the creation of insulating layers, gate oxides, and isolation structures in semiconductor devices. The theory of oxidation in the semiconductor field is primarily based on the reaction between silicon and oxygen, typically performed at elevated temperatures (usually above 900°C), to form silicon dioxide. The thickness of the oxide layer is determined by the duration of the oxidation process. Oxygen molecules diffuse through the existing silicon dioxide layer to reach the silicon-silicon dioxide interface, where the oxidation reaction continues. Dry oxidation and wet oxidation are two distinct processes used in semiconductor manufacturing for growing oxide layers on silicon wafers.

**Dry Oxidation:** Dry oxidation, also known as dry thermal oxidation, involves exposing a silicon wafer to an oxygen-rich environment at elevated temperatures without water vapor**.** This process typically occurs in a furnace and results in the growth of a silicon dioxide () layer on the wafer's surface. Dry oxidation is characterized by slow growth rates but yields high-quality oxide films with excellent electrical properties. It is often preferred for certain applications where precise control over thickness and uniformity is critical. However, the slow growth rate makes it less suitable for high-throughput production.

**Wet oxidation:** Wet oxidation involves exposing a silicon wafer to an oxygen-rich atmosphere in the presence of water vapor. This process also occurs at elevated temperatures, but the inclusion of water vapor accelerates the growth of the oxide layer compared to dry oxidation. Wet oxidation is known for its faster growth rates, making it suitable for high-volume manufacturing. While the oxide films grown through wet oxidation may have slightly inferior electrical properties compared to dry oxide, they are often more than sufficient for many applications. Wet oxidation is favored in situations where speed and cost-effectiveness are crucial considerations.

1. **Calculate oxide thickness based on the process parameters and compare it with the measured oxide thickness**



To calculate the oxide thickness based on process parameters, the Deal-Grove model can be used. It is widely used in semiconductor manufacturing for predicting the thickness of oxide layers. The estimated oxide thickness was 300nm. However, the measured oxide thickness was found to be 270 nm, after completing the abovementioned fabrication steps.

1. **Discuss if there is any discrepancy between estimated- and measured- thickness.**

The estimated oxide thickness was 300nm.

The measured oxide thickness is 270 nm.

So, there is a discrepancy between estimated and measured oxide thickness. However, some level of discrepancy is expected in semiconductor processes, while it needs to be within acceptable limits defined by industry standards, process specifications, and customer requirements.

**4. Discussion**

1. **Discuss probable sources of experimental error and how (if possible) they can be eliminated.**
2. **Source of Error:** Poor contact between the measurement probes and the wafer can produce resistance. **Elimination:** Proper probe alignment and contact should be ensured. A small amount of pressure should be applied to ensure good electrical contact.
3. **Source of Error:** Non-uniform coating of HDMS on the wafer surface. **Elimination:** The photoresist should be wiped off and the wafer should be cleaned again and dried with nitrogen vacuum before developing photoresist again. The cleanliness of the wafer surface should be ensured and high-quality HDMS should be used.
4. **Source of Error:** Misalignment between the mask and the wafer during exposure. **Elimination:** Precise alignment procedures should be implemented, and the mask aligner should be regularly calibrated.
5. **Source of Error:** Underdeveloped PR. **Elimination:** If the Photoresist is underdeveloped, PR should be developed again following the lithography process.
6. **Source of Error:** Residual oxide after etching. **Elimination:** If oxide is found after BOE etching, the wafer should be etched again in 30 secs interval until the oxide is removed.
7. **Source of Error:** Incomplete removal of photoresist leading to residual PR. **Elimination:** Thorough inspection through optical microscopes should be done to detect any remaining photoresist. If found, degreasing is necessary.
8. **Source of Error:** Incomplete removal of the BOE solution or other stripping chemicals after rinsing. **Elimination:** Thorough rinsing steps using deionized water should be implemented.

**b. Discuss if any of the processes can be further improved for this course.**

The current processes are well-established and efficient. Continuous monitoring and optimization have already been implemented, and it can be said that the existing materials meet industry standards and procedures deliver high-quality outputs. Thus, at this point, further improvements may not be necessary.

**5. References:**

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