SRI VAISHNAVI JAMALAPURAPU

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EDUCATION

University of Washington **Sep 2023 – June 2025**

Master of Science (Thesis) - Electrical Engineering **GPA: 3.6/4.0**

Coursework: CMOS I, CMOS II, Analog Integrated Circuit Design, Advanced Embedded Systems Design, Computer Architecture, Signal Processing, Acoustical Engineering

G. Narayanamma Institute of Technology and Science **Aug 2019 – May 2023**

Bachelor of Technology - Electronics and Communication Engineering

Coursework: Computer Organization and Architecture, LPVLSI, Digital Systems and Designs, Material Science and Engineering, Integrated Circuit Technology, Computer Aided Design, Microprocessor System Design

SKILLS

Programming Languages:Verilog, Assembly Language, C, MATLAB, Python, MS Office

Physical Design and Tools: MentorGraphics, Intel Quartus Prime, LTSpice,NGSpice, Klayout, RTL

Technical Skills: Statistics, Analog Design, Arithmetic Algorithm Design, Physical Design, Digital design, Processor Design, Mask Alignment, Inductively Coupled Plasma Etching, Wet Etching, Dry Etching, Sputtering, Thermal Oxidation, Chemical Vapour Deposition, Failure Mode and Analysis, Probe Testing, Wafer Metrology, Optical Microscopy, UV Lithography, Contact Printing, Spin Coating, Routing, Circuit Design, ReRAM Memory cells

OS: Linux, Windows

RELEVANT EXPERIENCE

SiF Fabrication Development for Silicon Photonic Transceivers **Apr 2024 – Present**

Graduate Student Researcher,[*EMiT Lab*],*University of Washington* Seattle, WA

- Engaged in the development of Optical DAC Based Transmitters within a Silicon-Integrated-Fabric (SiF) 3D Package on-site at **Washington Nanofabrication Facility (WNF)**, employing advanced packaging techniques and 3D integration through direct bonding to refine the SiF interposer layer.
- Minimized interconnect parasitics, reduced pad sizes, and implemented interconnect traces on glass substrates, resulting in a 10X increase in throughput (1100 units per hour) and optimized tacking processes within 10 seconds.
- Ensured high mechanical and electrical reliability, and scalability for any silicon-interposer, applicable to advanced packaging constructs, dielet assembly on interposers, wafer-scale packaging, and high-performance computing applications.

ReRAM Memory Device Optimization **Jan 2024 – Present**

Graduate Student Researcher, University of Washington Seattle, WA

- Conducting independent research on ReRAM, a high-speed, non-volatile memory "brain-like computing" algorithm, with a specific focus on improving device characteristics such as **state retention and endurance.**
- Conducting comprehensive research into a range of advanced fabrication techniques to ensure the longevity of devices and their performance under optimal operating conditions, includes evaluating different processes to identifying for enhancing device reliability and efficiency.
- Aiming to achieve low operating voltages (1V), long cycling endurance(10^{17} cycles), enhanced data retention (10 years) and super scalability (10nm).

Microfabrication Lab, University of Washington [*webpage*] **Jan 2024 – March 2024**

Graduate Student Researcher, University of Washington Seattle, WA

- Fabricated a microchip with dimensions 270um in diameter which consisted of 40um,20um,10um,5um NMOS, 40um,20um,10um,5um PMOS, Al Resistor, Boron Resistor, Phosphorous Resistor, NAND, NOR, Capacitors and CMOS Inverter.
- Included six photomasks, five RCA Cleanings, two wet oxidation techniques, one dry oxidation technique, three pre-deposition techniques : one p-well, one p+, one n+, one drive-in and one metallization techniques.
- Utilized state-of-the art equiment and processes such as UV photolithography, Plasma Sputtering, Wet Etching, Thermal Oxidation and Spin Coating.

SELECTED PROJECTS

Linearized N-Path for Self-Interference Cancellation [Github] **April 2024 –Present**

- Developed adaptive and reconfigurable n-path linear filters to achieve high programmability across various applications, facilitating effective self-interference cancellation through innovative n-path filter designs.
- Engineered a anaolog tunable voltage bias circuit enabling selection between common mode and transistor mode, incorporating a resistive ladder to achieve precise voltage ranges between 0-0.8V and 1-1.8V with a resolution of 25mV, enhancing flexibility and performance in integrated circuit applications.
- Collaborated with [efabless] and the University of Washington's Electrical and Computer Engineering Department, leveraging project funding to successfully tape out a high-performance chip, showcasing advanced semiconductor development and real-world fabrication processes.

Arithmetic Design: Implementation of Wallace Tree Multiplier, Verilog HDL **May 2022 – Aug 2023**

- Designed an arithmetic digital model for Wallace Tree multiplier, known to be the fastest multiplier, using Kogge Stone Adders in place of traditional Carry Look Ahead Adders to record the efficiency and power consumption using **Verilog Hardware Description Language.**
- Resulted in a faster algorithm with regular layout and a controlled fan-out of two. The delay of this structure is determined by $log_2(n)$, with $[n(log_2(n)) - n + 1]$ computation nodes.

Fingerprint Based Voting System using Arduino Nano, A Design Project : **Jan 2023 – May 2023**

- Innovated and deployed a fingerprint-authenticated voting model with Arduino Nano, enhancing election security and real-time results; publication featured in the International Journal of Applied Engineering and Mathematics in 2023.