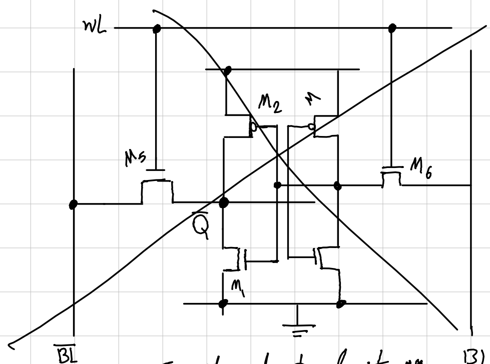
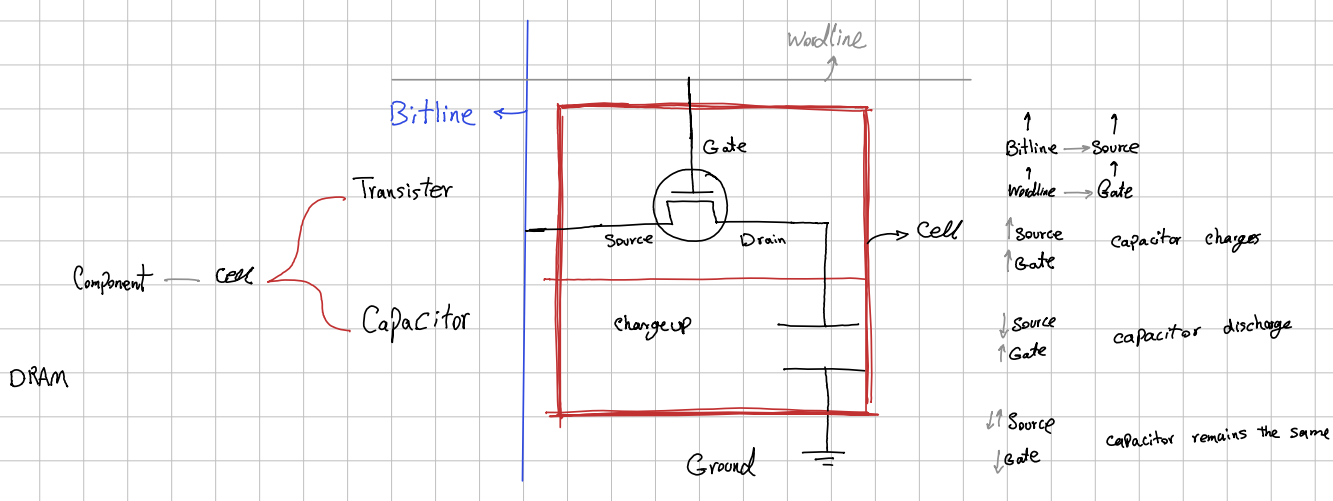
SRAM

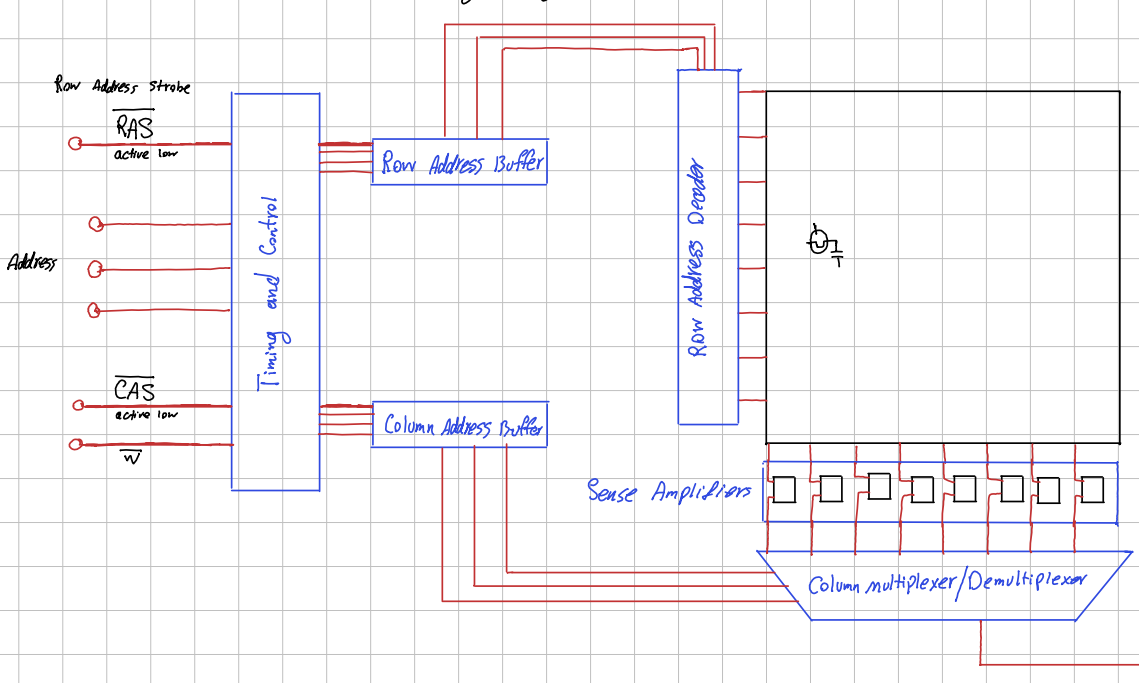
bistable memory cells and resistant to noises

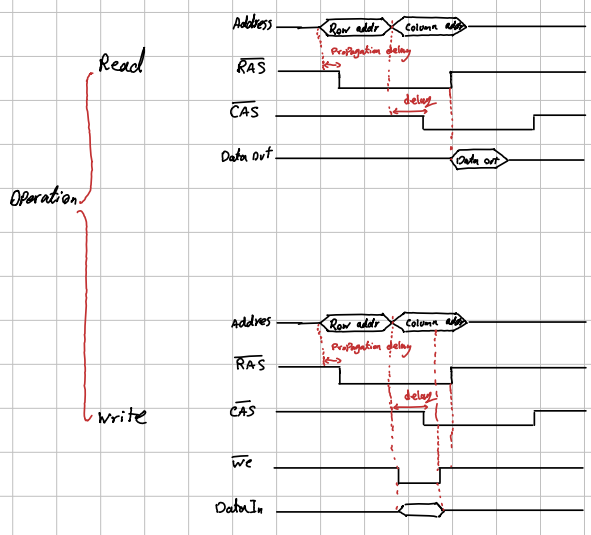


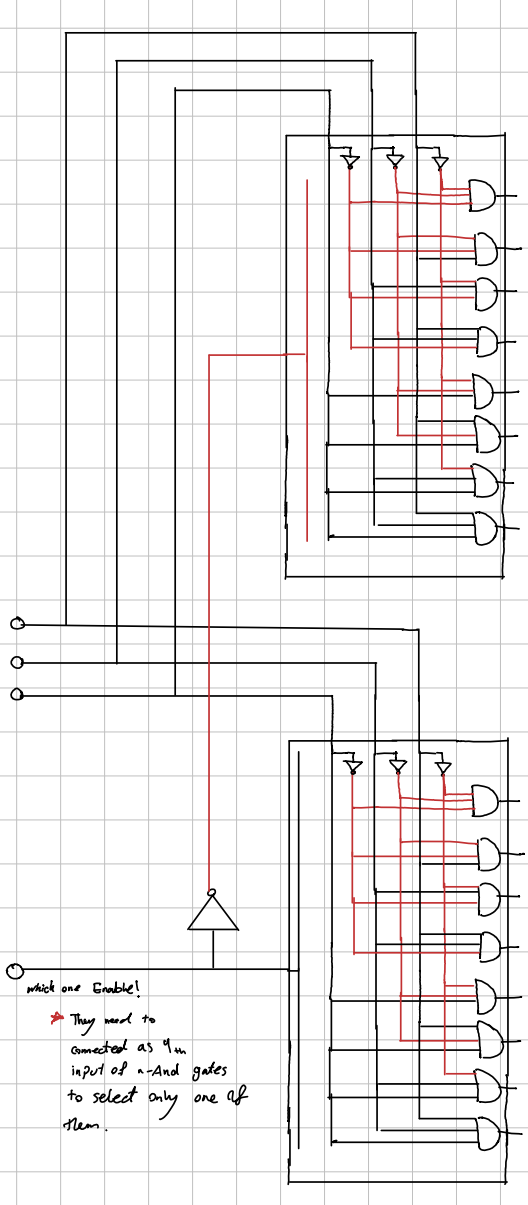
I can't understand it

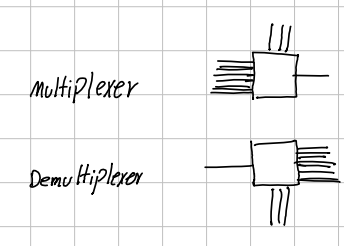


* Read is Destructive operation since Partially charge/Discharge

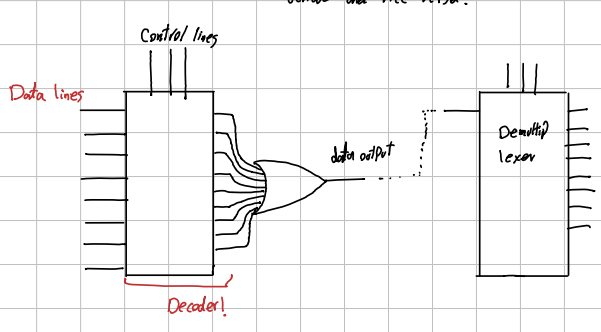






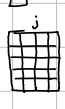


mostly used to Convert Parallel transmition to Serial and vice versa.

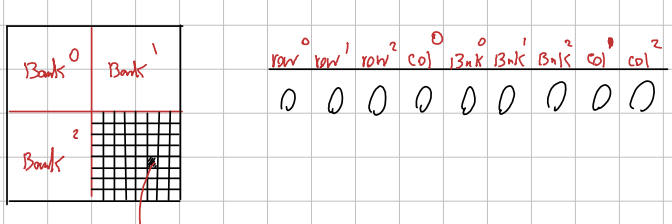


Reading → multiplexer
Writing → Demultiplexer

DRAM cell □
Super cell



I don't understand it though I guess it is just referring to multiple "banks" in a single DRAM chip!



* It should be 8 banks I couldn't make it though

Bunch of DRAM chips make a module
- single → SIMM (72 pins) — Inline memory Module
- DIMM (168 pins) → Dual

	SRAM	DRAM
transister / bit	6	1
relative access time	X	100 X
relative Cost	10 X	X
application	Cache memory	main / video memory

Read cycle:

Bus Interface

CPU

I/O bridge

main memory Controller

I/O bridge

P56

Lec 9_Sam

Write cycle: