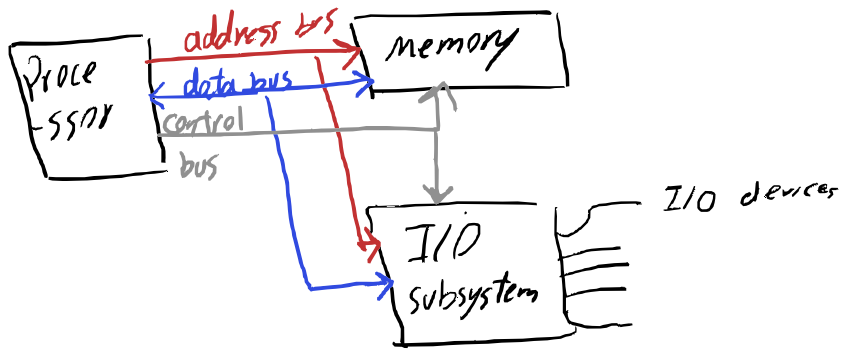
Computer system



System bus
- address — Limit memory capacity
- data — each data transfer size
- Control — it has set of control signals, memory Read - I/O write, interupt, bus request.

Ex. 20-bit address → 2^{20} Byte memory capacity (1MB)

16-bit data → 16 bit of data in each transfer

★ data transfers is called "Transaction's. the initiator is "master and the target is "Slave"

★ in a bus cycle there could be 1 transaction or burst of transactions if supported

In most cases there are multiple masters therefore there is bus Protocols in which They have to send request to bus request control line and wait for bus grant control line to respond.