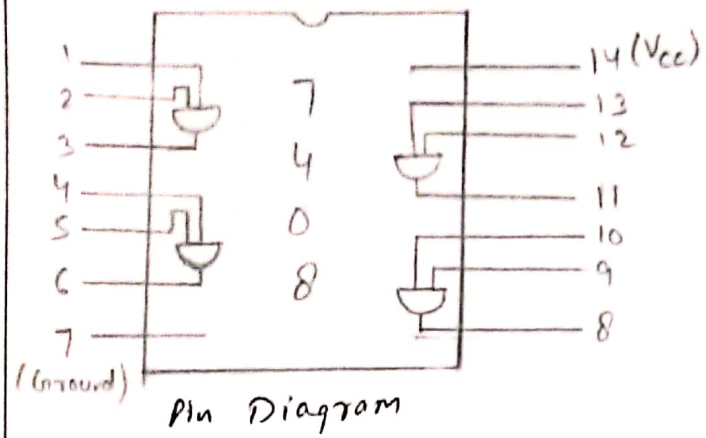
AND Gate (7408)



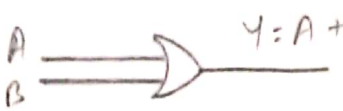
Pin Diagram

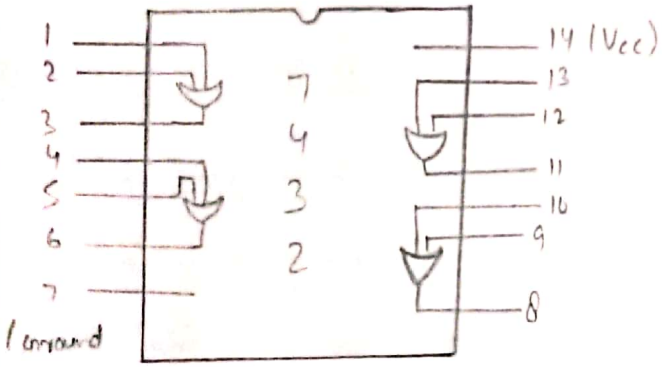
Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Expression → $Y = A \cdot B$

OR Gate (7432)





Pin Diagram

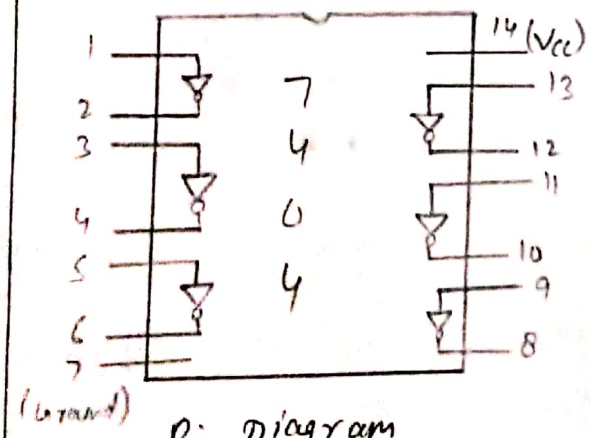
Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Expression →

$Y = A + B$

NOT Gate (7404)



Pin Diagram

Truth Table

A	Y
0	1
1	0

Expression →

$Y = \bar{A}$

Logic Design Components

Circuit that takes the logical decisions and process are called logic gates. Each gate has one or more input and only one output.

OR, AND and NOT are basic gate. NAND, NOR are known as universal gates. Basic gates form these gates

AND Gate:-

The AND gates performs a logical multiplication commonly known as AND functions. The output is high when both the Inputs are high. The output is low level when any one of the input is low.

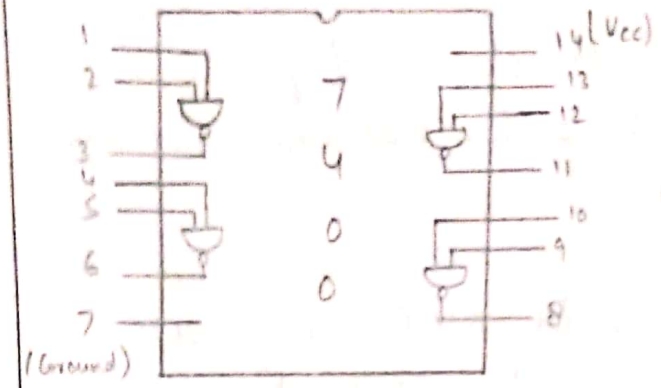
OR Gate

The OR gates performs a logical additional commonly known as OR functions. The function output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT Gates

The NOT gate is called as an inverter. The output is high when the input is low. The output is low when the input is high.

NAND Gate (7400)



Pin Diagram

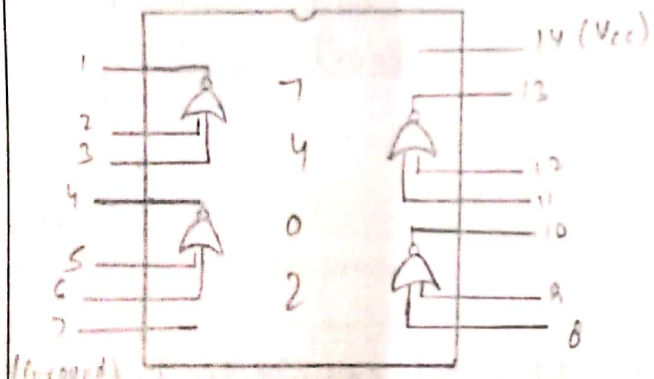
Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Expression

$Y = \overline{A \cdot B}$

NOR Gate (7402)



Pin Diagram

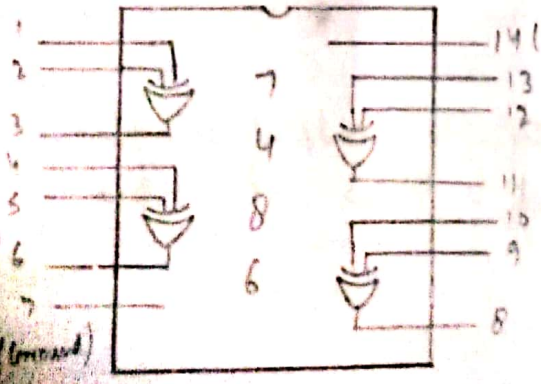
Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Expression

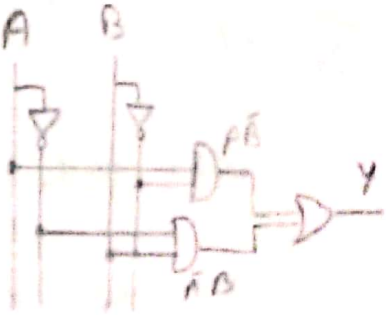
$Y = \overline{A + B}$

EX-OR Gate (7486)



Pin Diagram

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



Expression

$Y = A\bar{B} + \bar{A}B$

$= A \oplus B$

NAND Gate

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and anyone of the inputs is low. The output is low level when both inputs are high.

NOR Gate

The NOR gate is a contraction of OR-NOT gate. The output is high when both inputs are low. The output is low when one or both inputs are high.

EX-OR Gate

The output is high when anyone of the inputs is high. The output is low when both the input are low and both the inputs are high.

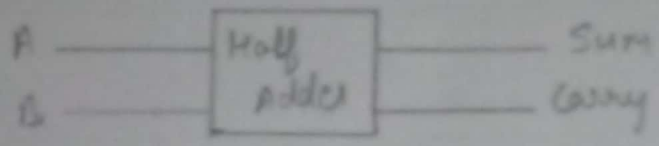
Procedure

i) Connections are given as per circuit diagram
ii) Logical inputs are given as per circuit diagram
iii) Observe the output and verify the truth table.

Result

The truth table has been verified.

Half Adder

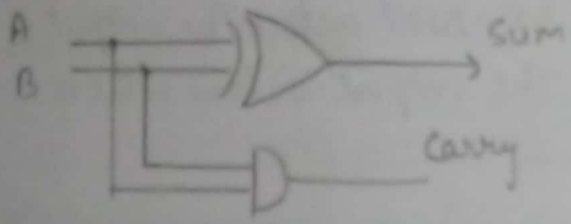


A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

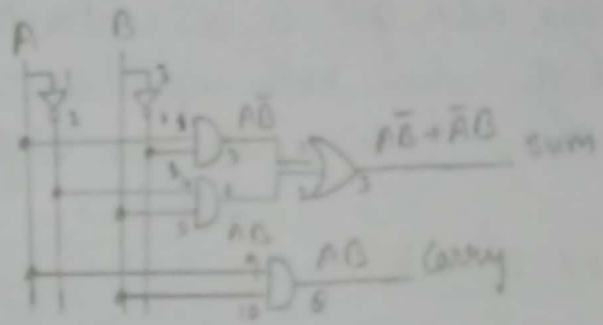
$Sum = \bar{A}B + A\bar{B} = A \oplus B$

$Carry = A \cdot B$

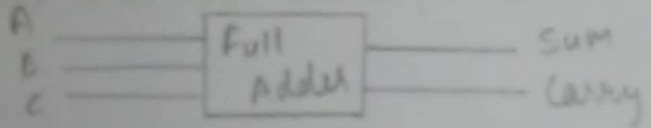
Using X-OR Gate



Using Basic Gates



Full Adder



A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(B\bar{C} + \bar{B}C) + A(\bar{B}\bar{C} + BC)$

$= \bar{A}(B \oplus C) + A\overline{(B \oplus C)}$

$= A \oplus B \oplus C$

$Carry = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$= C(\bar{A}B + A\bar{B}) + AB(\bar{C} + C)$

$= C(A \oplus B) + AB$

Adders And Subtractors

Aim: Design and implement half adder, full adder, half subtractor, full subtractor using basic gates

Components

S.No.	Particulars	IC Numbers	Quantity
1	2 Input AND gate	7408	As per requirements
2	2 Input OR gate	7432	As per requirements
3	NOT gate	7404	As per requirements
4	X-OR gate	7486	As per requirements
5	Patch Cards	—	As per requirements
6	Digital IC transistor bit	—	1

Theory

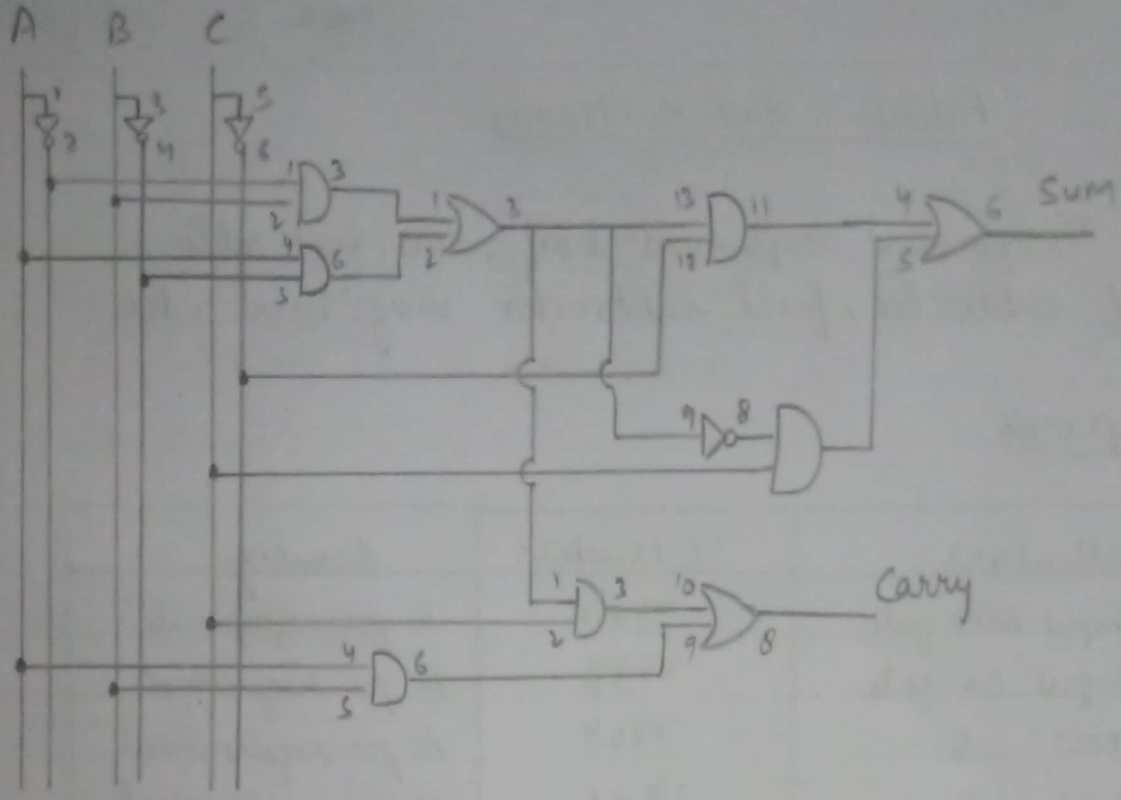
An adder, also called summer, is a digital circuit that performs addition of numbers.

• Half Adder

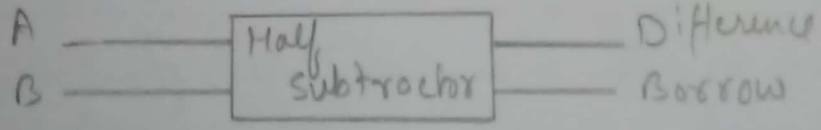
It's a combinational circuit that performs addition of two bits, the circuit needs two binary outputs, with one producing sum output and other produce carry output. The half-adder is useful to add one binary digit quantity.

• Full Adder

This type of adder is a little more difficult to implement



Half Subtractor

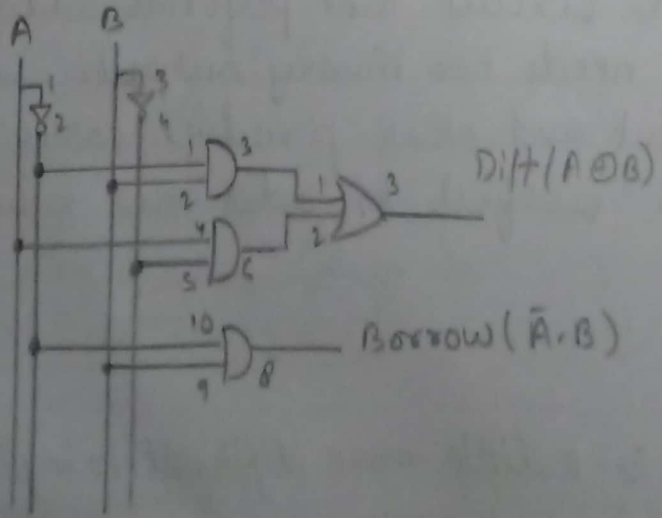


A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$Difference = \bar{A}B + A\bar{B}$

$= A \oplus B$

$Borrow = \bar{A}B$



than a half-adder. The main difference between a half-adder and a full-adder has threee inputs and two outputs. The first two inputs are A and B and the third input is Cin designated as carry. The output carry is designated as Cout and the normal output sum is designated as S

• Half Subtractor

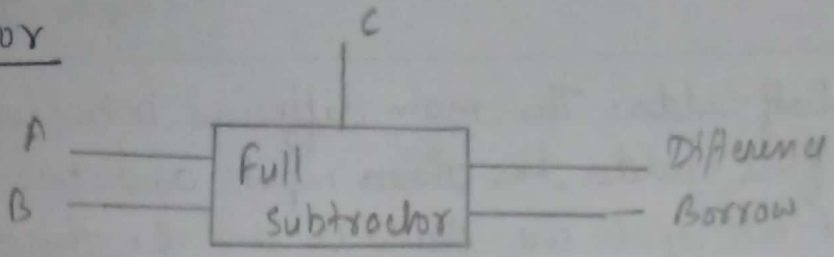
A half subtractor is a multiple combinational logic network that does the subtraction of two bits of binary data. It has input variables and the two output variables. Two input are corresponding to two input bits and two output variables correspond to the difference bit and borrow bit.

Full Subtractor

A combinational logic circuit performs a subtraction between the two binary bits by considering borrow of the lower significant stage is called as full subtractor. In this, subtraction of the two digits is performed by taking into consideration whether a 1 has already borrowed by the previous adjacent lowered minuend bit or not

It has three input terminals in which two terminals corresponds to the two bits to be subtracted (minuend A and subtracted B), and borrow bit Bi corresponds to the borrow operation. There are two outputs, one corresponds to the difference D output and other borrow Bo

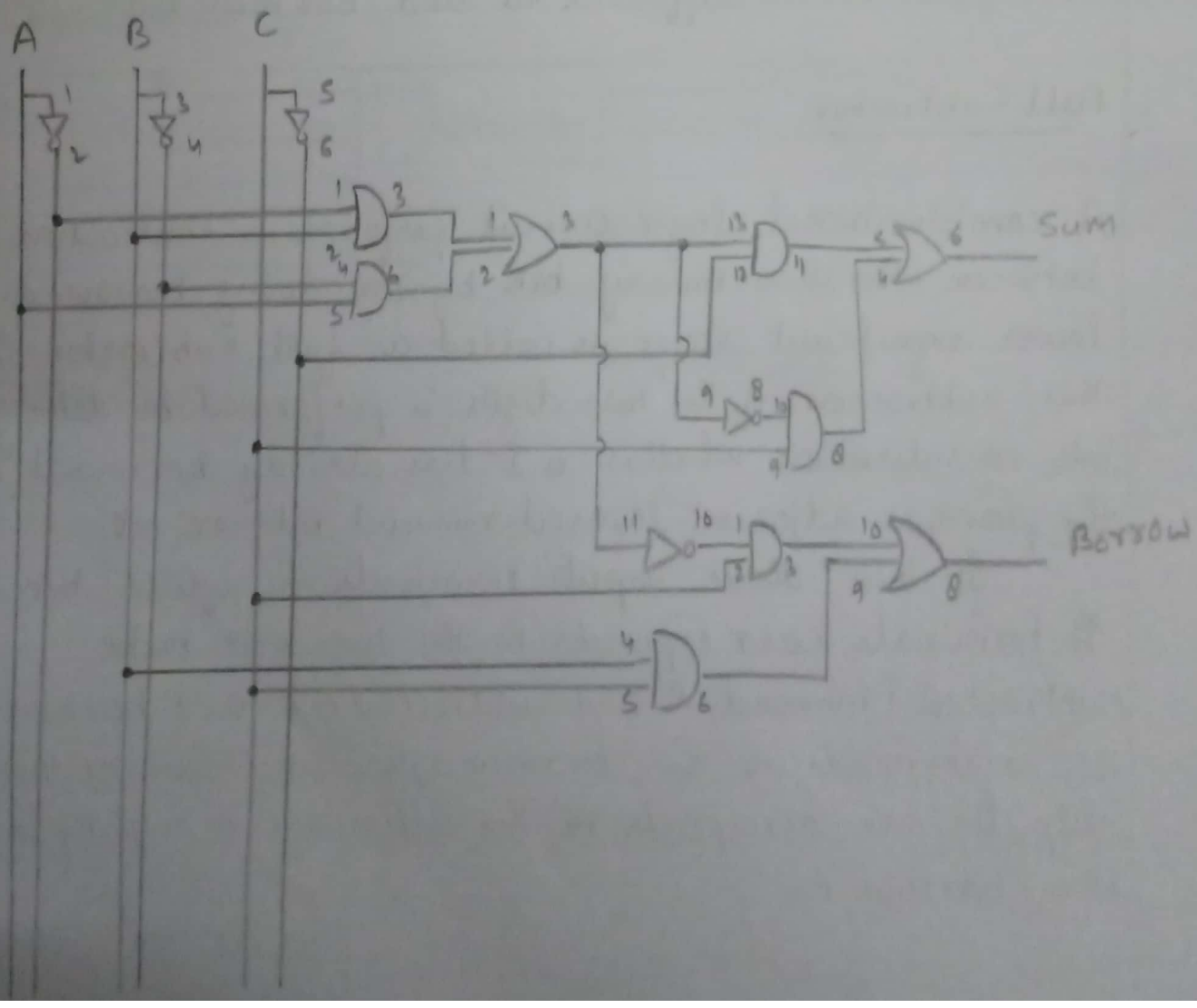
Full Subtractor



A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$\text{Difference} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$
$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$
$$= A \oplus B \oplus C$$

$$\text{Borrow} = A\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + ABC$$
$$= C(\bar{A}B + A\bar{B}) + BC(\bar{A} + A)$$
$$= C(\overline{A \oplus B}) + BC$$



Procedure :-

i) Connections are made as shown in the logic diagram
ii) verify the truth table for all the logic circuits.

Results

i) Circuit verified for half adder
ii) Circuit verified for full adder
iii) Circuit verified for half subtractor
iv) Circuit verified for full subtractor.