Digital Design and Computer Architecture: Lab Report		
Lab 1: Drawing Basic Circuits		
Date	10.08.2021	Grade
Names	Manuele Rossetti & Jacques Stimolo	
		Lab session / lab room

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and other required material. Only one of the members of each group should submit. All members of the group will get the same grade.

The name of the submitted file should be *Lab1_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.

Note 1: Please include all the required material. No links/shortcuts are accepted.

Note 2: The deadline for the report is a hard deadline and it will not be extended.

Exercise 1

(a) Assume that we were only using 2-input AND gates and 2-input XNOR gates to create our comparator in Part 1 in this week's lab manual. How many of each gate would you use for a comparator of width 8, 16, 32 and 64 bits? What is the logic depth in each case?

*Note: The **logic depth** of a combinational circuit is defined as the number of **basic logic gates** (e.g., AND, OR, NOT, XOR, etc.) in the longest signal path (path from input to output). The **width** of the comparator indicates the number of bits of each input signal to compare.*

Comparator Width	2-input XNOR gates	2-input AND gates	Logic depth
8 bits	8	7	15
16 bits	16	15	31
32 bits	32	31	63
64 bits	64	63	127

(b) Given the comparator width is N, derive general expressions for calculating the following:

(i) The number of 2-input XNOR gates

F(N) = N

(ii) The number of 2-input AND gates

F(N) = N-1

(iii) The logic depth

F(N) = 2N-1

Exercise 2

Use two instances of the 1-bit comparator we designed in Part 2 in this week's lab to implement a 2-bit comparator. Draw the schematic of your design.

Note: You can either draw on a paper like in the lab session or use a tool such as circuitlab.com to draw a schematic on your computer.

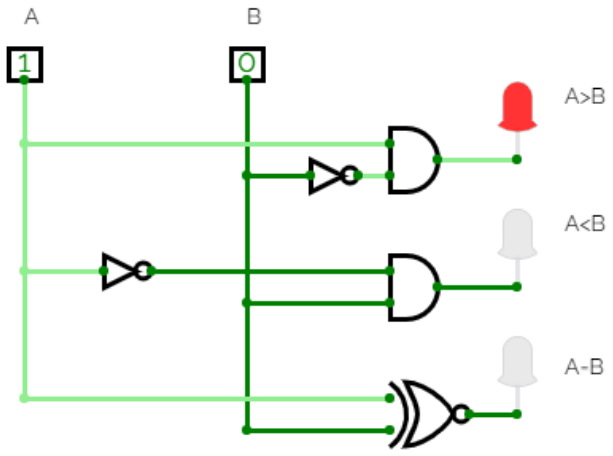


Figure 1: 1-Bit comparator

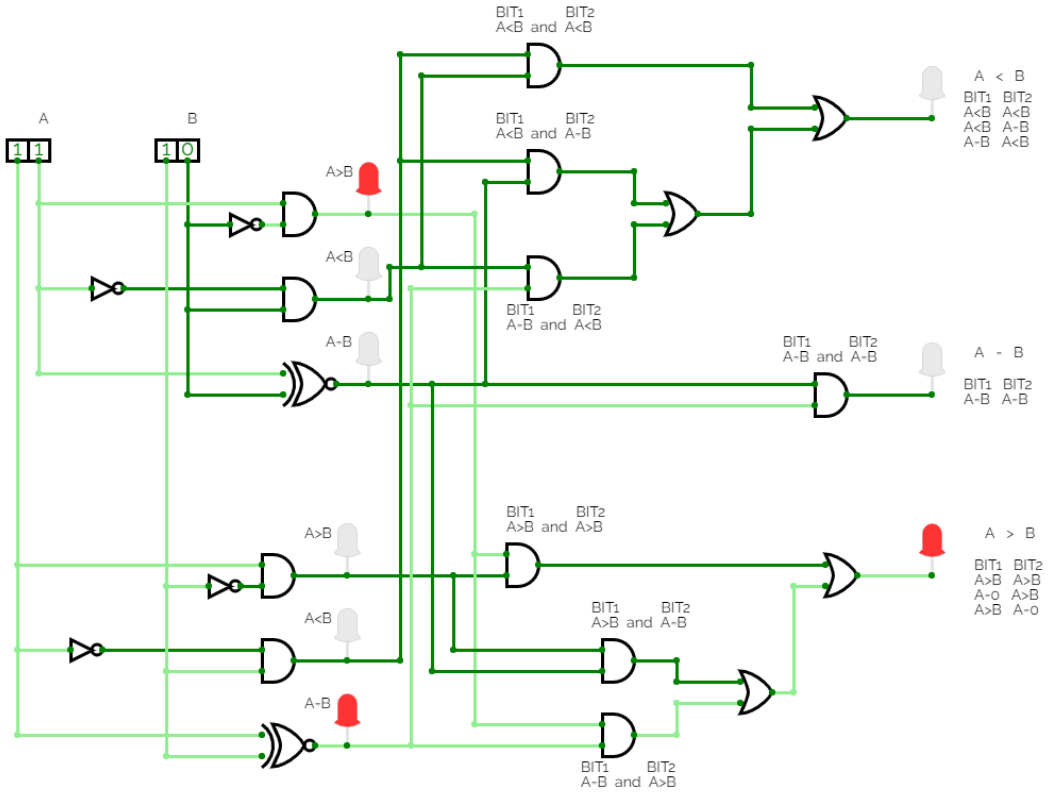


Figure 2: 2-Bit comparator implemented directly from two 1-bit comparators.

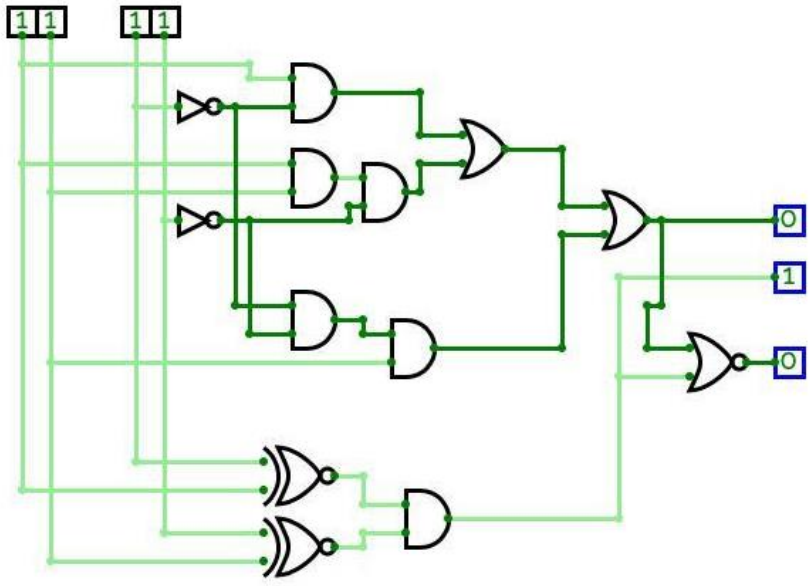
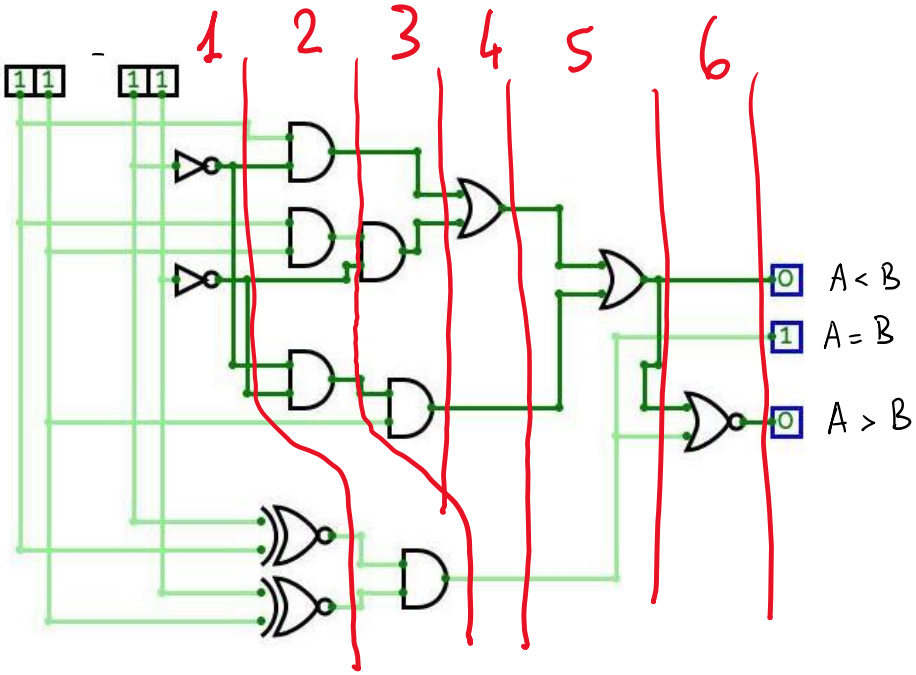


Figure 3: Compact 2-Bit comparator

Exercise 3

What is the logic depth of each of the output ports in the circuit of Exercise 2?

Note: You need to calculate the logic depth of an output port based on the path that contains the highest number of basic logic gates from the inputs to the output port.



Comparator output	Logic depth (Path with highest number of basic gates)
A < B	5
A = B	2
A > B	6

Feedback

If you have any comments about the exercise please add them here: mistakes in the text, difficulty level of the exercise, anything that will help us improve it for the next time.

No comment.