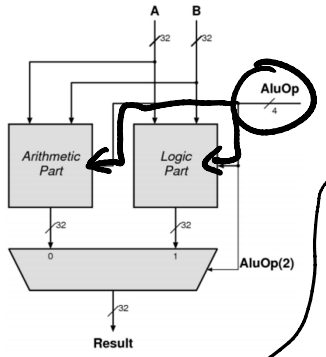
Lab 5

mercoledì, 14 aprile 2021 16:49

Part 1:

AluOp	Mnemonic	Result =	Description
0000	add	A + B	Addition
0010	sub	A - B	Subtraction
0100	and	A and B	Logical and
0101	or	A or B	Logical or
0110	xor	A xor B	Exclusive or
0111	nor	A nor B	Logical nor
1010	slt	(A - B)[31]	Set less than
Others	n.a.	Don't care	

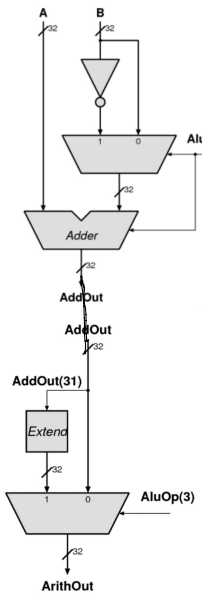



```
module VLC(A,B,AluOp,result);
input [31:0]A,B;
input [3:0]AluOp;
output [31:0] result;
wire [31:0] ArithmOut,LogicOut;

arithmetic(A,B,AluOp,ArithmOut);
logic(A,B,AluOp,LogicOut);

assign result = (AluOp[2]) ? LogicOut : ArithmOut;
endmodule
```

Arithmetic part:

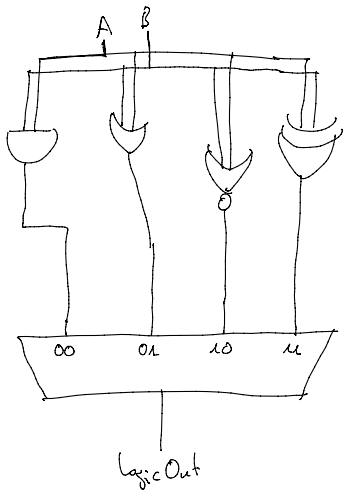



```
module arithmetic(A,B,AluOp,ArithmOut);
input [31:0] A,B;
input [3:0] AluOp;
output ArithmOut;
wire [31:0] AdderOut;   = AddOut
wire [31:0] extended;   = output after
                          expanding AddOut(31)

//Check if add or sub has to be done:
assign AdderOut = (AluOp[1]) ? (A+B) : (A+(~B));

//Check if output is slt or adderOut:
assign extended = 31'b0;
assign extended[31] = AdderOut[31];
assign ArithmOut = (AluOp[3]) ? extended : AdderOut;
endmodule
```

Logic Part:




```
module logic(A,B,AluOp,LogicOut);
input [31:0] A,B;
input [3:0] AluOp;
output reg LogicOut;
wire [31:0] AND,OR,NOR,XOR;


and(AND,A,B);
or(OR,A,B);
nor(NOR,A,B);
xor(XOR,A,B);



always @ (*)
    case(AluOp[2:1])
        0: LogicOut <= AND;
        1: LogicOut <= OR;
        2: LogicOut <= NOR;
        3: LogicOut <= XOR;
    endcase
endmodule
```

Part 2:

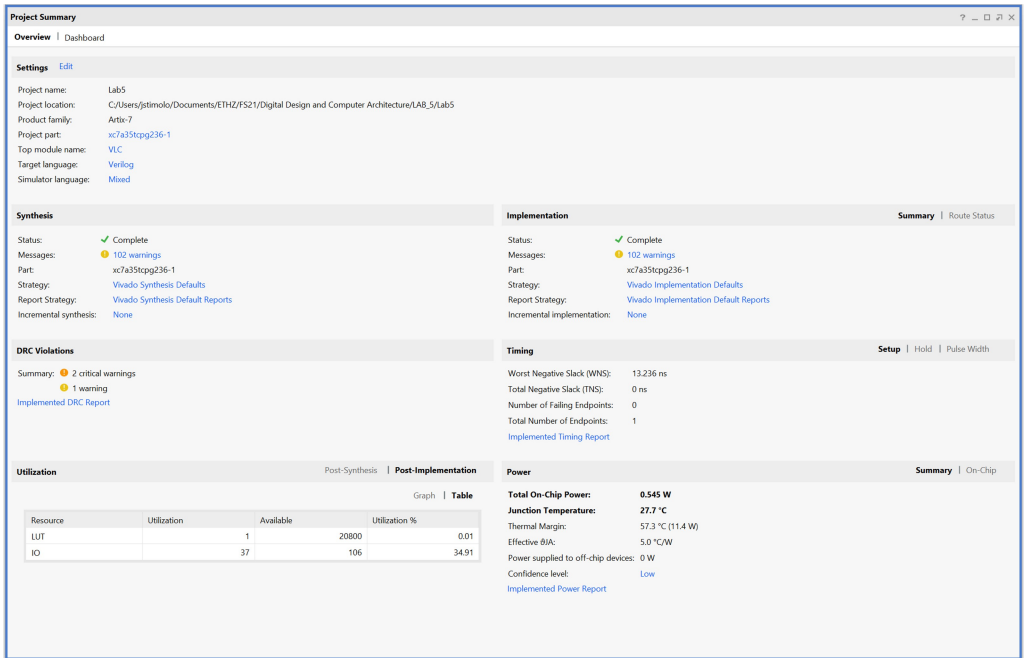
$2 \cdot 32$ bits $= 64$ bits $\Rightarrow 2^{64}$ combinations

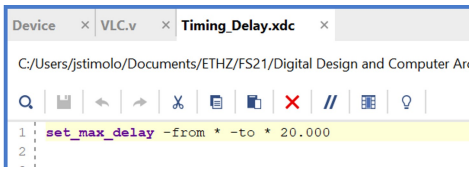
7 combinations for the ALU

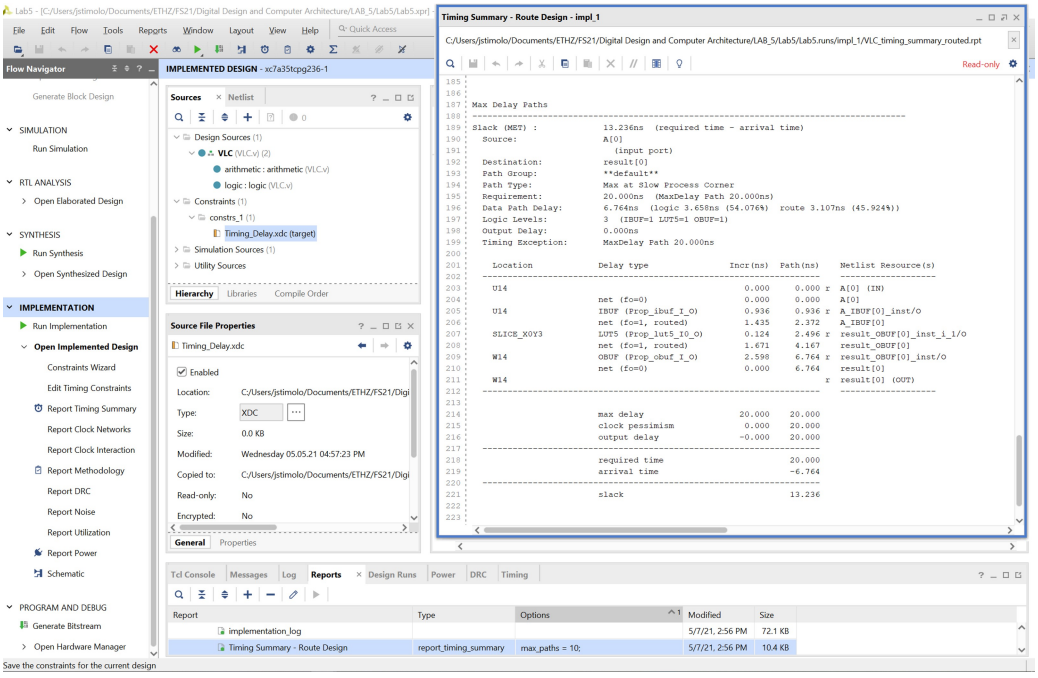
$\Rightarrow$ Tests to do: (1 Test $\Rightarrow$ 1 sec)

$7 \cdot 2^{64} \approx 1.3 \cdot 10^{20}$ s $\approx 4 \cdot 10^{12}$ years (4 billions years)

Part 3:


Project Summary
Overview | Dashboard
Settings Edit
Project name: Lab5
Project location: C:/Users/jstimolo/Documents/ETHZ/FS21/Digital Design and Computer Architecture/LAB_5/Lab5
Product family: Artix-7
Project part: xc7a35tcpg236-1
Top module name: VLC
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Complete
Messages: 102 warnings
Part: xc7a35tcpg236-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary | Route Status
Status: Complete
Messages: 102 warnings
Part: xc7a35tcpg236-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 2 critical warnings
1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): 13.236 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource Utilization Available Utilization %
LUT 1 20800 0.01
IO 37 106 34.91
Power
Summary | On-Chip
Total On-Chip Power: 0.545 W
Junction Temperature: 27.7 °C
Thermal Margin: 57.3 °C (11.4 W)
Effective θJA: 5.0 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report


Device
VLC.v
Timing_Delay.xdc
C:/Users/jstimolo/Documents/ETHZ/FS21/Digital Design and Computer Ar
1 set_max_delay -from * -to * 20.000
2


Flow Navigator
IMPLEMENTED DESIGN - xc7a35tcpg236-1
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
Netlist
Design Sources (1)
VLC (VLC.v) (2)
arithmetic : arithmetic (VLC.v)
logic : logic (VLC.v)
Constraints (1)
constrs_1 (1)
Timing_Delay.xdc (target)
Simulation Sources (1)
Utility Sources
Hierarchy
Libraries
Compile Order
Source File Properties
Timing_Delay.xdc
Enabled
Location: C:/Users/jstimolo/Documents/ETHZ/FS21/Digi
Type: XDC
Size: 0.0 KB
Modified: Wednesday 05.05.21 04:57:23 PM
Copied to: C:/Users/jstimolo/Documents/ETHZ/FS21/Digi
Read-only: No
Encrypted: No
General
Properties
Timing Summary - Route Design - impl_1
C:/Users/jstimolo/Documents/ETHZ/FS21/Digital Design and Computer Architecture/LAB_5/Lab5/Lab5.runs/impl_1/VLC_timing_summary_routed.rpt
Read-only
Max Delay Paths
Slack (MET) : 13.236ns (required time - arrival time)
Source: A[0]
(input port)
Destination: result[0]
Path Group: **default**
Path Type: Max at Slow Process Corner
Requirement: 20.000ns (MaxDelay Path 20.000ns)
Data Path Delay: 6.764ns (logic 3.658ns (54.076%) route 3.107ns (45.924%))
Logic Levels: 3 (IBUF=1 LUT5=1 OBUF=1)
Output Delay: 0.000ns
Timing Exception: MaxDelay Path 20.000ns
Location Delay type Incr(ns) Path(ns) Netlist Resource(s)
U14 0.000 0.000 r A[0] (IN)
net (fo=0) 0.000 0.000 A[0]
U14 IBUF (Prop_ibuf_I_O) 0.936 0.936 r A_IBUF[0]_inst/O
net (fo=1, routed) 1.435 2.372 A_IBUF[0]
SLICE_X0Y3 LUT5 (Prop_lut5_I0_O) 0.124 2.496 r result_OBUF[0]_inst_i_1/O
net (fo=1, routed) 1.671 4.167 result_OBUF[0]
W14 OBUF (Prop_obuf_I_O) 2.598 6.764 r result_OBUF[0]_inst/O
net (fo=0) 0.000 6.764 result[0]
W14 r result[0] (OUT)
max delay 20.000 20.000
clock pessimism 0.000 20.000
output delay -0.000 20.000
required time 20.000
arrival time -6.764
slack 13.236
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Report Type Options Modified Size
implementation_log 5/7/21, 2:56 PM 72.1 KB
Timing Summary - Route Design report_timing_summary max_paths = 10; 5/7/21, 2:56 PM 10.4 KB
Save the constraints for the current design