

Detector R&D Report

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Chapter 1

Vertex Detectors

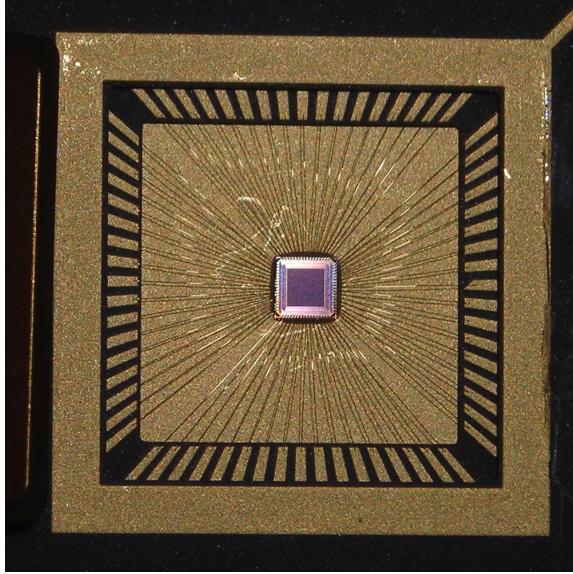
1.1 Motviation and Constraints for Vertex Detectors at Linear Colliders

1.2 ChronoPixel

1.2.1 Introduction

The ChronoPixel is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps of pixel hits by charged particles in a nominal ILC bunch train. This information is read out in the time interval between bunch trains. The ChronoPixel option for the ILC vertex detector was described in the ILC DBD [1]. By the time of the DBD, 2 prototypes had been built and tested, and the summary of test results was also presented in the DBD. The main points are:

- We have proven that we can record time stamps in every pixel with time resolution down to 150 ns.
- We have tested sparse readout, allowing to read only pixels with hits, thus reducing readout time to the level allowing readout of all pixels in the sensor in the intervals between bunch crossings.
- We have tested pulsed power for the analog part of the pixels and have proven [2] that turning power ON about 100 μ s before bunch train and turning it off between bunch trains does not create any problems for threshold setting accuracy in the comparators.
- We have tested the idea of building all in-pixel electronics only from NMOS transistors, thus eliminating the need for a special process (deep p-well) to protect signal charge from parasitic collection by in-pixel transistors. We have proven [3] that all NMOS electronics can be built in this way, and that this does not significantly increase the power consumption compared to CMOS electronics.
- We have tested the compensation of comparator offsets using analog calibration, when the value of the offset is stored as a voltage on the capacitor in each pixel. This has an advantage over digital calibration (where the offset value is stored as code in the special register) in that there are no discrete levels, and the accuracy of such a calibration scheme is not affected by the size of the register or the spread of the initial offsets.



1.2.2 Recent Milestones

- Test of prototype 2 revealed some problems. Possible solutions for these problems were discussed with Sarnoff engineers.
- A new contract with Sarnoff for the design of prototype 3 was signed in August 2013.
- Prototype 3 was manufactured in September 2014. Tests have shown that problems revealed in prototype 2 were solved.

The most recent report [4] on the status of ChronoPixel was presented by N. Sinev in April 2015 at ALCW in Tsukuba, Japan.

1.2.3 Engineering Challenges

- The Vertex Detector for ILC faces many engineering challenges. The sensors need to be thinned to about $50\text{ }\mu\text{m}$ to reduce the amount of material in the detector. Support structures also need to be very light, but provide enough stability. Power dissipation of the entire detector should be small to be able to use only air cooling.
- If acceptable levels of the sensor diode capacitance can be achieved, the signal-to-noise ratio will improve. However, a lower value of the capacitance will make the pixels more sensitive to cross-talk through capacitive coupling. Reducing this coupling can be a challenge.
- Transition from small prototypes (few mm^2) to ILC detector size ($\approx 10\text{ cm}^2$) may meet additional problems. One of them will be the effect of Lorentz forces on the power supply buses, especially in the case of power pulsing. Power pulsing is the only way to achieve acceptable power dissipation in the vertex detector. However, it will generate varying Lorentz forces, acting on power supply lines. This may produce vibrations, which are unacceptable for the required spatial resolution of the detector.

1.2.4 Future Plans

- To achieve signal-to-noise ratio required for close to 100% signal registration efficiency. We have achieved very low sensor capacitance in prototype 3, and the signal-to-noise ratio with such a sensor capacitance for ^{55}Fe signal is about 60, however, for minimum ionizing particles the signal will be much smaller, depending on epitaxial layer thickness and charge collection efficiency. The signal-to-noise ratio for standard 7 μm epitaxial layer will be 20 if the charge collection efficiency is 100%, which is unlikely (we have not measured it yet). So we probably will need to increase the epitaxial layer thickness.
- To achieve the required pixel size (prototype 3 will have 25 μm pixels, we would eventually like 15 μm). It may require going to a technology with feature size less than 65 nm. There seems to be no problems in that, but both – good signal-to-noise ratio and pixel size requirements may be challenging.
- To achieve acceptable level of inter-pixel and digital-to-analog circuit cross talks and parasitic feedback.
- Depending on available funding, to build a complete sensor with a large enough area and full feature readout.

1.2.5 Applications Outside of Linear Colliders

With some modifications (for example, adding time-time converter) ChronoPixel architecture can be applied for any experiment requiring time stamping of individual hits – it may be HL-LHC, CLIC and so on.

1.3 CMOS

1.3.1 Introduction

CMOS Pixel Sensors (CPS) combine high granularity with low material budget and allow integrating the full signal processing circuitry on the sensor substrate. Being moreover cost effective because of the underlying industrial market, CPS are attractive for a wide range of applications. They are developed for the ILC since more than fifteen years and were shown to rather easily comply with the required spatial resolution and material budget of an ILC vertex detector and their radiation tolerance was observed to go well beyond the ILC requirements [5]. The state of the art of the technology is illustrated by the 400 ULTIMATE sensors operated in the STAR-PXL detector [6] at RHIC/BNL since 2014 and by the 10-100 times faster sensors developed for the upgrade of the ALICE Inner Tracker System (ITS) [7].

The achieved read-out speed of the CPS developed for an ILC vertex detector is already quite satisfactory [5], but is worth improving in order to facilitate track seeding at nominal ILC running conditions and to introduce a safety margin reflecting the uncertainties affecting the predicted beam related background rate.

The technology should in fact allow single bunch tagging, provided power consumption and, in turn, power cycling remain under control. The flexibility and detection performances of CPS are also indicating attractive perspectives for trackers, where relaxed constraints on the granularity may be exploited to find a well suited balance between speed, power saving and material budget. Ambitious goals for an ILC

experiment may therefore be considered since their development may be carried out for numerous years until the design inputs of a vertex detector ought to be fixed.

The charged particle detection performances of CPS are currently essentially limited by manufacturing parametres. The latter evolve steadily since several years in a direction which makes them increasingly suited to the ILC vertexing and tracking. Besides achievements targetted with existing processes, the present R&D addresses also improvements expected from the evolution of the CMOS industry, mainly driven by the trend towards smaller feature sizes which would allow overcoming the conflict between the spatial resolution and the bunch tagging capability of CPS. This evolution is already well visible when comparing the performances achieved with the $0.35\text{ }\mu\text{m}$ process used for the STAR-PXL and the more recently addressed $0.18\text{ }\mu\text{m}$ process used for the ALICE experiment.

The R&D adresses presently four objectives :

- 2 or 3 CPS variants optimised for the different vertex detector layers :
 - inner layer : design privileging spatial resolution and read-out speed
 - outer layers : design privileging power saving, exploiting the less demanding spatial and time resolutions
- CPS adapted to tracking sub-systems, based on large pixels and privileging power saving
- ultra-light double sided ladders (called PLUME [8]) equipped with (identical or complementary) CPS on its two faces

1.3.2 Recent Milestones

Specific CPS are being developed since 2011 to equip the Inner Tracking System (ITS) of the ALICE experiment in the framework of its upcoming upgrade. The surface to cover exceeds 10 square meters, i.e. nearly two ordres of magnitude more than the STAR-PXL or an ILC vertex detector.

Two CPS are being developed, differing by their read-out architectures. The most conservative of them, called MISTRAL-0, reproduces the ULTIMATE sensor equipping the STAR-PXL and is thus based on a synchronous, rolling-shutter, read-out. The concept underlying the other sensor, called ALPIDE, features an asynchronous read-out based on a token ring relying on a pre-amplifier/shaper/discriminator chain implemented in the pixel array. It allows for a few microsecond read-out time and for a power consumption below 50 mW/cm^2 . These performances were demonstrated in 2014 [9] on a real scale prototype.

MISTRAL-O relies on large pixels to achieve a $20\text{ }\mu\text{s}$ read-out time and a power consumption below 100 mW/cm^2 while providing $10\text{ }\mu\text{m}$ resolution with its integrated binary encoding. Its read-out architecture was validated in 2014 with a real scale prototype [10] featuring 160,000 small ($22 \times 33\text{ }\mu\text{m}^2$ large) pixels. More recently [11], prototypes composed of three times larger pixels were tested on beam and demonstrated satisfactory charged particle detection performances at 30°C and after radiation loads exceeding those expected at the ILC by several ordres of magnitude.

In summary, the full chain of the ULTIMATE sensor has been reproduced in a $0.18\text{ }\mu\text{m}$ process with twice faster read-out frequency and improved sensitive volume (epitaxial layer) characteristics. The optimisation of this design for tracking systems, using relatively large pixels, is validated.

Moreover, a small prototype of a sensor optimised for the vertex detector outer layers was realised in the $0.18\text{ }\mu\text{m}$ process mentioned earlier. Low power is achieved using enlarged, $35\text{ }\mu\text{m}$ pitch, square pixels and the spatial resolution is kept below $4\text{ }\mu\text{m}$ by integrating a 3-bit ADC in each pixel. The approach was validated in the former $0.35\text{ }\mu\text{m}$ process with the MIMOSA-31 prototype, but the ADCs had to be kept at

the sensor periphery because of process limitations, translating into larger power consumption and slower read-out. Laboratory tests of the new prototype were performed since last Summer, showing satisfactory noise performances at nominal read-out speed, thus validating the concept.

1.3.3 Engineering Challenges

Squeezing the material budget of the double-sided PLUME ladders below $0.3\% X_0$ will be the main engineering challenge, as the design has to account for the necessity to power pulse the ladders in the strong experimental magnetic field. Power pulsing seems mandatory in case of continuous read-out as the sensor design is unlikely to end up with a power density suppressed enough to avoid switching the sensors off inbetween consecutive trains. The possibility to introduce micro-channel cooling in the ladders will be studied in order to mitigate the power pulsing requirements.

1.3.4 Future Plans

Several development directions will be pursued in the coming years, to improve the performances of the CPS and to assess the added value of the ultra-light double-sided ladder concept.

The development of CPS will mainly aim at realising a prototype of a new sensor series, called IBISCUS¹, composed of pixels with less than $20\text{ }\mu\text{m}$ pitch providing a read-out time of about $1\text{ }\mu\text{s}$ (using a token ring read-out).

The R&D on the other CPS versions mentioned earlier (for the vertex detector outer layers and for tracking sub-systems) will be pursued with coarser priority. Besides these continuous read-out architectures, a sensor composed of $4\text{ }\mu\text{m}$ pitch square pixels with analog output, foreseen to be read out inbetween trains like FPCCDs, will also be studied.

Different versions of double-sided ladders will be realised and their performances evaluated in terms of spatial accuracy, including alignment issues, and in terms of stability against power pulsing, possibly in a high magnetic field.

The two main alternative design options are going to be compared to each other. One version is based on a high precision sensor ($< 3\text{ }\mu\text{m}$) on one side featuring $\lesssim 50\text{ }\mu\text{s}$ integration time, while a fast sensor ($\sim 2 - 3\text{ }\mu\text{s}$) equips the other side which provides $\sim 5\text{ }\mu\text{m}$ resolution. The other version is based on a single sensor equipping both ladder sides, which offers $\sim 4\text{ }\mu\text{m}$ spatial resolution and about $5\text{ }\mu\text{s}$ time resolution.

1.3.5 Applications Outside of Linear Colliders

CPS developed at IPHC in perspective of the ILC are used in several devices, as illustrated by the non-exhaustive list below:

- Several high precision transparent beam telescopes, adapted to ($< 1\text{ GeV}$) electron beams, are equipped with the MIMOSA-26 or -28 (alias ULTIMATE) sensors
- The first generation of sensors with full on-chip signal processing developed at IPHC (in a $0.35\text{ }\mu\text{m}$ CMOS process) was applied to the STAR-PXL detector at RHIC, which completed successfully its first data campaign in 2014 and has started its 2015 run
- The upgraded ALICE ITS will be the next equipment based on CPS; it will provide insight of a token ring architecture pioneering the one considered for the IBISCUS chip mentioned above; it will also provide running experience with a tracker based on CPS

¹standing for Ilc Bunch Identifying Sensor Compatible with Ultraprecise Spatial resolution

- The Micro-Vertex Detector of the CBM experiment at FAIR/GSI will also be based on the CPS presently developed for the ALICE-ITS upgrade
- The sensors were, or are, being applied outside of subatomic physics. They were for instance used in the FIRST experiment at GSI, for hadrontherapy monitoring; they are presently developed for soft X-Ray imaging and brain-imaging.

Sensors featuring pixels about 5 times larger than those equipping the STAR-PXL were fabricated in 2014, with different pixel design optimisations. Such large pixels are more exposed to the effects of signal charge recombination. The purpose of the paper is, among others, to show that the charge particle detection efficiency is not degraded, even after radiation loads representative of upcoming trackers, such the upgraded ALICE Inner Tracking System. The charged particle detection performances of these large pixel CPS prototypes with integrated signal processing and binary outputs were studied by exposing the sensors to a 450 MeV electron beam. The results obtained will be exposed and shown to validate the concept for its evolution towards large area tracking devices, with the perspective of integrating logical strips in the sensor.

1.4 DEPFET Pixel Sensors

1.4.1 The DEPFET Collaboration

The [DEPFET collaboration](#) consists of nearly 100 members from 13 institutes. It currently takes responsibility for the following work packages:

Mechanics The DEPFET ladder integrates the support structure with the sensor wafer using state-of-the-art silicon processing technology. Read-out electronics and signal routing are integrated on the silicon wafer. The resulting all-silicon ladder is fully self-supporting. The mechanical properties of thin ladders in a realistic environment are studied in detail using detailed models (mock-ups) for Belle II and the ILC .

Cooling The DEPFET cooling concept for Belle II relies on two-phase CO₂ cooling for the end-of-ladder. The sensor is cooled moreover with a forced flow of cold gas. The CO₂ cooling plant is developed by KEK, while the design for the cooling block/support structure is performed within the collaboration. The impact of the linear collider cooling strategy - based on reducing the power dissipated using a pulsed power supply to the detector and cooling through a forced air flow - is studied. A novel cooling strategy for future applications based on mico-channels in the sensors is being evaluated in the collaboration. Solutions for monitoring of environmental parameters are being developed.

Ancillary ASICs The operation of a DEPFET detector requires ancillary electronics in the form of a read-out ASIC (the Drain Current Digitizer), a steering ASIC (SWITCHER) and on-detector ASICs for digital data processing (DHP). These ASICs are developed within the collaboration.

Data Acquisition and Trigger The development of off-detector electronics to process the data from the Belle II vertex detector.

Characterization of prototypes, laboratory and beam tests This work package has contributions from nearly all institutes involved in the DEPFET collaboration.

Table 1.1: Comparison of ILC and Belle II requirements of a vertex detector

	ILC	Belle II
occupancy	0.13 hits/ $\mu\text{m}^2/\text{s}$	0.4 hits/ $\mu\text{m}^2/\text{s}$
radiation	< 100 krad/yr $10^{11} \text{ MeVn}_{\text{eq}}/\text{yr}$	> 1 Mrad/yr $2 \times 10^{12} \text{ MeVn}_{\text{eq}}/\text{yr}$
duty cycle	1/200	1
frame time	25 – 100 μs	20 μs
momentum range	100 keV – 500 GeV	$<\sim 1 \text{ GeV}$
angular acceptance	6°– 174°	17°– 150°
spatial resolution	excellent: 3 – 5 μm	moderate
pixel size	$20 \times 20 \mu\text{m}$	$50 \times 75 \mu\text{m}$
material budget	0.15% X_0/layer	0.21% X_0/layer

Currently, the construction of the Belle II vertex detector [12] is the main focus of the collaboration. The requirements of the Belle II vertex detector are similar to those of the ILC, and more stringent in some aspects. The Belle II construction project therefore has considerable synergy with developments for a future linear collider. The LC-specific effort is focused on the development of small-pixel devices and the design of a forward vertex detector. We envisage that after the installation of the Belle II detector (2016) the balance between both projects is restored.

1.4.2 Introduction

The DEPFET technology implements amplification within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted high-resistivity silicon wafer. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate. The amplified signal is extracted from the pixel matrix by a numbers of ASICs [13, 14] mounted directly on the sensor: The SWITCHER, Drain Current Digitizer (DCD) [15, 16] and Data Handling Processor (DHP) [17].

The DEPFET in-pixel amplification allows for a comfortable signal-to-noise ratio with a very thin active detector. The reduced sensor thickness of 75 μm for Belle II, 50 μm for the Linear Collider, is the key to remain within the material budget of 0.15% of a radiation length per layer. DEPFET prototypes with $20 \times 20 \mu\text{m}^2$, small enough to meet the stringent spatial resolution specifications of the ILC, have successfully been operated in beam tests [18, 19]. The DEPFET matrix is read out in rolling shutter mode at a rate of 100 ns/row. For the column depths relevant for the ILC and Belle II a frame rate of several tens of μs is achieved [20]. The expected performance of a DEPFET-based vertex detector meets the specifications drawn up by the ILD experiment. DEPFET is also considered as a back-up solution to the SiD concept, in case the single bunch crossing time stamping proves to be out of reach.

1.4.3 Recent Milestones

The concept of a DEPFET active pixel detector for vertex detection at collider experiments was initiated in the linear collider community (for TESLA). The operation principle was extensively proven [18, 19] on small-scale prototypes. A recent reassessment of the DEPFET potential for a linear collider at the energy frontier is found in [20] and in the report [21] for the ECFA detector R&D review in 2014. A large-scale,

$75\text{ }\mu\text{m}$ thin Belle II ladder with the ancillary ASICs integrated on the sensor was successfully submitted to a test in an electron beam at DESY in January 2014[22].

The first full-scale DHP prototype was implemented in IBM 90 nm CMOS technology. As this technology was discontinued, more recent designs were submitted in the TSMC 65 nm CMOS process. DHPT v.1.0 comprises temperature independent current references, 11 bias 8-bit DACs with current output, an integrated temperature measuring system and JTAG control. This design has been successfully tested during early 2014[13].

1.4.4 Engineering Challenges

Vertex detector ladders with a thickness of several tens of microns and a spatial resolution of well below $10\text{ }\mu\text{m}$ require very robust mechanical properties. The power generated by the sensors and ASICs must be removed with the smallest impact on the detector material. Measurements on thin ladders under a realistic load, including pulsed powering according to the ILC beam structure, prove the excellent mechanical properties of the all-silicon ladder [23].

1.4.5 Future Plans

Currently, the construction of the Belle II vertex detector (to be installed by 2016 for the first physics run in 2017) implies a large effort of R&D, including:

- Develop the die-attach technology in a controlled atmosphere required for the mounting of passive components on the DEPFET active pixel detector ladders. The first milestone is a fully integrated electrical prototype based on the EMCM.
- First tests that will determine if all the ASICs on the ladder are fully functional
- The integration of read-out and steering ASICs on the pixel sensor to be performed using a flip-chip technique and so-called bump-bonding, using microscopic solder balls.
- The production of the Belle II vertex detector modules, a joint effort of the DEPFET collaboration
- The test of the last version of the DHP chips

In the near future we hope to characterize the performance of a thin ILC-design prototypes with pixels of $20 \times 20\text{ }\mu\text{m}^2$

- Perform an engineering design for a DEPFET all-silicon module with the required petal geometry
- A detailed characterization of the response of the device
- Design of the ancillary ASICs, taking full responsibility for future design cycles of the Front End read-out chip, the Drain Current Digitizer (DCD) that is relevant to the ILC and a Belle II upgrade. This chip converts the analog signal from the detector to digital and has a crucial impact on the detector performance.

In the longer term the DCD and DHP are envisaged to evolve into a single chip. Being large arrays of DEPFET pixels a promising technology for the vertex detector of the planned ILC, adaptation of the DCD and DHP chips must also be done.

In the near future we hope to characterize the performance of ILC design prototypes with pixels of $20 \times 20 \mu\text{m}^2$. Important experience is furthermore gained with the thermal and mechanical properties of ultra-thin ladders. Measurements on thin ladders under a realistic load, including pulsed powering according to the ILC beam structure, prove the excellent mechanical properties of the all-silicon ladder. A complete mock-up for the innermost disks is under construction.

1.4.6 Applications Outside of Linear Colliders

The concept of a DEPFET active pixel detector for vertex detection at collider experiments was initiated in the linear collider community (for TESLA). The election of DEPFET technology for the Belle II detector therefore represents an important spin-off of linear collider detector R&D. DEPFET is also considered a strong candidate technology for the vertex detector at a future circular collider (<http://cepc.ihep.ac.cn/preCDR/volume.html>). DEPFET detectors are furthermore used for X-ray imaging at the XFEL [24]. Future space missions envisage the use of DEPFET sensors [25]. Their use in microscopy is being studied.

1.5 FPCCD

1.5.1 Collaborating Institutions

1.5.2 Introduction

Fine pixel CCD (FPCCD) is one of the candidate sensor options for the vertex detector of the ILD detector at the ILC [26, 27, 28]. In the present design, FPCCD sensors for the innermost layer of the vertex detector have a pixel size of $5 \mu\text{m}$ and a fully depleted epitaxial layer with a thickness of $15 \mu\text{m}$. Because of the small size of the pixels, the occupancy is acceptably low even if the hits are accumulated for one nominal ILC bunch train (1 ms). The efforts of the FPCCD collaboration are currently focused on pixel characterization and development, while we also pursue developments to the cooling system, electronics downstream of ASICs and the reconstruction software [29].

1.5.3 Recent Milestones

R&D activity for the FPCCD vertex detector at present is mainly focused on FPCCD sensors and a detector cooling system using 2-phase CO_2 . One of the achievements of FPCCD sensors after DBD is the fabrication of real size ($12.3 \times 62.4 \text{ mm}^2$) sensors with $50 \mu\text{m}$ total thickness. Figure 1.1 shows the real size prototype sensor. It has 8 readout nodes, and each channel has different pixel sizes of $12 \mu\text{m}$, $8 \mu\text{m}$, and $6 \mu\text{m}$. We have started a neutron damage test using small ($6 \text{ mm} \times 6 \text{ mm}$) FPCCD prototypes [30]. A prototype sensor was irradiated by a neutron beam of few tens of MeV at the CYRIC facility of Tohoku University. The detailed analysis on the irradiated sensor is still on-going. In order to increase the radiation immunity of FPCCD sensors, particularly to reduce the transfer inefficiency due to radiation damage, the sensors should be cooled down to -40°C . We have started R&D on a two-phase CO_2 cooling system for this purpose. There are several examples of utilizing two-phase CO_2 cooling systems for high energy physics experiments. For these cases, the CO_2 coolant is circulated using liquid pumps. This method is, however, not so efficient for very low temperature cooling of -40°C . Therefore, we adopted a CO_2 gas compressor for the circulation of CO_2 coolant. Figure 1.2 shows a simplified schematic diagram of the system. A prototype system has been constructed, and cooling between -40°C and $+15^\circ\text{C}$ has been successfully demonstrated using this system.

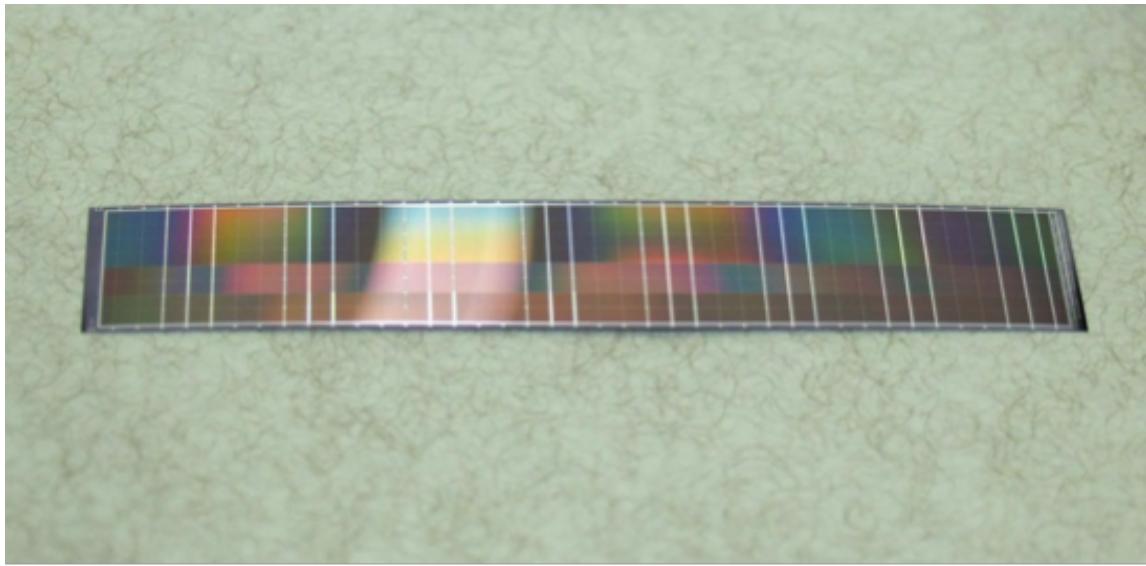


Figure 1.1: Real size FPCCD sensor thinned down to $50 \mu\text{m}$

1.5.4 Engineering Challenges

In the present design of the ILD vertex detector, two sensor layers are mounted on both sides of a light-weight ladder of 2 mm thickness. Our goal of the material budget of this ladder is $0.3\% \text{ X}_0/\text{ladder} = 0.15\% \text{ X}_0/\text{layer}$. This goal would not be so easy to accomplish, and we need a lot of R&D effort. The ladders have to be cooled down to -40°C . We plan to achieve this cooling by heat conduction to the end-plate on which thin cooling tubes for 2-phase CO_2 are attached. The design of this structure is not trivial, and we need R&D including thermal simulation. There are challenges both with the mechanical structure and the electronics circuit for the ladder R&D. We have not started this effort yet.

1.5.5 Future Plans

We have been doing our R&D on the FPCCD vertex detector based on a Grant-in-aid for science research which expires at the end of FY2015. By that time, we plan to carry out the following R&D items:

- Characterization of FPCCD sensors including beam tests and radiation damage tests
- Development of FPCCD sensors with the pixel size of $5 \mu\text{m}$, which is our ultimate goal
- Construction of prototype ladders for inner layers
- Development of readout electronics downstream of ASICs

If new funding is secured in future, the following R&D items have to be done:

- Development of larger FPCCD sensors and prototype ladders for outer layers
- Development of readout electronics which can fit in the small space of real experiment
- Construction of a real size engineering prototype and its cooling test

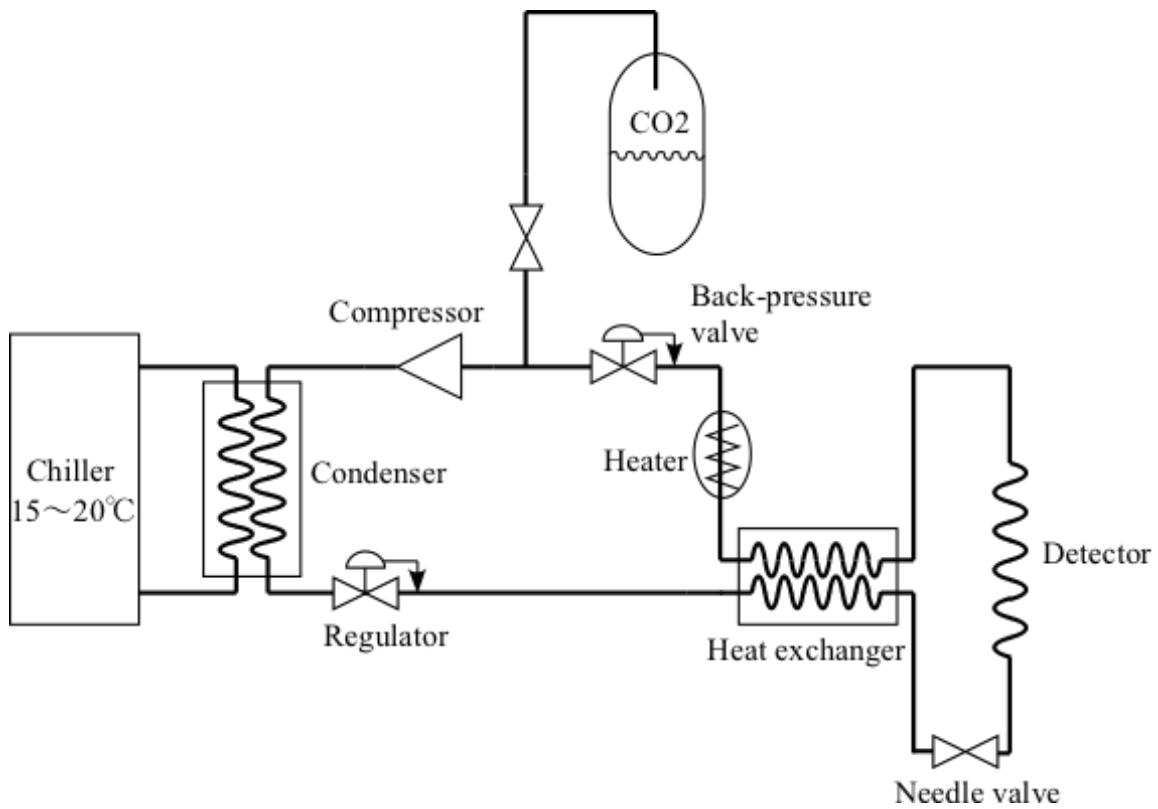


Figure 1.2: A simplified schematic diagram of the two-phase CO_2 cooling system

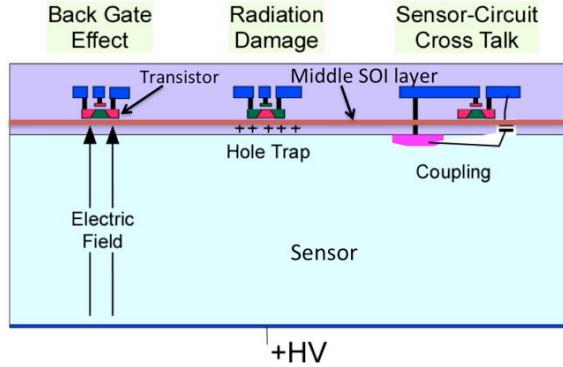


Figure 1.3: Major issues in the SOI pixel detector and introduction of a middle-SOI layer

1.5.6 Applications Outside of Linear Colliders

Because of the relatively slow readout speed, the application of FPCCD sensors to other high energy physics experiments would be limited. However, high spatial resolution of small pixel size must be applicable to measurements of X-ray imaging. Two-phase CO₂ cooling system can be applied to any other detectors which require efficient cooling between -40 °C and near room temperature. Our system, which uses a CO₂ gas compressor, has a great advantage for low temperature operation near -40 °C compared with systems using liquid pumps for circulation.

1.6 SOI

1.6.1 Introduction

1.6.2 Recent Milestones

At present, major issues in the SOI pixel development are “back-gate effect”, “hole trap under the transistors by radiation,” and “sensor-circuit cross talks” as shown in Figure 1.3. For these, we have been developing a double SOI technology. The developed double SOI wafer has an additional middle-SOI(Si) layer under the transistors. The conduction layer of the middle-SOI can solve all the three issues. We could successfully process the double-SOI wafer (Figure 1.4). Threshold shift by radiations is successfully recovered by applying compensating voltage to the middle SOI layer (Figure 1.5).

1.6.3 Engineering Challenges

The impact parameter resolution for the ILC vertex detector is required to be a few μm . This means the pixel size must be less than about $20 \mu\text{m}^2$. On the other hand, each pixel must register arrival time of the hits during bunch train, which requires many transistors and capacitors to be located in each pixel. A solution to this is 3D vertical integration of the circuit layers. SOI technology is ideally suited for 3D integration, since the thinning is stopped at the buried oxide (BOX). We already tried 3D SOI pixel chip in collaboration with T-Micro Co. Ltd. The process flow of micro-bump 3D connection is shown in Figure 1.6. This process achieves a resistance of ($\sim 6 \Omega/\text{bump}$) between upper and lower tiers for 1,000 daisy chain (2,000 bumps) as shown in Figure 1.7. However, to achieve the density of digital circuitry necessary for ILC operations,

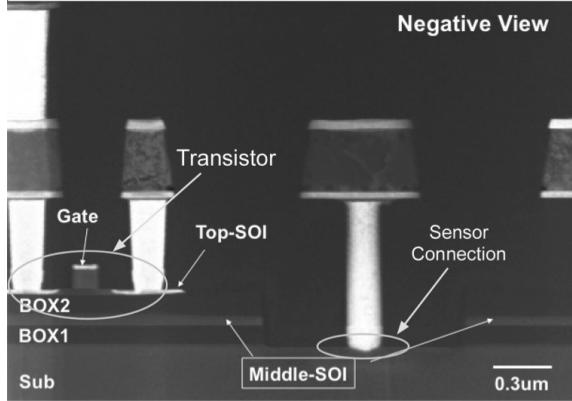


Figure 1.4: Cross section of the double SOI chip after processing

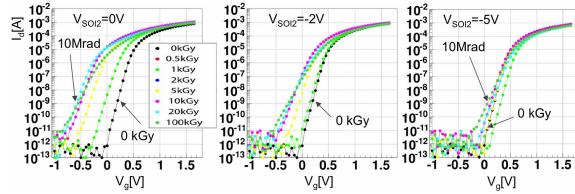


Figure 1.5: Threshold shift recovery by applying compensating voltage (V_{SOI2}) to the middle Si layer

32 nm technology may be necessary for the upper tier in the ILC. This requires bonding of two different technology wafers. The 3D integration of different technology wafers (or chips) is still an engineering challenge.

1.6.4 Future Plans

Detector R&D plans for the coming years; We are planning following items for the coming year.

- Sep. 2014 : Complete architecture study for the ILC pixel detector.
- Mar. 2015 : Design and fabrication of first test chip for the ILC.
- Dec. 2015 : Beam test of the test chip.

1.7 3D Pixel Development

1.7.1 Introduction

This R&D area covers sensors and electronics integrated utilizing 3-dimensional electronics technology. This technology is distinct from 3D sensors and builds on efforts in the electronics industry to stack multiple layers of electronics to form dense assemblies of complex devices. It is important for Particle Physics in that it allows very fine pitch ($4 \mu m$) integration of sensors with multiple layers of electronics, allows

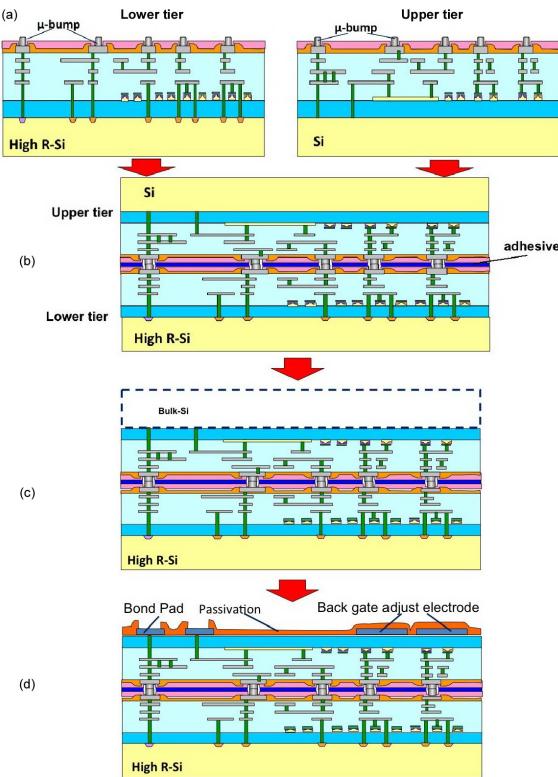


Figure 1.6: Micro-bump 3D integration process flow of the SOI pixel

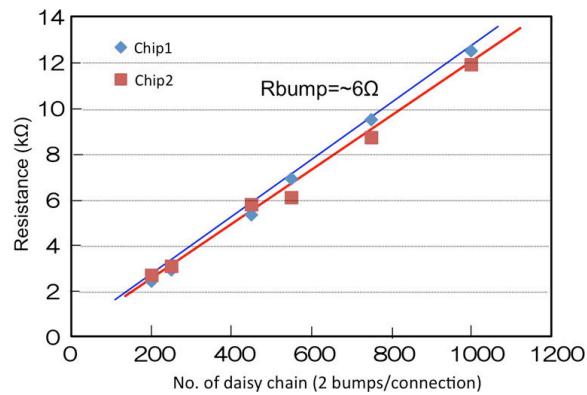


Figure 1.7: Resistance of micro-bump daisy chain between upper and lower tiers

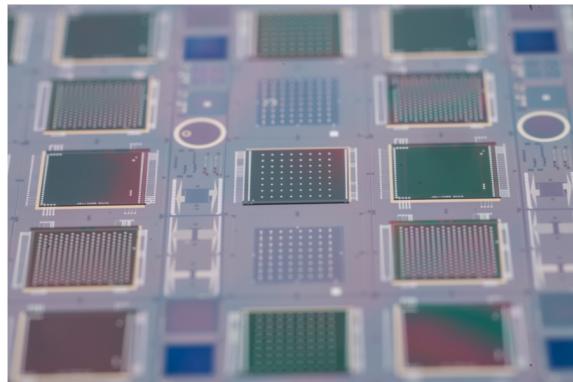


Figure 1.8: 3D chips placed on BNL sensor wafers. VIP is middle left and right

interconnection to both the top and bottom of devices, and provides techniques for low mass, thinned devices. The interconnection of top and bottom means that sensors can be bonded to complex electronics with no wasted area for interconnect and optimal delivery of power and ground.

1.7.2 Recent Milestones

We have completed our multi-year effort to demonstrate commercial 3D technology. This consists of two tiers of $0.13\text{ }\mu\text{m}$ CMOS interconnected with Direct Oxide Bonding (DBI) technology and access using Through-Silicon-Vias (TSV). The DBI bonds are at $4\text{ }\mu\text{m}$ pitch. Fermilab sponsored the first 3D multi-project run for Particle Physics. The wafers were delivered last summer. Fermilab had three chips on the run: VICTR – a CMS track trigger chip, VIPIC – an X-ray imaging chip, and VIP – an ILC vertex chip. Tests of the VIPIC and VICTR have shown working devices. Tests for the VIP chip were delayed due to lack of funding and personnel. We have recently restarted this work and initial tests are promising with the readout token successfully passed through the VIP.

In addition to the development of the 3D chips we have also explored the use of DBI to connect the 3D electronics with sensors. Brookhaven Laboratory fabricated a sensor wafer with regions that mate to the VIP, VIPIC and VICTR chips. The chips are ground to expose the top TSVs and contacts are deposited. The assembly is then attached to a handle wafer and the TSVs which project from the other side are exposed. Wafers are then process for DBI bonding and individual die from the 3D wafer are bonded to the sensor wafer. Finally the top “handle” silicon is ground and etched to reveal the previously formed contacts. The total thickness of the readout at the end of this process is about $25\text{ }\mu\text{m}$ (Figure 1.8). These wafers were received at the end of March 2014 and are being tested. Due to the fact that contacts to a 3D assembly can be made to the body of the die, rather than its edge, no space needs to be reserved for wire bond contacts at the edge. This raises the possibility of fabricating large, complex pixel detector arrays of 4-side butted devices using sensors with active edges. We are in the process of demonstrating this technology utilizing active edge sensors fabricated at VTT and using wafer-to-wafer bonding to a 3D readout wafer. The active edge wafers are based on a silicon-on-insulator stack and thus can be fabricated with essentially arbitrarily thin sensors, in this case $200\text{ }\mu\text{m}$. Sensor and dummy readout wafers have been fabricated and a test wafer is being etched at SLAC. We expect to have DBI bonded assemblies this summer.

1.7.3 Engineering Challenges

Major engineering challenges include:

- Development of widely commercially available 3D technologies. Based partly on our development the silicon brokers CMP, CMC, and MOSIS now include 3D multi-project runs as part of their standard offerings.
- Development of high yield 3D bonded chip-to-wafer devices. This is the subject of our active edge project.
- This development shares with other vertexing technologies the problems of low mass mechanical support, power delivery, and cooling. An SOI-based device can be made thin without special effort. Such thinned device will need low mass backing hybrid circuitry, presumably flex on carbon fiber or a similar technology

1.7.4 Future Plans

- Complete the 3D active edge project
- Apply our concepts to x-ray imaging devices
- ILC developments would await renewed funding in the US.

1.7.5 Applications outside of Linear Colliders

As stated above the technology is already being developed for CMS and x-ray imaging applications. The large area sensor concept is applicable for a variety of focal plane array concepts.

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1.8 CLICpix

1.8.1 Introduction

The precision physics needs at the CLIC TeV-scale linear electron-positron collider require a vertex-detector system with excellent flavour-tagging capabilities through a measurement of displaced vertices in an environment with high rates of beam-induced background events [37]. As a result, the CLIC vertex-detector system needs to have excellent spatial resolution ($3\text{ }\mu\text{m}$), full geometrical coverage extending to low polar angles, extremely low material budget ($0.2\% X_0$ per layer), low occupancy facilitated by time-tagging (10 ns precision), and sufficient heat removal from sensors and readout. A concept based on hybrid pixel-detector technology is under development for the CLIC vertex detector. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin planar sensors or active HV-CMOS sensors via low-mass interconnects. The power dissipation of the readout chips is reduced by means of power pulsing, allowing for a cooling system based on forced gas flow. Through-Silicon Via (TSV) vertical interconnects remove the need for wire bonding connections on the side of the readout ASICs and therefore allow for an efficient tiling to form larger modules with minimal inactive areas.

1.8.2 Recent Milestones

A broad hardware R&D program is in place, addressing the challenges for the CLIC vertex detector in an integrated approach [38]. Recent achievements in the sensor and readout domain include:

Hybrid pixel assemblies with ultra-thin planar sensors Planar pixel sensors with $55\text{ }\mu\text{m}$ pitch and different thicknesses ($50\text{--}300\text{ }\mu\text{m}$) were procured from different vendors and bump-bonded to Timepix [39] readout ASICs (100 and $700\text{ }\mu\text{m}$ thickness). Slim-edge sensor designs are compared to designs with active edges. Preliminary beam-test results show very good efficiencies in both cases, extending beyond the edge pixels [40]. For $50\text{ }\mu\text{m}$ sensor thickness and nominal readout parameters, the fraction of multi-pixel clusters is approximately 20%. Single-point resolutions of approximately $3\text{ }\mu\text{m}$ have been extracted for clusters of two pixels using charge interpolation and taking into account non-linear charge sharing.

CLICpix demonstrator ASIC A CLICpix demonstrator chip has been produced in 65 nm CMOS technology, including a 64×64 pixel matrix and power-pulsing capability [41]. The pixel size is $25\text{ }\mu\text{m}\times 25\text{ }\mu\text{m}$. Simultaneous 4-bit Time-Of-Arrival (ToA) and Time-Over-Threshold (ToT) measurements are implemented in each pixel, allowing for a front-end time slicing with approximately 10 ns and for measuring the charge to improve the position resolution through interpolation. The full chip can be read out in less than $800\text{ }\mu\text{s}$ (for 10% occupancy), using a 320 MHz readout clock and zero suppression. The power consumption of the chip is dominated by the analog frontend with a peak power corresponding to 2 W/cm^2 . The total average power consumption can be reduced to a value below the target of 50 mW/cm^2 by means of power gating for the analog part and clock gating for the digital part. Readout tests have confirmed that the CLICpix demonstrator chip is fully functional and the power consumption and performance are in agreement with simulations [42]. Hybrid modules of CLICpix ASICs with planar slim-edge sensor prototypes are currently in production.

Capacitively coupled active HV-CMOS sensors Hybrid assemblies of CLICpix prototype chips with CCPDv3 active sensors have been produced and tested. The sensors are implemented in a 180 nm high-voltage CMOS process [43]. A deep n-well above the low-resistivity (few Ωcm) p substrate surrounds low-voltage p-wells and acts as the signal collecting electrode. A nominal operation voltage

of -60 V at the n-well results in a depletion layer of approximately 10–20 μm in the p substrate. The fast drift signal collected in this depletion layer passes through a two-stage transimpedance amplifier in each pixel and the resulting voltage signal is capacitively coupled to the CLICpix ASIC through a layer of glue a few microns thick. Laboratory tests with radioactive sources show a good signal-to-noise performance for the active sensor output. Preliminary test-beam results with CLICpix-CCPDv3 assemblies suggest a detection efficiency of > 99% for minimum ionising particles and a high fraction of single-pixel clusters with a position resolution of approximately 7 μm , as expected for 25 μm pixel pitch.

Through Silicon Vias (TSV) A “via last” TSV process developed in collaboration with CEA-LETI has demonstrated the feasibility of TSVs on functional readout ASICs from the Medipix/Timepix chip family [44]. The project uses Medipix3 readout wafers produced in 130 nm CMOS technology. The wafers are thinned to 120 μm and the resulting vias have a diameter of 60 μm . An ongoing continuation of the TSV project aims at producing TSVs in Timepix3 ASIC wafers thinned to 50 μm .

1.8.3 Engineering Challenges

The detector performance requirements lead to challenging constraints for the mechanical and electrical integration of the vertex-detector components and its cooling system. An integrated approach is followed, addressing several of the critical R&D issues in these domains:

Power delivery and power pulsing A low-mass power-pulsing and power-delivery system optimised for the small duty cycle of the CLIC machine has been developed [45]. Controlled current sources deliver a low and almost constant current (< 300 mA per ladder) into the vertex region through low-mass cables. The energy needed by the readout ASICs during the time of the collisions and detector readout is stored locally in silicon capacitors. Low-dropout regulators provide the necessary stability of the output voltage for the analog ($\Delta V \approx 16\text{mV}$) and the digital part ($\Delta V \approx 70\text{mV}$) of the readout ASICs. Prototypes have been tested successfully with dummy loads emulating the power consumption of the 12 readout ASICs in a half ladder. The total contribution of the powering infrastructure to the material budget of each barrel layer is approximately 0.1% X_0 . It is expected to decrease to less than 0.05% X_0 with evolving silicon-capacitor technology.

Cooling Even with power pulsing a total power of approximately 500 W will be dissipated in the vertex detectors alone. To limit the amount of material in the vertex-detector region, a cooling system based on forced air flow is under development [46]. Finite-element Computational Fluid Dynamics (CFD) simulations show that air cooling is feasible. For a mass flow of 20 g/s, the temperature increase in the vertex detector is limited to approximately 40 °C. The proposed cooling scheme is being validated in thermal mockups. Preliminary results confirm the validity of the simulations.

Mechanical supports The low overall material budget leaves only about 0.05% X_0 per detection layer for mechanical supports. Prototypes based on Carbon-Fibre-Reinforced Polymers (CFRP) are under study [47]. Bending-stiffness calculations have been validated in finite-element simulations and with bending tests. Measurements within an air-cooling mockup show that the air-flow induced vibrations are at an acceptable level of approximately 1 – 2 μm RMS amplitude for the direction perpendicular to the detector plane and at nominal flow conditions.

Assembly and access scenarios Assembly and access scenarios for in-situ testing have been developed, taking into account the constraints from the surrounding detector elements [47]. Realistic cabling layouts are proposed and evaluated in terms of their impact on the global and local material budget.

1.8.4 Future Plans

The technical development programme for the CLIC vertex detector aims at building demonstration modules for the main components of the vertex detector system in time for the next update of the European Strategy for Particle Physics in 2018/19. To reach this medium-term goal, several technology prototypes are under development. Ultra-thin edgeless hybrid pixel assemblies with Timepix3 readout ASICs (including ASICs thinned to 50 µm and processed with TSVs) are currently in production. The next version of the CLICpix demonstrator ASIC (CLICpix2) is foreseen to be produced in the second half of 2015. It contains a larger pixel matrix (128×128) and higher dynamic range (8-bit ToA and 5-bit ToT). Slim-edge and edgeless sensors matching the 128×128 CLICpix2 footprint have already been produced and an improved version of the CCPD active HV-CMOS sensor will be submitted for production by the end of 2015.

1.8.5 Applications Outside of Linear Colliders.

The CLIC vertex-detector R&D shares its main challenges of simultaneously achieving small pixel pitch, low material budget and fast timing with other future pixel detector projects, such as the developments for the upgrades of the LHC detectors for high-luminosity operation or for future circular colliders. Synergies with these projects are exploited for example in the context of the RD53 collaboration for 65 nm hybrid readout ASICs [48] and via the AIDA2020 project for Advanced European Infrastructures for Detectors at Accelerators [49]. Moreover the CLICpix ASIC is derived from the Timepix/Medipix family of hybrid readout ASICs [50], which have a wide range of applications in medical imaging and material science.

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
ChronoPix	University of Oregon Yale University Sarnoff Corporation	ChronoPix is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps per pixel	April 2014: Device tests of prototype 2 inform the design of prototype 3 to be submitted to foundry	Improve S/N to at least 20 Further reduce pixel size from 25 µm to eventually 15 µm. Requires feature size less than 65 nm Reduce inter-pixel and digital-to-analog circuit cross talk and parasitic feedback
CMOS MAPS	IPHC Strasbourg DESY, Hamburg University of Bristol University of Frankfurt	The CMOS pixel sensor uses as a sensitive volume the 10–20 µm thin high-resistivity epitaxial Si-layer deposited on low resistivity substrate of commercial CMOS processed chips. The generated charge is kept in a thin epi-layer atop the low resistivity silicon bulk by potential wells that develop at the boundary and reaches an n-well collection diode by thermal diffusion.	2016 : production of CPS for the ALICE-ITS upgrade 2018/19 : production of CPS for the micro-vertex detector of the CBM experiment at FAIR/GSI 2018/19 : validation of light double-sided ladder concept combining highly granular sensors on one side with timestamping sensors on the other side < 2020 : validation of power pulsing of double-sided ladders inside a high magnetic field 2022/23 : finalisation of the R&D on various CPS adapted to the different layers of a very high performance vertex detector at the ILC	Until 2018-2019: Development and production of CPS for the ALICE-ITS and CBM-MVD Development of various CPS optimised for the different layers of a vertex detector at the ILC, with emphasis on bunch tagging Development of low material double-sided ladders
DEPFET	University of Barcelona, Spain University of Bonn, Germany Heidelberg University, Germany Giessen University, Germany University of Göttingen KIT Karlsruhe, Germany IFJ PAN, Krakow, Poland MPI Munich MPG HLL Munich, Germany Charles University, Prague, Czech Republic IFIC, CSIC-UVEG, Valencia, Spain DESY, Hamburg, Germany IFCA, CSIC-UC, Santander, Spain	The DEPFET technology implements a single active element within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted, detector-grade bulk silicon. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate.	2014: Full-scale 75 µm thin Belle II ladder in beam test at DESY	Development of die-attach technology Full-scale test of all ASICs on ladder Integration of read-out and steering ASICs on pixel sensor using flip-chip technique and microscopic solder ball bump-bonding Production of Belle II vertex detector modules Tests of the last version of the DHP chips Engineering design for all-silicon module with petal geometry required for ILC Detailed characterization of device response Design of ancillary ASICs, taking full responsibility for future design cycles of the FE read-out chip, called Drain Current Digitizer
FPCCD	KEK Shinshu University Tohoku University JAXA, Japan Aerospace Exploration Agency	Fine Pixel CCD sensors have pixel sizes of 5 µm and a fully depleted epitaxial layer with a thickness of 15 µm	Fabrication of real size (12.3 mm × 62.4 mm) sensors with 50 µm total thickness Neutron irradiation of a small (6 mm × 6 mm) FPCCD sensor Construction of a prototype cooling system and demonstration of cooling between -40°C and +15°C	Characterization of FPCCD sensors including beam tests and radiation damage studies Development of FPCCD sensors with a pixel size of 5 µm Construction of prototype ladders for the inner layers of a vertex detector Development of readout electronics downstream of ASICs Development of larger FPCCD sensors and prototype ladders for outer layers Development of readout electronics with a small footprint Construction of a real size engineering prototype and cooling test
3D Pixels	Brown University Cornell University Fermilab Northern Illinois University SLAC University of Illinois Chicago	3D technology allows very fine pitch (4 µm) integration of sensors with multiple layers of electronics, allows interconnection oto both the top and bottom of devices, and provides techniques for low mass, thinned devices.	Completed multi-year effort to demonstrate commercial 3D technology, consisting of 0.13 CMOS interconnected with Direct Oxide bonding technology and access using TSV. Received readout wafers with thickness of 25 µm, processed with TSV and DBI to connect to 3D electronics Currently working on active edge demonstrator devices	Complete the 3D active edge project Apply concepts to x-ray imaging devices Re-start ILC developments pending renewed funding
SOI	KEK University of Tsukuba Tohoku University Osaka University	In the Silicon-On-Insulator (SOI) technology the sensing and processing functionalities are separated in different layers; the sensing is provided by a high-resistive substrate connected through an insulating layer with the processing layer.		Sep 2014: Complete architecture study for the ILC pixel detector Mar 2015: Design and fabrication of first test chip for the ILC Dec 2015: Beam test of the chip
CLICpix	Cambridge University CERN University of Geneva Karlsruhe Institute of Technology (KIT) University of Liverpool SLAC Institute of Space Science Bucharest Spanish Network for Linear Colliders	Hybrid pixel-detector technology comprising fast, low-power and small-pitch readout. ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin planar or active HV-CMOS sensors via low-mass interconnects.	Beam tests of prototype assemblies with ultra-thin sensors (50–300 µm) CLICpix demonstrator ASIC in 65 nm technology Beam tests of assemblies with capacitive coupling between CCPDv3 HV-CMOS active sensors and CLICpix ASICs Power-pulsing demonstrator with dummy loads Prototypes of carbon-fibre ladder supports Full-scale thermal mockup of the CLIC vertex-detector region	Demonstration modules for all major components in time for the next update of the European Strategy for Particle Physics in 2018/19

Chapter 2

Silicon Trackers

2.1 SCIPP Tracking R&D

2.1.1 Introduction

2.1.2 Recent Milestones

2.1.3 Engineering Challenges

2.1.4 Future Plans

2.1.5 Applications outside Linear Colliders

SCIPP has been involved in Linear Collider tracking R&D for a number of years, and its work has led to the development of a refined understanding of several generic tracking issues with potential applications for Linear Collider detectors. These include the use of resistive strips and dual-end readout for the determination of the longitudinal coordinate of the charge deposition on narrow electrodes [51] and limitations on silicon microstrip ladder length for precision narrow-strip sensors [52]. These studies are in fact dependent only on the properties of the electrode that collects the signal and propagates it to the readout electronics, and thus are independent of the sensor technology that generates the signals. Thus, this work may have relevance to detection issues across a wide array of fields. Ongoing tracking R&D is focused on the further development of the Long Shaping-Time Front End (LSTFE) microstrip readout ASIC. The properties of this ASIC have been explicitly optimized for the readout of long ladders of silicon strip sensors that are motivated by the need for precise low-mass central tracking for a Linear Collider Detector. With a small and straightforward change to the shaping properties of the ASIC, it could be re-optimized for use for the short strips and high occupancy that would be expected for ILC forward-tracking applications. Similar to most ILC-oriented readout designs, the LSTFE features a long shaping time optimized to reduce voltage-referenced readout noise, as appropriate for narrow-strip, long-ladder applications. Unique to the LSTFE design, however, is the use of time-over-threshold readout to estimate the analog pulse-height generated by subatomic particles passing through. A pulse-development and readout simulation developed at SCIPP suggests that the intrinsic statistical fluctuations of the charge-deposition process in 300 μm of silicon obviate the need for a precise measurement of deposited charge. A simulation of the centroid-finding (position-resolution) uncertainty provided by time-over-threshold readout showed little



Figure 2.1: Fractional pulse-height uncertainty (percent) versus injected charge (fC) for the LSTFE front-end ASIC. The development of this ASIC has been done solely at the Santa Cruz Institute for Particle Physics (SCIPP) within the University of California at Santa Cruz, and while slowed significantly due to the loss of support for Linear Collider Detector R&D, continues within SCIPP. Tasks that remain in developing a chip suitable for use in a Linear Collider Detector include the development of the digital back end; significant progress has already been made in defining the architecture of this section of the chip and in implementing this architecture in prototype form on an FPGA. Power cycling (switching the chip into a low-power quiescent mode for most of the 199 ms between beam crossings) also needs to be implemented.

degradation relative to that provided by an exact measurement of deposited charge. On the other hand, there are several advantages offered by the use of time-over-threshold readout. It is very simple to implement within a digital back-end to the LSTFE’s analog front end (the implementation would be on the same chip as the front-end readout), requiring only a measurement of the number of clock counts that the given channel is over threshold, and then the assembly and transmission of a single data word containing the time of the upward transition, the time over threshold after the transition, and the channel number. This happens in real time and is driven immediately off the chip into the DAQ, eliminating the need for buffering and ADC conversion. In particular, there is no limit to the rate at which particles can be detected other than the return-to-baseline of the analog signal, and so the data-accumulation rate capability of the device is very high. In addition, for forward tracking, for which short strips are envisioned, the shaping time can be shortened significantly. This will further improve the rate capability of the LSTFE readout, making it an excellent choice for the high-occupancy forward region. Figure 2.1 shows the measured fractional charge uncertainty for the LSTFE prototype ASIC; for depositions expected from minimum-ionizing particles (1 – 4 fC) the fractional charge measurement uncertainty is approximately 15%, which is small compared to the intrinsic fluctuations that arise from the deposition process.

References

- Jerome K. Carman et al. “Longitudinal resistive charge division in multi-channel silicon strip sensors”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 646.1 (2011), pp. 118–125. ISSN: 0168-9002
- Kelsey Collier et al. “Microstrip electrode readout noise for load-dominated long shaping-time systems”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 729 (2013), pp. 127–132. ISSN: 0168-9002

2.2 KPIX

2.2.1 Introduction

KPiX is a 1024 channel “System on a Chip” intended for bump bonding to large area Si sensors, enabling low multiple scattering Si strip tracking and high density Particle Flow calorimetry for SiD at the International Linear Collider (ILC).

Each channel consists of a dynamically switchable gain charge amplifier; shaping; threshold discrimination; and 4 sample and hold capacitors and 4 timing registers. The chip permits 4 separate measurements of amplitude and time of threshold crossing during each train, and amplitude digitization and readout during the intertrain period. The dynamic range is from sub minimum ionizing particle (mip) (in 320 μm silicon) to more than 2000 mip. KPiX also has a calibration system for each channel, servos for leakage compensation, “DC” reset for asynchronous operation for testing with cosmic rays, and polarity inversion for use with GEMs and similar detectors. The noise floor is about 0.15 fC (\approx 1000 electrons), and the maximum signal is 10 pC (utilizing the dynamic range switching). The full dynamic range corresponds to 17 bits.

2.2.2 Recent Milestones

ILC related R&D in the US is largely unfunded and small efforts are being kept alive on the margins. The KPiX R&D is such an example of necessary work for SiD that is marginally alive.

2.2.3 Engineering Challenges

At this time, KPiX is seen as the baseline readout system for the tracker and electromagnetic calorimeter. A stack of 13 EMCal sensors with bump bonded KPiX was assembled for a beam test at SLAC in the summer of 2013. That test discovered that two kinds of crosstalk are significant:

- In-time crosstalk occurs due to parasitic coupling of traces on metal 2 of the sensor to other pixels. The level of crosstalk increases with the size of the signal, and decreases with increased speed of the front end charge amplifier (meaning increased current and power dissipation). A new sensor design is being developed that uses metal 1 to shield the traces of metal 2, and these ideas will be tested in the next sensor prototype.
- Out-of-time cross talk occurs when many pixels are hit and reset simultaneously. The resets collectively cause other pixels to trigger, and a cascade builds up. This uses up all the KPiX buffers. The root cause of the problem appears to be some internal logic within KPiX that is not current limited, and will require design modification.

A more general issue is that both the EMCal and tracker sensors from Hamamatsu were ordered with Al pads, as it was believed that plating (by the zincate process) a stack of metals culminating with Au would be straightforward. This turns out to be wrong. Future sensors will be ordered with Au pads.

An additional issue is that the Tracker sensor was planned to be wire bonded to its (very thin) cable. The sensor oxide layer is not strong enough to allow wire bonding without damage, and so must be solder bumped. The pad pitch is small, and solder bumping the cable will be challenging. The trouble with the wire bonding to the sensor was unexpected. Another concern is that the current design of KPiX has deadtime after a pixel has accepted a trigger. Only the triggered pixel is affected; all the other pixels are available for signals. This deadtime is different from the usual notion of data acquisition deadtime where the entire detector is unavailable, but the correction to the luminosity integral is easy. Finally, the buffer requirement (4 in the current version of KPiX) is being re-evaluated in SiD simulations. A possible new architecture for KPiX is in early stages of evaluation. A small mechanical engineering effort has started to study the structure of the EMCal. The SiD EMCal has emphasized thin gaps between the tungsten layers to minimize the Moliere radius, and this implies that the structure is connected by columns at the vertices of the sensors. The DBD design shows hexagonal sensors, which indeed are the most efficient way of tiling large areas, but no consideration was given to the edges of these arrays. The design is being re-evaluated to optimize the cost-effectiveness over the whole area taking into account geometric efficiencies and total wafer cost. Tracker sensors are now at IZM for the pad plating and subsequent bonding of KPiX; they will then go to UCD for cable attachment and testing.

2.2.4 Future Plans

Assuming positive developments with Japan are announced soon, we expect the financial support to improve. It should be noted that an important effect of the withdrawal of support is that most of the US collaborators have been forced to move to other work.

- EMCal Sensors: A second round of prototypes will be designed and ordered with rectangular layout; shielded traces, and Au pads.
- Tracker Sensors: The current prototypes will be evaluated, and if appropriate tested in a beam.
- KPiX: A new architecture with little (or no) deadtime will be evaluated. A decision will be made to develop this new architecture or incrementally.
 - improve the existing design.
- The EMCal mechanical structure will be pushed towards a conceptual design.

2.2.5 Applications Outside of Linear Colliders

This work represents a significant step in the aggressive integration of silicon sensors with readout electronics, just short of integrating the electronics directly into the sensors. It has prompted consideration of this approach by CMS for calorimetry and by ATLAS for a muon system. It may have applications in sensors for light sources as well as other particle physics detectors.

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
KPIX				
LSTFE				

Chapter 3

Gaseous Trackers

3.1 Time Projection Chamber – Bonn

3.1.1 Introduction

The University of Bonn is studying the pixelized readout of a TPC for the ILD detector. The readout is based on the Timepix ASIC with a triple GEM or Micromegas based gas amplification.

3.1.2 Recent Milestones

The first studies were based on the triple GEM setup with a single Timepix chip. This readout was mounted in a small test detector in the Bonn laboratory. Here, the working principle was tested with a long drift distance. It could be demonstrated that the transverse spatial resolution of the reconstructed primary electrons was close to the expected diffusion limit of single electrons. The results are summarized in the following publications:

- C. Brezina et al. “Operation of a GEM-TPC With Pixel Readout”. In: *Nuclear Science, IEEE Transactions on* 59.6 (Dec. 2012), pp. 3221–3228. issn: 0018-9499
- J. Kaminski et al. “Time projection chamber with triple GEM and pixel readout”. In: *Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE*. Oct. 2008, pp. 2926–2929
- C Brezina et al. “A Time Projection Chamber with triple GEM and pixel readout”. In: *Journal of Instrumentation* 4.11 (2009), P11015
- Jochen Kaminski et al. “Time projection chamber with triple GEM and highly granulated pixel readout”. In: *Conf.Proc. C0908171* (2009), pp. 533–535
- Peter Schade and Jochen Kaminski. “A large {TPC} prototype for a linear collider detector”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 628.1 (2011). {VCI} 2010 Proceedings of the 12th International Vienna Conference on Instrumentation, pp. 128–132. issn: 0168-9002

The new focus are GridPix based detectors, where the gas amplification stage is a Micromegas produced in a postprocessing technique, which guarantees a high quality grid well aligned with the readout pixels.

This approach was pioneered by NIKHEF and the University of Bonn has modified the production process together with the Fraunhofer Institut IZM so that a wafer-based production of GridPix detectors is standard by now. The new GridPixels were tested on small prototype detectors and also assembled in an 8 GridPix module for the Large Prototype detector at DESY. A successful test beam campaign was performed last year.

- M Lupberger. "The Pixel-TPC: first results from an 8-InGrid module". In: *Journal of Instrumentation* 9.01 (2014), p. C01033
- W.J.C. Koppert et al. "GridPix detectors: Production and beam test results". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 732 (2013). Vienna Conference on Instrumentation 2013, pp. 245–249. ISSN: 0168-9002

The current work is focused on a new LP module with about 100 GridPixels. This module is a demonstrator that larger areas (400 cm^2) can be produced and operated. It shall be tested in the LP at the beginning of next year. For this a number of challenges have to be coped with. In particular commercial readout systems are not easily scalable. This is why Bonn has developed a cheap and easily expandable system based on the Scalable Readout System (SRS) of the RD51 collaboration. In addition Bonn is developing the software for reconstructing and analyzing the test beam and simulation data. For this the LCTPC software framework of MarlinTPC is used.

- Jason Abernathy et al. "MarlinTPC: A common software framework for TPC development". In: *Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE*. Oct. 2008, pp. 1704–1708

Finally, Bonn also takes part in designing new pixel chips. To test the new digitization and readout techniques two test chips were designed in collaboration with N'IKHEF. Then Bonn also contributed to the design of the Timepix successor chip, Timepix3, which is being tested now:

- A Kruth et al. "GOSSIPO-3: measurements on the prototype of a read-out pixel chip for Micro-Pattern Gaseous Detectors". In: *Journal of Instrumentation* 5.12 (2010), p. C12005
- C. Brezina et al. "GOSSIPO-4: Evaluation of a Novel PLL-Based TDC-Technique for the Readout of GridPix-Detectors". In: *Nuclear Science, IEEE Transactions on* PP.99 (2014), pp. 1–1. ISSN: 0018-9499
- Y Fu et al. "The charge pump PLL clock generator designed for the 1.56 ns bin size time-to-digital converter pixel array of the Timepix3 readout ASIC". in: *Journal of Instrumentation* 9.01 (2014), p. C01052

3.1.3 Engineering Challenges

The production of a module with 100 GridPixels requires 4 main components: The production of a large number of GridPixels with sufficiently good quality. This has been addressed by the new production method and a large batch is being produced. The challenge of the readout is being addressed by the new readout system. Finally the distribution of the LV power to all ASICs and the cooling of the ASICs still are unclear, but since both challenges are similar for most readout electronics, standard solutions are expected to be adequate.

3.1.4 Future Plans

On a short term the production of the 100 ASIC module is the main goal at Bonn. If this module has been successfully operated, we are interested in replacing the Timepix ASIC by the Timepix3 ASIC and produce

GridPix detectors with this improved chip. There are also some ideas of how to improve the grid structure and make it more reliable. Finally, the reconstruction and analysis software needs further improvement and has to be extended, so that simulated data for the final TPC (i.e. 10,000 hits per track) can be studied.

3.1.5 Applications Outside of Linear Colliders

A single InGrid detector will be installed this year in the CAST experiment for axion search. For a CLIC-TPC a highly granular (i.e. pixelized) readout structure is mandatory to lower the occupancy.

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
GEM				
Micromegas				

Chapter 4

Calorimeters

4.1 Scintillator Strips

4.1.1 Introduction

The CALICE scintillator strip-based ECAL (ScECAL) uses a scintillator strip structure to deliver the granularity and resolution required of an ILC detector. Each strip is individually read out by a Multi Pixel Photon Counter (MPPC, a silicon photon detector produced by Hamamatsu Photonics KK [64]). Although plastic scintillators have been widely used in calorimeters, this is the first time that a highly granular calorimeter has been made using scintillator strips. Such an ECAL has a smaller cost than alternative technologies using silicon sensors (e.g. [65]). The MPPC has promising properties for the ScECAL: a small size (active area of $1 \times 1 \text{ mm}^2$ in a package of $2.4 \times 1.9 \times 0.85 \text{ mm}^3$), excellent photon counting ability, low cost and low operation voltage (70 V), with disadvantages of temperature-dependent gain, saturation at high light levels, and the dark noise rate. The use of tungsten absorber material minimises the Moliere radius of the calorimeter, an important aspect for the effective separation of particle showers required by PFA reconstruction. The chosen strip geometry allows a reduction in the number of readout channels, while maintaining an effective granularity given by the strip width, by the use of appropriate reconstruction algorithms. One such algorithm, known as the Strip Splitting Algorithm [66], has been developed and demonstrated to perform well in jets expected at ILC.

4.1.2 Recent Milestones

- introducing a new scintillation light readout scheme, with different scintillator strip shape by having better homogeneity
- photo-sensor of increased number of pixels in $1 \text{ mm} \times 1 \text{ mm}$, this leads larger dynamic range for the calorimeter
- more experience on the FE read out board and ASICs

They are not published yet, instead some proceedings

4.1.3 Engineering Challenges

- wrapping the scintillator strip and align them on the FE read out layer automatically
- mass test facility for the read out layer

4.1.4 Future Plans

- deciding on the scintillator layer: shape of scintillator strip, how to read out scintillation light, the location of photo-sensor, size and shape of photo-sensor and mass production scheme
- developing photo-sensor with Hamamatsu photonics company, to have larger dynamic range and mass test scheme
- establish a detector fabrication plan

4.1.5 Applications Outside of Linear Colliders

- photo-sensor named MPPC from Hamamatsu Photonics KK is employed for the T2K experiment, CMS upgrade (HC-CAL), Belle II detector (end-cap muon)
- PET and SPECT development

4.2 Silicon-Tungsten ECAL in ILD

4.2.1 Introduction

The silicon-tungsten electromagnetic calorimeter for ILD aims to develop a highly granular detector optimized for particle flow performance. The calorimeter uses a sandwich architecture with $5 \times 5 \text{ mm}^2$ silicon pads as active elements embedded in an alveola structure made of tungsten. The group is active in the development of simulation software and algorithms for calorimeter reconstruction, as well as engineering for the design, and fabrication of the readout chips.

4.2.2 Recent Milestones

The work is now focusing on the construction of a technological prototype. This is a new milestone after the successful operation of the “Physics Prototype” in the years 2004–2011, including large scale beam tests at DESY, CERN at FNAL and data analysis [67]. An analysis of data recorded in 2007 [68] gives confidence that embedding the front end electronics into the calorimeter layers does not compromise the detector performance.

For the technological prototype, the SKIROC ASIC will be embedded into the calorimeter layers and mounted on 9 layer PCBs that will be as thin as 1.5 mm. Silicon wafers, the PCB and the 16 mounted circuits constitute the Active Signal Units or ASUs. Up to ten of these ASUs will be assembled to form a calorimeter layer. The technology of the interconnections was applied with success to first units of the technological prototype.

A series of beam tests with simplified ASUs have been carried out in the years 2012 and 2013 at DESY. The analysis of these data validated the concept of the front end electronics but will also allow for correcting a small number of shortcomings of the SKIROCs ASIC. These will be corrected in the version SKIROC2b

that is supposed to be produced at the end of 2014. A paper on the analysis of the 2012 data has been submitted to JINST in March 2014. Particularly in summer 2013 (i.e. Post-DBD phase), the SKIROC ASIC has been operated in power pulsed mode. For this bias currents of the ASIC are shut down and raised with a given frequency (5 Hz for ILC, 10 Hz in our beam tests). The good agreement between the MIP spectra obtained in power pulsed and conventional mode (see e.g. [69]) give confidence that this technology can indeed be applied for a calorimeter at a linear collider and more precisely at the ILC. More studies are needed as the technological prototype grows in size.

Other recent accomplishments include:

- R&D on scalable technology for all the involved large detector aspects (integration of embedded readout chips, on thin supporting electronics boards, in self-supporting tungsten–carbon mechanical elements ensuring the cooling and protection; all made of exchangeable elements with a quality control procedure; the associated DAQ).
- Realization of a large self-supporting W–Carbon fiber structure with integrated stress monitoring (using Fiber Bragg Grating)
- Beam tests of base sensor units of the technological prototype
- Submission of a paper on the analysis of 2012 beam test data to JINST [70],[71].
- Reconstruction tools adapted to the high granularity calorimeters (photon reconstruction [GARLIC], Advanced clustering [ARBOR], event displays [DRUID])
- Operation of SKIROC [72] in pulsed power mode (with 5 Hz as foreseen by ILC baseline and with 10 Hz as envisioned in high luminosity operation).
- SiECAL test beam experiments were carried out in Jul. 2012, Feb. and Jul. 2013 to test the SiECAL technological prototype. The front-end electronics of the prototype was integrated into an active layer to realize a highly granular calorimeter. In the 2012 test beam, we operated six layers under a continuous current mode. The achieved signal to noise ratio was greater than 10 with SKIROC2 ASICs. In the 2013 test beams, we successfully operated and took data with the prototype under a power pulsing mode. At the same time, we found several issues related to the power pulsing operation. Digital lines on the front-end electronics disrupts analog signals. We had to wait 600 μ s for the electronics to stably take the data. We measured pedestal signals in a magnetic field, and confirmed that active channels were working in stable up to 2 T.

As for the R&D of silicon sensors, we measured several new samples with different guard ring types. It is known that a Si sensor makes small fake signals along with its sensor edge when a large amount of current is generated by an electromagnetic shower in a calorimeter. If the fake signal is reasonably small, we can use the Si sensor for the ILD. To test the fake signal, we introduced an infrared laser system in Kyushu University to measure the Si sensor response with a similar condition of beam test in a laboratory scale. We are setting up a multi-pixel readout system without SKIROC2 ASIC. We can then measure the intrinsic Si sensor properties with the IR laser system. Studies on the SiECAL optimization have been performed with full ILD detector simulation. We performed simulation studies with different setting of PCB thickness, dead volume related the sensor edge, and fraction of dead channels. We found:

- The PCB thickness does not change the performance of the jet energy resolution.
- The dead volume proportionally degrades the performance, but the current Si sensor design is acceptable.

- The fraction of dead channels does not much degrade the jet energy resolution up to the fraction of 5%.

4.2.3 Plans of the near future

The different units of the SiW Ecal for the ILD detector need to be assembled into detector layers of up to two meter in length comprising up to 10 detection units dubbed ASUs. For this we propose to develop an assembly line, incorporating the reception and the test of the material, the alignment of the ASUs and the interconnection, with a continuous monitoring for quality control purposes. The deliverable is a still manual assembly bench capable for a small production of layers. Based on the manual assembly bench we will propose an automatized system for mass assembly together with industrial partners. A survey to search for partners is part of the proposal. A goal is to design the system such that it can be easily duplicated at other sides. In the ideal case the assembly bench is versatile enough to reply to needs for other detector systems than ILD (e.g. CMS). Other Detector R&D plans include:

- Test beam experiments with long SiECAL slabs using new front-end electronics with SKIROC2 ASICs,
- Completion of the SKIROC3 ASIC, which has all the features needed at the ILC.
- Combined test beam experiments with ScECAL and AHCAL,
- Development a DAQ system (set up of hardwares, development of software and firmware) for the combined tests.
- Further R&D of silicon sensors, using the IR laser system, to determine the final design.
- Irradiation test with several types of Si sensors.
- Looking for Japanese companies which can produce SiECAL front-end electronics in prospect of mass production.
- Further optimization of SiECAL and Hybrid ECAL with full ILD detector simulation.

4.2.4 Engineering Challenges

The following challenges will have to be addressed when proposing this technology for an ILC detector:

- Silicon wafer cost reduction when used for calorimetry; direct contact with producers established (Hamamatsu, On-Semi, ...).
- A chip with the good dynamic, noise, power dissipation (using power pulsing), etc.
- Integration in a compact device, ensuring all the requests (precision: electronic and mechanic, heat production, reliability)
- Industrialization of solutions; scalability of tests for a 100M channel detector.

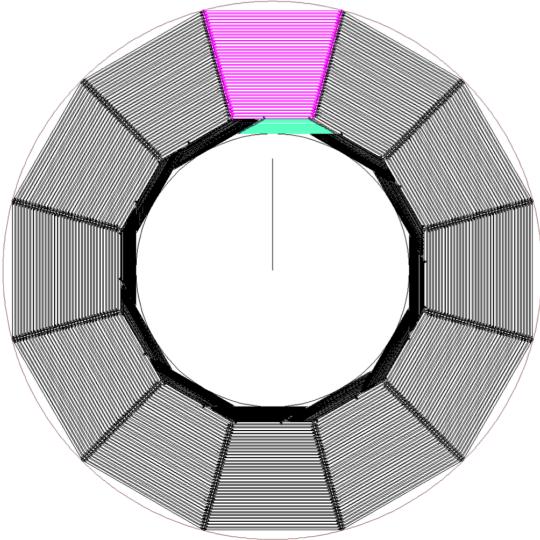


Figure 4.1

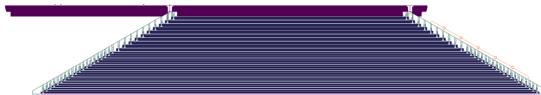


Figure 4.2

4.2.5 Applications Outside of Linear Colliders

- CEPC, TLEP and CMS upgrade have possible applications for this technology
- The compact Silicon-W design has been used in the PAMELA satellite (very similar to physics prototype) [73]

4.3 Silicon Tungsten SiD ECAL

This note describes the theory of the mechanical aspects of the E-Cal system for SiD. The E-Cal barrel consists of stacks of tungsten heavy metal plates which are arranged in modules surrounding the beamline. Full cylindrical coverage of the baseline design is attained with twelve modules (see Figure 4.1) occupying a radial envelope from 1265 mm to 1409 mm. The total barrel length is 3.53 m. Each module uses 20 inner plates which are 2.5 mm thick followed by ten 5 mm thick plates. Gaps between adjacent plates are 1.25 mm and house the silicon detectors with their associated cables (see Figure 4.2). These hexagonal silicon detectors are electrically connected to each other with thin, flexible circuits which are read out on both ends of a module (see Figure 4.3). Panels of detectors increase in width as they get closer to the beamline. To minimize silicon waste and to maximize coverage, fractions of hexagons complete the panel edges (see Figure 4.4). By cutting the silicon in strategic locations, only a few different silicon shapes may be needed to achieve the 31 different panel widths. The tungsten plates are connected together on their longitudinal edges as well as in the field of detectors. Space for fasteners in the field is achieved by chamfering the corners of the hexagonal detectors. The field fasteners hold the plates together, provide a uniform 1.25 mm standoff height, and assist with inter-plate shear. The fasteners near the edges of the plates close the module profile and lend torsional rigidity to the structure. An FEA simulation of the proposed configuration should be done to properly size the fasteners (see Figure 4.5). The modules, which weigh about 5 tons each, are mounted to stainless plates which are used as the first layer of the next detector system (H-Cal). This

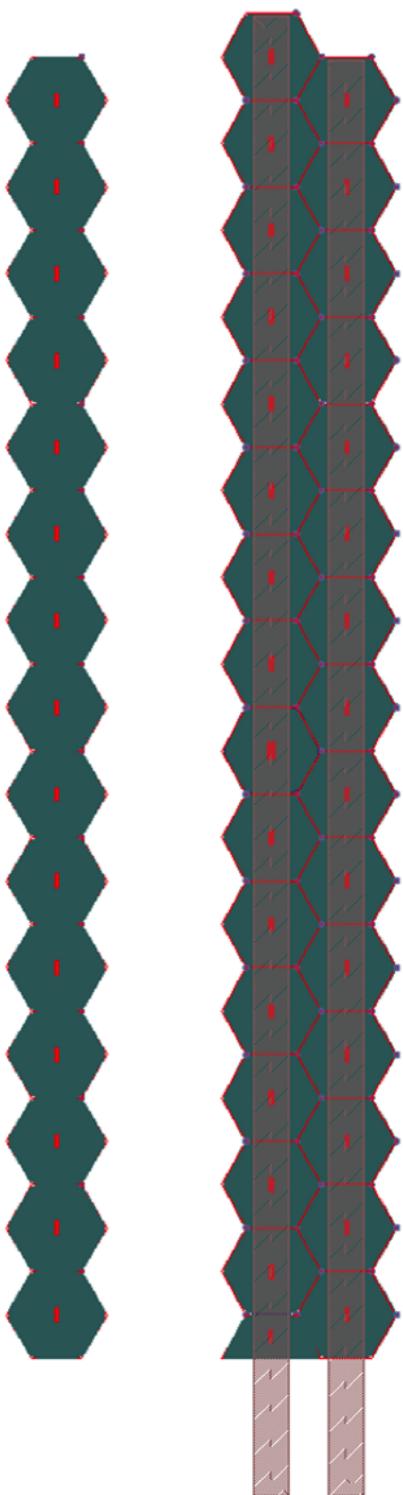


Figure 4.3

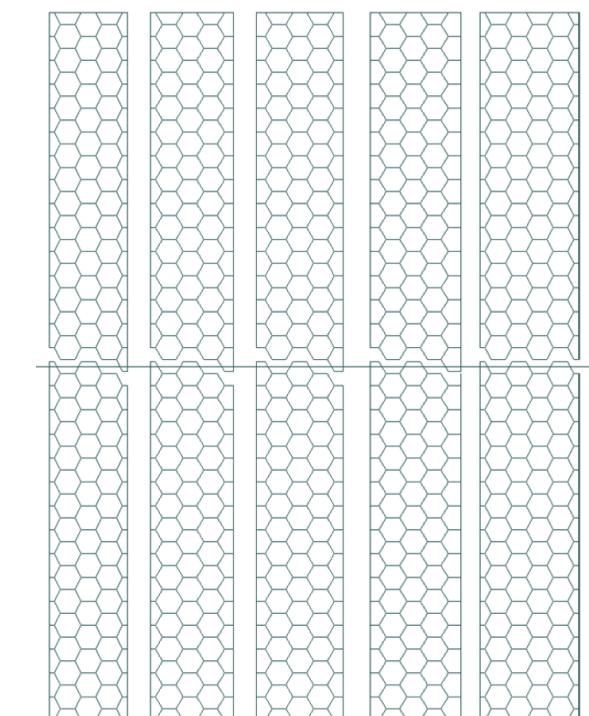


Figure 4.4

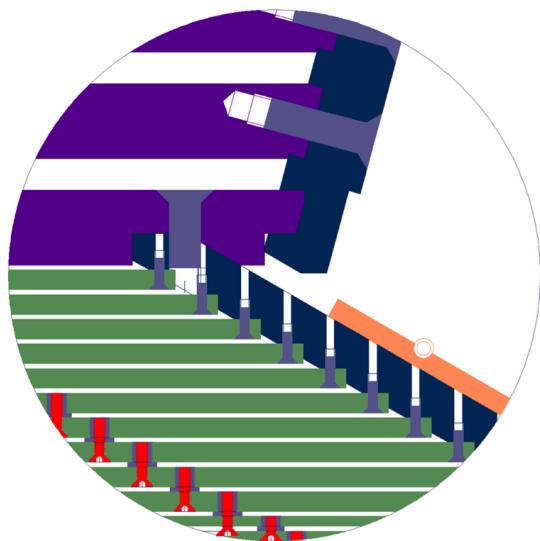


Figure 4.5

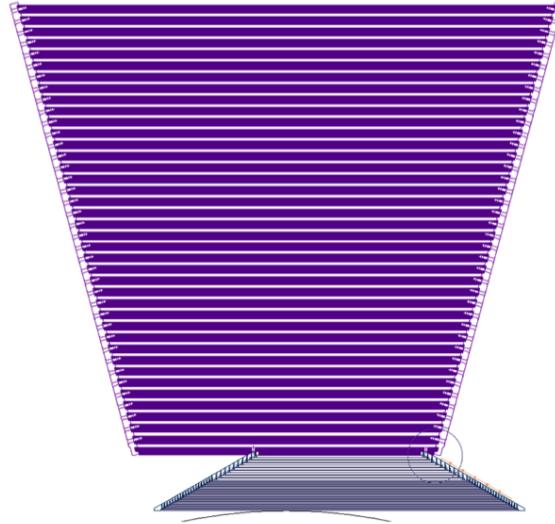


Figure 4.6

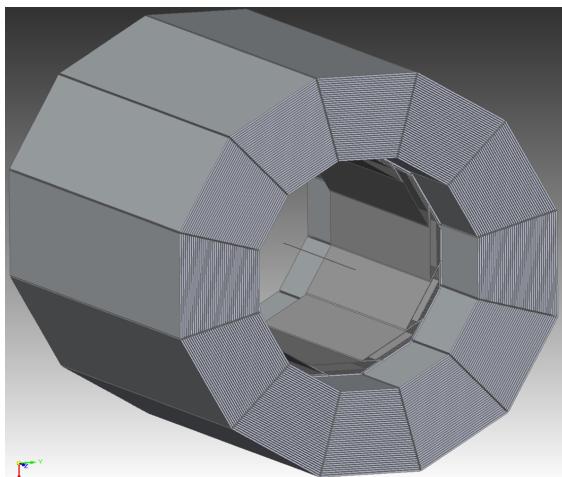


Figure 4.7

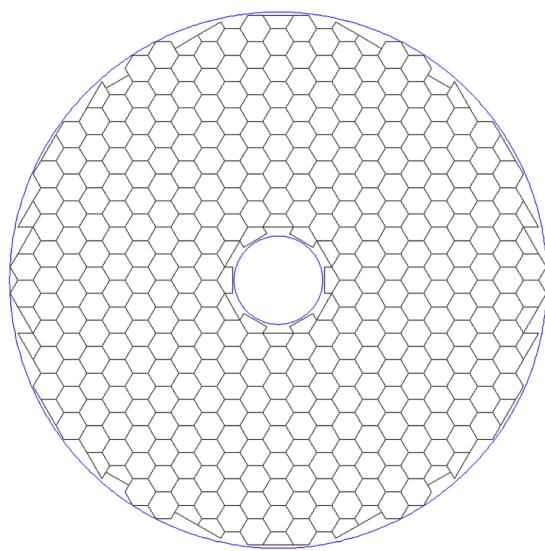


Figure 4.8

first H-Cal plate is unique in that its two longitudinal edges form a guide system to locate the E-Cal to the H-Cal system. The H-Cal modules are first bolted together to form the H-Cal barrel. Interleaving structural side battens maintain spacing for the H-Cal plates and extend inward to the E-Cal support plates. The inner ends of these battens act in concert as the female portion of the E-Cal guide system. The E-Cal modules are slid into place in the inner H-Cal bore. Extension plates complete the inner H-Cal first layer, since the E-Cal barrel is shorter. H-Cal detector panels are installed after this structure is complete (see Figure 4.7). Only simple detector layouts have been done for the E-Cal endcaps so far. These layouts show that using full and partial hexagons could yield fairly good coverage with only a few shapes. (see Figure 4.8).

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4.3.2 Recent Milestones

ILC related RD in the US is largely unfunded and small efforts are being kept alive on the margins. The KPiX RD is such an example of necessary work for SiD that is marginally alive. At this time, KPiX is seen as the baseline readout system for the tracker and electromagnetic calorimeter . A stack of 13 EMCal sensors with bump bonded KPiX was assembled for a beam test at SLAC in the summer of 2013. That test discovered that two kinds of crosstalk are significant:

- In-time crosstalk occurs due to parasitic coupling of traces on metal 2 of the sensor to other pixels. The level of crosstalk increases with the size of the signal, and decreases with increased speed of the front end charge amplifier (meaning increased current and power dissipation). A new sensor design is being developed that uses metal 1 to shield the traces of metal 2, and these ideas will be tested in the next sensor prototype.
- Out-of-time cross talk occurs when many pixels are hit and reset simultaneously. The resets collectively cause other pixels to trigger, and a cascade builds up. This uses up all the KPiX buffers. The root cause of the problem appears to be some internal logic within KPiX that is not current limited, and will require design modification.

A more general issue is that both the EMCal and tracker sensors from Hamamatsu were ordered with Al pads, as it was believed that plating (by the zincate process) a stack of metals culminating with Au would be straightforward. This turns out to be wrong. After many attempts at University of California Davis (UCD) and local industry, IZM has Ar ion etched the pad surfaces and sputtered a base layer, permitting the buildup of a stack that ended with Au, and permitting the attachment with solder bumps that had been placed during KPiX manufacture by TSMC. Testing of these sensors revealed 10% pixel to pixel shorts and

some opens of signal traces, that are suspected to be damage caused by the Ar ion etch. A new round of sensors has been ordered with the Metal 1 layer used to shield the Metal 2 traces from the diodes that they cross on the way to the KPiX bump pads, and with the Au pads being built by Hamamatsu.

An additional issue is that the Tracker sensor was planned to be wire bonded to its (very thin) cable. The sensor oxide layer is not strong enough to allow wire bonding without damage, and so must be solder bumped. The pad pitch is small, and solder bumping the cable will be challenging. The trouble with the wire bonding to the sensor was unexpected. Recent attempts with both bump bonding a cable and utilizing electrically conductive epoxy have failed. The best explanation is that the 150 °C thermal cycles associated with these attachments increased the stress on the KPiX bonds and caused the sensor pads to separate from the sensor. It is believed that something went wrong with the Hamamatsu process on both types of sensors, and is related to the wire bonding problem.

Another concern is that the current design of KPiX has deadtime after a pixel has accepted a trigger. Only the triggered pixel is affected; all the other pixels are available for signals. This deadtime is different from the usual notion of data acquisition deadtime where the entire detector is unavailable, but the correction to the luminosity integral is easy. Finally, the buffer requirement (4 in the current version of KPiX) is being re-evaluated in SiD simulations. A possible new architecture for KPiX is in early stages of evaluation. Another approach is the development of Monolithic Active Pixel (MAP) sensors for both SiD sensors using thinned HVCMS. The sensors would be approximately the same size as the current sensors. The tracker would have $40 \times 500 \mu\text{m}$ pixels, and would only need one buffer. A prototype to evaluate the pixel performance is being designed now. The EMCal sensor will have $1 \times 1 \text{ mm}$ pixels which should limit the required dynamic range and eliminate range switching, but would still need 16 buffers.

A small mechanical engineering effort has started to study the structure of the EMCal. The Sid EMCal has emphasized thin gaps between the tungsten layers to minimize the Moliere radius, and this implies that the structure is connected by columns at the vertices of the sensors. This work has been carried out to the level of a pre-conceptual design.

4.3.3 Engineering Challenges

4.3.4 Future Plans

Assuming positive developments with Japan are announced soon, we expect the financial support to improve. It should be noted that an important effect of the withdrawal of support is that most of the US collaborators have been forced to move to other work.

- EMCal Sensors: A second round of prototypes will be designed and ordered with rectangular layout; shielded traces, and Au pads.
- Tracker Sensors: The current prototypes will be evaluated, and if appropriate tested in a beam.
- KPiX: A new architecture with little (or no) deadtime will be evaluated. A decision will be made to develop this new architecture or incrementally improve the existing design.
- The EMCal mechanical structure will be pushed towards a conceptual design.

4.3.5 Applications outside Linear Colliders

This work represents a significant step in the aggressive integration of silicon sensors with readout electronics, just short of integrating the electronics directly into the sensors. It has prompted consideration

of this approach by CMS for calorimetry and by ATLAS for a muon system. It may have applications in sensors for light sources as well as other particle physics detectors.

4.4 DECAL

The studies of a digital ECAL (DECAL) continue in the UK, in spite of very significant funding difficulties. In December 2008, the STFC Executive recommended sufficient funding to allow the SPiDER Collaboration to construct a full physics prototype DECAL, as outlined in [74]. By December 2009, the funding for SPiDER had still not been issued and STFC informed the Collaboration that they would not do so.

The UK groups in SPiDER have demonstrated that the INMAPS technology developed specifically for the DECAL application is viable in terms of basic pixel efficiency. INMAPS is implemented as a $0.18\text{ }\mu\text{m}$ CMOS process in which a deep P-well implant stops signal charge from being absorbed in N-well circuits, and therefore allows the use of both NMOS and PMOS within the pixel, as well as (optionally) high resistivity silicon in the thin epitaxial layer to reduce the charge collection time.

4.4.1 Test Beams in 2010

Following a successful test beam run at CERN in September 2009 using 120 GeV pions, two further data taking runs have been carried out. The first of these was at DESY in March 2010, for which the primary goal was to quantify the peak electromagnetic shower density observed downstream of specific absorber materials. A secondary goal was to make further pixel efficiency measurements. Data were recorded with the 1-5 GeV electron beam, using a configuration in which four TPAC 1.2 sensors were aligned precisely along the beam direction using the same custom-built mechanical frame as at CERN. Absorber material (W, Fe, Cu) was placed downstream of these, followed immediately by a further pair of TPAC sensors, to study the shower density.

To complement the DESY run, similar, additional data was recorded at CERN in September 2010, using the EUDET telescope alone as it has finer pitch than the TPAC sensor, with positrons between 10 and 100 GeV. The same slabs as those at DESY were used together with new slabs due to the higher energies available at CERN. Initial results of shower multiplicities are presented in [75].

4.4.2 Pixel efficiency results

The studies of pixel efficiency from CERN 2009 testbeam and DESY were performed using a set of six TPAC 1.2 sensors aligned along the beam direction, in which the outer four sensors served as a beam telescope, while the two innermost sensors were considered as the devices under test. The trajectory of the beam particle was projected onto the plane of both of these sensors, and each pixel of the test sensors was examined for the presence of hits as a function of the distance from the projected track. The MIP hit efficiency was determined by fitting the distribution of hit probability to a flat top function, convoluted with a Gaussian of the appropriate resolution to allow for finite tracking performance. This efficiency, folded for all pixels together, is illustrated in Figure 4.9

The MIP efficiency was determined per pixel for both the DESY and CERN data, and for each of the four pixel variants tested. The variants (and corresponding marker color in Figure 4.9) are:

1. (red) in $12\text{ }\mu\text{m}$ standard (non-INMAPS) CMOS;
2. (black) $12\text{ }\mu\text{m}$ deep P-well CMOS;

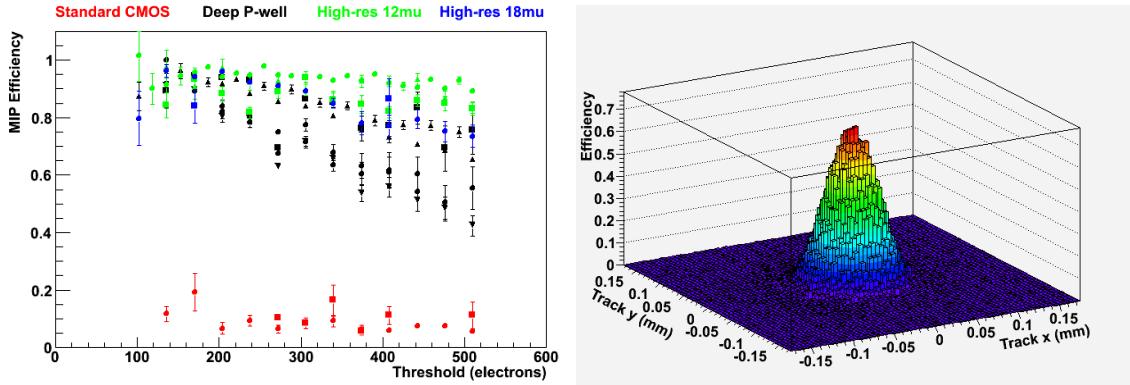


Figure 4.9: (left) Distribution of the probability of a pixel registering a hit in response to a MIP, as a function of distance to the projected track, and (right) MIP efficiency as a function of the sensor digital threshold, for all four sensor variants studied.

3. (green) deep P-well within a 12 μm high resistivity epitaxial layer;
4. (blue) deep P-well within an 18 μm high resistivity epitaxial layer.

The results [76] are summarized in Figure 4.9, for a range of the sensor digital thresholds representative of the signal levels expected in DECAL pixels due to charge spreading. (A typical MIP signal in a 12 μm epitaxial layer of silicon is 1200 electrons and a single pixel absorbs at most 50% of this due to charge spreading.)

From the results shown in the figure, it is observed that the standard, non-INMAPS sensors have markedly low efficiencies, which is attributed to signal charge being absorbed by in-pixel PMOS transistors. In contrast, the use of the deep P-well reduces the absorption of signal charge by N-wells in the circuitry, improving very substantially the pixel efficiency by a factor of ≈ 5 . The addition of the high resistivity epitaxial layer further improves the pixel efficiency to $\approx 100\%$.

4.4.3 Future plans

It is no longer an option to plan for a physics prototype DECAL and the short-term future of the DECAL project is extremely uncertain at present. A program of radiation hardness has been conducted on 2011 and the results are summarized in [75, 77]. This is in part to understand how the TPAC sensor would satisfy the requirements of ALICE ITS and SuperB. The studies which have been carried out so far are in the process of being finalized, and a series of papers, e.g. [78], are in preparation to document what has been achieved. The technology development has been taken over by the Arachnid collaboration who are testing the CHERWELL chip (designed and manufactured by the SPiDeR collaboration but never used due to money constraints) to evaluate the performance for ALICE and SuperB.

4.5 Resistive Plate Chambers

4.5.1 Description of the DHCAL

The Digital Hadron Calorimeter or DHCAL uses Resistive Plate Chambers (RPCs) as active elements. The chambers are read out with $1 \times 1 \text{ cm}^2$ pads and 1-bit (digital) resolution. A small-scale prototype was assembled and tested in the Fermilab test beam in 2007 to validate the concept. Based on the success of the small-scale test [1-6], a large prototype with up to 54 layers and close to 500,000 readout channels was built in 2008 – 2011. Each layer measured approximately $96 \times 96 \text{ cm}^2$ and was equipped with three chambers, stacked vertically on top of each other. For tests with particle beams the DHCAL layers were inserted into a main stack of 38 or 39 layers, followed by a tail catcher with up to 15 layers. For the tests performed at Fermilab the main stack contained steel absorber plates. At CERN the absorber plates were made of a Tungsten based alloy. In both cases the tail catcher featured steel absorber plates. In the various test beam campaigns combined, spanning the years 2010 – 2012, the DHCAL recorded around 14 Million muon events and 36 Million secondary beam events, where the latter contained a mixture of electrons, muons, pions, and protons.

4.5.2 Current R&D activities

The analysis and publication of the test beam results are currently the highest priority of the DHCAL group. Major challenges, such as the calibration (or equalization) of the response of the RPCs and the detailed simulation of the response of RPCs, are very close to having been overcome [7-11]. Parallel to the analysis of test beam data, the group is pursuing the following R&D activities:

Development of 1-glass RPCs

The DHCAL prototype featured a standard chamber design based on RPCs with two resistive plates. It is possible to eliminate one of the glass plates in future applications. The advantages are: close to unit pad multiplicity with significant simplification of the calibration and monitoring procedure, reduced thickness of the active element, higher rate capability, and insensitivity of the response to the surface resistivity of the resistive layer (used to apply the High Voltage). To date several 1-glass RPCs have been assembled. The chambers tested very well with cosmic rays. Tests in particle beams are planned for future test beam campaigns.

Development of high-rate RPCs

Due to the high bulk resistivity of glass (and Bakelite), RPCs are notoriously rate limited [79]. The DHCAL group is addressing this shortcoming with the developments of semi-conductive glass (in cooperation with COE college) and low-resistivity Bakelite (in co-operation with USTC). First chambers with samples of low-resistivity glass plates have been assembled and have been tested in the Fermilab test beam.

Development of a High-Voltage distribution system

With up to 50 layers in a single calorimeter module, a cost-effective way to distribute the High-voltage to individual layers is required. A system capable to regulate the voltage within a few 100 V, to monitor both the current and the voltage, and to switch off individual channels, is being developed. A first prototype controlling a single channel has been assembled and tested successfully with an RPC. The development is currently on hold due to lack of funding.

Development of a gas recycling system

The operation of RPCs requires a gas mixture, which is both costly and environmentally harmful. To limit the effect of releasing gas into the environment, the DHCAL group is developing a gas recycling system. The system is based on a new approach, appropriately labeled “Zero Pressure Containment”. A prototype of the gas collection subsystem is currently being assembled; however, progress is again slow due to lack of funding.

Development of the next generation front-end readout system

The next generation front-end readout system will contain several upgrades compared to the current system: higher channel count, token ring passing, low power operation, power pulsing, and improved internal charge injection systems. To proceed, the project is awaiting funding from both US and Chinese agencies.

4.5.3 Engineering challenges

Several engineering challenges remain to be addressed before an RPC-based DHCAL can be proposed as an option for a colliding beam detector. Following is an (incomplete) list of the major issues:

- Industrialization of the construction of RPCs.
- Design of the readout boards, covering the entire area of the layer (with varying width). The design is expected to feature only a minimum number of different boards.
- Design of the gas distribution system, which ensures equal pressure in all layers of a given module, independent of its orientation.
- Development of a cooling strategy for the front-end boards, which will include power pulsing, as well as active cooling.
- Development of a module assembly procedure.

4.5.4 Plans for the coming years

The activities of the coming years depend strongly on the progress with the Japanese intentions to host the ILC. Assuming the ILC project goes ahead, the DHCAL group will a) Complete the analysis and publication of the test beam data, b) Complete the R&D projects listed above, and c) Start the development of the design of calorimeter modules. In case, the ILC is not going forward, the group plans on completing the data analysis and to continue the tests of high-rate RPCs. Other R&D projects, such as the development of distribution systems, will be put on hold.

4.5.5 Applications beyond the ILC

The DHCAL technology was specifically developed for the hadron calorimeter of the ILC, with its low particle rate and radiation dose. To export the technology to other environments, the rate capability of the chambers and the radiation hardness of the readout need to be improved. The former is being addressed with low-resistivity plates (glass and Bakelite), while the latter will require a new front-end readout system based on an ASIC using a smaller feature size. Possible applications are the tail catcher of the forward

calorimeters of CMS and the outer wheels of the ATLAS muon system. Both options are being pursued actively.

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4.6 GEM

4.6.1 Introduction

The group pursues the development of Gas Electron Multiplier technology for instrumenting a digital hadronic calorimeter (DHCAL) at the ILC.

4.6.2 Recent Milestones

4.6.3 Engineering Challenges

4.6.4 Future Plans

4.6.5 Applications Outside of Linear Colliders

4.7 Analog HCAL

4.7.1 Introduction

With the advent of silicon photo-multipliers (SiPMs), the scintillator tile technology became a candidate for highly granular particle flow calorimetry. With analog read-out, energy and spatial resolution can be optimized independently. The particle flow performance is well understood; all published studies using PandoraPFA are based on this technology.

The CALICE AHCAL was the first large LC hadron calorimeter prototype to be exposed to test beams. Analysis is nearly complete and mostly published; the results validate the technology and the simulations.

The development of engineering solutions for a realistic detector is on its way. The integration of read-out electronics and calibration system into the detector layers has been demonstrated. The next step, an integrated stack, is being prepared. In parallel, as improved photo-sensors become available from industry, the design of the basic read-out cell – the tile with SiPM – is optimized with regard to mass production procedures.

4.7.2 Recent Milestones; past and present R&D

Test beam data analysis

The following results using data taken with the first AHCAL “physics” prototype in 2006 – 2011 at CERN and Fermilab have been published in peer-reviewed journals:

1. Detector construction, noise and aging studies [92]
2. Electromagnetic linearity and resolution [93]
3. Hadronic linearity and resolution, software compensation [94]
4. Test of particle flow algorithms (AHCAL with SiW ECAL) [95]
5. Studies using a scintillator SiPM based tail catcher [96]
6. Geant 4 validation with pion showers [97]
7. Geant 4 validation with tungsten absorber (low energy) [98]
8. Imaging capabilities, track segments [99]
9. Time structure of showers in Fe and W [100]
10. Geant 4 validation with protons [101]

We consider all of them as critical for validating a given HCAL technology. Papers [97], [98], [99], [100] and [101] appeared after the ILC TDR was handed over.

Preliminary results have been made public in the form of *CALICE Analysis Notes* after thorough internal reviewing on the following topics:

1. Combined performance SiW ECAL + AHCAL + Tail Catcher [102]
2. Leakage estimation using shower topology [103]
3. Parameterization of pion and proton shower shapes [104]
4. Geant 4 validation with tungsten absorber (high energy) [105]
5. Analogue, Digital and Semi-Digital Energy Reconstruction [106]
6. Extraction of h/e a from the longitudinal shower profiles [107]

Notes [105], [104], [106] and [107] appeared in the time since the release of the ILC TDR. The studies are actively being followed up towards final publication; only the leakage study is presently uncovered due to lack of manpower.

Studies of the combined performance of the AHCAL in conjunction with the scintillator tungsten ECAL with MPPC readout are on-going. Results are expected later this year and will make the analysis of the first generation test beam data complete.

Data taking with a first, partially instrumented stack of the second generation has started at DESY continued in fall 2014 with electrons and hadrons at CERN. A framework for analysis software exists, but calibration and correction procedures for timing measurements still need to be developed.

The CALICE test beam results are nowadays the primary source of validation for hadron shower simulation, according to Geant 4 representatives, and extremely valuable for other HEP experiments, e.g. at the LHC, as well.

We finally note that test beam analysis plays an important role in training our students. Roughly speaking, each paper or note corresponds to one or several PhD theses. It is a distributed effort; the results have been obtained at DESY, CERN, MPI Munich, Hamburg, Heidelberg, Mainz and Wuppertal universities, ITEP Moscow and Northern Illinois University.

Optimization of the scintillator SiPM read-out cell

As a consequence of the wide success of SiPM applications in other fields, e.g. in medical imaging, the development of improved sensors is dynamically pursued in industry, and several groups (DESY, Hamburg, ITEP, MEPhI, Shinshu, Tokyo) are in close contact with leading producers. Progress has been made in terms of dark rate, noise above MIP threshold and dynamic range. In addition, the samples are much more homogeneous than at the time of the first prototype, which results in a simplification of commissioning and calibration procedures.

In the time since the TDR, tile SiPM cells without wave-length shifting fiber have been developed, following a design by MPI Munich. One is based on machined, individually wrapped scintillator plates (Hamburg), the other one on injection-molded tiles (ITEP). Both are using sensors from KETEK, those on the molded tile have a very large dynamic range. 300 devices have been produced and tested at ITEP, and more than thousand devices have been produced and tested with semi-automatic procedures at Hamburg and Heidelberg. They been integrated into the test beam set-up in 2014 and tested at DESY and CERN.

This version is a good candidate for a baseline design for a full detector, but more data taking and analysis is needed.

Industrialisation of the SiPM and tile design and production procedures is now actively being addressed, and first assemblies with industrial facilities such as automatic pick-and-place machines have been made (Mainz). This needs to be continued in the coming years, fed back into the cell optimization, and awaits a feasibility demonstration at larger scale.

An alternative cell design, with photo-sensors integrated in the read-out electronics board, has been proposed some time ago (Northern Illinois), and the detailed development of the corresponding sensor and scintillator configuration is now being pursued (NIU, Mainz, ITEP). It has the potential to result in further simplifications (which should be read as cost and time savings), but poses higher performance requirements to the SiPM – which can now be met – and raises new issues in the quality assurance and integration chain. The goal is to fully develop such an alternative solution in the next 2 years.

Electronics and active layer integration

The design of the active layers (DESY) with integrated read-out ASICs (CNRS-OMEGA) and calibration system (Wuppertal) has been basically validated in beam tests of a single HCAL layer consisting of four base units (HBUs) at CERN in 2012 and reported in the TDR. An HBU reads 12×12 tiles with 4 ASICs. The present ASIC belongs to the 2nd generation ROC family used also in ECAL and SDHCAL. An HCAL layer carries interfaces for DAQ, calibration and power supply, which already have a compact design fulfilling space constraints at an ILC detector.

The main difference between the integrated electronics and that of the physics prototype is the self-triggered operation and on-detector zero-suppression, which implies much higher demands on controlling the noise behavior and ensuring a stable detector response. It is thus mandatory to re-establish the calorimeter performance with a full-scale beam test, including the operation with fast power cycling. However, this is out of reach with present funding levels.

Further R&D in the next years has to be done both on the ASIC and on the PCB. For the ASIC, development of a 3rd generation ROC chip will start after fixing open issues with the 2nd generation (OMEGA). The 3rd will have a more robust slow control architecture and possibly channel-wise buffer management which improves rate capabilities. In parallel, an alternative design of the analog part (Heidelberg), which can handle a larger range of sensor gain needs to be complemented with a digital part.

The PCB with integrated photo-sensors, as counterpart of the corresponding tile design (see 4.7.2), has been developed, taking automatic production and quality assurance into account. The PCB is also one of the main cost drivers of a particle flow HCAL. Dedicated R&D, in close cooperation with industrial manufacturers, is necessary to bring the cost down. First contacts have been made (DESY, Heidelberg, SKKU Korea), and new prototype boards are being manufactured in Korea.

System integration

While the integration of layers is well advanced, that of entire stacks or modules has only begun. Since the TDR release, efforts concentrated on developing a multi-layer DAQ capable of reading larger systems (DESY, Mainz, Prague). This was ready for beam tests at CERN in fall 2014. It involves integration of a dedicated module data concentrator, which collects signals from all layers for sending them to the off-detector data receiver.

Further work will be required to integrate the HCAL DAQ into a higher level system for the purpose of combined beam tests, for example with a tracking device for uniformity studies, or with an ECAL for inter-calibration and combined performance. The same is true for slow control data.

A power supply system with optimized channel density per module is being developed at Dubna.

It has been demonstrated that temperature-induced variations of the SiPM gain can be compensated by adjusting the bias voltage (Prague, Bergen). The approach has the potential to stabilise the detector response and trigger efficiency and thus simplify operations significantly. Automatic procedures based on this principle need to be developed and implemented for a test at system level.

On the mechanical side, a cooling system needs to be developed. The ASICs integrated in the detector layers are power-pulsed and do not need active cooling, but the interfaces, in particular the power regulators, do. A simple solution for beam tests exists (DESY), but a leak-less under-pressure based system for a large detector still needs to be prototyped.

Infrastructure for production, quality assurance and characterisation

The AHCAL is probably the sub-detector with the largest number of individual components. While the number of electronics boards, layers and interfaces is similar to other ECAL or HCAL options, the large quantity of tiles and SiPMs deserves special attention. This affects production and quality assurance, but also characterisation, i.e. test bench measurements of parameters to be used later for calibration purposes.

While it would be premature to discuss building up full production infra-structure, conceptual solutions need to be developed and exercised using demonstrators, which could be seen as prototypes of future installations. The demonstration requires reasonably large samples of detector elements, in the order of 10000, as they would be needed for a next generation full prototype.

A semi-automatic test stand for SiPMs and tiles has been developed at Heidelberg and used for the elements of the early 2014 beam test. It needs to be adapted for future designs, e.g. with SiPMs integrated in the PCB.

Automatic assembly of HBUs (Mainz), i.e. of placing and soldering tiles and SiPMs on the PCB, needs to be demonstrated in practice, too. First encouraging tests with individual samples have been reported, but obviously only larger scale tests can validate the concept. A versatile cosmic test stand for the characterisation of several complete active HBUs is under development (Mainz).

Absorber structure

The absorber structure bears more challenges than for conventional hadronic calorimeters. Due to the much finer longitudinal segmentation and the imperative to minimize the total radius inside the coil, there are many active gaps with tight tolerances. A design has been developed and prototyped, which achieves the required tolerances with a cost-effective roller-leveling process without machining off excess material (DESY). Two test structures have been built; one covers the full transverse cross section of a barrel module, the other the full lateral extension. The cassettes (DESY, MPI Munich) housing the active elements have the final design and are used in beam tests.

These structures need to be investigated with respect to their robustness against earthquakes (DESY). Simulations of the whole ILD structure have been made, and measurements on the test structures exposed to accelerating forces should be done in order to check the simulations.

As enough active elements become available for instrumenting several active layers at full size, the thermal simulations should be verified with measurements, too. This will constitute an important step in system integration, as it addresses the issues associated with large layers and in particular power distribution, power cycling and heat dissipation.

4.7.3 Summary

The AHCAL effort has produced a number of significant results in the time since the ILC TDR:

- Publication of 5 journal papers and 4 preliminary results in the form of internally reviewed notes, on Geant 4 validation with pions and protons in steel and tungsten, including new observables like track segments
- Development, production and beam test of a new, simplified tile SiPM system without wave-length shifting fibers and improved sensor performance
- Test with electron and hadron beams of a partially instrumented realistic absorber structure with second generation electronics, DAQ and services

4.7.4 Future Plans

The AHCAL is ready to make the next step towards a realistic full-scale prototype and a technical design report. In order to achieve this, coordinated R&D is required in the following areas:

Software and analysis:

- Completion of physics prototype test beam analysis
- 2nd generation prototype reconstruction and simulation software
- Development of timing reconstruction
- Analysis of 2nd generation test beam data

Tile SiPM system:

- Development of scintillator SiPM system with SiPM on the PCB
- Development of associated assembly, quality assurance and characterization procedures
- Development of associated PCB

4.7.5 Engineering Challenges

Electronics:

- 3rd generation ASIC of ROC family
- ASIC for larger range of SiPM gains
- PCB cost optimization

System integration:

- Scalable DAQ
- Module level data collector
- Integration of DAQ and slow control into higher level system

- Implementation of temperature compensation scheme
- Power supply system
- Cooling system

Mass production concepts:

- Semi-automatic test stands
- Automatic placement and soldering of tiles and SiPMs

Absorber structure:

- Earthquake stability calculations and tests
- Thermal tests with full-scale instrumented and powered structures

There are ample opportunities for new groups to join into any of these fields, depending on the special competences they wish to contribute.

Particular engineering challenges are

- Assess and ensure earthquake stability of the absorber structure whilst maintaining a minimum of dead material
- Developing an active layer element consisting of tiles, SiPMs and readout electronics that can be automatically assembled, including production and quality assurance procedures

4.8 Micromegas SDHCAL

4.8.1 Introduction

The Micromegas R&D is primarily intended for Particle Flow calorimetry at future linear colliders. It focuses on hadron calorimetry with large-area Micromegas segmented in very small readout cells of $1 \times 1 \text{ cm}^2$. This granularity provides unprecedented imaging capability which can be exploited to improve the measurement of jet energy. Past and current R&D efforts are described with emphasis on achievements since the publication of the ILC Detailed Baseline Design.

4.8.2 Hadron calorimeter design

The design of calorimeters at a future linear collider is optimised for the reconstruction of jets with a Particle Flow method. The SiD HCAL will be segmented in cells of $1 \times 1 \text{ cm}^2$. With a total instrumented area of 3000 m^2 , the number of readout channels will reach 30×10^6 . This unprecedented granularity can be achieved with gas detectors, thin PCBs and embedded front-end ASICs.

In addition, calorimeters will be placed inside the solenoid magnet to insure good matching of electron and charged hadron tracks with their energy deposits in the ECAL and HCAL. To limit cost, a very compact mechanical design is mandatory: e.g. the SiD HCAL would feature 40 layers within $\sim 110 \text{ cm}$. This design relies on very thin active layers to achieve fine sampling ($\sim 0.1 \lambda_{\text{int}} / \text{layer}$) and good hadron energy resolution ($\sim 50\%/\sqrt{E}$). The targeted active layer thickness and length in the barrel HCAL modules are 8 mm and 3 m respectively. To minimise dead zones, readout boards will be placed at the two ends of the

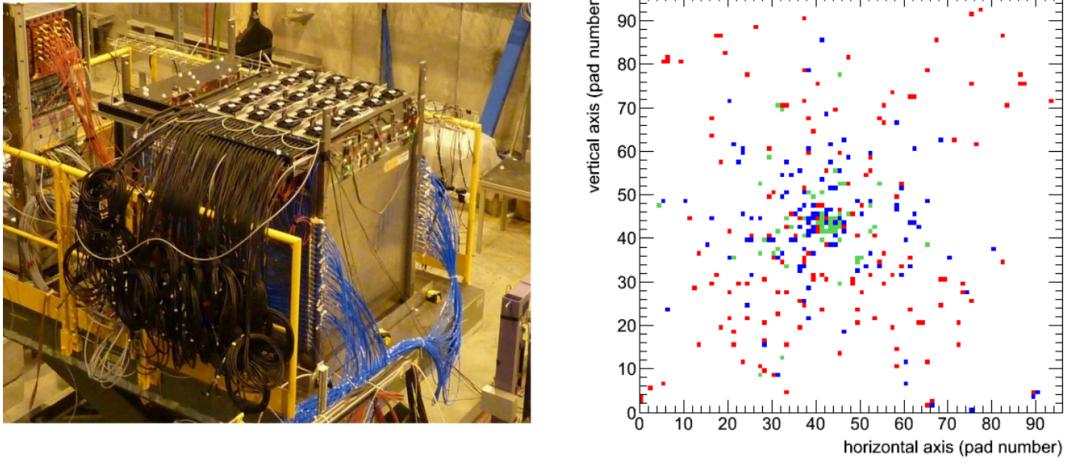


Figure 4.10: SDHCAL prototype in a beam line at the SPS at CERN (left). Event display of a 150 GeV pion shower measured in a Micromegas prototype after $2 \lambda_{\text{int}}$ of steel (right), the color indicates the threshold passed: red for 1, blue for 2 and green for 3.

barrel modules. Along the beam direction, ASIC will be daisy chained and PCBs connected together with flat connectors and cables.

Active cooling of the active layers is extremely challenging with this design. Instead, it is considered to limit heat dissipation and gradients inside the calorimeters by power-pulsing the front-end circuitry. Power-pulsing is possible because of the particular time structure of the ILC beam. This structure also drives the design of the ASICs which will be self-triggered. During collisions, signals will be processed and stored in memory with a timestamp synchronous to the ILC clock. Between bunch trains, memories are first read out, then the ASIC are turned off. With an ILC duty-cycle of 0.5%, the power consumption can be reduced down to $10 \mu\text{W} / \text{channel}$.

4.8.3 Recent Milestones

The SDHCAL

The SDHCAL is a prototype of imaging hadron calorimeter equipped with 50 layers of gaseous detectors of $1 \times 1 \text{ m}^2$ interleaved by steel absorbers (Figure 4.10 (left)). Each detectors is segmented in pads of $1 \times 1 \text{ cm}^2$ and the processed pad signal is coded over 2-bits (Figure 4.10 (right)). The number of readout channels per layer imposes to integrated the front-end electronics directly on the gaseous detector printed-circuit-boards (PCB). Several CALICE groups are involved in this project.

The $1 \times 1 \text{ m}^2$ Micromegas prototype

Mechanics The Micromegas layers for the SDHCAL are made out of 6 high-voltage units installed together inside a gaseous chamber (Figure 4.11 (right)). Each unit is an 8 layer PCB with a Bulk Micromegas mesh, readout pads and front-end ASICs; it is dubbed Active Sensor Unit (or ASU). A drift gap of 3 mm is defined by spacers and a frame. Spacers are inserted in between ASUs, resulting in an inactive area of 2%.

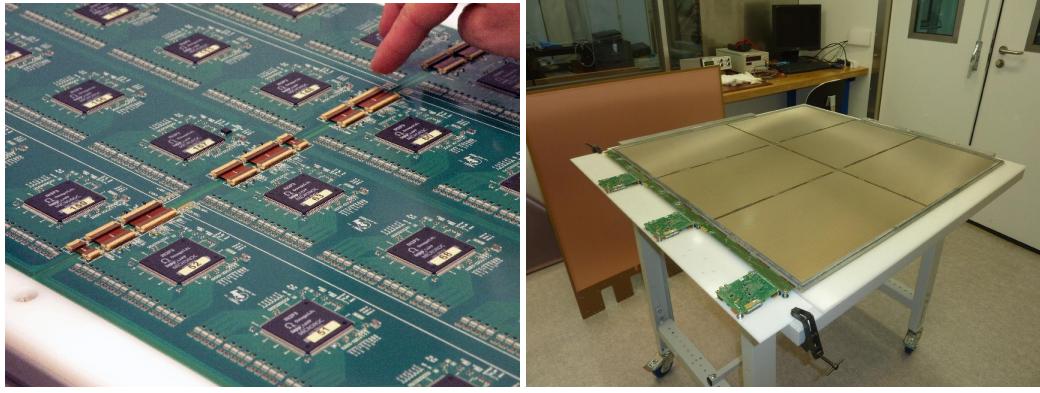


Figure 4.11: Photographs of interconnections between 2 Active Sensor Units (left) and a $1 \times 1 \text{ m}^2$ Micromegas prototype during assembly showing 6 of these units and a drift cover (right).

Electronics Electronics connections to the DAQ as well as services (power cables, gas pipes) are provided on one side of the prototype. ASU-to-ASU connections are therefore mandatory and are made with dedicated connectors and flexible cables (Figure 4.11 (left)). They are used to distribute clocks and supply power to the ASICs, high voltage to the meshes, to configure the ASICs and read out data. Prior to assembly, 4 ASUs were chained and functional electronic tests were successfully performed. These key features make the design of the $1 \times 1 \text{ m}^2$ Micromegas prototype fully scalable to the required size of a HCAL module at a future LC (at most 2 m in the SiD detector concept).

Noise and detection efficiency A few prototypes were constructed [108] and extensively tested in beam at CERN [109]. Noise conditions were excellent both during standalone tests and inside the CALICE SDHCAL. ASIC thresholds can be lowered down to about 20% of a minimum ionising particle (MIP) signal at a typical running gas gain of 1500. Efficiency in excess of 95% are easily reached while keeping a pad multiplicity below 1.1 for MIPs. The actual charge threshold is as low as 1–2 fC; it is achieved on ASIC test-boards as well as once mounted on ASUs. The contribution of the PCB internal capacitances to the overall detector noise is therefore negligible.

Standalone performance Thanks to a precise control of the gas gaps and electronics settings, ASIC-to-ASIC variations of efficiency are below the percent in all tested prototypes. Although the statistics is low, the construction process seems reproducible. Stability with rate in high-energy hadron showers is excellent. Except occasional sparks, no effect of beam rate was observed on the pion response up to roughly 30 kHz beam rate; which was the highest rate during the tests. The measured spark probability lies in the range of $10^{-6} \dots 10^{-5}$ per showering pion at a running gas gain of 1500.

Resistive prototypes

While the Bulk Micromegas mesh is made of steel wires and is very resistant to sparking, sensitive front-end ASICs can suffer irreversible damage. Protections in the form of current-limiting diodes networks soldered on PCB were proved so far efficient. To simplify the PCB design and possibly reduce the overall detector cost, it is however desirable to get rid of diodes. It is well known that sparks can be suppressed by means of resistive coatings on the anode pad plane. This solution is used with great success in tracking

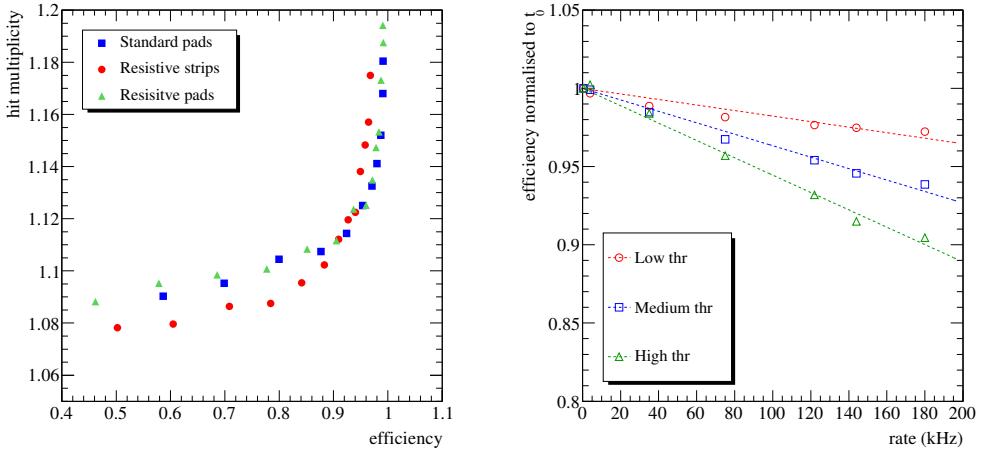


Figure 4.12: Pad multiplicity versus efficiency to 3 GeV electrons for 2 resistive and 1 non-resistive (or standard) Micromegas prototypes (left). Efficiency dependence on rate in a resistive prototype for 3 values of threshold (right). The electron beam spot is $\sim 2 \times 2 \text{ cm}^2$.

detectors. Because it modifies the signal development, it needs some adaptation to calorimetry so as to preserve linearity and keep a narrow pad response function for Particle Flow reconstruction.

First resistive designs using resistive strips and pads were implemented on small size prototypes. In a mixture of Ar/CO₂, full suppression of sparking was demonstrated up to gas gain in excess of 10⁴. At comparable gas gains, resistive and non-resistive prototypes show similar response to traversing charged particles, reaching high efficiency and low pad multiplicity. Compared to non-resistive ones, the evacuation of charge is slowed down in resistive prototypes which are thus subject to rate-dependent drops of gas gain. Expected efficiency losses have been observed at (3 GeV electrons) rates in excess of 10 kHz/cm². This limit is compatible with the resistivity of the coated material. At lower rates, it could be shown that the linearity of a Micromegas calorimeter to electrons is not affected by the resistive coatings, up to 5 GeV, which was the maximum energy available during the testbeam campaign.

4.8.4 Engineering Challenges

4.8.5 Detector R&D plans for the coming years

Plans for the coming years include maintaining a commitment to linear collider detector R&D and possibly seek new applications. Despite a decline of resources, an R&D program to optimise resistive Micromegas for calorimetry is established. Linearity, rate capability and spark protection in dense electromagnetic showers will be checked up to high-energy and for detector designs with a large variety of resistivity and geometry. These measurements will be necessary to validate the resistive Micromegas technology for calorimetry at a future LC. Also, the on-going R&D for high-luminosity LHC (HL-LHC) detector upgrades are an appealing perspective. In particular, the possibility to equip the backing part of the CMS forward calorimeter is being investigated. Such high-rate application will put strong stability constraints on resistive Micromegas, making the optimisation work mentioned above even more relevant.

On a longer term and if resources are sufficient, a Micromegas calorimeter prototype should be constructed so its performance can be compared to concurrent detector technologies. Some performance have already been studied with Monte Carlo simulation, the minimal prototype dimensions are known as well as its cost. This final step of the project naturally comes after optimisation of the resistive coating and would complete the R&D on Micromegas calorimetry.

4.8.6 Applications Outside of Linear Colliders

4.9 Glass RPC SDHCAL

4.9.1 Introduction

Hadronic calorimeter (HCAL) plays an essential role in PFA-based experiments as those proposed for the ILC. It allows to separate the deposits of charged and neutral hadrons and to precisely measure the energy of the neutrals. The contribution of the neutrals to the jet energy, around 10% on average, fluctuates in a wide range from event to event, and the accuracy of the measurement is the dominant contribution to the particle flow resolution for jet energies up to about 100 GeV. For higher energies, the performance is dominated by confusion, and both topological pattern recognition and energy information are important for correct track cluster assignment. High-granularity hadronic calorimeter is thus needed to achieve excellent jet energy resolution.

HCAL proposed for both projects of ILC (ILD and SiD), are sampling calorimeters with steel as absorber and scintillator tiles or gaseous devices with embedded electronics for the active part. The steel was chosen due to its rigidity which allows to build self-supporting structure without auxiliary supports (dead regions). Moreover, the moderate ratio of hadronic interaction length ($\lambda_I = 17$ cm) to electromagnetic radiation length ($X_0 = 1.8$ cm) of iron, allows a fine longitudinal sampling in terms of X_0 with a reasonable number of layers in λ_I , thus keeping the detector volume and readout channel count small. This fine sampling is beneficial both for the measurement of the sizable electromagnetic energy part in hadronic showers as for the topological resolution of shower substructure, needed for particle separation.

For the ILD project we propose gaseous detectors for the HCAL active layers: The Resistive Plate Chamber (RPC). This is motivated by the excellent efficiency and very good homogeneity the gaseous detectors could provide. Another important advantage of gaseous detectors is the possibility to have very fine lateral segmentation. Indeed, in contrast to scintillator tiles, the lateral segmentation of gaseous devices is determined by the electronics readout used to read them. Active layer thickness is also of importance for what concerns the ILC hadronic calorimeter to be placed inside the magnetic field. Highly efficient gaseous detectors can indeed be built with a thickness of less than 3 mm.

To obtain excellent resolution of hadronic shower energy measurement using a binary readout, a lateral segmentation of few millimeters is needed. This however leads to a huge number of electronics hardly affordable for the future ILC hadronic calorimeters. $1 \times 1 \text{ cm}^2$ cells were found to be a good compromise that still provides very good resolution at moderate energies. However, simulation studies show that saturation effects are expected to show up at higher energies (> 50 GeV). This happens when many particles cross one cell in the center of the hadronic shower. To reduce these effects, the choice of multi-threshold electronics (Semi-Digital) readout was envisaged to improve on the energy resolution by exploiting the particle density in more appropriate way.

High-granularity calorimeters imply however a huge number of electronics channels to operate them. This has two important consequences. The first is the power consumption and the resulting increase of temperature which affects the behavior of the active layers. The other consequence is the number of service

cables needed to power, read out these channels. These two aspects can deteriorate the performance of the HCAL and destroy the principle of PFA if they are not addressed properly.

The R&D pursued by the SDHCAL-GRPC groups has succeeded to pass almost all the technical hurdles of the PFA-based HCAL. The SDHCAL-GRPC groups have succeeded to build the first technological prototype of these new-generation calorimeters with 48 active layers of GRPC, 1 m^2 each. The prototype validates the concept of high-granularity gaseous detector and permits to study the energy resolution of hadrons one can obtains with such calorimeter.

4.9.2 Readout Electronics

The readout electronics of the two Semi-Digital HCAL (SDHCAL) projects were developed in common. An ASIC called HARDROC was first developed to read out the GRPC detectors proposed for the ILD project. To solve the problem of connections related to the high number of electronics channels, the option of a detector embedded electronics using the DAISY chain scheme was chosen and Printed Circuit Board (PCB) were conceived for the readout of large detectors GRPC.

Front-end ASIC

The HARDROC chip (HR) implements a multi-threshold readout which integrates the functionalities of amplification, shaping, digitization, internal triggering and local storage of the data. Each of its 64 channels consists of a fast low impedance current preamplifier with 8-bit variable gain (in the $[0, 2]$ range) followed by 3 fast shapers (15 ns shaping time). A low offset discriminator is present on each path and the three corresponding thresholds establish the multi-level readout. The thresholds are set using three integrated 10-bit Digital to Analog Converters (DAC). The outputs of the three discriminators are then encoded 3-to-2 bit and stored in an internal digital memory latched by a trigger event.

A trigger is generated when one of the lowest level discriminators is fired but can also be configured on the other thresholds. A frame consists of the 64 encoded discriminator outputs, plus a 24-bit time-stamp and a chip identifier is stored after a trigger is received. Noisy channels could be easily masked via the configuration parameters control. In order to avoid fake triggers produced by noisy channels, the output of each discriminator can be switched off from the trigger generator logic via the configuration parameters control (Slow Control hereafter) commands. The response of all the channels can be calibrated by injecting an analog signal through an integrated $2 \pm 0.02\text{ pF}$ input test capacitor; this is a useful tool to make the response of the different channels as uniform as possible [110].

The ASIC contains a 127-frame long digital memory. This allows to work in a triggerless mode and keep all the data accumulated during the bunch crossing. Once the memory is full the acquisition is stopped, the readout is performed and the ASIC can start acquisition again. The Gray-coded time-stamp is derived from an external 5 MHz clock.

An essential feature of the HR is the possibility to be operated in the power-pulsing mode (PP) that consists of switching off almost all power-consumption functionalities in between the bunch crossings (BC) of the ILC electron beams. With the ILC duty cycle of one 1 ms of BC every 200 ms, this mode allows a reduction factor of more than 100 of power consumption. Thanks to this reduction, the temperature increase of the HCAL is moderate and only simple cooling system is needed to operate it efficiently.

Active Sensor Units

To read out the 1 m^2 detector of the SDHCAL, an electronic board with the same size is needed. This electronic board is an important piece in the present design. It hosts both the pick-up pads and the ASICs

in addition to the connections linking the pads to the ASICs and those among the different ASICs. To ensure good transmission qualities and low cross-talk, 8-layer Printed Circuit Board (PCB) is designed. Feasibility constraints, make the tasks of circuit production, components soldering, testing and handling of the assemblies, exceedingly difficult in the case of a single board of one square meter. The solution of dividing that circuit into 6 smaller but more manageable PCB was adopted. Each of these small ASUs hosts 24 chips to read out 48×32 pads of 1 cm^2 each. This dressed PCB is dubbed Active Sensor Unit (ASU). The base pattern connecting 64 pads arranged in a 8×8 matrix to the ASIC's pins is shown in Figure 4.14. This is identical to the one used in the ASUs of the small GRPC chambers described in reference [110]. The routing of each input signal from its own pad up to chip pin has been carefully optimized to reduce the cross-talk. All input signals are laid out in the same analog signal layer which is sandwiched between two GND layers. The routing of digital signals was kept well separated from the vias connecting signals from one layer to another. In the case of the GRPC related ASU, the HARDROC base pattern is replicated 4×6 times in the $33.33\text{ cm} \times 50\text{ cm}$ board. 4 1.6 mm diameter holes are present on the four angles of a PCB to be used for fixation purposes as will be explained later. The routing was conceived so two of the ASUs can be associated to form one slab hosting 48 ASICs. Each slab is then connected to one Detector Interface board (DIF). The connection between the DIF and the slab as well as the connection of the two ASUs is performed thanks to tiny connectors allowing the different clocks, signals as well as the power to circulate between the two ASUs. Three slabs are then assembled to form the required electronics board. To ensure the same electric reference level for the six ASUs, the GND layer of the six ASUs is connected to a copper gasket on all the common sides. Similar schemes could be proposed for GRPC detectors with larger size.

Front-end and back-end boards

The interface between the ASUs and the data acquisition system (DAQ) is realised by the detector interface board called DIF. The main elements of the DIF is an FPGA and USB, HDMI and SAMTEC connectors. It manages the control signals (e.g. clock, busy/ready, external/internal trigger, power-pulsing) and supply power to the ASICs and also performs the readout of the ASIC memories. DIFs are read out by other FPGA-based boards called Data Concentrator Cards (DCC). They can be connected up to 9 DIFs through HDMI links and are controlled by a synchronous DCC (or SDCC). The SDCC can connects to up to 9 DCCs to which it distributes the clock and the commands. It is also connected to the computer network for the user to control the DAQ.

In the case of Micromegas ASUs, a small additional board called inter-DIF is used between the DIF and ASU to provide the high voltage to the meshes and drift electrode.

Acquisition Software

To exploit the data collected by the SDHCAL detectors an acquisition software was developed. This software is organized in three parts. The first one allows to access the hardware devices (DIF, SDCC) through an FTDI chip associated to each of these devices. It transmits the configurations parameters to ASICs through these devices and collect the data as well. The second part is the configuration data base. It gives the possibility to store and retrieve all parameters needed by the DAQ system. The database itself is hosted on an Oracle server at CC IN2P3 (Villeurbanne, France). To interface this SQL database with the DAQ software and to allow users to insert and query data without knowledge of SQL, a C++ library has been written. A special care was taken to allow to download the parameters associated to a given parameters of the prototype (roughly 550000 parameters) in few seconds. The third part concerns the data collection. Data from different DIFs may be readout at a different times but will have the same Bench Crossing IDentifier (BCID) for a given trigger. The logical way to keep synchronicity is to store in a BCID indexed

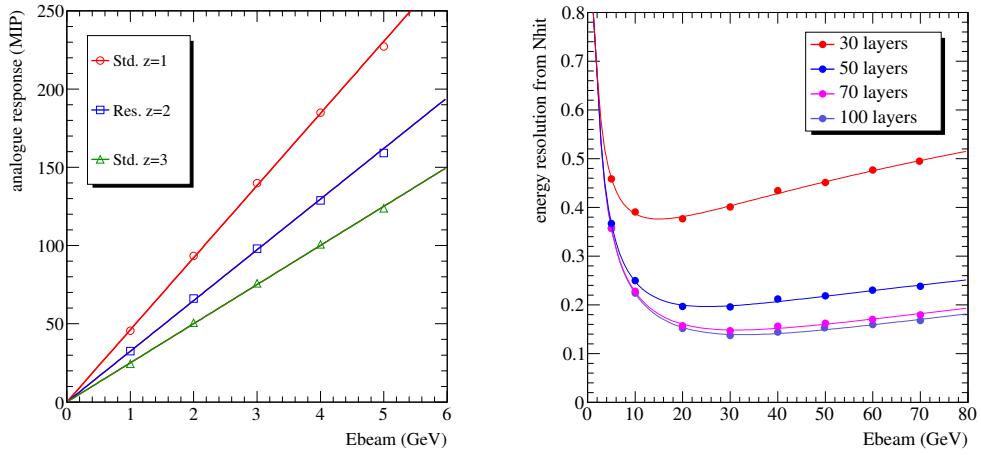


Figure 4.13: Electron response of a virtual Micromegas SDHCAL deduced from measurements of longitudinal shower profiles in non-resistive ($z=1$ and $z=3$) and resistive ($z=2$) Micromegas prototypes placed behind increasing thicknesses of passive material (left). Geant4 calculation of the energy resolution to pions of a Micromegas DHCAL of 30 to 100 layers based on simple hit counting (right).

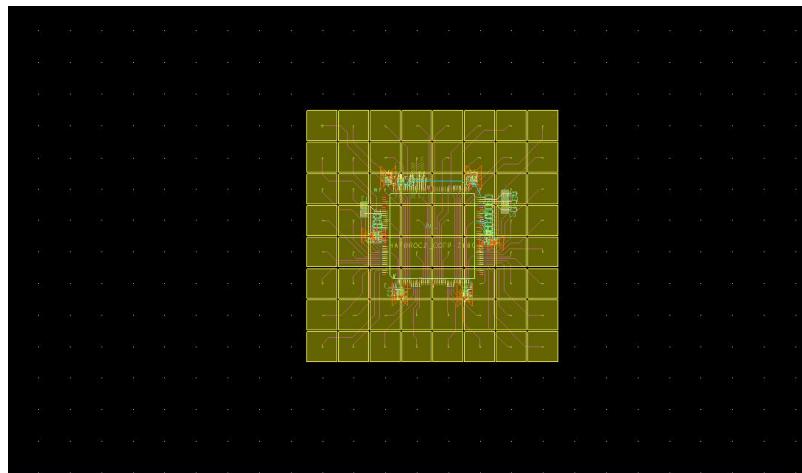


Figure 4.14: Pads connection to the ASIC's pins

map the buffers of all read DIFs but it requires to manage memory allocation, access and cleaning. This was achieved thanks to the abilities offered by recent Linux kernels to use file based shared memory. In addition, whenever several computers are involved in the data taking, as it is the case for the SDHCAL prototype, a communication framework is needed. The CMS data acquisition XDAQ framework was chosen. This provides communication tools with both binary and XML, an XML description of the computer and software architecture, a web-server implementation of all data acquisition application and a scalable event builder. A monitoring system was also developed to have an online follow-up of the acquisition during data collection.

4.9.3 GRPC-SDHCAL for ILD

Detector Development

The structure of GRPC proposed as an active layer of the HCAL proposed for ILD is shown in Figure 4.15. It is made out of two glass plates of 0.7 mm and 1.1 mm thickness. The thinner is used to form the anode while the thicker forms the cathode. Ceramic balls of 1.2 mm diameter are used as spacers between the glass plates. The balls are glued on only one of the glass plates. In addition to those balls, 13 cylindrical fiber-glass buttons of 4 mm diameter are also used. Contrary to the ceramic balls the buttons are glued to both plates ensuring thus a robust structure.

Special spacers (ceramic balls) were used to maintain uniform gas gap of 1.2 mm. Their number and distribution were optimized to reduce the noise and dead zones (0.1%). The distance between the spacers (10 cm) was fixed so that the deviation of the gap distance between the two plates under the glass weight and the electric force does not exceed 45 microns. The choice of these spacers rather than fishing lines was intended to reduce the dead zones (0.1%). It was also aimed at reducing the noise contribution observed along the fishing lines in standard GRPC chambers. The gas volume is closed by a 1.2 mm thick and 3 mm wide glass-fiber frame glued on both glass plates. The glue used for both the frame and the spacers was chosen for its chemical passivity and long term performance.

The resistive coating on the glass plates which is used to apply the high voltage and thus to create the electric field in the gas volume was found to play important role in the pad multiplicity associated to a mip [110]. To find the best coating for GRPC chambers many products were tested. Finally, a new product based on two components was chosen. By changing the two components ratio one can obtain the needed surface resistivity. Commercial products like Licron™ and Statguard™ which are used for Electro-Static Discharge (ESD) applications were tried and few 1 m^2 chambers were built using those products and intensively tested. Both products failed to satisfy our application either for long term stability under the high voltage (Licron using those products) or due to the impossibility to obtain the surface uniformity needed for our application (Statguard using those products). Eventually, two products were identified, both of which are based on colloids containing graphite. Both can be applied using the silk screen print method, which ensures very uniform surface quality. One of these products is a single component paint with a dry surface resistivity of $1 - 10 \text{ M}\Omega/\square$. The second product comes as two components which must be mixed by the user. The surface resistivity may be adjusted over a wide range by changing the mix ratio. Both products require baking at around 170° C to attain a stable surface resistivity. One product based on colloids containing graphite was finally selected. The product can be applied using the silk screen print method, which ensures very uniform surface quality. In addition, the product is made of two components and it was found that by changing the mix ratio the surface resistivity may be adjusted over a wide range.

The measured surface resistivity at various points over a 1 m^2 glass coated with the previous paint showed a mean value of $1.2 \text{ M}\Omega/\square$ and a ratio of the maximum to minimum values of less than 2. A study was also made of the repeatability of the surface resistivity between different mix batches. It was found

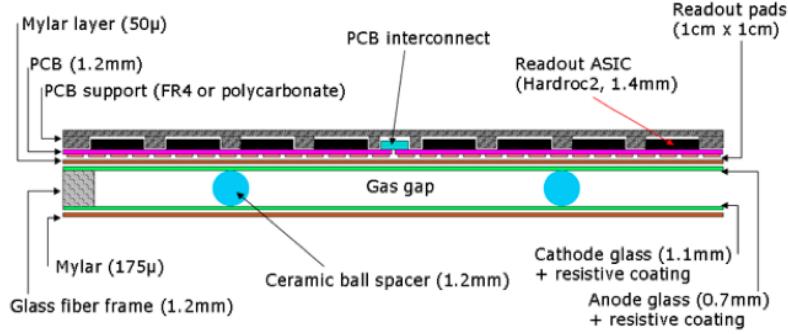


Figure 4.15: Cross-section through a 1 m^2 chamber

that surface resistivity in the range $0.5 - 2 \text{ M}\Omega/\square$ could be reliably reproduced. For 1 m^2 GRPCs the painting is applied on the whole glass plate except for 3 mm from the edges. This distance, corresponding to the frame width, was optimized so the dead zone of the detector is reduced while external sparks due to the presence of the metallic cassette in the vicinity is completely eliminated.

Another important aspect of this development concerns the gas circulation within the GRPC taking into account that for ILD SDHCAL gas outlets should all be on one side. A genuine system was proposed. It is based on channeling the gas along one side of the chamber and releasing it into the main gas volume at regular intervals. A similar system is used to collect the gas on the opposite side. A finite element model has been established to check the gas distribution [111]. The simulation confirms that the gas speed is reasonably uniform over most of the chamber area.

In order to improve on the gas distribution in large chambers taking into account the requirement that both gas outlets should be on the same side of the detector to satisfy all possible mechanical structures proposed for ILD hadronic calorimeter, new schemes were studied. The one we finally adopted allows us to improve the gas distribution by channeling the gas along one side of the chamber and releasing it into the main gas volume at regular intervals thanks to 1.2 mm diameter PEEK™ tubes fixed 2 cm from the chamber side. A similar system is used to collect the gas at the other side of the chamber. A finite element model has been established to check the gas distribution [111]. The simulation confirms that the gas speed is reasonably uniform over most of the chamber area. as can be seen in Figure 4.16.

The GRPC and its associated electronics are housed in a special cassette which protects the chamber and ensures that the readout board is in intimate contact with the anode glass. The cassette is a thin box consisting of 2.5 mm thick stainless steel plates separated by 6 mm wide stainless steel spacers. Its plates are also a part of the absorber.

The electronics board is assembled thanks to a polycarbonate spacer which is also used to fill the gaps between the readout chips and to improve the overall rigidity of the detector. The electronics board is fixed on the small plate of the cassette. Thanks to tiny screws and the new set is fixed on the other plate which hosts the detector and the spacers. The whole width of the cassette is 11 mm with only 6 of them corresponding to the sensitive medium including the GRPC detector and the readout electronics.

4.9.4 Prototype

A technological prototype corresponding to the SDHCAL option proposed in the ILC LOI was built. 48 cassettes as the one described above were built. They fulfilled a stringent quality control. It is worth

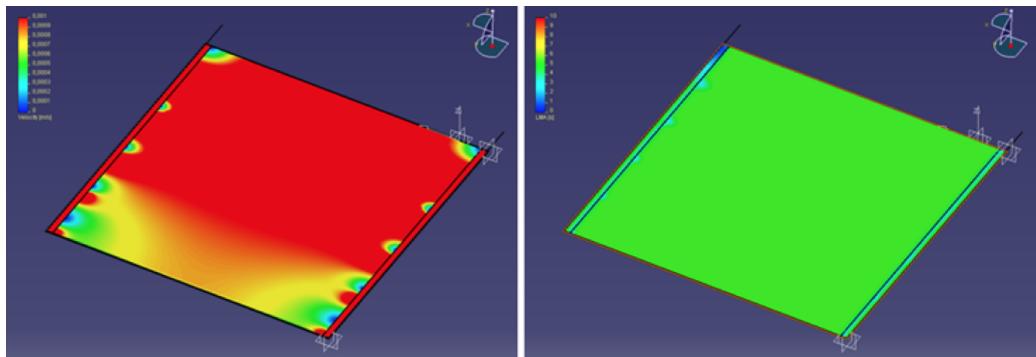


Figure 4.16: Left: Gas speed profile in the range 0–1 mm/s; Right: Least mean age profile in the range 0–10 s

mentioning that 10500 HR ASICs were produced and tested using a dedicated robot for this purpose. The yield was found to be higher than 92%. The ASICs were then fixed on the PCBs to make a 1 m² and itself fixed on the cassette cover once successfully tested.

The cassettes were inserted in a self-supporting mechanical structure that was conceived and built in collaboration with the Spanish group of CIEMAT. The structure is made of Stainless Steel plates of 1.5 cm each. The plates were machined to have an excellent flatness and well controlled thickness. The flatness of the plates was measured using a laser-based interferometer system. It was found that the flatness of the plates are less than 500 microns. This results guarantees that for the SDHCAL V structure proposed for ILD, a tolerance of less than 1 mm is achievable.

The first cassettes were extensively tested using a cosmic-rays bench and later particles beam at CERN. Both the efficiency and the multiplicity of the GPC cassettes were studied. These studies showed high efficiency and good homogeneity and validated the cassette concept.

The prototype construction lasted less than 6 months. A commissioning test at CERN in 2011 allowed to understand the whole system behavior. More precisely a problem related to the acquisition system of the more than 430000 channels was found and fixed.

In parallel a single cassette was tested in a magnetic field of 3 Tesla (H2 line at CERN) applying the power-pulsed mode. The TB results indicated clearly that the use of the power-pulsed mode in such a magnetic field is possible. The behavior of the detector (efficiency, Figure ??, multiplicity, Figure ??) was found to be similar to those obtained in the absence of both the magnetic field and the power-pulsed mode.

In April 2012 the prototype was exposed to pion, muon, electron beams of both the PS and the SPS of CERN (Figure 4.17). Power-pulsed mode was applied to the whole prototype using the beam cycle structure (0.3 ms time duration for the PS beam and 9 s for the SPS beam every 45 s). A basic water-based cooling system was used to keep under control the temperature increase particularly in the case of the SPS where the consumption reduction is only 5 (to compare with a factor of more than 100 in the ILC case). An acquisition mode similar to that of the ILC was operated. The data were collected continuously in a triggerless mode. The DAQ stops when the memory of one ASIC is full. Data are then transferred to a storage station and then the acquisition starts again. Figures ?? and ?? show the efficiency and pad multiplicity of the prototype GPC chambers measured using the muon beam.

The SDHCAL prototype results obtained with a minimum data treatment (no grain correction) show clearly that excellent linearity and good resolution could be achieved on large energy scale as can be shown in Figures ?? and ?? . Useless to mention that the high granularity of the SDHCAL allows one to study thoroughly the hadronic showers topology and to improve on the energy resolution by, among others,

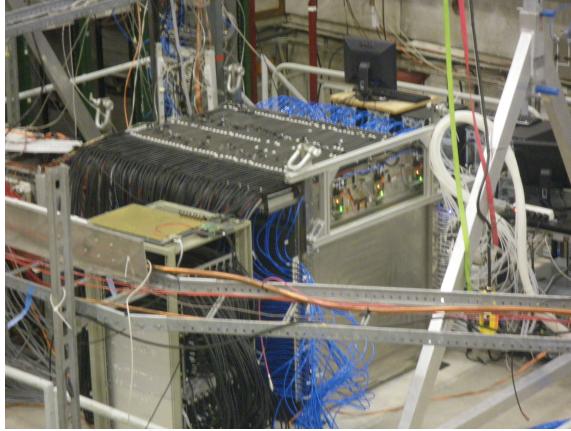


Figure 4.17: Cross-section through a 1 m^2 chamber.

separating the electromagnetic and the hadronic contribution. The separation between close-by showers will also get big benefit thanks to the high granularity on the one hand and to the very clean detector response ($< 1\text{ Hz/cm}^2$) on the other hand. These two points are being worked and recent results confirm this.

The quality of data obtained during three weeks of data taking validates completely the SDHCAL concept as proposed in the LOI. This is especially encouraging since no gain correction was applied to the electronics channels to equalize their response. However a gain correction mode is elaborated and tested during the TB. It will be applied in the future to assess the effect of such correction on the energy resolution.

4.9.5 ILD Preparation

The expertise acquired with the construction and the commissioning of the technological prototype and the obtained results were used to implement a realistic simulation of the ILD HCAL. Physics channels such as the $t\bar{t}H$ were studied using the SDHCAL option and results were found identical to those obtained with the scintillator tile option despite the fact that the jet energy reconstruction code was optimized for the latter.

In addition, the French groups participated actively in the HCAL part of the ILC TDR (ILD part) by proposing a genuine mechanical structure for the hadronic calorimeter (called V-structure). The V structure was conceived to eliminate the projective holes and cracks so none of the particles produced close to the detector centre could escape detection. The V structure has additional advantages. It eliminates in principle the space between the barrel and the Endcaps avoiding the shower deformation which results not only because of this space but also of the different cables and services needed in CMS-like mechanical structures. In this structure the different services such as the gas tubes, data collection and electric cables of both the barrel and the Endcaps are taken out from the outer radius side. Detailed studies have shown that the deformation of this structure is extremely low and its robustness was verified experimentally with the SDHCAL technological prototype built with a self-supporting structure respecting the spirit of the V one. Services and Integration issues were also worked out. Besides, realistic costing was performed, based on the prototype experience.

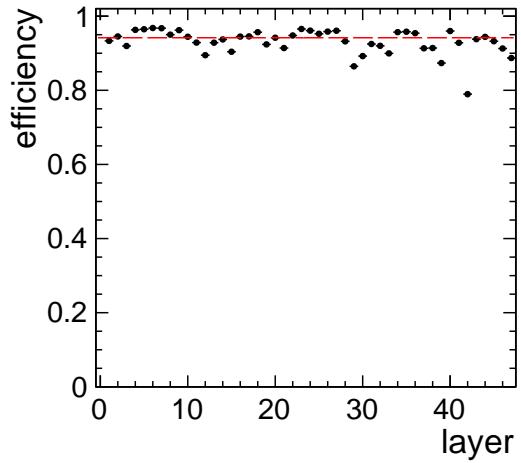


Figure 4.18: Efficiency of the GRPC prototype

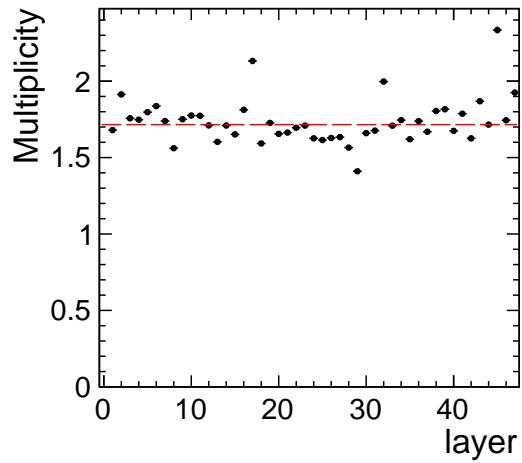


Figure 4.19: Pad multiplicity of the GRPC prototype.



Figure 4.20: GRPC setup in the CERN SPS-H2 line magnetic field.

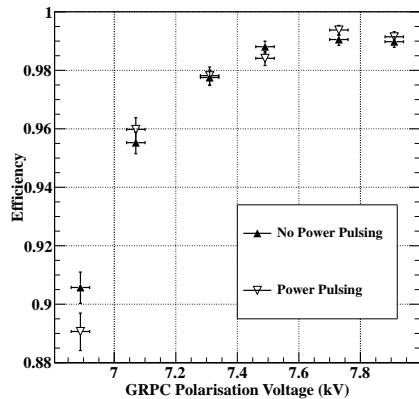


Figure 4.21: Efficiency scan over high voltage, with and without power pulsing.

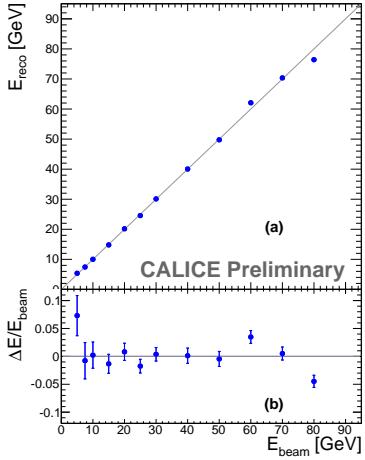


Figure 4.22: (a): Mean reconstructed energy for pion showers and (b): relative deviation of the pion mean reconstructed energy with respect to the beam energy.

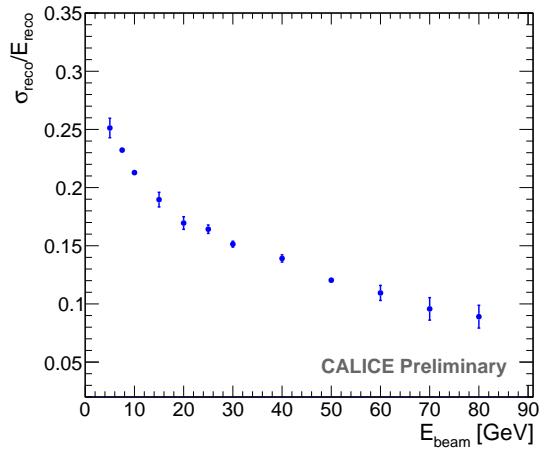


Figure 4.23: $\frac{\sigma_{reco}}{E_{reco}}$ of the reconstructed pion energy E_{reco} as a function of the beam energy.

4.9.6 Recent Milestones

4.9.7 Engineering Challenges

4.9.8 Detector R&D plans for the coming years

Large GPC of 1m^2 were developed and built for the technological prototype. However, larger GPC are needed in the future DHCAL with the largest one being $290 \times 91\text{ cm}^2$. These large chambers with gas inlet and outlet on one side need a dedicated study to guarantee a uniform gas gap everywhere notwithstanding the angle of the plate. It is necessary also to ensure an efficient gas distribution as it was done for the 1 m^2 chambers. To obtain this different gas distribution systems were studied. A new scheme with two gas inlets and one outlet was found to ensure an excellent homogeneity of the gas distribution. This system will be used in the near future to build large detectors exceeding 2 m^2 . The readout of such chambers needs also to be as efficient as the one of the technological prototype 1 m^2 . An upgrade of the HR ASIC allowing larger dynamic range was conceived, produced and successfully tested [4.24](#). The new ASIC (HR3) allows to be directly addressed and easily bypassed in case of failure thanks to the I2C protocol. In addition and contrary to the HR2, the 64 channels of the new ASIC are independent which allows a better calibration procedure. In addition to the previous challenges we need to improve on the interface boards (DIF) needed to control the ASICs synchronization and data transfer. Indeed, the space left between the active layer of one module and the cryostat is only 5 cm. This means that the DIF components should be optimized to cope with the volume availability. A new design with new functionalities of the DIF is proposed. A TPC/IP protocol is adopted for data transfer and a TTC one for the clock synchronisation. A microprocessor implemented on the new DIF is in charge of the communication between the ASICs and the DIF's FPGA. The new DIF is capable to address up to 432 ASIC. New PCB design that allows to assemble few boards to cover up to 3 m^2 GPC detector is being conceived. Care is taken to ensure robust and flexible but still tiny connection between the different PCB to build large one. Finally a new technique based on electron beam welding is

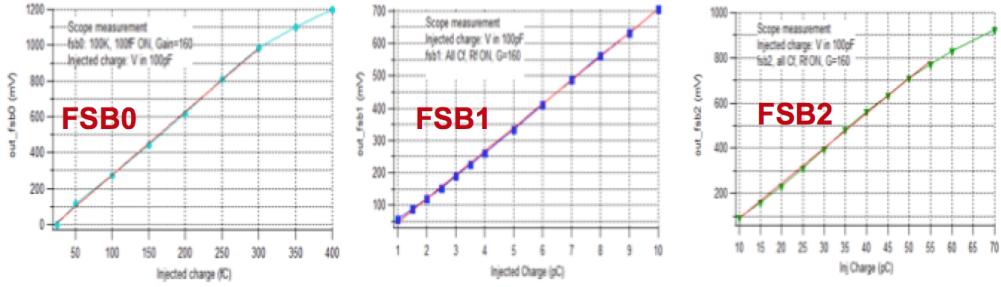


Figure 4.24: Dynamic range of the fast shapers associated to the three thresholds of the new version of HARDROC.



Figure 4.25: A prototype of an SDHCAL mechanical structure assembled using the electron beam welding technique.

being tested to build a mechanical structure. This intends to reduce the steel quantity used to assemble the absorber plates while guaranteeing a minimum deformation. First attempts have taken place at CERN recently 4.25 and more study is ongoing to determine the best protocol one should follow to obtain optimal results.

4.9.9 Applications Outside of Linear Colliders

4.10 DualReadout

4.10.1 Introduction

The scientific goal of RD52 (previously the DREAM collaboration) is to understand the fundamental limitations to hadronic energy resolution and, in general, the limitations to achieving high-quality calorimetric performance in Gaussian energy resolution, mean response linearity, and ease and precision of calibration.

Hadron detection with a dual-readout calorimeter

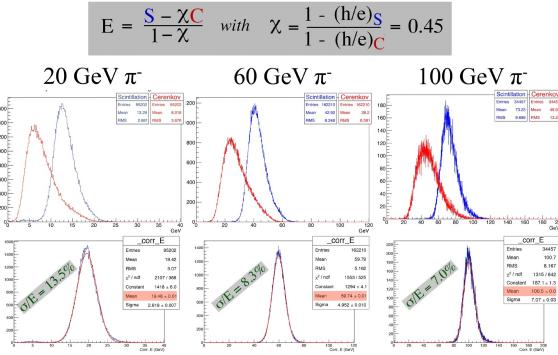


Figure 4.26: Raw scintillation and Cerenkov data for 20, 60, and 100 GeV pion beam, and the dual readout response below

4.10.2 Recent Milestones

The essential features of our fiber dual-readout calorimeters are (a) near-perfect optical conduits (fibers) for read-out, (b) fine spatial sampling on the mm-scale, (c) dual measurement of scintillation light in scintillating fibers (all charged particles) and simultaneous Cerenkov light in clear fibers (only electromagnetic particles), (d) absolute fiber-absorber volume uniformity, and (e) low-noise readout with PMTs below 100 MeV per ton of calorimeter. This design achieves a Gaussian response, a linearity near 1% from 20-300 GeV, and excellent energy resolution. The calibration is by a direct electron beam into each calorimeter tower.

About 30 dual-readout papers are published in Nucl. Intrs. Meths., Rev. Sci. Instr., and JINST, including dual-readout in several crystals, a planar geometry, as well as fibers in several geometries. We have built and tested Pb-based and Cu-based dual-readout modules and are designing a W-based test module. Typical readout of the Pb-modules is shown in Figure 4.26 for 20, 60, and 100 GeV pion beams in the H8 beam of the North Area at CERN. Simple dual-readout yields a Gaussian and linear response, currently limited by lateral leakage fluctuations in the Pb-based modules of about 1 tonne. The record holder for linear, Gaussian energy resolution is still the SPACAL module of 20 years ago, built by Wigmans at CERN to demonstrate the newly understood concept of “compensation”. SPACAL was a Pb-scintillating fiber module of mass 20 tonnes that collected scintillation light for 100-200 ns to achieve compensation from the $np \rightarrow np$ recoils in the scintillating fibers. We show in Fig. 2 the hadronic energy resolutions for single pions for SPACAL, DREAM, and the new RD52 modules, plotted vs. $1/\sqrt{E}$, so that the slope is the stochastic term and the intercept is the constant term. A calorimeter with the ILC goal for hadronic energy resolution of $\sigma/E = 30\%/\sqrt{E}$ is shown as the thin red line. We have not yet achieved this goal, but we know we are limited merely by lateral leakage fluctuations which can be suppressed by a larger module. As shown in Fig. 2 we are closing in. There are several improvements over the results in Figure 4.27 for (a) Cerenkov photoelectron yield, (b) photocathode efficiency, (c) fiber quality, (d) optical uniformity and, finally, (e) absorber mass. All of these are planned for testing one year from now at CERN. We expect, based on our data, simulations, and our understanding, that we are likely to achieve a resolution of about $30\%/\sqrt{E}$ with a small constant term. This would result in 3% energy resolution at 100 GeV and about 2% energy resolution at the highest SPS beam energies available at CERN.

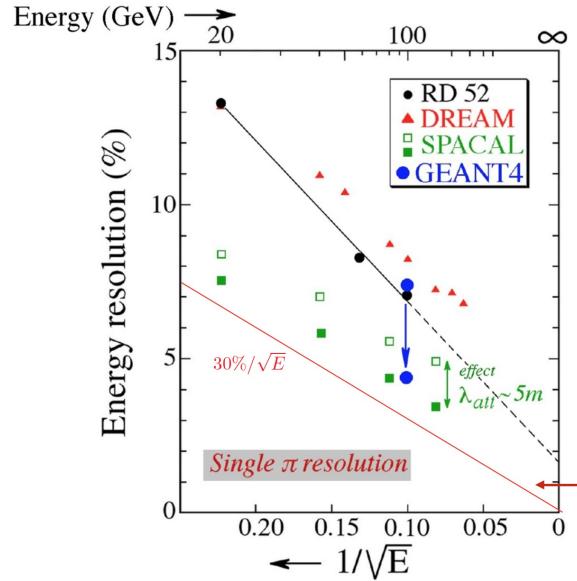


Figure 4.27: Hadronic energy resolution for SPACAL, DREAM, and RD52 modules

4.10.3 Engineering Challenges

Manufacturing of the high-precision absorber, whether Pb or Cu or W. Assembly of a large calorimeter involves a lot of fibers which can and must be automated. Control of the optics to 1% is a challenge. It should be emphasized that we do not have engineers working on RD52, but rather find simple solutions which achieve the physics goals without expending large funds. On a construction project, engineering design would improve all our results.

4.10.4 Future Plans

Solving the problems of projective geometry; implementation of SiPM readout; manufacture of a tungsten W-absorber with full dual-readout capability; test of a gaseous dual-readout calorimeter.

4.10.5 Applications Outside of Linear Colliders

High precision calorimetry is vital to many experiments, both collider and fixed target; dual-readout is considered for a space station experiment; and, a high-precision dual-readout calorimeter is being considered for an electron-ion col- lider.

4.10.6 References

Complete papers, figures, proposals, status reports, and photos are accessible at our website: <http://highenergy.phys.ttu.edu/dream>

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities	
Scintillator ECAL	Nihon Dental University Shinshu University Tokyo University, ICEPP Tsukuba University				
SiliconECAL ILD	LPNHE-ParisLAL University of Tokyo Kyushu University SKKU (Suwon, Korea) LLR/Palaiseau OMEGA/Palaiseau LPSC/Grenoble				
SiliconECAL SiD					
AHCAL	DESY Hamburg Heidelberg MPI Munich Wuppertal Mainz Omega CERN ITEP MEPHI Dubna Prague NIU Tokyo University, ICEPP Bergen Shinshu	The analog hadron calorimeter is based on small plastic scintillator tiles read out with SiPM. It uses fully integrated electronics with power pulsing, auto-trigger and time-stamping capability.	2014 - multi-layer test beam campaign at CERN with technical prototype electronics, including large-size layers (4 HBUs) 2015 - First beam tests of full HBU with SMD SiPMs fabricated with automated assembly procedure	2015 Test beams at DESY and SPS with >15 HBUs 2016/17 Test beam at SLAC with 15 layer EM stack, powerpulsing & ILC time structure, tests in magnetic field further develop SMD SiPM HBUs, explore "mega-tile" options Hadronic beam tests with a prototype with 1m ³ fully instrumented volume (depends on pending funding request)	
DHCAL (RPC)	Argonne National Laboratory Boston University COE College (Iowa) University of Iowa Shanghai Jiao Tong University – SJTU (in discussion) University of Science and Technology of China – USTC (in discussion)				
SDHCAL (RPC)	SDHCAL(micromegas)	CALICE (LAPP) CEA Saclay Institute of Nuclear and Particle Physics, Demokritos	Micromegas is a thin steel micromesh that separates the gas volume in a region of charge conversion and a region of charge multiplication. It is interesting for EM and H calorimetry because its signal is proportional to the energy deposit in the gas. To avoid discharge upon very large energy deposits, it now incorporates resistive elements on the readout electrodes.	2012: construction and successful test of 1x1 m ² realistic prototypes for the CALICE SDHCAL. 2014: demonstration of discharge suppression with small resistive prototypes. 2015: optimisation of the resistive prototypes for best linearity and rate capability.	Construction of a Micromegas calorimeter prototype for measuring performance to electrons and later hadrons.
GEM DHCAL	University of Texas, Arlington				
Dual Readout RD52	RD52	Texas Tech University Iowa State University INFN Pavia INFN Pisa INFN Cagliari INFN Rome INFN Cosenza LIP Lisbon INFN Lecce CERN Tufts University			
FCAL		AGH-University of Science and Technology, Cracow, Poland CERN, Geneva, Switzerland DESY, Zeuthen, Germany IFIN-HH, Bucharest, Romania IFJPN, Cracow, Poland ISS Bucharest, Romania LAL Orsay, France JINR Dubna, Russia NCPEP Minsk, Belarus Pontificia Universidad Católica de Chile, Santiago, Chile Tel Aviv University, Tel Aviv, Israel Tohoku University Sendai, Japan University of Colorado Boulder, USA University of California Santa Cruz, USA VINCA Institute of Nuclear Science & University of Belgrade, Belgrade, Serbia			

Chapter 5

Forward Calorimeters

5.1 FCAL

5.1.1 Introduction

Two special calorimeters are foreseen in the very forward regions of a linear collider detector, denoted hereafter as LumiCal and BeamCal. These calorimeters will deliver both a fast and a precise measurement of the luminosity and extend the detector coverage to low polar angles, important e.g. for new particle searches with missing energy signature. Detailed Monte Carlo studies have been performed in all member institutes to optimize the design of the calorimeters, estimate the background from physics processes and understand the impact of beam-beam interactions on the luminosity measurement [112]. A sketch of the design is shown in Figure 5.1 (left). To ensure a high efficiency for single high energy electron detection on top of the large and widely spread background from beamstrahlung very compact calorimeters are needed. In addition, compact calorimeters facilitate the reconstruction of Bhabha scattering events. Due to the high

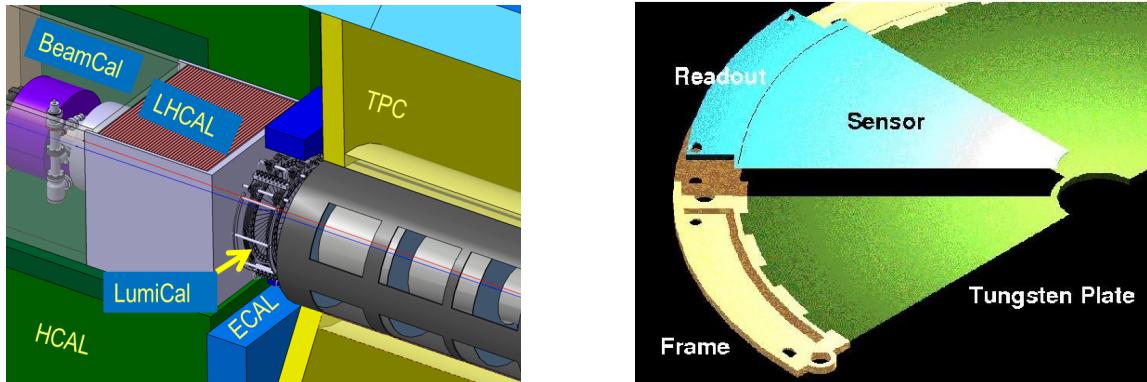


Figure 5.1: Left: The very forward region of the ILD detector. LumiCal, BeamCal and LHCAL are carried by the support tube for the final focusing quadrupole QD0 and the beam-pipe. TPC denotes the central track chamber, ECAL the electromagnetic and HCAL the hadron calorimeter. Right: A half layer of an absorber disk with a sensor sector and front-end electronics.

occupancy originating from beamstrahlung and two-photon processes, both calorimeters need a dedicated fast readout. In addition, the lower polar angle range of BeamCal is exposed to a large flux of low energy electrons, resulting in depositions up to one MGy per year. Hence, radiation hard sensors are needed.

5.1.2 Mechanical Concept

Since in both calorimeters a robust electron and photon shower measurement is essential, a small Molière radius will be preferable. Compact cylindrical sandwich calorimeters using tungsten absorber disks of one radiation length thickness, interspersed with finely segmented silicon (LumiCal) or GaAs (BeamCal) sensor planes, as sketched in Figure 5.1 (right), are found to match the requirements from physics [112].

5.1.3 Recent Milestones

5.1.4 Engineering Challenges

Engineering challenges within the current and future research within FCAL are the following:

- a slim assembled sensor plane. The space between absorber planes must be kept as small as possible. The fan-out to move the signals from the sensor pads to the outside radius must be very thin and hence a new connectivity technology must be applied.
- multichannel front-end and ADC ASICs for the prototype. A compromise must be found between integration, miniaturization and costs.
- operation using power pulsing.
- a dedicated solution for data concentration, data reduction and transmission.
- precise alignment and position monitoring.

5.1.5 Future Plans

Sensors and ASICs

Large area GaAs sensors, as shown in Figure 5.2, were developed and produced in collaboration with partners in industry. The Liquid Encapsulated Czochralski technology is used. The sensors were doped by a shallow donor (Sn or Te), and then compensated with Chromium. This results in a semi-insulating GaAs material with a resistivity of about $10^7 \Omega\text{m}$. The sensors are 0.5 mm thick with pads of a few mm^2 area. The operation voltage is about 100 V with leakage current per pad less than 500 nA.

Prototypes of LumiCal sensors have been designed and manufactured by Hamamatsu Photonics. Their shape is a ring segment of 30°. The thickness of the n-type silicon bulk is 0.320 mm. The pitch of the concentric p⁺ pads is 1.8 mm and the gap between two pads is 0.1 mm. The bias voltage for full depletion ranges between 39 and 45 V, and the leakage currents per pad are below 5 nA [113].

Dedicated ASICs were designed choosing an architecture [114, 115] comprising a charge sensitive amplifier and a shaper. ASICs, containing 8 front-end channels, were designed and fabricated in 0.35 μm CMOS technology. A micro-graph of the prototype, glued and bonded on the PCB, is shown Figure 5.3. A variable gain in both the charge amplifier and the shaper is implemented by a mode switch. The peaking time of the shaper output signal is 60 ns. More results of the measurements of the performance were

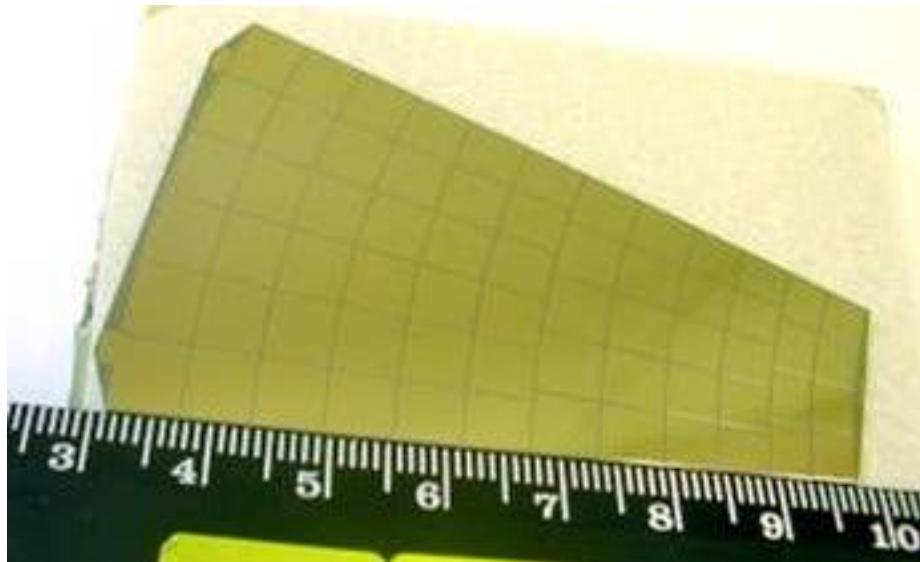


Figure 5.2: A GaAs pad sensor developed for BeamCal.

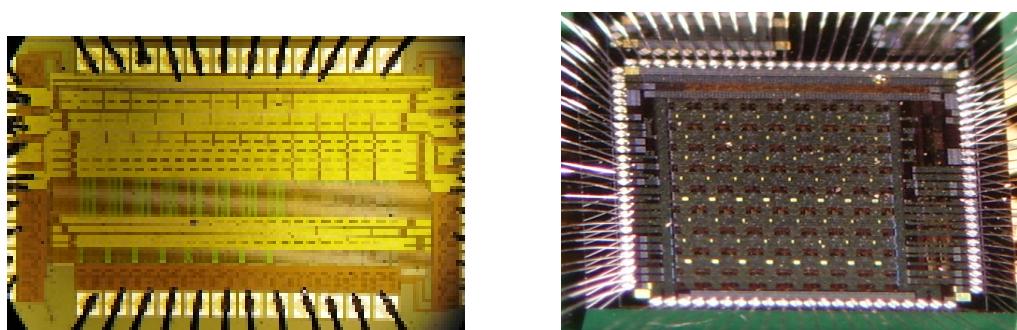


Figure 5.3: Left: Micrograph of front-end ASIC. Right: Micrograph of ADC ASIC.

published elsewhere [116]. A dedicated low-power, small-area, multichannel ADC is designed and produced [117]. It comprises eight 10-bit power and frequency (up to 24 MS/s) scalable pipeline ADCs and the necessary auxiliary components. A micro-graph of the prototype is shown in Figure 5.3.

A dedicated ASIC development is ongoing for BeamCal [118] with a special option for a fast readout of an reduced amount of information from each bunch-crossing to be used for a fast feedback system for beam-tuning. A prototype of a pixel sensor readout for the pair monitor, positioned in front of BeamCal was designed in SoI technology [119].

5.1.6 Test-beam Results

Several test-beam campaigns were done to investigate the performance of single fully instrumented sensor planes, both for LumiCal and BeamCal. Prototypes of sensor planes assembled with FE and ADC ASICs, as shown in Figure 5.4, were built using LumiCal and BeamCal sensors [120]. The detector plane prototypes



Figure 5.4: Photograph of LumiCal readout module with sensor connected.

were installed in an electron beam and the trajectories of beam particles were measured by four planes of a silicon strip telescope. The front-end electronics outputs were sampled synchronously with the beam clock, a mode used at the ILC. Data were taken for different pads and also for regions covering pad boundaries. Signal-to-noise ratios of better than 20 are measured for beam particles both for LumiCal and BeamCal sensors, as illustrated in Figure 5.5 (left). The impact point on the sensor is reconstructed from the telescope information. Using a color code for the signals on the pads the structure of the sensor becomes nicely visible, as also seen in Figure 5.5 (right). The sensor response was found to be uniform over the pad area and to drop by about 10% in the area between pads.

5.1.7 Radiation Damage Studies

Two studies of the radiation tolerance of potential BeamCal sensors have been carried out. The radiation tolerance of prototype GaAs sensors has been explored by exposing the sensors to direct irradiation from a high-intensity electron beam of about 10 MeV [121], which is an energy expected from beamstrahlung remnants at the ILC. It was found that the sensors can be operated up to approximately 1 MGy of this type of radiation without a significant increase in the leakage current [122]; however, significant loss in the response to ionizing particles was observed. In addition, several different silicon-diode sensor technologies

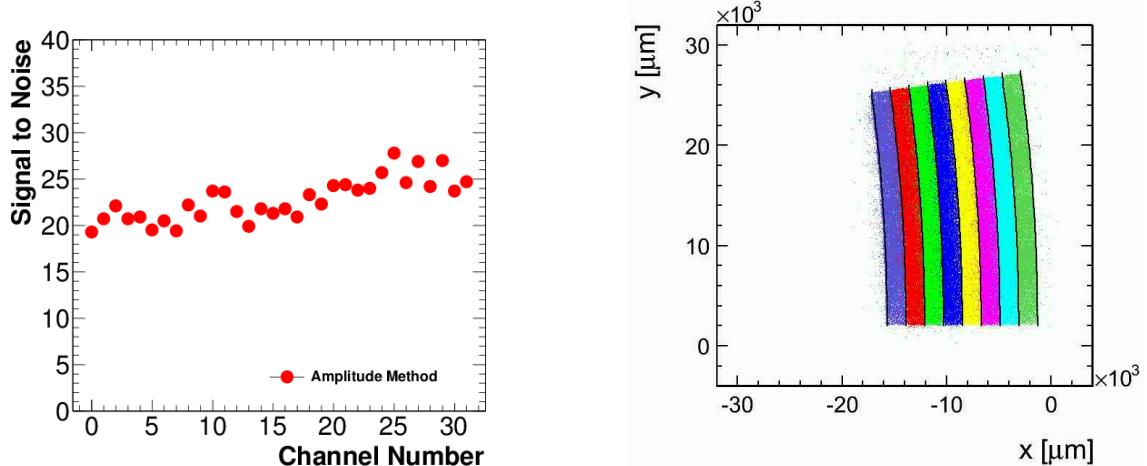


Figure 5.5: Left: The signal-to-noise ratio of all readout channels. Right: Distribution of the predicted impact points on pads with a color coded signal.

were exposed to varying levels of radiation induced by the SLAC End Station A Test Beam (ESTB). For this study, the ESTB test beam, with energies varying between 3 and 11 GeV, was directed into a tungsten beam stop. The beam stop was split at approximately shower-max and the sensor inserted, leading to an exposure incorporating the full spectrum of particle species that will irradiate the BeamCal sensors. Both n-type bulk oxygenated float-zone and magnetic Czochralski detectors were explored, with exposures varying from 0.2 to 2.2 MGy as allowed by the limited exposure rate and beam availability. It was found that, after allowing for a short period of controlled annealing, all sensor types withstood the maximum dose that they received with little loss in response to ionizing particles [123], but with some increase in leakage current. Further annealing studies, geared towards achieving a minimal post-irradiation leakage current, continue. Further irradiation studies in the ESTB are planned for the spring running periods of 2014 and 2015. The sensor assessment (“charge-collection efficiency”) apparatus at the Santa Cruz Institute for Particle Physics is being adapted for the evaluation of pad sensors, which will allow for radiation damage studies of the prototype GaAs sensors in this realistic electromagnetic shower environment. Studies to push the silicon diode sensors to higher levels of irradiation are also planned.

5.1.8 Technological Prototype

Currently the goal of FCAL is to prepare a calorimeter prototype for test-beam measurements. These measurements are essential firstly to develop and test engineering solutions to build a very compact calorimeter and secondly to verify the results of Monte Carlo studies. Depending on the test beam results the calorimeter may be redesigned. For the prototype calorimeter a mechanical structure, a sufficient amount of front-end and ADC ASICs, FPGAs for data concentration and a data acquisition system are needed.

Mechanical Stack

A flexible mechanical structure, as shown in Figure 5.6, has been built as part of the AIDA I project at CERN, to compose a calorimeter prototype instrumented both with LumiCal and BeamCal sensors. Tungsten

absorber plates, glued on a permaglass frame, are precisely positioned on a rod assembly, and interspersed with fully assembled sensor planes. The flatness of the absorber plates is better than $50\text{ }\mu\text{m}$ to allow high

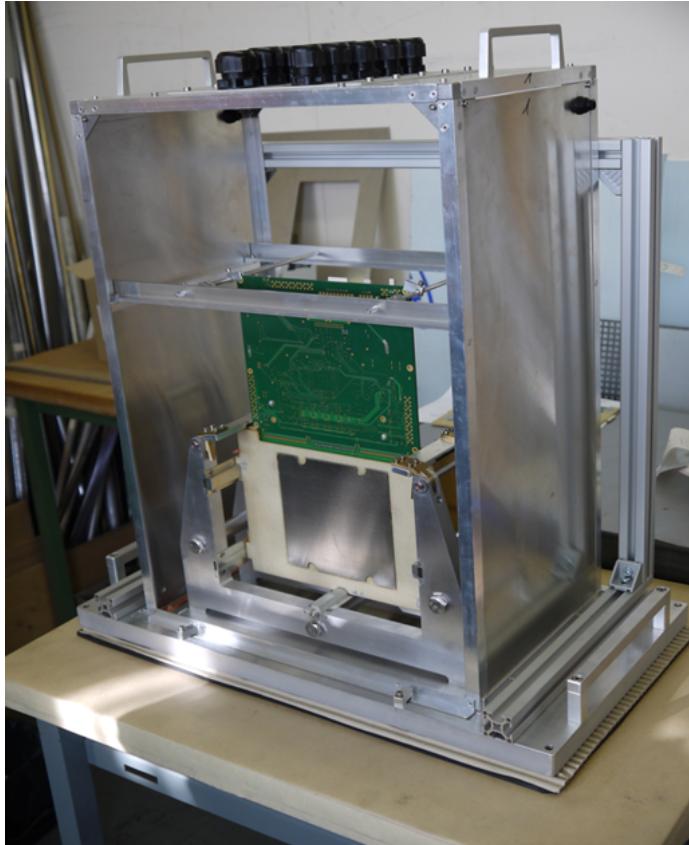


Figure 5.6: Photograph of the flexible mechanical structure. Tungsten absorber plates, glued on permaglass frames, are put into slots of the rod assembly.

compact packing of sensor and absorber planes.

Alignment and Position Monitoring

A laboratory set-up for position monitoring has been constructed by IFJPAN Cracow using semi-transparent silicon sensors. Test measurements demonstrated that position monitoring with μm precision is possible.

Front-End and ADC ASICs

To match the requirements of extremely low power consumption and taking into account possible radiation fields in the very forward region, a new development of the front-end and ADC ASICs in deep sub-micron 130 nm CMOS technology has been pursued within AIDA by UST Cracow. These ASICs will be sufficiently fast to be used both in LumiCal and BeamCal. The overall readout architecture, so far successfully produced in 350 nm CMOS technology and used in the test-beam measurements as described above, has not been

changed and comprises separated front-end and ADC ASICs for each readout channel. For both FE and

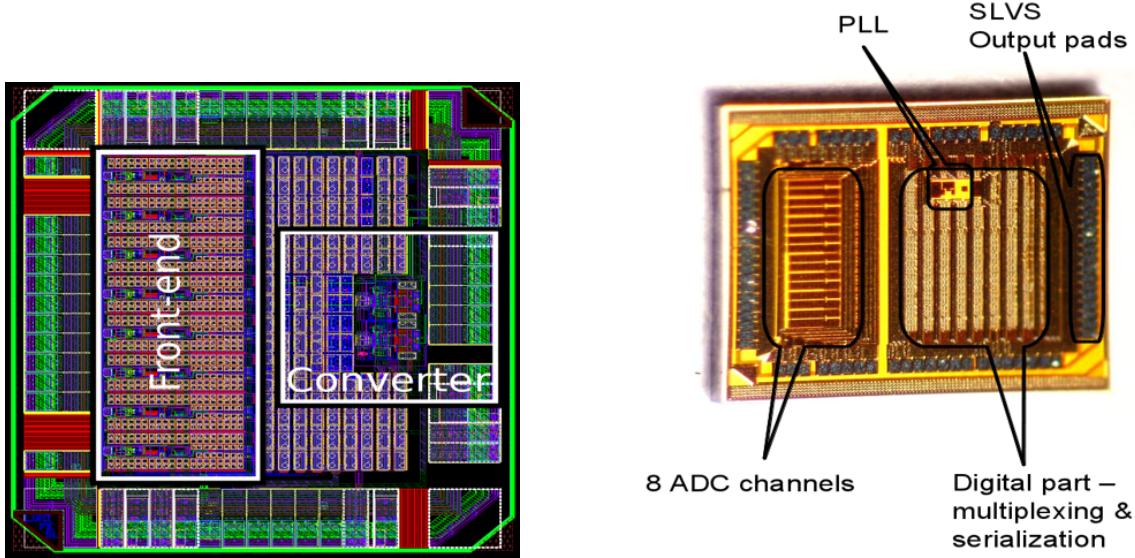


Figure 5.7: Left: 8 channel FE ASIC in 130 nm technology. Right: ADC ASIC in 130 nm technology.

ADC ASICs prototypes, shown in Figure 5.7, are under test.

Data Concentrator and DAQ

In order to operate a large amount of sensor planes the readout has to be orchestrated. For this purpose a FPGA based data concentrator is foreseen which may deliver data in the so called AIDA protocol. The design of this device is currently under discussion. The higher level DAQ will depend on the functionality of the data concentrator. For the readout of test-beam data we have software, mainly developed by University of Tel Aviv, which can be easily adopted. For a final device FCAL will follow the developments of a common DAQ for all subdetectors.

5.1.9 Applications Outside of Linear Colliders

The expertise acquired within FCAL for radiation hard sensors and fast front-end electronics was used to build, commission and operate fast beam-conditions monitors at the CMS experiment at LHC. Radiation hard sensors developed within FCAL are used as beam-loss monitors with excellent time resolution at FLASH and LHC. A design for beam-loss monitors for XFEL is prepared. In addition, front-end ASICs are under development for the upgrade of the LHCb tracker.

Chapter 6

Software Tools

6.1 LCIO

6.1.1 Introduction

6.1.2 Recent Milestones

The LCIO software toolkit [124] was developed to provide a common event data model (EDM) and persistency format for Linear Collider physics and detector simulations. It was developed as a joint effort between SLAC and DESY and has been adopted by all of the detector concepts for both ILC and CLIC. Many of the subdetector R&D groups (e.g. CALICE and LCTPC) have also adopted LCIO for both their simulation needs and for testbeam data. Major R&D Efforts: The software toolkit consists of an Application Programming Interface (API) as well as reference implementations in Java and C++ and a binding to python. This, plus its deliberately simple design and well-documented EDM, has allowed the LC community to mix-and-match its software applications. Events simulated in C++ can be reconstructed in Java and analysed in python, providing enormous flexibility to the end user, who can concentrate on analyses and not be hampered by programming language limitations.

6.1.3 Engineering Challenges

The implementation of a complete EDM for all HEP applications is very difficult, if not impossible. LCIO has succeeded by reducing the problem to its simplest solution, but providing end users flexibility to adapt to their specific needs. Custom classes can be implemented using extensions to existing classes or using generic objects and relations between collections of data. The LCIO development team has also added functionality as new classes have been requested by users. Maintaining strict control over the structure of the LCIO EDM and persistency has ensured that any LCIO file can be opened and interpreted without having access to the code which created it.

6.1.4 Future Plans

Continued development of LCIO will be driven by user demand and developer's resources.

6.1.5 Applications Outside of Linear Colliders

The Heavy Photon Search experiment at Thomas Jefferson National Laboratory has adopted LCIO as its event data model and data persistency format. Physics and detector studies for CLIC and the Muon Collider have also used LCIO. The authors of the Whizard [125] event generator have expressed interest in using LCIO as their binary persistency format for Monte Carlo events. This could lead to its integration into other experiments. Because of its simple and well-documented persistency format LCIO is a perfect candidate for HEP data archiving applications.

6.2 LCSim

6.2.1 Collaborating Institutions

The core software has been developed at SLAC. A number of packages were contributed by university and other national lab groups when such efforts were supported by DOE.

6.2.2 Introduction

6.2.3 Recent Milestones

Simulation of physics processes and detector response is crucial to the design of new HEP experiments such as those proposed for the ILC. There are stringent requirements on the design of tools for detector R&D which differentiate them from typical experiment-specific simulation and reconstruction code. They must:

- allow easy reconfiguration to support different detector geometries and technologies,
- make it easy to develop, implement and compare new reconstruction algorithms,
- be very easy for users to set up and quickly become productive with,
- work on a wide variety of operating systems and computing platforms,
- be easy to develop and support using a fraction of the manpower that would be available to an established experimental collaboration.

The lcsim physics and detector response simulation and event reconstruction toolkit was developed at SLAC to provide a flexible and performant suite of software programs to allow fast and efficient studies of multiple detector designs for the ILC. The primary goal of the group has been to develop computing infrastructure to allow physicists from universities and other labs to quickly and easily conduct physics analyses and contribute to detector R&D. These tools include the Geant4-based detector response simulation program (slic), and the Java-based reconstruction and analysis tools (org.lcsim) [126].

6.2.4 Engineering Challenges

The lcsim software pioneered the use of runtime-defined detector geometries. Although LCIO [124] provided a common event data model for all ILC groups, the community was never able to agree upon a common geometry system for both simulation and reconstruction. DD4hep [127] is an effort within the AIDA Common Software Tools project to provide such functionality. Although it adopted many lcsim

concepts, the implementation of the software has taken its own course. The largest challenge to the lcsim effort at the moment (beyond lack of funding) is to maintain some connection to the geometry definition functionality promised by DD4hep.

6.2.5 Future Plans

The core functionality is being kept current by upgrading to the latest versions of Geant4, etc. Due to lack of funding, the project is currently primarily responding to user requests for additional functionality.

6.2.6 Applications Outside of Linear Colliders

The flexibility and power of this simulation package make it not only useful for the application domain for which it was developed (viz. HEP collider detector physics), but also for other physics experiments, and could very easily be applied to other disciplines, e.g. biomedical or aerospace, to efficiently use the full power of the Geant4 toolkit to simulate the interaction of particles with fields and matter. The Heavy Photon Search experiment at Thomas Jefferson National Laboratory has adopted slic as its detector response simulation package and the org.lcsim toolkit for its event reconstruction needs. Physics and detector studies for CLIC and the Muon Collider have also used both slic and the org.lcsim software. The software could be easily used for physics and detector studies at detectors at future circular colliders.

6.3 PandoraPFA

6.3.1 Collaborating Institutions

Development of the Pandora framework and algorithms has been based exclusively in Cambridge, but detector optimisation studies have involved close collaboration with other institutes. ECAL and analogue HCAL studies have involved DESY, Shinsu University (Japan), and CERN. Upcoming (semi-)digital HCAL studies will involve the University of Lyon (France).

6.3.2 Introduction

6.3.3 Recent Milestones

The PandoraPFA software package [128, 129] has been developed entirely in Cambridge. It consists of a robust and efficient C++ software development kit (SDK) and libraries of reusable pattern-recognition algorithms that exploit functionality provided by the SDK. Algorithms have been developed to provide a particle flow reconstruction of events in fine-granularity detectors, such as those proposed for use at the ILC or CLIC. The reconstruction uses over 60 algorithms in order to carefully trace the paths of visible particles through the detector. The output is a complete list of the particles in an event, each with a reconstructed four-momentum and an identified particle-type. The algorithms represent the state-of-the-art in particle flow calorimetry at a Linear Collider. The Pandora Linear Collider algorithms have recently been used for extensive detector optimisation studies, assessing the physics performance of the ILD_o1_v06 detector model with different configurations of the electromagnetic and hadronic calorimeters. A selection of the key plots is shown overleaf. A summary document is under construction and will be submitted for publication.

6.3.4 Engineering Challenges

The implementation of large numbers of pattern-recognition algorithms in C++ can be extremely difficult. Algorithms must work as intended, be easy to maintain/extend and have tight control of memory management. The Pandora SDK addresses these issues directly: it provides a sophisticated Event Data Model and performs all event memory- management. Access to event objects and modification of these objects can only occur via algorithms requesting services provided by the Pandora SDK. A key remaining challenge is to ensure algorithms are efficient and scale kindly with the number of input objects in an event. This is a matter for the algorithm author, rather than the framework, but the Pandora SDK provides a number of constructs to help address performance. These include KD-trees, which provide $\log(n)$ look-up of e.g. hits within a search-volume around a specified space-point. There is a cost associated with constructing KD-trees, but the reduction in e.g. hit-hit permutations can be enormous.

6.3.5 Future Plans

Continued development of Pandora SDK and pattern-recognition algorithms, plus provision of support to users of Pandora. On-going Linear Collider work (including work performed by new PhD students in Cambridge) includes improvement of π^0 reconstruction and efforts to further improve the ability to identify and separate neutral hadrons from nearby charged hadrons. Detector optimisation studies will continue and will include full examination of performance of Pandora algorithms with digital and semi-digital HCAL detector models.

6.3.6 Applications Outside of Linear Colliders

The Pandora SDK has been designed to aid development of pattern-recognition algorithms in generic fine-granularity detectors. As such, its use is not limited to the ILC. Pandora algorithms now provide a successful particle flow reconstruction in an upgrade model of the CMS detector, even in dense pile-up conditions. Algorithms have also been developed for reconstruction of cosmic ray and neutrino-induced events in liquid argon time projection chambers, having significant impact in the neutrino-physics community.

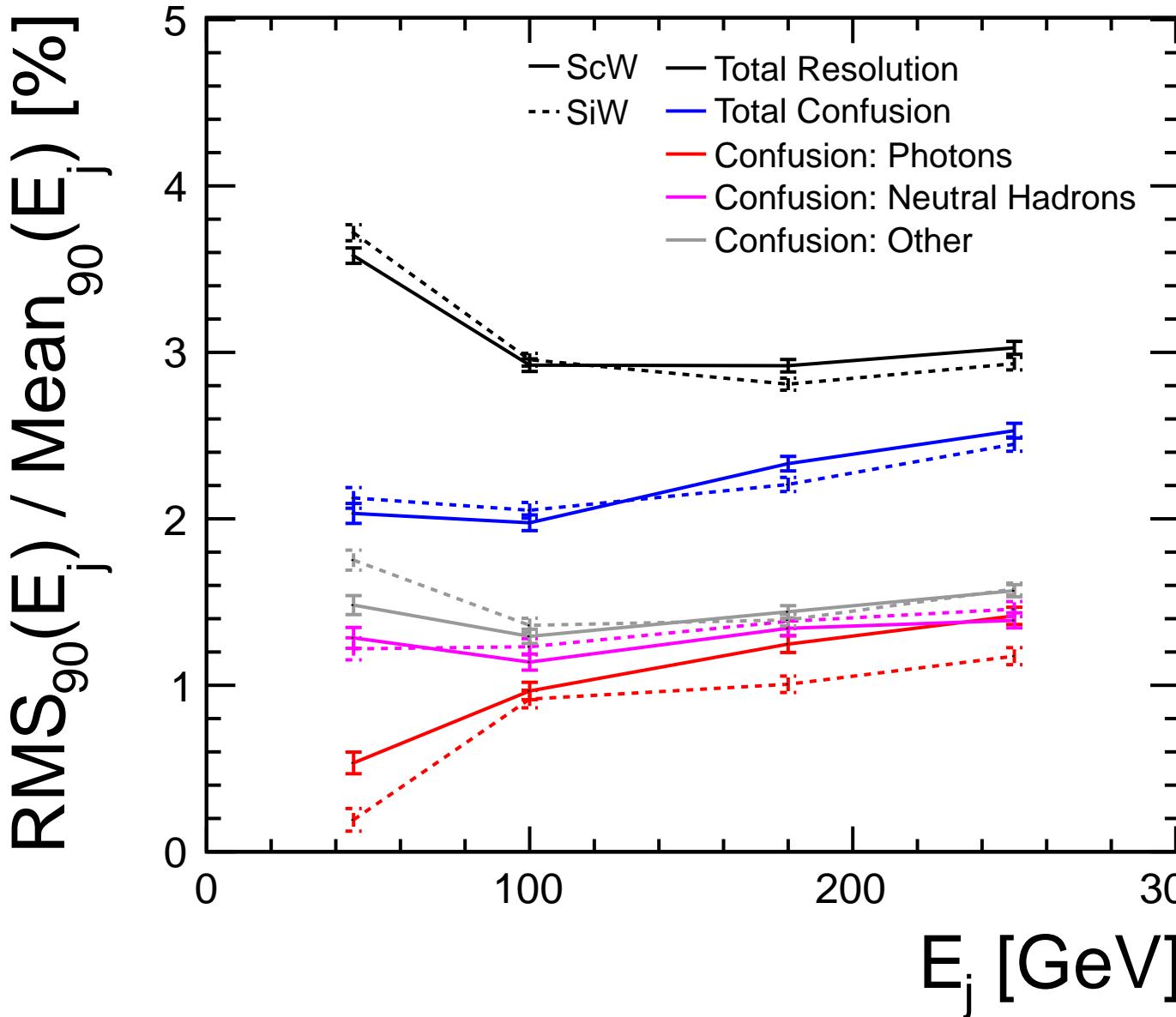


Figure 6.1: Jet energy resolution as a function of jet energy, including a breakdown of the resolution into contributing “confusion” terms. Illustrates performance of Pandora algorithms for ILD_o1_v06 with Silicon (Si) or Scintillator (Sc) as ECAL active material.

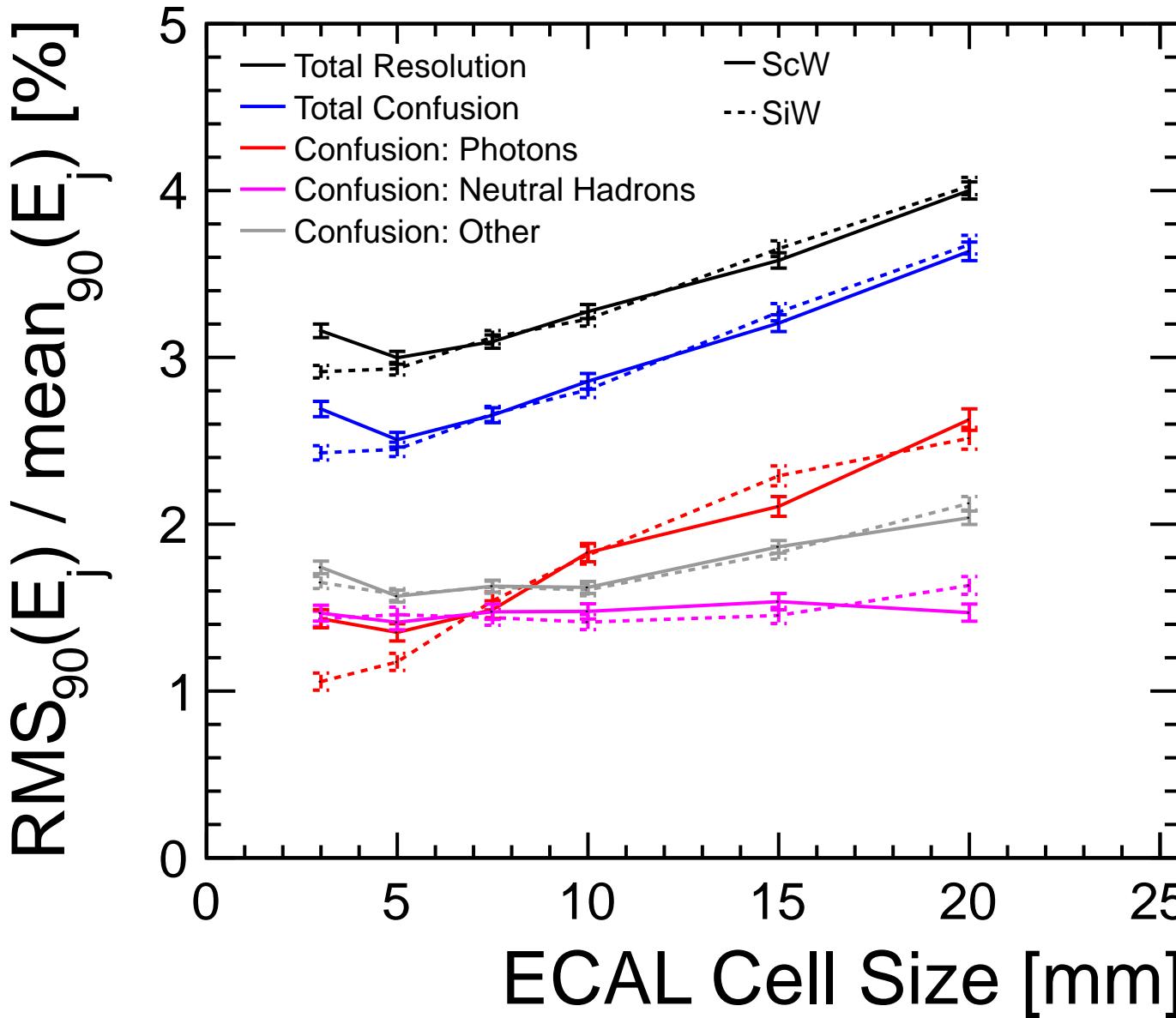


Figure 6.2: Jet energy resolution as a function of the ECAL cell size, for 250 GeV jets in ILD_o1_v06. As expected, the photon confusion term (ability to separate photons from nearby hadrons) drives performance changes.

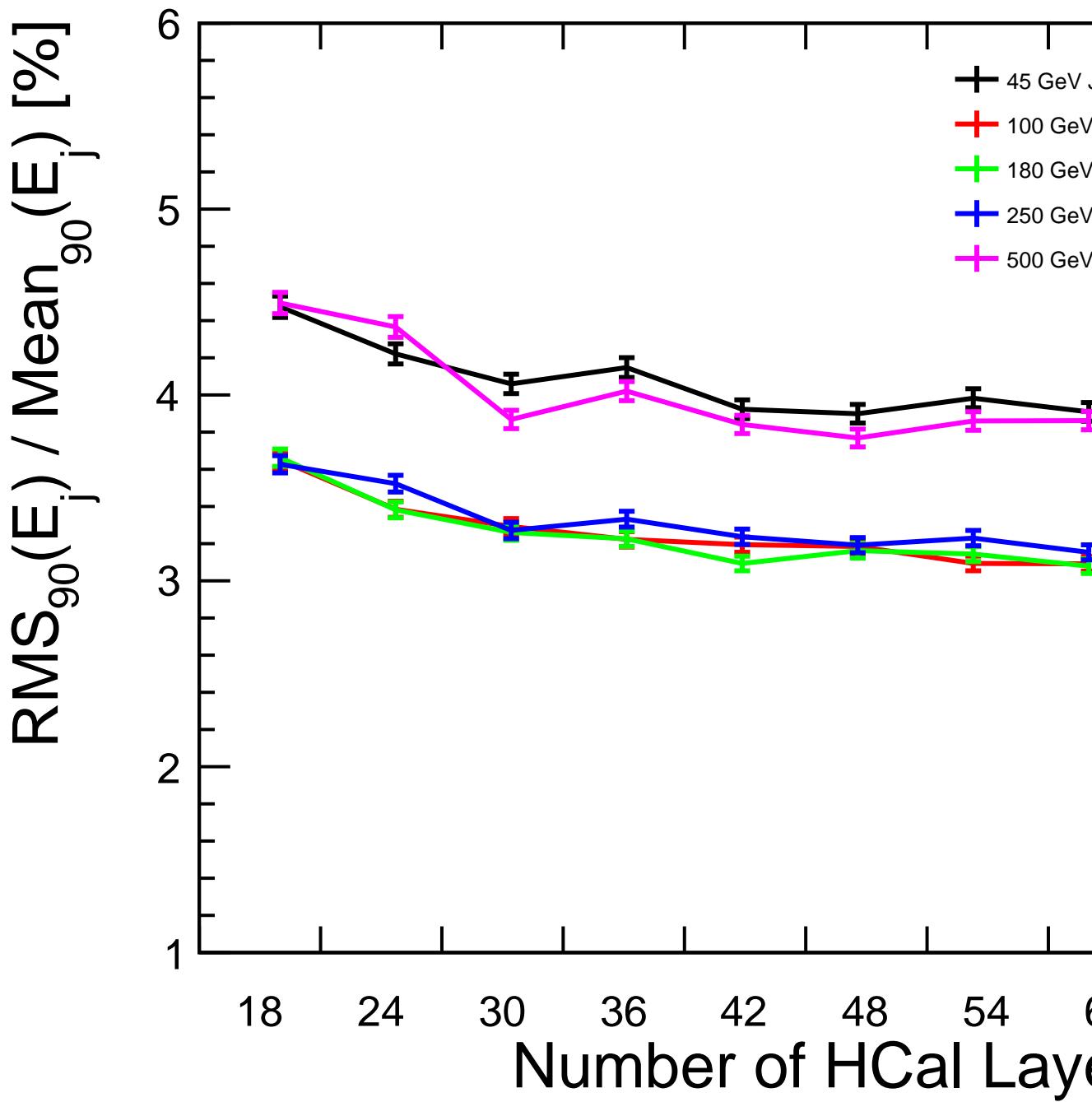


Figure 6.3: Jet energy resolution as a function of the number of layers in the HCAL, for a range of different energy jets in ILD_o1_v06.

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
LCIO				
LCSim				

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