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Vertex Detector R&D

1.1 Motviation and Constraints for Vertex Detectors at Linear Colliders

1.2 3D Pixel Development

1.2.1 Introduction

This R&D area covers sensors and electronics integrated utilizing 3-dimensional electronics technology. This technology is distinct from 3D sensors and builds on efforts in the electronics industry to stack multiple layers of electronics to form dense assemblies of complex devices. It is important for Particle Physics in that it allows very fine pitch (4 µm) integration of sensors with multiple layers of electronics, allows interconnection to both the top and bottom of devices, and provides techniques for low mass, thinned devices. The interconnection of top and bottom means that sensors can be bonded to complex electronics with no wasted area for interconnect and optimal delivery of power and ground.

1.2.2 Recent Milestones

We have completed our multi-year effort to demonstrate commercial 3D technology. This consists of two tiers of 0.13 µm CMOS interconnected with Direct Oxide Bonding (DBI) technology and access using Through-Silicon-Vias (TSV). The DBI bonds are at 4 µm pitch. Fermilab sponsored the first 3D multi-project run for Particle Physics. The wafers were delivered last summer. Fermilab had three chips on the run: VICTR – a CMS track trigger chip, VIPIC – an X-ray imaging chip, and VIP – an ILC vertex chip. Tests of the VIPIC and VICTR have shown working devices. Tests for the VIP chip were delayed due to lack of funding and personnel. We have recently restarted this work and initial tests are promising with the readout token successfully passed through the VIP.

In addition to the development of the 3D chips we have also explored the use of DBI to connect the 3D electronics with sensors. Brookhaven Laboratory fabricated a sensor wafer with regions that mate to the VIP, VIPIC and VICTR chips. The chips are ground to expose the top TSVs and contacts are deposited. The assembly is then attached to a handle wafer and the TSVs which project from the other side are exposed. Wafers are then process for DBI bonding and individual die from the 3D wafer are bonded to the sensor wafer. Finally the top "handle" silicon is ground and etched to reveal the previously formed contacts. The

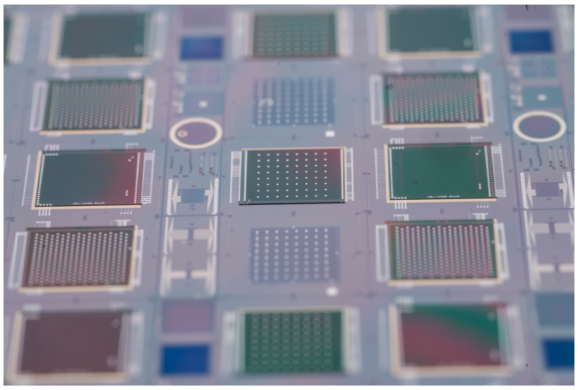

Figure 1.1: 3D chips placed on BNL sensor wafers. VIP is middle left and right

total thickness of the readout at the end of this process is about 25 µm (Figure 1.1). These wafers were received at the end of March 2014 and are being tested. Due to the fact that contacts to a 3D assembly can be made to the body of the die, rather than its edge, no space needs to be reserved for wire bond contacts at the edge. This raises the possibility of fabricating large, complex pixel detector arrays of 4-side butted devices using sensors with active edges. We are in the process of demonstrating this technology utilizing active edge sensors fabricated at VTT and using wafer-to-wafer bonding to a 3D readout wafer. The active edge wafers are based on a silicon-on-insulator stack and thus can be fabricated with essentially arbitrarily thin sensors, in this case 200 µm. Sensor and dummy readout wafers have been fabricated and a test wafer is being etched at SLAC. We expect to have DBI bonded assemblies this summer.

1.2.3 Engineering Challenges

Major engineering challenges include:

- Development of widely commercially available 3D technologies. Based partly on our development the silicon brokers CMP, CMC, and MOSIS now include 3D multi-project runs as part of their standard offerings.
- Development of high yield 3D bonded chip-to-wafer devices. This is the subject of our active edge project.
- This development shares with other vertexing technologies the problems of low mass mechanical support, power delivery, and cooling. An SOI-based device can be made thin without special effort. Such thinned device will need low mass backing hybrid circuitry, presumably flex on carbon fiber or a similar technology

1.2.4 Future Plans

- Complete the 3D active edge project
- Apply our concepts to x-ray imaging devices
- ILC developments would await renewed funding in the US.

1.2.5 Applications outside of Linear Colliders

As stated above the technology is already being developed for CMS and x-ray imaging applications. The large area sensor concept is applicable for a variety of focal plane array concepts.

1. Grzegorz W. Deptuch et al. "Results of Tests of Three-Dimensionally Integrated Chips Bonded to Sensors". In: *IEEE Trans.Nucl.Sci.* (2013)

2. R. Yarema, G. Deptuch, and R. Lipton. "Recent Results for 3D Pixel Integrated Circuits using Copper-Copper and Oxide-Oxide Bonding". In: *Proceedings of Science* (2014)

3. P. Maj et al. "Tests of the First Three-Dimensionally Integrated Chip for Photon Science". In: *PoS* Vertex2012 (2013), p. 027

4. G. Deptuch et al. "3D Technologies for Large Area Trackers". In: *ArXiv e-prints* (July 2013). arXiv: 1307.4301 [physics.ins-det]

5. R Lipton et al. "Combining the two 3Ds". In: *Journal of Instrumentation* 7.12 (2012), p. C12010

6. R Yarema et al. "Vertically integrated circuit development at Fermilab for detectors". In: *Journal of Instrumentation* 8.01 (2013), p. C01052

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
ChronoPix	University of Oregon Yale University Sarnoff Corporation	ChronoPix is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps per pixel	April 2014: Device tests of prototype 2 inform the design of prototype 3 to be submitted to foundry	Improve S/N to at least 20 Further reduce pixel size from 25 µm to eventually 15 µm. Requires feature size less than 65 nm Reduce inter-pixel and digital-to-analog circuit cross talk and parasitic feedback
CMOS MAPS	IPHC Strasbourg DESY, Hamburg University of Bristol University of Frankfurt	The CMOS pixel sensor uses as a sensitive volume the 10 – 20 µm thin high-resistivity epitaxial Si-layer deposited on low resistivity substrate of commercial CMOS processed chips. The generated charge is kept in a thin epi-layer atop the low resistivity silicon bulk by potential wells that develop at the boundary and reaches an n-well collection diode by thermal diffusion.	2016 : production of CPS for the ALICE-ITS upgrade 2018/19 : production of CPS for the micro-vertex detector of the CBM experiment at FAIR/GSI 2018/19 : validation of light double-sided ladder concept combining highly granular sensors on one side with timestamping sensors on the other side < 2020 : validation of power pulsing of double-sdied ladders inside a high magnetic field 2022/23 : finalisation of the R&D on various CPS adapted to the different layers of a very high performance vertex detector at the ILC	Until 2018-2019: Development and production of CPS for the ALICE-ITS and CBM-MVD Development of various CPS optimised for the different layers of a vertex detector at the ILC, with emphasis on bunch tagging Development of low material double-sided ladders
DEPFET	University of Barcelona, Spain University of Bonn, Germany Heidelberg University, Germany Giessen University, Germany University of Göttingen KIT Karlsruhe, Germany IFJ PAN, Krakow, Poland MPI Munich MPG HLL Munich, Germany Charles University, Prague, Czech Republic IFIC, CSIC-UVEG, Valencia, Spain DESY, Hamburg, Germany IFCA, CSIC-UC, Santander, Spain	The DEPFET technology implements a single active element within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted, detector-grade bulk silicon. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate.	2014: Full-scale 75 µm thin Belle II ladder in beam test at DESY	Development of die-attach technology Full-scale test of all ASICs on ladder Integration of read-out and steering ASICs on pixel sensor using flip-chip technique and microscopic solder ball bump-bonding Production of Belle II vertex detector modules Tests of the last version of the DHP chips Engineering design for all-silicon module with petal geometry required for ILC Detailed characterization of device response Design of ancillary ASICs, taking full responsibility for future design cycles of the FE read-out chip, called Drain Current Digitizer
FPCCD	KEK Shinshu University Tohoku University JAXA, Japan Aerospace Exploration Agency	Fine Pixel CCD sensors have pixel sizes of 5 µm and a fully depleted epitaxial layer with a thickness of 15 µm	Fabrication of real size (12.3 mm × 62.4 mm) sensors with 50 µm total thickness Neutron irradiation of a small (6 mm × 6 mm) FPCCD sensor Construction of a prototype cooling system and demonstration of cooling between −40°C and +15°C	Characterization of FPCCD sensors including beam tests and radiation damage studies Development of FPCCD sensors with a pixel size of 5 µm Construction of prototype ladders for the inner layers of a vertex detector Development of readout electronics downstream of ASICs Development of larger FPCCD sensors and prototype ladders for outer layers Development of readout electronics with a small footprint Construction of a real size engineering prototype and cooling test
3D Pixels	Brown University Cornell University Fermilab Northern Illinois University SLAC University of Illinois Chicago	3D technology allows very fine pitch (4 µm) integration of sensors with multiple layers of electronics, allows interconnection oto both the top and bottom of devices, and provides techniques for low mass, thinned devices.	Completed multi-year effort to demonstrate commercial 3D technology, consisting of 0.13 CMOS interconnected with Direct Oxide bonding technology and access using TSV. Received readout wafers with thickness of 25 µm, processed with TSV and DBI to connect to 3D electronics Currently working on active edge demonstrator devices	Complete the 3D active edge project Apply concepts to x-ray imaging devices Re-start ILC developments pending renewed funding
SOI	KEK University of Tsukuba Tohoku University Osaka University	In the Silicon-On-Insulator (SOI) technology the sensing and processing functionalities are separated in different layers; the sensing is provided by a high-resistive substrate connected through an insulating layer with the processing layer.		Sep 2014: Complete architecture study for the ILC pixel detector Mar 2015: Design and fabrication of first test chip for the ILC Dec 2015: Beam test of the chip
CLICPix	CERN Spanish Network for Future Linear Colliders University of Liverpool Institute of Space Science, Bucharest University of Bristol	A detector concept is based on hybrid planar pixel-detector technology. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology. The target thickness for both the sensor and readout layers is only 50 mm each. Slim-edge sensor designs are under study and TSV technology is foreseen for vertical interconnection.		Development of hybrid pixel readout ASIC with 25 µm pitch, analog readout, time stamping and power pulsing functionality, implemented in 65 nm CMOS technology Development of ultra-thin (50 µm) planar pixel sensors, as well as active sensors with capacitive coupling Low-mass fine-pitch interconnects between sensor and ASIC Through-silicon-via technology for powering, configuration and readout of the ASIC Low-mass powering infrastructure, including power-pulsing with local energy storage Low-mass carbon fiber supports Detector cooling based on forced air flow Concepts for mechanical integration and detector assembly Detector layout optimization studies

Bibliography

[1] Grzegorz W. Deptuch et al. “Results of Tests of Three-Dimensionally Integrated Chips Bonded to Sensors”. In: *IEEE Trans.Nucl.Sci.* (2013).

[2] R. Yarema, G. Deptuch, and R. Lipton. “Recent Results for 3D Pixel Integrated Circuits using Copper-Copper and Oxide-Oxide Bonding”. In: *Proceedings of Science* (2014).

[3] P. Maj et al. “Tests of the First Three-Dimensionally Integrated Chip for Photon Science”. In: *PoS* Vertex2012 (2013), p. 027.

[4] G. Deptuch et al. “3D Technologies for Large Area Trackers”. In: *ArXiv e-prints* (July 2013). arXiv: 1307.4301 [physics.ins-det].

[5] R Lipton et al. “Combining the two 3Ds”. In: *Journal of Instrumentation* 7.12 (2012), p. C12010.

[6] R Yarema et al. “Vertically integrated circuit development at Fermilab for detectors”. In: *Journal of Instrumentation* 8.01 (2013), p. C01052.