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Chapter 1

Vertex Detector R&D

1.1 ChronoPixel

1.1.1 Introduction

The ChronoPixel is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps of pixel hits by charge particles in a nominal ILC bunch train. This information is read out in the time interval between bunch trains. The ChronoPixel option for ILC vertex detector was described in the ILC DBD [1]. By the time of the DBD, 2 prototypes were built and tested, and summary of test results were also presented in the DBD. They are listed below:

- We have proven that we can record time stamps in every pixel with time resolution better than 300 ns (we have tested it down to 150 ns). reference
- We have tested sparse readout, allowing to read only pixels with hits, thus reducing readout time to the level allowing readout of all pixels in the sensor in the intervals between bunch crossings.
- We have tested pulsed power for the analog part of the pixels and have proven that turning power ON in about 100 μ s before bunch train and turning it off between bunch trains does not create any problems for threshold setting accuracy in the comparators. reference
- We have tested the idea of building all in-pixel electronics only from NMOS transistors, thus eliminating the need for special process (deep p-well) to protect signal charge from parasitic collection by in-pixel transistors. We have proven that all NMOS electronics can be built in this way, and that this does not significantly increase the power consumption compared to CMOS electronics. reference
- We have tested compensation of comparator offsets using analog calibration, when the value of the offset is stored as a voltage on the capacitor in each pixel. This has an advantage over digital calibration (where the offset value is stored as code in the special register) in that there are no discrete levels, and accuracy

of such a calibration scheme is not affected by the size of the register or the spread of the initial offsets.

1.1.2 Recent Milestones

- Test of prototype 2 revealed some problems. Possible solutions for these problems were discussed with Sarnoff engineers.
- A new contract with Sarnoff for the design of prototype 3 was signed in August 2013.
- The submission of prototype 3 to the foundry for manufacturing is expected by the end of April 2014.

The most recent report on chronopixel status was presented by N. Sinev at LCWS13 on November 2013 at Tokyo

1.1.3 Engineering Challenges

-
- Achieving low capacitance of the sensor diode in a 65 nm and smaller feature size process. Following standard design rules for such a process led to much higher diode capacitance than hoped for. The third prototype attempts to solve this problem using non-standard “native diode” from the design library. This needs to be checked once the prototype is delivered.
 - If acceptable levels of the sensor diode capacitance can be achieved, the signal/noise ratio will improve. However, a lower value of the capacitance will make the pixels more sensitive to cross-talks through capacitive coupling. Reducing this coupling can be a challenge.
 - Transition from small prototypes (few mm²) to ILC detector size (10 cm²) may meet additional problems. One of them will be the effect of Lorentz forces on the power supply buses, especially in the case of power pulsing. Power pulsing is the only way to achieve acceptable power dissipation in the vertex detector. However, it will generate varying Lorentz forces, acting on power supply lines. This may produce vibrations, which are unacceptable for the required spatial resolution of the detector.

Integration
Challenges
missing

1.1.4 Main directions of the R&D for the next 5 years

- Achieve signal-to-noise ratio required for close to 100% signal registration efficiency. So far we got a signal-to-noise ratio of around 10 in prototype 2, and we would like at least 20. We know a few ways to improve it - increasing epitaxial layer thickness, increasing epitaxial layer resistivity, or reducing sensor capacitance. The most attractive would be reducing sensor capacitance, as it does not require special processes, however there are some problems to be solved with this approach.

- Achieve the required pixel size (prototype 3 will have 25 μm pixels, we would eventually like 15 μm). It may require going to a technology with feature size less than 65 nm. There seems to be no problems in that, but both - good signal-to-noise ratio and pixel size requirements may be challenging.
- Achieve acceptable level of inter-pixel and digital to analog circuit cross talks and parasitic feed backs.
- Depending on available funding, try to build a complete sensor with a large enough area and full feature readout.

1.1.5 Applications Outside of Linear Colliders

With some modifications (for example, adding time-time converter) Chronopixel architecture can be applied for any experiment requiring time stamping of individual hits - it may be HL-LHC, CLIC and so on.

1.2 CMOS

1.2.1 Collaborating Institutions

1.2.2 Introduction

1.2.3 Recent Milestones

1.2.4 Engineering Challenges

1.2.5 Future Plans

1.2.6 Applications Outside of Linear Colliders

1.3 DEPFET Pixel Sensors

1.3.1 The DEPFET Collaboration

The [DEPFET collaboration](#) consists of nearly 100 members from 13 institutes. It currently takes responsibility for the following work packages

Thin self-supporting “all-silicon” sensors The sensors are produced in-house, and the mechanical properties of thin ladders in a realistic environment are studied in detail using a Belle II mock-up. LC-specific studies are also performed within this collaboration

Cooling The DEPFET cooling concept for Belle II relies on two-phase CO₂ cooling for the end-of-ladder. The sensor is cooled moreover with a forced flow of cold gas. The CO₂ cooling plant is developed by KEK, while the design for the cooling block/support structure is performed within the collaboration. A novel cooling strategy for future applications based on mico-channels in the

sensors is being evaluated in the collaboration. Solutions for monitoring of environmental parameters are being developed.

Read-out and steering ASIC production The operation of a DEPFET detector requires ancillary electronics in the form of a read-out ASIC (the Drain Current Digitizer), a steering ASIC (SWITCHER) and on-detector ASICs for digital data processing (DHP). These ASICs are developed within the collaboration.

Data Acquisition and Trigger The development of off-detector electronics to process the data from the Belle II vertex detector.

Characterization of prototypes, laboratory and beam tests This work package has contributions from nearly all institutes involved in the DEPFET collaboration.

Currently, the construction of the Belle II vertex detector is the main focus of the collaboration. The requirements of the Belle II vertex detector are similar to those of the ILC, and more stringent in some aspects. The Belle II construction project therefore has considerable synergy with developments for a future linear collider. The LC-specific effort is focused on the development of small-pixel devices and the design of a forward vertex detector. We envisage that after the installation of the Belle II detector (2016) the balance between both projects is restored. studied.

1.3.2 Introduction

The DEPFET technology implements a single active element within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted high-resistivity silicon wafer. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate.

The following is too detailed for the Introduction

The Front-end Electronics (FE), i.e., readout electronics, is currently organized by a set of several ASICs [2]: The SWITCHER, Drain Current Digitizer (DCD) [3, 4] and Data Handling Processor (DHP) [5] chips. The SWITCHER control chips select segments of the sensor array for read-out. A separate driver supplies the clear pulse of up to 20 V to remove the collected signal from the internal gate after read-out. Several designs of the SWITCHER versions optimized for Belle II requirements have been produced and tested successfully in two different CMOS technologies (0.35 μm and 0.18 μm). The drain current signals from 256 columns of pixels are processed and digitized by the DCD. The analog input stage keeps the column line potential constant (necessary to achieve fast readout), compensates for variations in the DEPFET pedestal currents, and amplifies and shapes the signal. The last DCD version is implemented in UMC 0.18um CMOS technology using special radiation hard design techniques (e.g. enclosed NMOS gates) in the analog part. This DCD chip is optimized specifically for Belle II requirements. The derandomized raw data from the DCD are

Table 1.1: Comparison of ILC and Belle II requirements of a vertex detector

	ILC	Belle II
occupancy	0.13 hits/ $\mu\text{m}^2/\text{s}$	0.4 hits/ $\mu\text{m}^2/\text{s}$
radiation	< 100 krad/yr $10^{11} \text{ MeVn}_{\text{eq}}/\text{yr}$	> 1 Mrad/yr $2 \times 10^{12} \text{ MeVn}_{\text{eq}}/\text{yr}$
duty cycle	1/200	1
frame time	25 – 100 μs	20 μs
momentum range	100 keV - 500 GeV	$\sim 1 \text{ GeV}$
angular acceptance	6°- 174°	17°- 150°
spatial resolution	excellent: 3 – 5 μm	moderate
pixel size	$20 \times 20 \mu\text{m}$	$50 \times 75 \mu\text{m}$
material budget	0.15% X_0/layer	0.21% X_0/layer

transmitted to the DHP using fast parallel 8-bit digital outputs. This third ASIC, located on the end of ladder area immediately behind the DCD, performs data processing (pedestal subtraction, common code correction), compression (zero suppression), buffering and fast serialization. It furthermore controls the other read-out ASICs.

1.3.3 Recent Milestones

The concept of a DEPFET active pixel detector for vertex detection at collider experiments was initiated in the linear collider community (for TESLA). The operation principle was extensively proven on small-scale prototypes. A recent reassessment of the DEPFET potential for a linear collider at the energy frontier is found in [6]. A full-scale, 75 μm thin Belle II ladder was successfully submitted to a test in a beam of charged at DESY in January 2014.

The first full-scale DHP prototype was implemented in IBM 90 nm CMOS technology. As this technology was discontinued, more recent designs were submitted in the TSMC 65 nm CMOS process. DHPT v.1.0 comprises temperature independent current references, 11 bias 8-bit DACs with current output, an integrated temperature measuring system and JTAG control. This design has been successfully tested during early 2014 .

Reference

Reference

particles? pions?

Reference

1.3.4 Engineering Challenges

Vertex detector ladders with a thickness of several tens of microns and a spatial resolution of well below 10 μm require very robust mechanical properties. The power generated by the sensors and ASICs must be removed with the smallest impact on the detector material. Measurements on thin ladders under a realistic load, including pulsed powering according to the ILC beam structure, prove the excellent mechanical properties of the all-silicon ladder.

Reference

1.3.5 Future Plans

Currently, the construction of the Belle II vertex detector (to be installed by 2016) implies a large effort of R&D, including:

- Develop the die-attach technology in a controlled atmosphere required for the mounting of passive components on the DEPFET active pixel detector ladders. The first milestone is a fully integrated electrical prototype based on the EMCM.
- First tests that will determine if all the ASICs on the ladder are fully functional
- The integration of read-out and steering ASICs on the pixel sensor to be performed using a flip-chip technique and so-called bump-bonding, using microscopic solder balls.
- The production of the Belle II vertex detector modules, a joint effort of the DEPFET collaboration
- The test of the last version of the DHP chips

In the near future we hope to characterize the performance of ILC-design prototypes with pixels of $20 \times 20 \mu\text{m}^2$

- Perform an engineering design for a DEPFET all-silicon module with the required petal geometry
- A detailed characterization of the response of the device
- Design of the ancillary ASICs, taking full responsibility for future design cycles of the Front End read-out chip, the Drain Current Digitizer (DCD) that is relevant to the ILC and a Belle II upgrade. This chip converts the analog signal from the detector to digital and has a crucial impact on the detector performance.

In the longer term the DCD and DHP are envisaged to evolve into a single chip. Being large arrays of DEPFET pixels a promising technology for the vertex detector of the planned ILC, adaptation of the DCD and DHP chips must also be done.

In the near future we hope to characterize the performance of ILC design prototypes with pixels of $20 \times 20 \mu\text{m}^2$. Important experience is furthermore gained with the thermal and mechanical properties of ultra-thin ladders. Measurements on thin ladders under a realistic load, including pulsed powering according to the ILC beam structure, prove the excellent mechanical properties of the all-silicon ladder. A complete mock-up for the innermost disks is under construction.

1.3.6 Applications Outside of Linear Colliders

The concept of a DEPFET active pixel detector for vertex detection at collider experiments was initiated in the linear collider community (for TESLA). The election of DEPFET technology for the Belle II detector therefore represents an important spin-off of linear collider detector R&D. DEPFET detectors are furthermore used for X-ray imaging at the XFEL . Future space missions envisage the use of DEPFET sensors. Reference

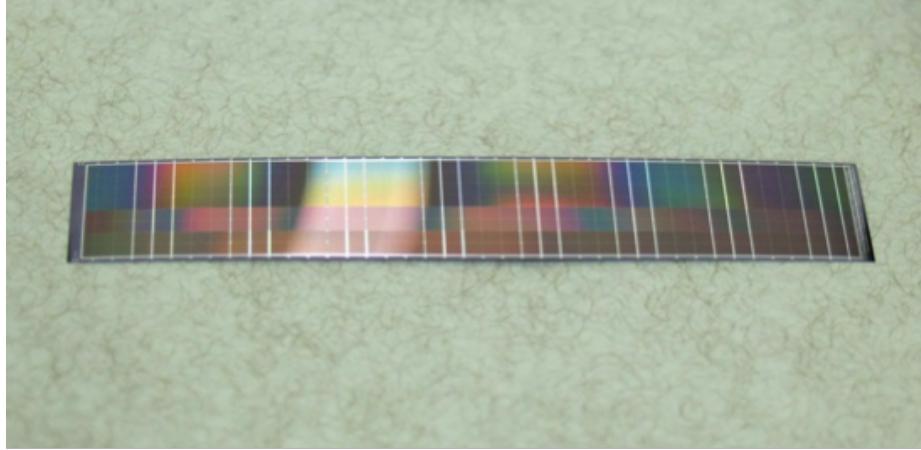


Figure 1.1: Real size FPCCD sensor thinned down to $50\text{ }\mu\text{m}$

1.4 FPCCD

1.4.1 Collaborating Institutions

1.4.2 Introduction

Fine pixel CCD (FPCCD) is one of the candidate sensor options for the vertex detector of the ILD detector at the ILC [7, 8, 9]. In the present design, FPCCD sensors for the innermost layer of the vertex detector have a pixel size of $5\text{ }\mu\text{m}$ and a fully depleted epitaxial layer with a thickness of $15\text{ }\mu\text{m}$. Because of the small size of the pixels, the occupancy is acceptably low even if the hits are accumulated for one nominal ILC bunch train (1 ms). The efforts of the FPCCD collaboration are currently focused on pixel characterization and development, while we also pursue developments to the cooling system, electronics downstream of ASICs and the reconstruction software [10].

1.4.3 Recent Milestones

R&D activity for the FPCCD vertex detector at present is mainly focused on FPCCD sensors and a detector cooling system using 2-phase CO_2 . One of the achievements of FPCCD sensors after DBD is the fabrication of real size ($12.3 \times 62.4\text{ mm}^2$) sensors with $50\text{ }\mu\text{m}$ total thickness. Figure 1.1 shows the real size prototype sensor. It has 8 readout nodes, and each channel has different pixel sizes of $12\text{ }\mu\text{m}$, $8\text{ }\mu\text{m}$, and $6\text{ }\mu\text{m}$. We have started a neutron damage test using small ($6\text{ mm} \times 6\text{ mm}$) FPCCD prototypes [11]. A prototype sensor was irradiated by a neutron beam of few tens of MeV at the CYRIC facility of Tohoku University. The detailed analysis on the irradiated sensor is still ongoing. In order to increase the radiation immunity of FPCCD sensors, particularly to reduce the transfer inefficiency due to radiation damage, the sensors should be cooled down to $-40\text{ }^\circ\text{C}$. We have started R&D on a two-phase CO_2 cooling system for this purpose. There are several examples of utilizing two-phase CO_2 cooling systems for

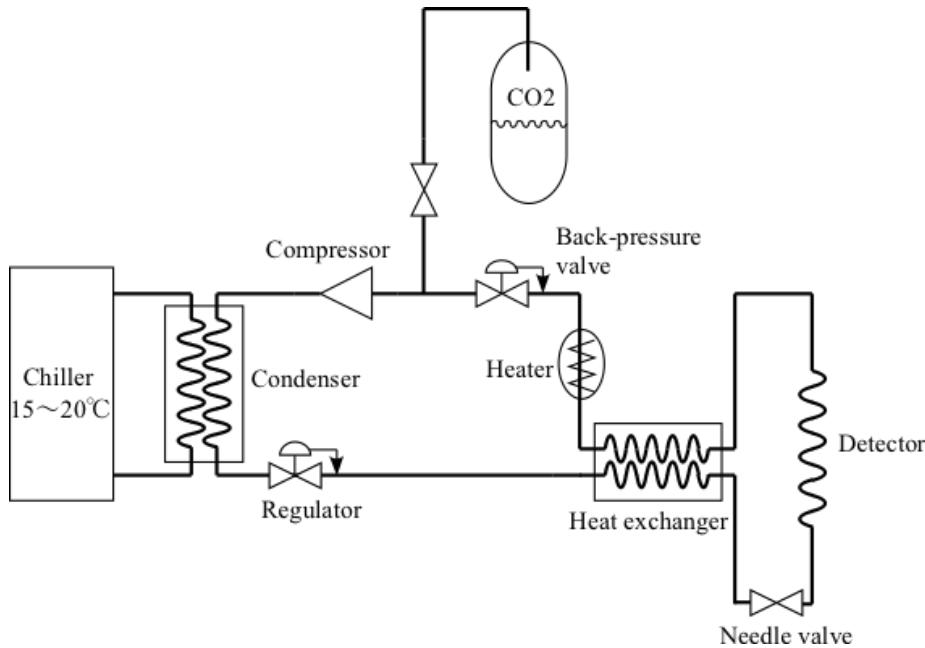


Figure 1.2: A simplified schematic diagram of the two-phase CO_2 cooling system

high energy physics experiments. For these cases, the CO_2 coolant is circulated using liquid pumps. This method is, however, not so efficient for very low temperature cooling of -40°C . Therefore, we adopted a CO_2 gas compressor for the circulation of CO_2 coolant. Figure 1.2 shows a simplified schematic diagram of the system. A prototype system has been constructed, and cooling between -40°C and $+15^\circ\text{C}$ has been successfully demonstrated using this system.

1.4.4 Engineering Challenges

In the present design of the ILD vertex detector, two sensor layers are mounted on both sides of a light-weight ladder of 2 mm thickness. Our goal of the material budget of this ladder is $0.3\% \text{ X}_0/\text{ladder} = 0.15\% \text{ X}_0/\text{layer}$. This goal would not be so easy to accomplish, and we need a lot of R&D effort. The ladders have to be cooled down to -40°C . We plan to achieve this cooling by heat conduction to the end-plate on which thin cooling tubes for 2-phase CO_2 are attached. The design of this structure is not trivial, and we need R&D including thermal simulation. There are challenges both with the mechanical structure and the electronics circuit for the ladder R&D. We have not started this effort yet.

1.4.5 Future Plans

We have been doing our R&D on the FPCCD vertex detector based on a Grant-in-aid for science research which expires at the end of FY2015. By that time, we plan to carry out the following R&D items:

- Characterization of FPCCD sensors including beam tests and radiation damage tests
- Development of FPCCD sensors with the pixel size of $5\text{ }\mu\text{m}$, which is our ultimate goal
- Construction of prototype ladders for inner layers
- Development of readout electronics downstream of ASICs

If new funding is secured in future, the following R&D items have to be done:

- Development of larger FPCCD sensors and prototype ladders for outer layers
- Development of readout electronics which can fit in the small space of real experiment
- Construction of a real size engineering prototype and its cooling test

1.4.6 Applications Outside of Linear Colliders

Because of the relatively slow readout speed, the application of FPCCD sensors to other high energy physics experiments would be limited. However, high spatial resolution of small pixel size must be applicable to measurements of X-ray imaging. Two-phase CO_2 cooling system can be applied to any other detectors which require efficient cooling between $-40\text{ }^\circ\text{C}$ and near room temperature. Our system, which uses a CO_2 gas compressor, has a great advantage for low temperature operation near $-40\text{ }^\circ\text{C}$ compared with systems using liquid pumps for circulation.

1.5 SOI

1.5.1 Introduction

1.5.2 Recent Milestones

At present, major issues in the SOI pixel development are “back-gate effect”, “hole trap under the transistors by radiation,” and “sensor-circuit cross talks” as shown in Figure 1.3. For these, we have been developing a double SOI technology. The developed double SOI wafer has an additional middle-SOI(Si) layer under the transistors. The conduction layer of the middle-SOI can solve all the three issues. We could successfully process the double-SOI wafer (Figure 1.4). Threshold shift by radiations is successfully recovered by applying compensating voltage to the middle SOI layer (Figure 1.5).

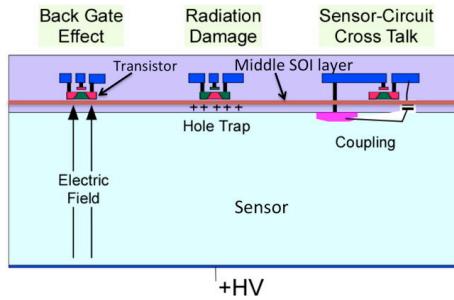


Figure 1.3: Major issues in the SOI pixel detector and introduction of a middle-SOI layer

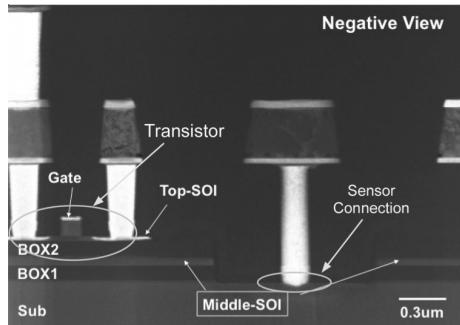


Figure 1.4: Cross section of the double SOI chip after processing

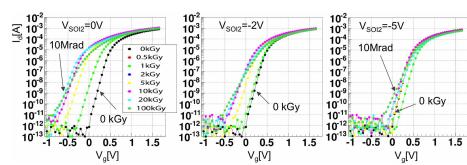


Figure 1.5: Threshold shift recovery by applying compensating voltage (V_{SOI2}) to the middle Si layer

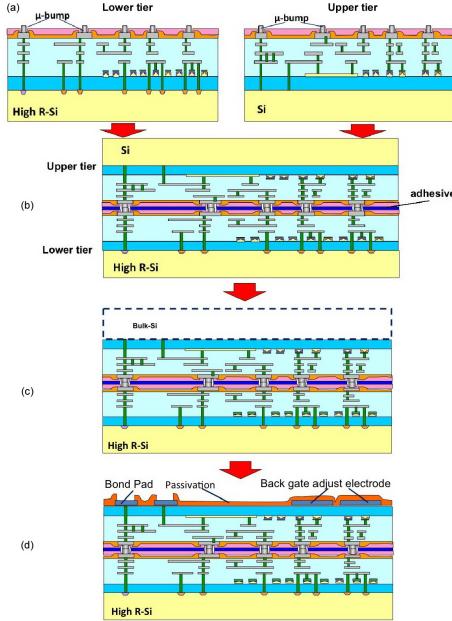


Figure 1.6: Micro-bump 3D integration process flow of the SOI pixel

1.5.3 Engineering Challenges

The impact parameter resolution for the ILC vertex detector is required to be a few μm . This means the pixel size must be less than about $20 \mu\text{m}^2$. On the other hand, each pixel must register arrival time of the hits during bunch train, which requires many transistors and capacitors to be located in each pixel. A solution to this is 3D vertical integration of the circuit layers. SOI technology is ideally suited for 3D integration, since the thinning is stopped at the buried oxide (BOX). We already tried 3D SOI pixel chip in collaboration with T-Micro Co. Ltd. The process flow of micro-bump 3D connection is shown in Figure 1.6. This process achieves a resistance of ($\sim 6 \Omega/\text{bump}$) between upper and lower tiers for 1,000 daisy chain (2,000 bumps) as shown in Figure 1.7. However, to achieve the density of digital circuitry necessary for ILC operations, 32 nm technology may be necessary for the upper tier in the ILC. This requires bonding of two different technology wafers. The 3D integration of different technology wafers (or chips) is still an engineering challenge.

1.5.4 Future Plans

Detector R&D plans for the coming years; We are planning following items for the coming year.

- Sep. 2014 : Complete architecture study for the ILC pixel detector.
- Mar. 2015 : Design and fabrication of first test chip for the ILC.

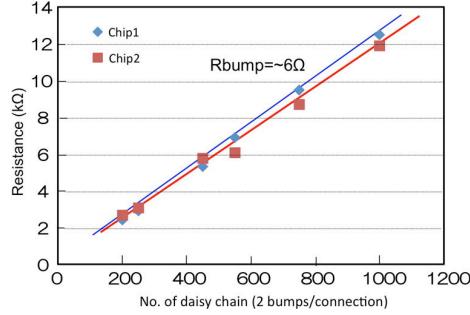


Figure 1.7: Resistance of micro-bump daisy chain between upper and lower tiers

- Dec. 2015 : Beam test of the test chip.

1.6 3D Pixel Development

1.6.1 Introduction

This R&D area covers sensors and electronics integrated utilizing 3-dimensional electronics technology. This technology is distinct from 3D sensors and builds on efforts in the electronics industry to stack multiple layers of electronics to form dense assemblies of complex devices. It is important for Particle Physics in that it allows very fine pitch ($4\text{ }\mu\text{m}$) integration of sensors with multiple layers of electronics, allows interconnection to both the top and bottom of devices, and provides techniques for low mass, thinned devices. The interconnection of top and bottom means that sensors can be bonded to complex electronics with no wasted area for interconnect and optimal delivery of power and ground.

1.6.2 Recent Milestones

We have completed our multi-year effort to demonstrate commercial 3D technology. This consists of two tiers of $0.13\text{ }\mu\text{m}$ CMOS interconnected with Direct Oxide Bonding (DBI) technology and access using Through-Silicon-Vias (TSV). The DBI bonds are at $4\text{ }\mu\text{m}$ pitch. Fermilab sponsored the first 3D multi-project run for Particle Physics. The wafers were delivered last summer. Fermilab had three chips on the run: VICTR – a CMS track trigger chip, VIPIC – an X-ray imaging chip, and VIP – an ILC vertex chip. Tests of the VIPIC and VICTR have shown working devices. Tests for the VIP chip were delayed due to lack of funding and personnel. We have recently restarted this work and initial tests are promising with the readout token successfully passed through the VIP.

In addition to the development of the 3D chips we have also explored the use of DBI to connect the 3D electronics with sensors. Brookhaven Laboratory fabricated a sensor wafer with regions that mate to the VIP, VIPIC and VICTR chips. The chips are ground to expose the top TSVs and contacts are deposited. The assembly is then

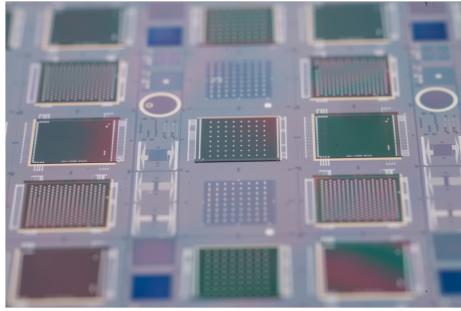


Figure 1.8: 3D chips placed on BNL sensor wafers. VIP is middle left and right

attached to a handle wafer and the TSVs which project from the other side are exposed. Wafers are then processed for DBI bonding and individual die from the 3D wafer are bonded to the sensor wafer. Finally the top “handle” silicon is ground and etched to reveal the previously formed contacts. The total thickness of the readout at the end of this process is about 25 μm (Figure 1.8). These wafers were received at the end of March 2014 and are being tested. Due to the fact that contacts to a 3D assembly can be made to the body of the die, rather than its edge, no space needs to be reserved for wire bond contacts at the edge. This raises the possibility of fabricating large, complex pixel detector arrays of 4-side butted devices using sensors with active edges. We are in the process of demonstrating this technology utilizing active edge sensors fabricated at VTT and using wafer-to-wafer bonding to a 3D readout wafer. The active edge wafers are based on a silicon-on-insulator stack and thus can be fabricated with essentially arbitrarily thin sensors, in this case 200 μm . Sensor and dummy readout wafers have been fabricated and a test wafer is being etched at SLAC. We expect to have DBI bonded assemblies this summer.

1.6.3 Engineering Challenges

Major engineering challenges include:

- Development of widely commercially available 3D technologies. Based partly on our development the silicon brokers CMP, CMC, and MOSIS now include 3D multi-project runs as part of their standard offerings.
- Development of high yield 3D bonded chip-to-wafer devices. This is the subject of our active edge project.
- This development shares with other vertexing technologies the problems of low mass mechanical support, power delivery, and cooling. An SOI-based device can be made thin without special effort. Such thinned device will need low mass backing hybrid circuitry, presumably flex on carbon fiber or a similar technology

1.6.4 Future Plans

- Complete the 3D active edge project
- Apply our concepts to x-ray imaging devices
- ILC developments would await renewed funding in the US.

1.6.5 Applications outside of Linear Colliders

As stated above the technology is already being developed for CMS and x-ray imaging applications. The large area sensor concept is applicable for a variety of focal plane array concepts.

1. Grzegorz W. Deptuch et al. “Results of Tests of Three-Dimensionally Integrated Chips Bonded to Sensors”. In: *IEEE Trans.Nucl.Sci.* (2013)
2. R. Yarema, G. Deptuch, and R. Lipton. “Recent Results for 3D Pixel Integrated Circuits using Copper-Copper and Oxide-Oxide Bonding”. In: *Proceedings of Science* (2014)
3. P. Maj et al. “Tests of the First Three-Dimensionally Integrated Chip for Photon Science”. In: *PoS Vertex2012* (2013), p. 027
4. G. Deptuch et al. “3D Technologies for Large Area Trackers”. In: *ArXiv e-prints* (July 2013). arXiv: [1307.4301 \[physics.ins-det\]](https://arxiv.org/abs/1307.4301)
5. R Lipton et al. “Combining the two 3Ds”. In: *Journal of Instrumentation* 7.12 (2012), p. C12010
6. R Yarema et al. “Vertically integrated circuit development at Fermilab for detectors”. In: *Journal of Instrumentation* 8.01 (2013), p. C01052

1.7 CLICPix

1.7.1 Introduction

To achieve the physics goals of flavour tagging at CLIC, a vertex pixel detector with high spatial precision ($3\text{ }\mu\text{m}$ single-point resolution), 10 ns time stamping and ultra-low mass (0.2% X_0 per detection layer) will be required.

1.7.2 Recent Milestones

- Development of the CLICpix hybrid pixel readout ASIC with $25\text{ }\mu\text{m}$ pitch, analog readout, time stamping, and power-pulsing functionality, implemented in 65 nm CMOS technology
- Development of ultra-thin ($50\text{ }\mu\text{m}$) planar pixel sensors, as well as active sensors with capacitive coupling
- Low-mass fine-pitch interconnects between sensor and ASIC
- Through-silicon via technology for powering, configuration and readout of the ASIC
- Low-mass powering infrastructure, including power-pulsing with local energy storage
- Low-mass carbon-fibre supports
- Detector cooling based on forced air-flow
- Concepts for mechanical integration and detector assembly
- Detector layout optimisation studies

1.7.3 Engineering Challenges

Chapter 2

Tracking Detectors

2.1 SCIPP Tracking R&D

2.1.1 Introduction

2.1.2 Recent Milestones

2.1.3 Engineering Challenges

2.1.4 Future Plans

2.1.5 Applications outside Linear Colliders

SCIPP has been involved in Linear Collider tracking R&D for a number of years, and its work has led to the development of a refined understanding of several generic tracking issues with potential applications for Linear Collider detectors. These include the use of resistive strips and dual-end readout for the determination of the longitudinal coordinate of the charge deposition on narrow electrodes [18] and limitations on silicon microstrip ladder length for precision narrow-strip sensors [19]. These studies are in fact dependent only on the properties of the electrode that collects the signal and propagates it to the readout electronics, and thus are independent of the sensor technology that generates the signals. Thus, this work may have relevance to detection issues across a wide array of fields. Ongoing tracking R&D is focused on the further development of the Long Shaping-Time Front End (LSTFE) microstrip readout ASIC. The properties of this ASIC have been explicitly optimized for the readout of long ladders of silicon strip sensors that are motivated by the need for precise low-mass central tracking for a Linear Collider Detector. With a small and straightforward change to the shaping properties of the ASIC, it could be re-optimized for use for the short strips and high occupancy that would be expected for ILC forward-tracking applications. Similar to most ILC-oriented readout designs, the LSTFE features a long shaping time optimized to reduce voltage-referenced readout noise, as appropriate for narrow-strip, long-ladder applications. Unique to the LSTFE design, however, is the use of time-over-threshold readout to estimate the analog pulse-height generated by

subatomic particles passing through. A pulse-development and readout simulation developed at SCIPP suggests that the intrinsic statistical fluctuations of the charge-deposition process in 300 μm of silicon obviate the need for a precise measurement of deposited charge. A simulation of the centroid-finding (position-resolution) uncertainty provided by time-over-threshold readout showed little degradation relative to that provided by an exact measurement of deposited charge. On the other hand, there are several advantages offered by the use of time-over-threshold readout. It is very simple to implement within a digital back-end to the LSTFE’s analog front end (the implementation would be on the same chip as the front-end readout), requiring only a measurement of the number of clock counts that the given channel is over threshold, and then the assembly and transmission of a single data word containing the time of the upward transition, the time over threshold after the transition, and the channel number. This happens in real time and is driven immediately off the chip into the DAQ, eliminating the need for buffering and ADC conversion. In particular, there is no limit to the rate at which particles can be detected other than the return-to-baseline of the analog signal, and so the data-accumulation rate capability of the device is very high. In addition, for forward tracking, for which short strips are envisioned, the shaping time can be shortened significantly. This will further improve the rate capability of the LSTFE readout, making it an excellent choice for the high-occupancy forward region. Figure 2.1 shows the measured fractional charge uncertainty for the LSTFE prototype ASIC; for depositions expected from minimum-ionizing particles (1 – 4 fC) the fractional charge measurement uncertainty is approximately 15%, which is small compared to the intrinsic fluctuations that arise from the deposition process.

References

- Jerome K. Carman et al. “Longitudinal resistive charge division in multi-channel silicon strip sensors”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 646.1 (2011), pp. 118–125. ISSN: 0168-9002
- Kelsey Collier et al. “Microstrip electrode readout noise for load-dominated long shaping-time systems”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 729 (2013), pp. 127–132. ISSN: 0168-9002

2.2 KPIX

2.2.1 Introduction

KPiX is a 1024 channel “System on a Chip” intended for bump bonding to large area Si sensors, enabling low multiple scattering Si strip tracking and high density Particle Flow calorimetry for SiD at the International Linear Collider (ILC).

Each channel consists of a dynamically switchable gain charge amplifier; shaping; threshold discrimination; and 4 sample and hold capacitors and 4 timing registers. The chip permits 4 separate measurements of amplitude and time of threshold crossing during each train, and amplitude digitization and readout during the intertrain period.

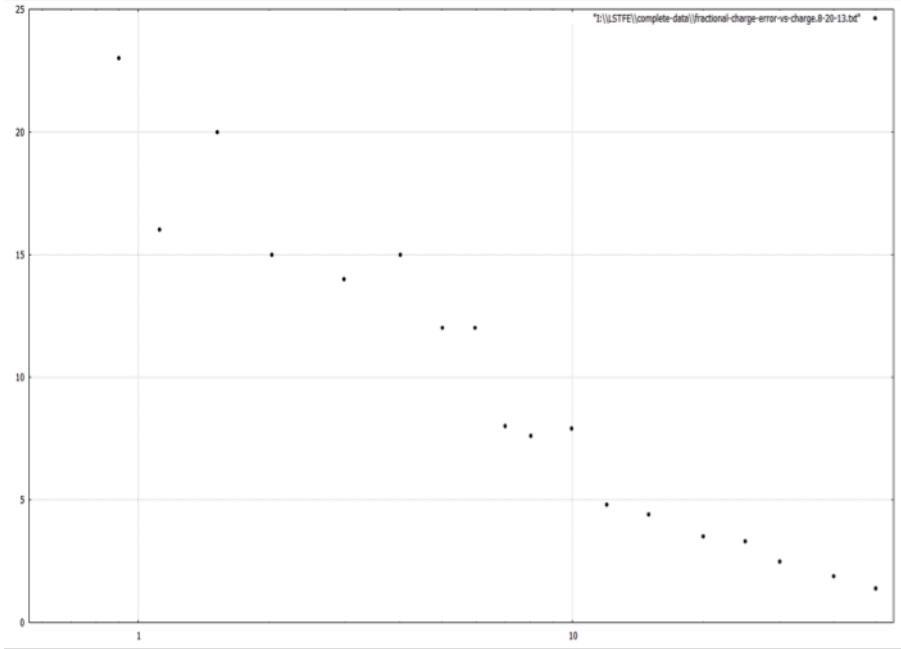


Figure 2.1: Fractional pulse-height uncertainty (percent) versus injected charge (fC) for the LSTFE front-end ASIC. The development of this ASIC has been done solely at the Santa Cruz Institute for Particle Physics (SCIPP) within the University of California at Santa Cruz, and while slowed significantly due to the loss of support for Linear Collider Detector R&D, continues within SCIPP. Tasks that remain in developing a chip suitable for use in a Linear Collider Detector include the development of the digital back end; significant progress has already been made in defining the architecture of this section of the chip and in implementing this architecture in prototype form on an FPGA. Power cycling (switching the chip into a low-power quiescent mode for most of the 199 ms between beam crossings) also needs to be implemented.

The dynamic range is from sub minimum ionizing particle (mip) (in 320 μm silicon) to more than 2000 mip. KPiX also has a calibration system for each channel, servos for leakage compensation, “DC” reset for asynchronous operation for testing with cosmic rays, and polarity inversion for use with GEMs and similar detectors. The noise floor is about 0.15 fC (\approx 1000 electrons), and the maximum signal is 10 pC (utilizing the dynamic range switching). The full dynamic range corresponds to 17 bits.

2.2.2 Recent Milestones

ILC related R&D in the US is largely unfunded and small efforts are being kept alive on the margins. The KPiX R&D is such an example of necessary work for SiD that is marginally alive.

2.2.3 Engineering Challenges

At this time, KPiX is seen as the baseline readout system for the tracker and electromagnetic calorimeter. A stack of 13 EMCal sensors with bump bonded KPiX was assembled for a beam test at SLAC in the summer of 2013. That test discovered that two kinds of crosstalk are significant:

- In-time crosstalk occurs due to parasitic coupling of traces on metal 2 of the sensor to other pixels. The level of crosstalk increases with the size of the signal, and decreases with increased speed of the front end charge amplifier (meaning increased current and power dissipation). A new sensor design is being developed that uses metal 1 to shield the traces of metal 2, and these ideas will be tested in the next sensor prototype.
- Out-of-time cross talk occurs when many pixels are hit and reset simultaneously. The resets collectively cause other pixels to trigger, and a cascade builds up. This uses up all the KPiX buffers. The root cause of the problem appears to be some internal logic within KPiX that is not current limited, and will require design modification.

A more general issue is that both the EMCal and tracker sensors from Hamamatsu were ordered with Al pads, as it was believed that plating (by the zincate process) a stack of metals culminating with Au would be straightforward. This turns out to be wrong. Future sensors will be ordered with Au pads.

An additional issue is that the Tracker sensor was planned to be wire bonded to its (very thin) cable. The sensor oxide layer is not strong enough to allow wire bonding without damage, and so must be solder bumped. The pad pitch is small, and solder bumping the cable will be challenging. The trouble with the wire bonding to the sensor was unexpected. Another concern is that the current design of KPiX has deadtime after a pixel has accepted a trigger. Only the triggered pixel is affected; all the other pixels are available for signals. This deadtime is different from the usual notion of data acquisition deadtime where the entire detector is unavailable, but the correction to the luminosity integral is easy. Finally, the buffer requirement (4 in the current version of KPiX) is being re-evaluated in SiD simulations. A possible new

architecture for KPiX is in early stages of evaluation. A small mechanical engineering effort has started to study the structure of the EMCal. The SiD EMCal has emphasized thin gaps between the tungsten layers to minimize the Moliere radius, and this implies that the structure is connected by columns at the vertices of the sensors. The DBD design shows hexagonal sensors, which indeed are the most efficient way of tiling large areas, but no consideration was given to the edges of these arrays. The design is being re-evaluated to optimize the cost-effectiveness over the whole area taking into account geometric efficiencies and total wafer cost. Tracker sensors are now at IZM for the pad plating and subsequent bonding of KPiX; they will then go to UCD for cable attachment and testing.

2.2.4 Future Plans

Assuming positive developments with Japan are announced soon, we expect the financial support to improve. It should be noted that an important effect of the withdrawal of support is that most of the US collaborators have been forced to move to other work.

- EMCal Sensors: A second round of prototypes will be designed and ordered with rectangular layout; shielded traces, and Au pads.
- Tracker Sensors: The current prototypes will be evaluated, and if appropriate tested in a beam.
- KPiX: A new architecture with little (or no) deadtime will be evaluated. A decision will be made to develop this new architecture or incrementally.
 - improve the existing design.
- The EMCal mechanical structure will be pushed towards a conceptual design.

2.2.5 Applications Outside of Linear Colliders

This work represents a significant step in the aggressive integration of silicon sensors with readout electronics, just short of integrating the electronics directly into the sensors. It has prompted consideration of this approach by CMS for calorimetry and by ATLAS for a muon system. It may have applications in sensors for light sources as well as other particle physics detectors.

2.3 Time Projection Chamber – Bonn

This needs contributions from the other institutes. Take from LCTPC report to ECFA

2.3.1 Introduction

The University of Bonn is studying the pixelized readout of a TPC for the ILD detector. The readout is based on the Timepix ASIC with a triple GEM or Micromegas based gas amplification.

2.3.2 Recent Milestones

The first studies were based on the triple GEM setup with a single Timepix chip. This readout was mounted in a small test detector in the Bonn laboratory. Here, the working principle was tested with a long drift distance. It could be demonstrated that the transverse spatial resolution of the reconstructed primary electrons was close to the expected diffusion limit of single electrons. The results are summarized in the following publications:

- C. Brezina et al. “Operation of a GEM-TPC With Pixel Readout”. In: *Nuclear Science, IEEE Transactions on* 59.6 (Dec. 2012), pp. 3221–3228. ISSN: 0018-9499
- J. Kaminski et al. “Time projection chamber with triple GEM and pixel readout”. In: *Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE*. Oct. 2008, pp. 2926–2929
- C. Brezina et al. “A Time Projection Chamber with triple GEM and pixel readout”. In: *Journal of Instrumentation* 4.11 (2009), P11015
- Jochen Kaminski et al. “Time projection chamber with triple GEM and highly granulated pixel readout”. In: *Conf.Proc. C0908171* (2009), pp. 533–535
- Peter Schade and Jochen Kaminski. “A large {TPC} prototype for a linear collider detector”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 628.1 (2011). {VCI} 2010 Proceedings of the 12th International Vienna Conference on Instrumentation, pp. 128–132. ISSN: 0168-9002

The new focus are GridPix based detectors, where the gas amplification stage is a Micromegas produced in a postprocessing technique, which guarantees a high quality grid well aligned with the readout pixels. This approach was pioneered by NIKHEF and the University of Bonn has modified the production process together with the Fraunhofer Institut IZM so that a wafer-based production of GridPix detectors is standard by now. The new GridPixels were tested on small prototype detectors and also assembled in an 8 GridPix module for the Large Prototype detector at DESY. A successful test beam campaign was performed last year.

- M. Lupberger. “The Pixel-TPC: first results from an 8-InGrid module”. In: *Journal of Instrumentation* 9.01 (2014), p. C01033
- W.J.C. Koppert et al. “GridPix detectors: Production and beam test results”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 732 (2013). Vienna Conference on Instrumentation 2013, pp. 245–249. ISSN: 0168-9002

The current work is focused on a new LP module with about 100 GridPixels. This module is a demonstrator that larger areas (400 cm^2) can be produced and operated. It shall be tested in the LP at the beginning of next year. For this a number of challenges have to be coped with. In particular commercial readout systems are not easily scalable. This is why Bonn has developed a cheap and easily expandable system based on the Scalable Readout System (SRS) of the RD51 collaboration. In addition Bonn is developing the software for reconstructing and analyzing the test beam and simulation data. For this the LCTPC software framework of MarlinTPC is used.

- Jason Abernathy et al. “MarlinTPC: A common software framework for TPC development”. In: *Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE*. Oct. 2008, pp. 1704–1708

Finally, Bonn also takes part in designing new pixel chips. To test the new digitization and readout techniques two test chips were designed in collaboration with N'IKHEF. Then Bonn also contributed to the design of the Timepix successor chip, Timepix3, which is being tested now:

- A Kruth et al. “GOSSIPO-3: measurements on the prototype of a read-out pixel chip for Micro-Pattern Gaseous Detectors”. In: *Journal of Instrumentation* 5.12 (2010), p. C12005
- C. Brezina et al. “GOSSIPO-4: Evaluation of a Novel PLL-Based TDC-Technique for the Readout of GridPix-Detectors”. In: *Nuclear Science, IEEE Transactions on* PP.99 (2014), pp. 1–1. ISSN: 0018-9499
- Y Fu et al. “The charge pump PLL clock generator designed for the 1.56 ns bin size time-to-digital converter pixel array of the Timepix3 readout ASIC”. in: *Journal of Instrumentation* 9.01 (2014), p. C01052

2.3.3 Engineering Challenges

The production of a module with 100 GridPixels requires 4 main components: The production of a large number of GridPixels with sufficiently good quality. This has been addressed by the new production method and a large batch is being produced. The challenge of the readout is being addressed by the new readout system. Finally the distribution of the LV power to all ASICs and the cooling of the ASICs still are unclear, but since both challenges are similar for most readout electronics, standard solutions are expected to be adequate.

2.3.4 Future Plans

On a short term the production of the 100 ASIC module is the main goal at Bonn. If this module has been successfully operated, we are interested in replacing the Timepix ASIC by the Timepix3 ASIC and produce GridPix detectors with this improved chip. There are also some ideas of how to improve the grid structure and make it more reliable. Finally, the reconstruction and analysis software needs further improvement and has to be extended, so that simulated data for the final TPC (i.e. 10,000 hits per track) can be studied.

2.3.5 Applications Outside of Linear Colliders

A single InGrid detector will be installed this year in the CAST experiment for axion search. For a CLIC–TPC a highly granular (i.e. pixelized) readout structure is mandatory to lower the occupancy.

Chapter 3

Calorimeter R&D

3.1 Scintillator Strips

3.1.1 Introduction

3.1.2 Recent Milestones

- introducing a new scintillation light readout scheme, with different scintillator strip shape by having better homogeneity
- photo-sensor of increased number of pixels in 1mmx1mm, this leads larger dynamic range for the calorimeter
- more experience on the FE read out board and ASICs

They are not published yet, instead some proceedings

3.1.3 Engineering Challenges

- wrapping the scintillator strip and align them on the FE read out layer automatically
- mass test facility for the read out layer

3.1.4 Future Plans

- optimizing scintillator layer: shape of scintillator strip, how to read out scintillation light, the location of photo-sensor, size and shape of photo-sensor and mass production scheme
- developing photo-sensor with Hamamatsu photonics company, to have larger dynamic range and mass test scheme
- establish a detector fabrication plan

3.1.5 Applications Outside of Linear Colliders

- photo-sensor named MPPC from Hamamatsu photonics INC is employed for the T2K experiment, CMS upgrade (HC-CAL), BELLII detector (endocarp muon)
- PET and SPECT development

3.2 Silicon-Tungsten ECAL in ILD

3.2.1 Introduction

The silicon-tungsten electromagnetic calorimeter for ILD aims to develop a highly granular detector optimized for particle flow performance. The calorimeter uses a sandwich architecture with $5 \times 5 \text{ mm}^2$ silicon pads as active elements embedded in an alveola structure made of tungsten. The group is active in the development of simulation software and algorithms for calorimeter reconstruction, as well as engineering for the design, and fabrication of the readout chips.

3.2.2 Recent Milestones

The work is now focusing on the construction of a technological prototype. This is a new milestone after the successful operation of the “Physics Prototype” in the years 2004–2011, including large scale beam tests at DESY, CERN at FNAL and data analysis [31]. An analysis of data recorded in 2007 [32] gives confidence that embedding the front end electronics into the calorimeter layers does not compromise the detector performance.

For the technological prototype, the SKIROC ASIC will be embedded into the calorimeter layers and mounted on 9 layer PCBs that will be as thin as 1.5 mm. Silicon wafers, the PCB and the 16 mounted circuits constitute the Active Signal Units or ASUs. Up to ten of these ASUs will be assembled to form a calorimeter layer. The technology of the interconnections was applied with success to first units of the technological prototype.

A series of beam tests with simplified ASUs have been carried out in the years 2012 and 2013 at DESY. The analysis of these data validated the concept of the front end electronics but will also allow for correcting a small number of shortcomings of the SKIROCs ASIC. These will be corrected in the version SKIROC2b that is supposed to be produced at the end of 2014. A paper on the analysis of the 2012 data has been submitted to JINST in March 2014. Particularly in summer 2013 (i.e. Post-DBD phase), the SKIROC ASIC has been operated in power pulsed mode. For this bias currents of the ASIC are shut down and raised with a given frequency (5 Hz for ILC, 10 Hz in our beam tests). The good agreement between the MIP spectra obtained in power pulsed and conventional mode (see e.g. [33]) give confidence that this technology can indeed be applied for a calorimeter at a linear collider and more precisely at the ILC. More studies are needed as the technological prototype grows in size.

Other recent accomplishments include:

update?

- R&D on scalable technology for all the involved large detector aspects (integration of embedded readout chips, on thin supporting electronics boards, in self-supporting tungsten–carbon mechanical elements ensuring the cooling and protection; all made of exchangeable elements with a quality control procedure; the associated DAQ).

is this completed?

- Realization of a large self-supporting W–Carbon fiber structure with integrated stress monitoring (using Fiber Bragg Grating)

date?

- Beam tests of base sensor units of the technological prototype

- Submission of a paper on the analysis of 2012 beam test data to JINST [34],[35].

Recent?

- Reconstruction tools adapted to the high granularity calorimeters (photon reconstruction [GARLIC], Advanced clustering [ARBOR], event displays [DRUID])

Reference

- Operation of SKIROC [36] in pulsed power mode (with 5 Hz as foreseen by ILC baseline and with 10 Hz as envisioned in high luminosity operation).

Reference

- SiECAL test beam experiments were carried out in Jul. 2012, Feb. and Jul. 2013 to test the SiECAL technological prototype. The front-end electronics of the prototype was integrated into an active layer to realize a highly granular calorimeter. In the 2012 test beam, we operated six layers under a continuous current mode. The achieved signal to noise ratio was greater than 10 with SKIROC2 ASICs. In the 2013 test beams, we successfully operated and took data with the prototype under a power pulsing mode. At the same time, we found several issues related to the power pulsing operation. Digital lines on the front-end electronics disrupts analog signals. We had to wait 600 μ s for the electronics to stably take the data. We measured pedestal signals in a magnetic field, and confirmed that active channels were working in stable up to 2 T.

Reference

As for the R&D of silicon sensors, we measured several new samples with different guard ring types. It is known that a Si sensor makes small fake signals along with its sensor edge when a large amount of current is generated by an electromagnetic shower in a calorimeter. If the fake signal is reasonably small, we can use the Si sensor for the ILD. To test the fake signal, we introduced an infrared laser system in Kyushu University to measure the Si sensor response with a similar condition of beam test in a laboratory scale. We are setting up a multi-pixel readout system without SKIROC2 ASIC. We can then measure the intrinsic Si sensor properties with the IR laser system. Studies on the SiECAL optimization have been performed with full ILD detector simulation. We performed simulation studies with different setting of PCB thickness, dead volume related the sensor edge, and fraction of dead channels. We found:

- The PCB thickness does not change the performance of the jet energy resolution.
- The dead volume proportionally degrades the performance, but the current Si sensor design is acceptable.

- The fraction of dead channels does not much degrade the jet energy resolution up to the fraction of 5%.

3.2.3 Plans of the near future

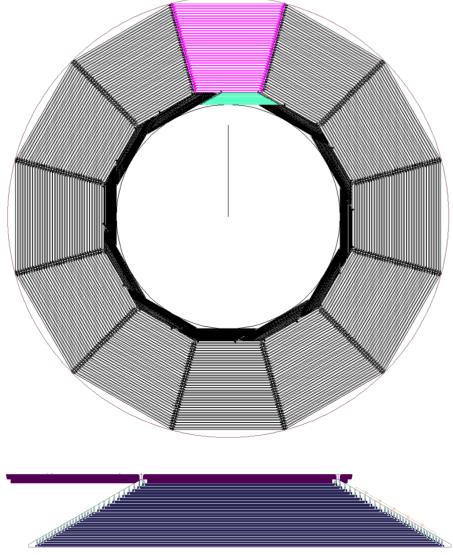
The different units of the SiW Ecal for the ILD detector need to be assembled into detector layers of up to two meter in length comprising up to 10 detection units dubbed ASUs. For this we propose to develop an assembly line, incorporating the reception and the test of the material, the alignment of the ASUs and the interconnection, with a continuous monitoring for quality control purposes. The deliverable is a still manual assembly bench capable for a small production of layers. Based on the manual assembly bench we will propose an automatized system for mass assembly together with industrial partners. A survey to search for partners is part of the proposal. A goal is to design the system such that it can be easily duplicated at other sides. In the ideal case the assembly bench is versatile enough to reply to needs for other detector systems than ILD (e.g. CMS). Other Detector R&D plans include:

- Test beam experiments with long SiECAL slabs using new front-end electronics with SKIROC2 ASICs,
- Completion of the SKIROC3 ASIC, which has all the features needed at the ILC.
- Combined test beam experiments with ScECAL and AHCAL,
- Development a DAQ system (set up of hardwares, development of software and firmware) for the combined tests.
- Further R&D of silicon sensors, using the IR laser system, to determine the final design.
- Irradiation test with several types of Si sensors.
- Looking for Japanese companies which can produce SiECAL front-end electronics in prospect of mass production.
- Further optimization of SiECAL and Hybrid ECAL with full ILD detector simulation.

3.2.4 Engineering Challenges

The following challenges will have to be addressed when proposing this technology for an ILC detector:

- Silicon wafer cost reduction when used for calorimetry; direct contact with producers established (Hamamatsu, On-Semi, ...).
- A chip with the good dynamic, noise, power dissipation (using power pulsing), etc.



- Integration in a compact device, ensuring all the requests (precision: electronic and mechanic, heat production, reliability)
- Industrialization of solutions; scalability of tests for a 100M channel detector.

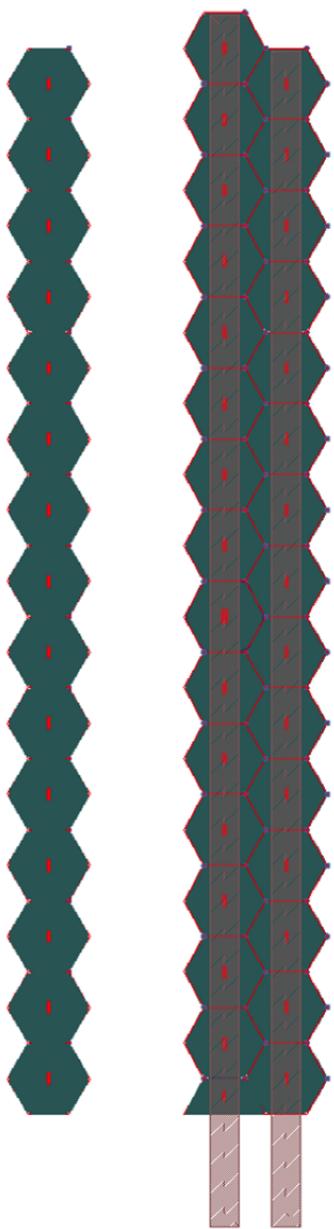
3.2.5 Applications Outside of Linear Colliders

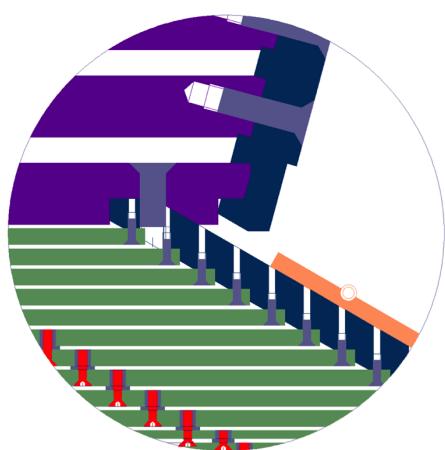
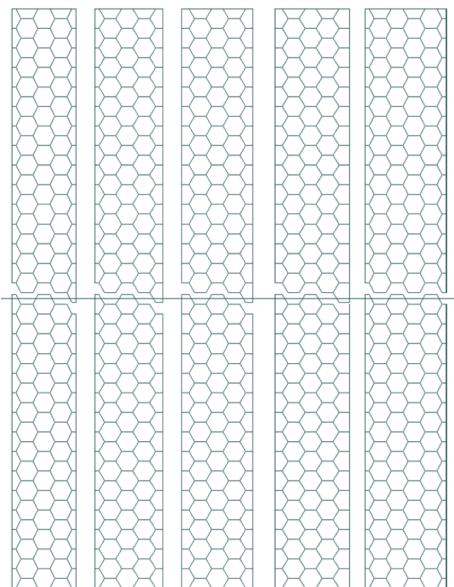
- CEPC, TLEP and CMS upgrade have possible applications for this technology
- The compact Silicon-W design has been used in the PAMELA satellite (very similar to physics prototype) [37]

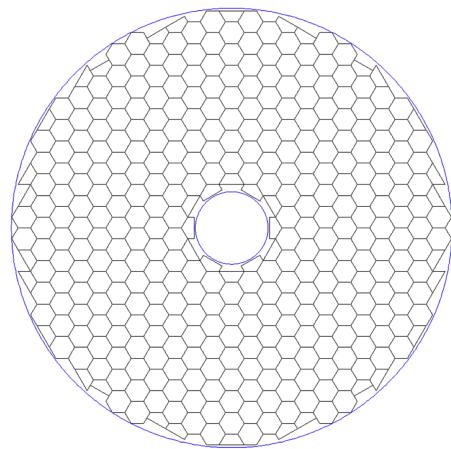
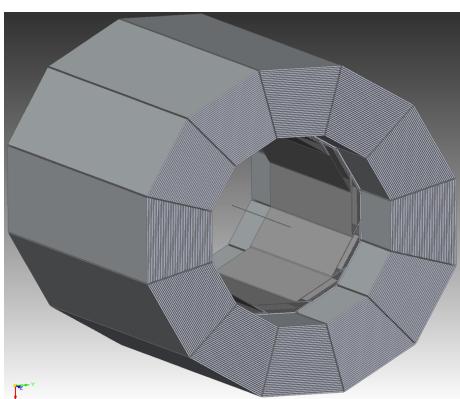
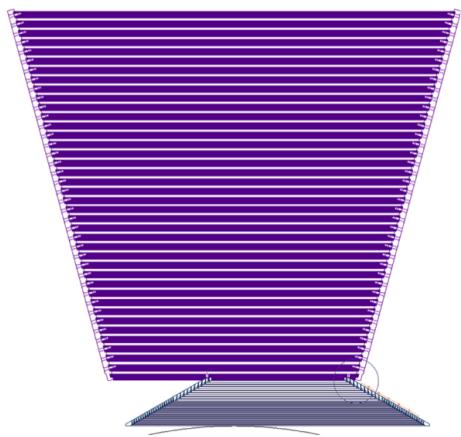
3.3 Silicon Tungsten SiD ECAL

3.3.1 Introduction

This note describes the theory of the mechanical aspects of the E-Cal system for SiD. The E-Cal barrel consists of stacks of tungsten heavy metal plates which are arranged in modules surrounding the beamline. Full cylindrical coverage of the baseline design is attained with twelve modules (see figure 1) occupying a radial envelope from 1265mm to 1409mm. The total barrel length is 3.53m. Each module uses 20 inner plates which are 2.5mm thick followed by ten 5mm thick plates. Gaps between adjacent plates are 1.25mm and house the silicon detectors with their associated cables (see figure 2). These hexagonal silicon detectors are electrically connected to each other with thin, flexible circuits which are read out on both ends of a module (see figure 3). Panels of detectors increase in width as they get closer to the beamline. To minimize silicon waste and to maximize coverage, fractions of hexagons complete







the panel edges (see figure 4). By cutting the silicon in strategic locations, only a few different silicon shapes may be needed to achieve the 31 different panel widths. The tungsten plates are connected together on their longitudinal edges as well as in the field of detectors. Space for fasteners in the field is achieved by chamfering the corners of the hexagonal detectors. The field fasteners hold the plates together, provide a uniform 1.25mm standoff height, and assist with inter-plate shear. The fasteners near the edges of the plates close the module profile and lend torsional rigidity to the structure. An FEA simulation of the proposed configuration should be done to properly size the fasteners (see figure 5). The modules, which weigh about 5 tons each, are mounted to stainless plates which are used as the first layer of the next detector system (H-Cal). This first H-Cal plate is unique in that its two longitudinal edges form a guide system to locate the E-Cal to the H-Cal system. The H-Cal modules are first bolted together to form the H-Cal barrel. Interleaving structural side battens maintain spacing for the H-Cal plates and extend inward to the E-Cal support plates. The inner ends of these battens act in concert as the female portion of the E-Cal guide system. The E-Cal modules are slid into place in the inner H-Cal bore. Extension plates complete the inner H-Cal first layer, since the E-Cal barrel is shorter. H-Cal detector panels are installed after this structure is complete (see figure 7). Only simple detector layouts have been done for the E-Cal endcaps so far. These layouts show that using full and partial hexagons could yield fairly good coverage with only a few shapes. (see figure 8).

3.4 Resistive Plate Chambers

3.4.1 Description of the DHCAL

The Digital Hadron Calorimeter or DHCAL uses Resistive Plate Chambers (RPCs) as active elements. The chambers are read out with $1 \times 1 \text{ cm}^2$ pads and 1-bit (digital) resolution. A small-scale prototype was assembled and tested in the Fermilab test beam in 2007 to validate the concept. Based on the success of the small-scale test [1-6], a large prototype with up to 54 layers and close to 500,000 readout channels was built in 2008 – 2011. Each layer measured approximately $96 \times 96 \text{ cm}^2$ and was equipped with three chambers, stacked vertically on top of each other. For tests with particle beams the DHCAL layers were inserted into a main stack of 38 or 39 layers, followed by a tail catcher with up to 15 layers. For the tests performed at Fermilab the main stack contained steel absorber plates. At CERN the absorber plates were made of a Tungsten based alloy. In both cases the tail catcher featured steel absorber plates. In the various test beam campaigns combined, spanning the years 2010 – 2012, the DHCAL recorded around 14 Million muon events and 36 Million secondary beam events, where the latter contained a mixture of electrons, muons, pions, and protons.

3.4.2 Current R&D activities

The analysis and publication of the test beam results are currently the highest priority of the DHCAL group. Major challenges, such as the calibration (or equalization) of

the response of the RPCs and the detailed simulation of the response of RPCs, are very close to having been overcome [7-11]. Parallel to the analysis of test beam data, the group is pursuing the following R&D activities:

Development of 1-glass RPCs

The DHCAL prototype featured a standard chamber design based on RPCs with two resistive plates. It is possible to eliminate one of the glass plates in future applications. The advantages are: close to unit pad multiplicity with significant simplification of the calibration and monitoring procedure, reduced thickness of the active element, higher rate capability, and insensitivity of the response to the surface resistivity of the resistive layer (used to apply the High Voltage). To date several 1-glass RPCs have been assembled. The chambers tested very well with cosmic rays. Tests in particle beams are planned for future test beam campaigns.

Development of high-rate RPCs

Due to the high bulk resistivity of glass (and Bakelite), RPCs are notoriously rate limited [38]. The DHCAL group is addressing this shortcoming with the developments of semi-conductive glass (in cooperation with COE college) and low-resistivity Bakelite (in co-operation with USTC). First chambers with samples of low-resistivity glass plates have been assembled and have been tested in the Fermilab test beam.

Development of a High-Voltage distribution system

With up to 50 layers in a single calorimeter module, a cost-effective way to distribute the High-voltage to individual layers is required. A system capable to regulate the voltage within a few 100 V, to monitor both the current and the voltage, and to switch off individual channels, is being developed. A first prototype controlling a single channel has been assembled and tested successfully with an RPC. The development is currently on hold due to lack of funding.

Development of a gas recycling system

The operation of RPCs requires a gas mixture, which is both costly and environmentally harmful. To limit the effect of releasing gas into the environment, the DHCAL group is developing a gas recycling system. The system is based on a new approach, appropriately labeled “Zero Pressure Containment”. A prototype of the gas collection subsystem is currently being assembled; however, progress is again slow due to lack of funding.

Reference

Development of the next generation front-end readout system

The next generation front-end readout system will contain several upgrades compared to the current system: higher channel count, token ring passing, low power operation, power pulsing, and improved internal charge injection systems. To proceed, the project is awaiting funding from both US and Chinese agencies.

3.4.3 Engineering challenges

Several engineering challenges remain to be addressed before an RPC-based DHCAL can be proposed as an option for a colliding beam detector. Following is an (incomplete) list of the major issues:

- Industrialization of the construction of RPCs.
- Design of the readout boards, covering the entire area of the layer (with varying width). The design is expected to feature only a minimum number of different boards.
- Design of the gas distribution system, which ensures equal pressure in all layers of a given module, independent of its orientation.
- Development of a cooling strategy for the front-end boards, which will include power pulsing, as well as active cooling.
- Development of a module assembly procedure.

3.4.4 Plans for the coming years

The activities of the coming years depend strongly on the progress with the Japanese intentions to host the ILC. Assuming the ILC project goes ahead, the DHCAL group will a) Complete the analysis and publication of the test beam data, b) Complete the R&D projects listed above, and c) Start the development of the design of calorimeter modules. In case, the ILC is not going forward, the group plans on completing the data analysis and to continue the tests of high-rate RPCs. Other R&D projects, such as the development of distribution systems, will be put on hold.

3.4.5 Applications beyond the ILC

The DHCAL technology was specifically developed for the hadron calorimeter of the ILC, with its low particle rate and radiation dose. To export the technology to other environments, the rate capability of the chambers and the radiation hardness of the readout need to be improved. The former is being addressed with low-resistivity plates (glass and Bakelite), while the latter will require a new front-end readout system based on an ASIC using a smaller feature size. Possible applications are the tail catcher of the forward calorimeters of CMS and the outer wheels of the ATLAS muon system. Both options are being pursued actively.

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3.5 GEM

3.5.1 Introduction

The group pursues the development of Gas Electron Multiplier technology for instrumenting a digital hadronic calorimeter (DHCAL) at the ILC. The

3.5.2 Recent Milestones

3.5.3 Engineering Challenges

3.5.4 Future Plans

- To be determined

3.5.5 Applications Outside of Linear Colliders

3.6 FCAL

3.6.1 Introduction

Overall text is too long

Two special calorimeters are foreseen in the very forward regions of a linear collider detector, denoted hereafter as LumiCal and BeamCal. These calorimeters will deliver both a fast and a precise measurement of the luminosity and extend the detector coverage to low polar angles, important e.g. for new particle searches with missing energy signature. Detailed Monte Carlo studies have been performed in all member institutes to optimize the design of the calorimeters, estimate the background from physics processes and understand the impact of beam-beam interactions on the luminosity measurement [51]. A sketch of the design is shown in Figure 3.1 (left). To ensure a high efficiency for single high energy electron detection on top of the large and widely spread background from beamstrahlung very compact calorimeters are needed. In addition, compact calorimeters facilitate the reconstruction of Bhabha scattering events. Due to the high occupancy originating from beamstrahlung and

why compact? What does this mean?
Molière radius? outer radius?

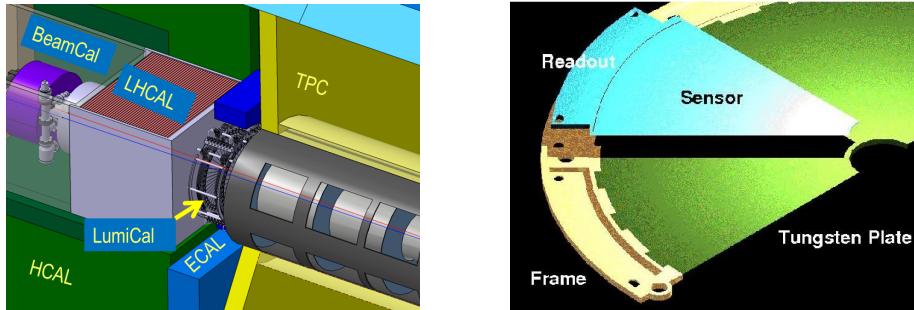


Figure 3.1: Left: The very forward region of the ILD detector. LumiCal, BeamCal and LHCAL are carried by the support tube for the final focusing quadrupole QD0 and the beam-pipe. TPC denotes the central track chamber, ECAL the electromagnetic and HCAL the hadron calorimeter. Right: A half layer of an absorber disk with a sensor sector and front-end electronics.

two-photon processes, both calorimeters need a dedicated fast readout. In addition, the lower polar angle range of BeamCal is exposed to a large flux of low energy electrons, resulting in depositions up to one MGy per year. Hence, radiation hard sensors are needed.

3.6.2 Mechanical Concept

Since in both calorimeters a robust electron and photon shower measurement is essential, a small Molière radius will be preferable. Compact cylindrical sandwich calorime-

ters using tungsten absorber disks of one radiation length thickness, interspersed with finely segmented silicon (LumiCal) or GaAs (BeamCal) sensor planes, as sketched in Figure 3.1 (right), are found to match the requirements from physics [51].

3.6.3 Recent Milestones

3.6.4 Engineering Challenges

Engineering challenges within the current and future research within FCAL are the following:

- a slim assembled sensor plane. The space between absorber planes must be kept as small as possible. The fan-out to move the signals from the sensor pads to the outside radius must be very thin and hence a new connectivity technology must be applied.
- multichannel front-end and ADC ASICs for the prototype. A compromise must be found between integration, miniaturization and costs.
- operation using power pulsing.
- a dedicated solution for data concentration, data reduction and transmission.
- precise alignment and position monitoring.

what is the challenge?

be more specific

be more specific

3.6.5 Future Plans

Sensors and ASICs

Large area GaAs sensors, as shown in Figure 3.2, were developed and produced in collaboration with partners in industry. The Liquid Encapsulated Czochralski technology is used. The sensors were doped by a shallow donor (Sn or Te), and then compensated with Chromium. This results in a semi-insulating GaAs material with a resistivity of about $10^7 \Omega\text{m}$. The sensors are 0.5 mm thick with pads of a few mm^2 area. The operation voltage is about 100 V with leakage current per pad less than 500 nA.

Prototypes of LumiCal sensors have been designed and manufactured by Hamamatsu Photonics. Their shape is a ring segment of 30°. The thickness of the n-type silicon bulk is 0.320 mm. The pitch of the concentric p⁺ pads is 1.8 mm and the gap between two pads is 0.1 mm. The bias voltage for full depletion ranges between 39 and 45 V, and the leakage currents per pad are below 5 nA [52].

Dedicated ASICs were designed choosing an architecture [53, 54] comprising a charge sensitive amplifier and a shaper. ASICs, containing 8 front-end channels, were designed and fabricated in 0.35 μm CMOS technology. A micro-graph of the prototype, glued and bonded on the PCB, is shown Figure 3.3. A variable gain in both the charge amplifier and the shaper is implemented by a mode switch. The peaking time of the shaper output signal is 60 ns. More results of the measurements of the performance were published elsewhere [55]. A dedicated low-power, small-area,

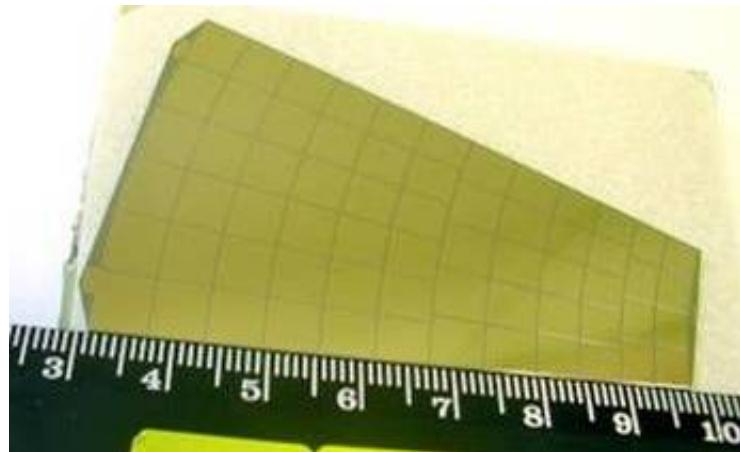


Figure 3.2: A GaAs pad sensor developed for BeamCal.

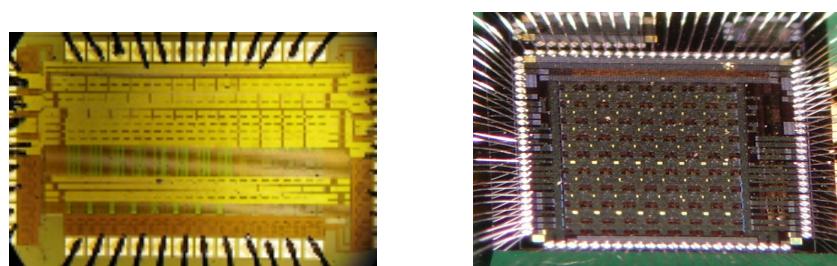


Figure 3.3: Left: Micrograph of front-end ASIC. Right: Micrograph of ADC ASIC.

multichannel ADC is designed and produced [56]. It comprises eight 10-bit power and frequency (up to 24 MS/s) scalable pipeline ADCs and the necessary auxiliary components. A micro-graph of the prototype is shown in Figure 3.3.

what is MS/s

A dedicated ASIC development is ongoing for BeamCal [57] with a special option for a fast readout of an reduced amount of information from each bunch-crossing to be used for a fast feedback system for beam-tuning. A prototype of a pixel sensor readout for the pair monitor, positioned in front of BeamCal was designed in SoI technology [58].

has this been introduced before?

3.6.6 Test-beam Results

Several test-beam campaigns were done to investigate the performance of single fully instrumented sensor planes, both for LumiCal and BeamCal. Prototypes of sensor planes assembled with FE and ADC ASICs, as shown in Figure 3.4, were built using LumiCal and BeamCal sensors [59]. The detector plane prototypes were installed in an



Figure 3.4: Photograph of LumiCal readout module with sensor connected.

electron beam and the trajectories of beam particles were measured by four planes of a silicon strip telescope. The front-end electronics outputs were sampled synchronously with the beam clock, a mode used at the ILC. Data were taken for different pads and also for regions covering pad boundaries. Signal-to-noise ratios of better than 20 are measured for beam particles both for LumiCal and BeamCal sensors, as illustrated in Figure 3.5 (left). The impact point on the sensor is reconstructed from the telescope information. Using a color code for the signals on the pads the structure of the sensor becomes nicely visible, as also seen in Figure 3.5 (right). The sensor response was found to be uniform over the pad area and to drop by about 10% in the area between pads.

3.6.7 Radiation Damage Studies

Two studies of the radiation tolerance of potential BeamCal sensors have been carried out. The radiation tolerance of prototype GaAs sensors has been explored by exposing the sensors to direct irradiation from a high-intensity electron beam of about 10 MeV [60], which is an energy expected from beamstrahlung remnants at the ILC.

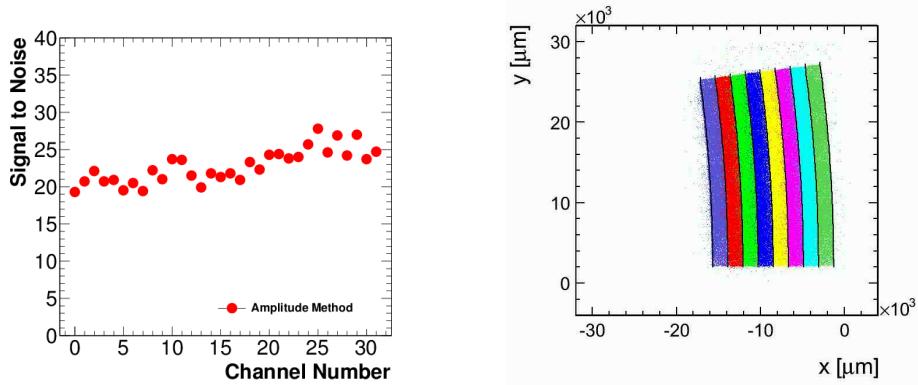


Figure 3.5: Left: The signal-to-noise ratio of all readout channels. Right: Distribution of the predicted impact points on pads with a color coded signal.

It was found that the sensors can be operated up to approximately 1 MGy of this type of radiation without a significant increase in the leakage current [61]; however, significant loss in the response to ionizing particles was observed. In addition, several different silicon-diode sensor technologies were exposed to varying levels of radiation induced by the SLAC End Station A Test Beam (ESTB). For this study, the ESTB test beam, with energies varying between 3 and 11 GeV, was directed into a tungsten beam stop. The beam stop was split at approximately shower-max and the sensor inserted, leading to an exposure incorporating the full spectrum of particle species that will irradiate the BeamCal sensors. Both n-type bulk oxygenated float-zone and magnetic Czochralski detectors were explored, with exposures varying from 0.2 to 2.2 MGy as allowed by the limited exposure rate and beam availability. It was found that, after allowing for a short period of controlled annealing, all sensor types withstood the maximum dose that they received with little loss in response to ionizing particles [62], but with some increase in leakage current. Further annealing studies, geared towards achieving a minimal post-irradiation leakage current, continue. Further irradiation studies in the ESTB are planned for the spring running periods of 2014 and 2015. The sensor assessment (“charge-collection efficiency”) apparatus at the Santa Cruz Institute for Particle Physics is being adapted for the evaluation of pad sensors, which will allow for radiation damage studies of the prototype GaAs sensors in this realistic electromagnetic shower environment. Studies to push the silicon diode sensors to higher levels of irradiation are also planned.

update?

3.6.8 Technological Prototype

Currently the goal of FCAL is to prepare a calorimeter prototype for test-beam measurements. These measurements are essential firstly to develop and test engineering solutions to build a very compact calorimeter and secondly to verify the results of Monte Carlo studies. Depending on the test beam results the calorimeter may be redesigned. For the prototype calorimeter a mechanical structure, a sufficient amount

of front-end and ADC ASICs, FPGAs for data concentration and a data acquisition system are needed.

Mechanical Stack

A flexible mechanical structure, as shown in Figure 3.6, has been built as part of the AIDA I project at CERN, to compose a calorimeter prototype instrumented both with LumiCal and BeamCal sensors. Tungsten absorber plates, glued on a permaglass frame, are precisely positioned on a rod assembly, and interspersed with fully assembled sensor planes. The flatness of the absorber plates is better than $50\text{ }\mu\text{m}$ to allow

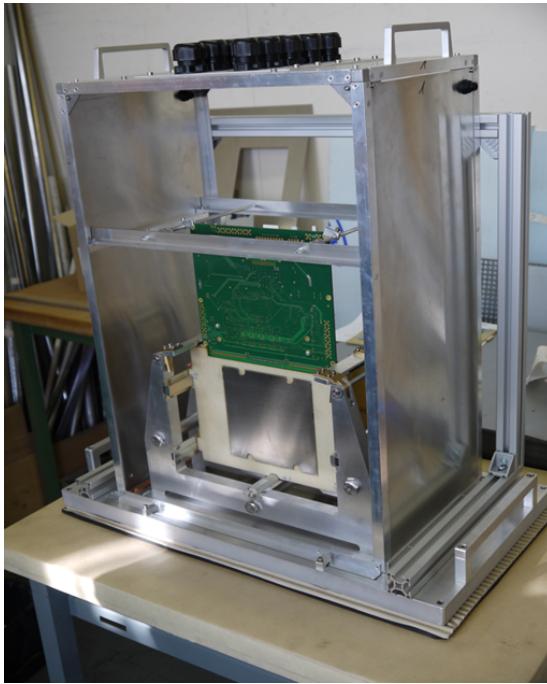


Figure 3.6: Photograph of the flexible mechanical structure. Tungsten absorber plates, glued on perma-glass frames, are put into slots of the rod assembly.

high compact packing of sensor and absorber planes.

Alignment and Position Monitoring

A laboratory set-up for position monitoring has been constructed by IFJPAN Cracow using semi-transparent silicon sensors. Test measurements demonstrated that position monitoring with μm precision is possible.

Front-End and ADC ASICs

To match the requirements of extremely low power consumption and taking into account possible radiation fields in the very forward region, a new development of the front-end and ADC ASICs in deep sub-micron 130 nm CMOS technology has been pursued within AIDA by UST Cracow. These ASICs will be sufficiently fast to be used both in LumiCal and BeamCal. The overall readout architecture, so far successfully produced in 350 nm CMOS technology and used in the test-beam measurements as described above, has not been changed and comprises separated front-end and ADC ASICs for each readout channel. For both FE and ADC ASICs prototypes, shown in

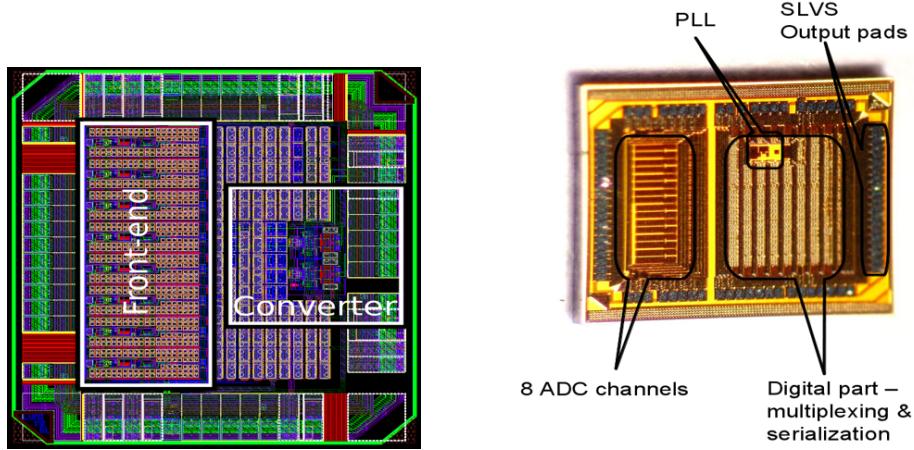


Figure 3.7: Left: 8 channel FE ASIC in 130 nm technology. Right: ADC ASIC in 130 nm technology.

Figure 3.7, are under test.

Data Concentrator and DAQ

In order to operate a large amount of sensor planes the readout has to be orchestrated. For this purpose a FPGA based data concentrator is foreseen which may deliver data in the so called AIDA protocol. The design of this device is currently under discussion. The higher level DAQ will depend on the functionality of the data concentrator. For the readout of test-beam data we have software, mainly developed by University of Tel Aviv, which can be easily adopted. For a final device FCAL will follow the developments of a common DAQ for all subdetectors.

3.6.9 Applications Outside of Linear Colliders

The expertise acquired within FCAL for radiation hard sensors and fast front-end electronics was used to build, commission and operate fast beam-conditions monitors at the CMS experiment at LHC. Radiation hard sensors developed within FCAL are used as beam-loss monitors with excellent time resolution at FLASH and LHC. A design

for beam-loss monitors for XFEL is prepared. In addition, front-end ASICs are under development for the upgrade of the LHCb tracker.

3.7 Analog HCAL

3.7.1 Introduction

With the advent of silicon photo-multipliers (SiPMs), the scintillator tile technology became a candidate for highly granular particle flow calorimetry. With analogue read-out, energy and spatial resolution can be optimized independently. The particle flow performance is well understood; all published studies using Pandora are based on this technology.

The CALICE AHCAL was the first large LC hadron calorimeter prototype to be exposed to test beams. Analysis is nearly complete and mostly published; the results validate the technology and the simulations.

The development of engineering solutions for a realistic detector is on its way. The integration of read-out electronics and calibration system into the detector layers has been demonstrated. The next step, an integrated stack, is being prepared. In parallel, as improved photo-sensors become available from industry, the design of the basic read-out cell – the tile with SiPM – is optimized with regard to mass production procedures.

3.7.2 Recent Milestones

Past and present R&D: test beam data analysis

The following results using data taken the first AHCAL “physics” prototype in 2006 – 2011 at CERN and Fermilab have been published in peer-reviewed journals:

1. Detector construction, noise and ageing studies
2. Electromagnetic linearity and resolution
3. Hadronic linearity and resolution, software compensation
4. Test of particle flow algorithms (AHCAL with SiW ECAL)
5. Studies using a scintillator SiPM based tail catcher
6. Geant 4 validation with pion showers
7. Geant 4 validation with tungsten absorber (low energy)
8. Imaging capabilities, track segments

We consider all of them as critical for validating a given HCAL technology. Papers 6, 7 and 8 appeared in the last year since the ILC TDR was handed over.

Preliminary results have been made public in the form of CALICE analysis notes after intense internal reviewing on the following topics:

1. Combined performance SiW ECAL + AHCAL + Tail Catcher
2. Leakage estimation using shower topology
3. Time structure of showers in Fe and W
4. Geant 4 validation with protons
5. Parameterisation of pion and proton shower shapes
6. Geant 4 validation with tungsten absorber (high energy)

Notes 4, 5 and 6 appeared in the last year since the release of the ILC TDR. The studies are actively been followed up towards final publication; only the leakage study is presently uncovered due to lack of manpower.

Studies of the combined performance of the AHCAL in conjunction with the scintillator tungsten ECAL with MPPC readout are on-going. Results are expected in the coming year and will make the analysis of the first generation test beam data complete.

Data taking with a first, partially instrumented stack of the second generation has started at DESY and will continue in fall 2014 with electrons and hadrons at CERN. A framework for analysis software exists, but there is still a lot to do. In particular, calibration and correction procedures for timing measurements need to be developed.

The CALICE test beam results are nowadays the primary source of validation for hadron shower simulation, according to Geant 4 representatives, and extremely valuable for other HEP experiments, e.g. at the LHC, as well.

We finally note that test beam analysis plays an important role in training our students. Roughly speaking, each paper or note corresponds to one or several PhD theses. It is a distributed effort; the results have been obtained at DESY, CERN, MPI Munich, Hamburg, Heidelberg, Mainz and Wuppertal universities, ITEP Moscow and Northern Illinois University. Past and present R&D: technology 1. Optimisation of the scintillator SiPM read-out cell

As a consequence of the wide success of SiPM applications in other fields, e.g. in medical imaging, the development of improved sensors is dynamically pursued in industry, and several groups (ITEP, MEPhI, Shinshu, Hamburg) are in close contact with leading producers. Progress has been made in terms of dark rate, noise above MIP threshold and dynamic range. In addition, the samples are much more homogenous than at the time of the first prototype, which results in a simplification of commissioning and calibration procedures.

In the time since the TDR, tile SiPM cells without wave-length shifting fibre have been developed, following a design by MPI Munich. One is based on machined, individually wrapped scintillator plates (Hamburg), the other one on injection-moulded tiles (ITEP). Both are using sensors from KETEK, those on the moulded tile have a very large dynamic range. 300 devices have been produced and tested at ITEP, and more than thousand devices have been produced and tested with semi-automatic procedures at Hamburg and Heidelberg. Part of them has been integrated into the test beam set-up early this year. This version is a good candidate for a baseline design for a full detector, but more data taking and analysis is needed.

Industrialisation of the SiPM and tile design and production procedures is a long-standing item, but tests with industrial facilities such as automatic pick-and-place machines have begun only recently (Mainz). This needs to be continued in the coming years, fed back into the cell optimisation, and awaits a feasibility demonstration at larger scale.

An alternative design, with photo-sensors integrated in the read-out electronics board, has been proposed some time ago (Northern Illinois), but the detailed development of the corresponding sensor and scintillator configuration has only recently been taken up again (NIU, Mainz, ITEP). It has the potential to result in further simplifications (which should be read as cost and time savings), but poses higher performance requirements to the SiPM and raises new issues in the quality assurance and integration chain. The goal is to develop such an alternative solution in the next 2–3 years.

2. Electronics and active layer integration

The design of the active layers (DESY) with integrated read-out ASICs (LAL/OMEGA) and calibration system (Wuppertal) has been basically validated in beam tests of a single HCAL layer consisting of four base units (HBUs) at CERN in 2012 and reported in the TDR. An HBU reads 12×12 tiles with 4 ASICs. The present ASIC belongs to the 2nd generation ROC family used also in ECAL and SDHCAL. An HCAL layer carries interfaces for DAQ, calibration and power supply, which already have a compact design fulfilling space constraints at an ILC detector.

The main difference between the integrated electronics and that of the physics prototype is the self-triggered operation and on-detector zero-suppression, which implies much higher demands on controlling the noise behaviour and ensuring a stable detector response. It is thus mandatory to re-establish the calorimeter performance with a full-scale beam test. However, this is out of reach with present funding levels.

Further R&D in the next years has to be done both on the ASIC and on the PCB. For the ASIC, development of a 3rd generation ROC chip will start after fixing open issues with the 2nd generation (OMEGA). The 3rd will have a more robust slow control architecture and channel-wise buffer management which improves rate capabilities. In parallel, an alternative design of the analogue part (Heidelberg), which can handle a larger range of sensor gain needs to be complemented with a digital part.

The PCB with integrated photo-sensors, as counterpart of the corresponding tile design (see 1.), needs to be developed, taking automatic production and quality assurance into account. The PCB is also one of the main cost drivers of a particle flow HCAL. Dedicated R&D, in close cooperation with industrial manufacturers, is necessary to bring the cost down. First contacts have been made (DESY, Heidelberg, SKKU Korea).

3. System integration

While the integration of layers is well advanced, that of entire stacks or module has only begun. Since the TDR release, efforts concentrated on developing a multi-layer DAQ capable of reading larger systems (DESY, Mainz). An intermediate version has been used in an electron beam test of an 8 layer stack at DESY in early 2014.

Work has been intensified to further develop the DAQ towards a scalable system, with the goal to have it ready for beam tests at CERN starting in fall 2014. It involves integration of a dedicated module data concentrator, which collects signals from all

layers for sending them to the off-detector data receiver.

Further work will be required to integrate the HCAL DAQ into a higher level system for the purpose of combined beam tests, for example with a tracking device for uniformity studies, or with an ECAL for inter-calibration and combined performance. The same is true for slow control data.

A power supply system with optimised channel density per module is being developed at Dubna.

It has been demonstrated that temperature-induced variations of the SiPM gain can be compensated by adjusting the bias voltage (Prague, Bergen). The approach has the potential to stabilise the detector response and trigger efficiency and thus simplify operations significantly. Automatic procedures based on this principle need to be developed and implemented for a test at system level.

On the mechanical side, a cooling system needs to be developed. The ASICs integrated in the detector layers are power-pulsed and do not need active cooling, but the interfaces, in particular the power regulators, do. A simple solution for beam tests is on the way (DESY), but a leak-less under-pressure based system for a large detector still needs to be prototyped.

4. Infrastructure for production, quality assurance and characterisation

The AHCAL is probably the sub-detector with the largest number of individual components. While the number of electronics boards, layers and interfaces is similar to other ECAL or HCAL options, the large quantity of tiles and SiPMs deserves special attention. This affects production and quality assurance, but also characterisation, i.e. test bench measurements of parameters to be used later for calibration purposes.

While it would be premature to discuss building up full production infra-structure, conceptual solutions need to be developed and exercised using demonstrators, which could be seen as prototypes of future installations. The demonstration requires reasonably large samples of detector elements, in the order of 10000, as they would be needed for a next generation full prototype.

A semi-automatic test stand for SiPMs and tiles has been developed at Heidelberg and used for the elements of the early 2014 beam test. It needs to be adapted for future designs, e.g. with SiPMs integrated in the PCB.

Automatic assembly of HBUs (Mainz), i.e. of placing and soldering tiles and SiPMs on the PCB, needs to be demonstrated in practice, too. First encouraging tests with individual samples have been reported, but obviously only larger scale tests can validate the concept.

5. Absorber structure

The absorber structure bears more challenges than conventional hadronic calorimeters. Due to the much finer longitudinal segmentation and the imperative to minimise the total radius inside the coil, there are many active gaps with tight tolerances. A design has been developed and prototyped, which achieves the required tolerances with a cost-effective roller-levelling process without machining off excess material (DESY). Two test structures have been built; one covers the full transverse cross section of a barrel module, the other the full lateral extension. The cassettes (DESY, MPI Munich) housing the active elements have the final design and are used in beam tests.

These structures need to be investigated with respect to their robustness against earthquakes (DESY). Simulations of the whole ILD structure have been initiated, and

measurements on the test structures exposed to accelerating forces should be done.

As enough active elements become available for instrumenting several active layers at full size, the thermal simulations should be verified with measurements, too.

3.7.3 Summary

The AHCAL effort has produced a number of significant results in the time since the ILC TDR:

- Publication of 3 journal papers and 3 preliminary results in the form of internally reviewed notes, on Geant 4 validation with pions and protons in steel and tungsten, including new observables like track segments
- Development, production and beam test of a new, simplified tile SiPM system without wave-length shifting fibres and improved sensor performance
- Test with electron beams of a small stack with second generation electronics and DAQ in a realistic absorber structure

The AHCAL is ready to make the next step towards a realistic full-scale prototype and a technical design report. In order to achieve this, coordinated R&D is required in the following areas:

Software and analysis:

- Completion of physics prototype test beam analysis
- 2nd generation prototype reconstruction and simulation software
- Development of timing reconstruction
- Analysis of 2nd generation test beam data

Tile SiPM system:

- Development of scintillator SiPM system with SiPM on the PCB
- Development of associated assembly, quality assurance and characterisation procedures
- Development of associated PCB

Electronics:

- 3rd generation ASIC of ROC family
- ASIC for larger range of SiPM gains
- PCB cost optimisation

System integration:

- Scalable DAQ

- Module level data collector
- Integration of DAQ and slow control into higher level system
- Implementation of temperature compensation scheme
- Power supply system
- Cooling system

Mass production concepts:

- Semi-automatic test stands
- Automatic placement and soldering of tiles and SiPMs

Absorber structure:

- Earthquake stability calculations and tests
- Thermal tests with full-scale instrumented and powered structures

There are ample opportunities for new groups to join into any of these fields, depending on the special competences they wish to contribute.

Particular engineering challenges are

- Assess and ensure earthquake stability of the absorber structure whilst maintaining a minimum of dead material
- Developing an active layer element consisting of tiles, SiPMs and readout electronics that can be automatically assembled, including production and quality assurance procedures

3.7.4 Engineering Challenges

3.7.5 Future Plans

3.8 SDHCAL

3.8.1 Introduction

The Micromegas R&D pursued at LAPP is primarily intended for Particle Flow calorimetry at future linear colliders. It focuses on hadron calorimetry with large-area Micromegas segmented in very small readout cells of $1 \times 1 \text{ cm}^2$. This granularity provides unprecedented imaging capability which can be exploited to improve the measurement of jet energy. Past and current R&D efforts are described with emphasis on achievements since the publication of the ILC Detailed Baseline Design.

3.8.2 Hadron calorimeter design

The design of calorimeters at a future linear collider is optimised for the reconstruction of jets with a Particle Flow method. The SiD HCAL will be segmented in cells of $1 \times 1 \text{ cm}^2$. With a total instrumented area of 3000 m^2 , the number of readout channels will reach 30×10^6 . This unprecedented granularity can be achieved with gas detectors, thin PCBs and embedded front-end ASICs.

In addition, calorimeters will be placed inside the solenoid magnet to insure good matching of electron and charged hadron tracks with their energy deposits in the ECAL and HCAL. To limit cost, a very compact mechanical design is mandatory: e.g. the SiD HCAL would feature 40 layers within $\sim 110 \text{ cm}$. This design relies on very thin active layers to achieve fine sampling ($\sim 0.1 \lambda_{\text{int}} / \text{layer}$) and good hadron energy resolution ($\sim 50\% / \sqrt{E}$). The targeted active layer thickness and length in the barrel HCAL modules are 8 mm and 3 m respectively. To minimise dead zones, readout boards will be placed at the two ends of the barrel modules. Along the beam direction, ASIC will be daisy chained and PCBs connected together with flat connectors and cables.

Active cooling of the active layers is extremely challenging with this design. Instead, it is considered to limit heat dissipation and gradients inside the calorimeters by power-pulsing the front-end circuitry. Power-pulsing is possible because of the particular time structure of the ILC beam. This structure also drives the design of the ASICs which will be self-triggered. During collisions, signals will be processed and stored in memory with a timestamp synchronous to the ILC clock. Between bunch trains, memories are first read out, then the ASIC are turned off. With an ILC duty-cycle of 0.5%, the power consumption can be reduced down to $10 \mu\text{W} / \text{channel}$.

3.8.3 Recent Milestones

The SDHCAL

The SDHCAL is a prototype of imaging hadron calorimeter equipped with 50 layers of gaseous detectors of $1 \times 1 \text{ m}^2$ interleaved by steel absorbers (Figure 3.8 (left)). Each detector is segmented in pads of $1 \times 1 \text{ cm}^2$ and the processed pad signal is coded over 2-bits (Figure 3.8 (right)). The number of readout channels per layer imposes to integrate the front-end electronics directly on the gaseous detector printed-circuit-boards (PCB). Several CALICE groups are involved in this project. The LAPP group developed technologically advanced Micromegas prototypes in view of test in the SDHCAL. It also took responsibility of part of the data acquisition system (DAQ).

The $1 \times 1 \text{ m}^2$ Micromegas prototype

Mechanics The Micromegas layers for the SDHCAL are made out of 6 high-voltage units installed together inside a gaseous chamber (Figure 3.9 (right)). Each unit is an 8 layer PCB with a Bulk Micromegas mesh, readout pads and front-end ASICs; it is dubbed Active Sensor Unit (or ASU). A drift gap of 3 mm is defined by spacers and a frame. Spacers are inserted in between ASUs, resulting in an inactive area of 2%.

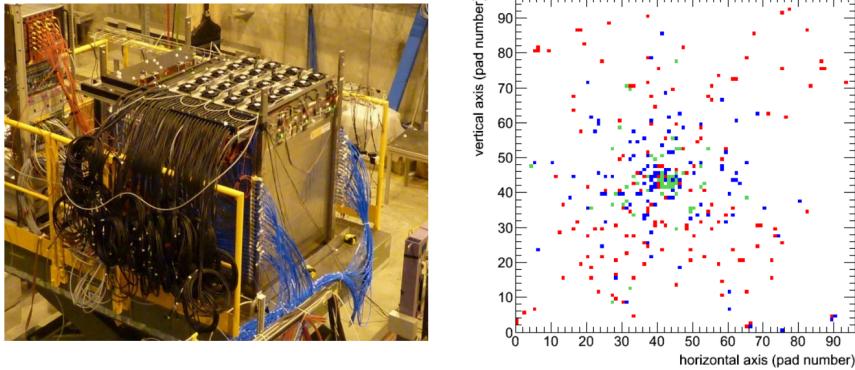


Figure 3.8: SDHCAL prototype in a beam line at the SPS at CERN (left). Event display of a 150 GeV pion shower measured in a Micromegas prototype after $2 \lambda_{\text{int}}$ of steel (right), the color indicates the threshold passed: red for 1, blue for 2 and green for 3.

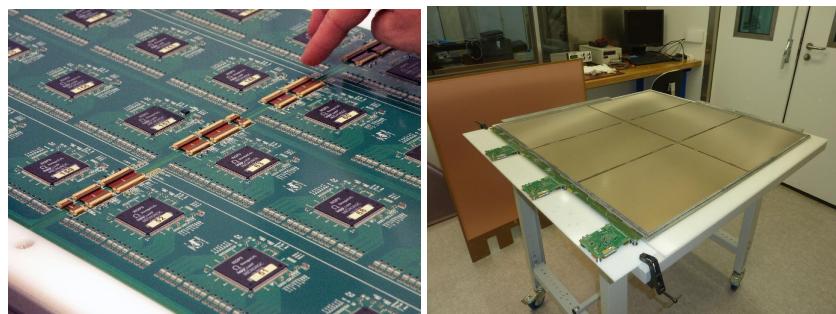


Figure 3.9: Photographs of interconnections between 2 Active Sensor Units (left) and a $1 \times 1 \text{ m}^2$ Micromegas prototype during assembly showing 6 of these units and a drift cover (right).

Electronics Electronics connections to the DAQ as well as services (power cables, gas pipes) are provided on one side of the prototype. ASU-to-ASU connections are therefore mandatory and are made with dedicated connectors and flexible cables (Figure 3.9 (left)). They are used to distribute clocks and supply power to the ASICs, high voltage to the meshes, to configure the ASICs and read out data. Prior to assembly, 4 ASUs were chained and functional electronic tests were successfully performed. These key features make the design of the $1 \times 1 \text{ m}^2$ Micromegas prototype fully scalable to the required size of a HCAL module at a future LC (at most 2 m in the SiD detector concept).

Noise and detection efficiency A few prototypes were constructed [63] and extensively tested in beam at CERN [64]. Noise conditions were excellent both during standalone tests and inside the CALICE SDHCAL. ASIC thresholds can be lowered down to about 20% of a minimum ionising particle (MIP) signal at a typical running gas gain of 1500. Efficiency in excess of 95% are easily reached while keeping a pad multiplicity below 1.1 for MIPs. The actual charge threshold is as low as 1–2 fC; it is achieved on ASIC test-boards as well as once mounted on ASUs. The contribution of the PCB internal capacitances to the overall detector noise is therefore negligible.

Standalone performance Thanks to a precise control of the gas gaps and electronics settings, ASIC-to-ASIC variations of efficiency are below the percent in all tested prototypes. Although the statistics is low, the construction process seems reproducible. Stability with rate in high-energy hadron showers is excellent. Except occasional sparks, no effect of beam rate was observed on the pion response up to roughly 30 kHz beam rate; which was the highest rate during the tests. The measured spark probability lies in the range of $10^{-6} \dots 10^{-5}$ per showering pion at a running gas gain of 1500.

Resistive prototypes

While the Bulk Micromegas mesh is made of steel wires and is very resistant to sparking, sensitive front-end ASICs can suffer irreversible damage. Protections in the form of current-limiting diodes networks soldered on PCB were proved so far efficient. To simplify the PCB design and possibly reduce the overall detector cost, it is however desirable to get rid of diodes. It is well known that sparks can be suppressed by means of resistive coatings on the anode pad plane. This solution is used with great success in tracking detectors. Because it modifies the signal development, it needs some adaptation to calorimetry so as to preserve linearity and keep a narrow pad response function for Particle Flow reconstruction.

First resistive designs using resistive strips and pads were implemented on small size prototypes. In a mixture of Ar/CO₂, full suppression of sparking was demonstrated up to gas gain in excess of 10^4 . At comparable gas gains, resistive and non-resistive prototypes show similar response to traversing charged particles, reaching high efficiency and low pad multiplicity. Compared to non-resistive ones, the evacuation of charge is slowed down in resistive prototypes which are thus subject to rate-dependent drops of gas gain. Expected efficiency losses have been observed at

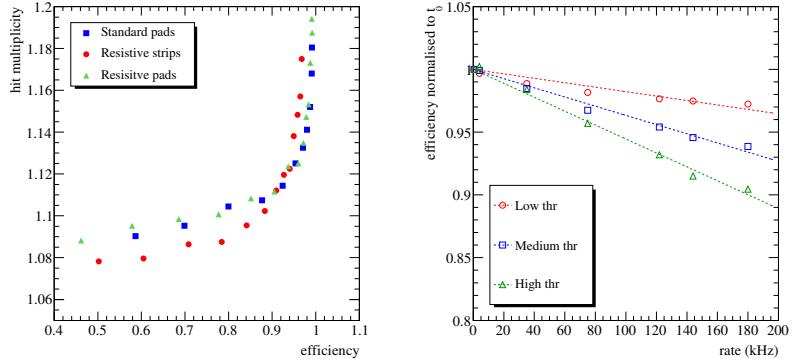


Figure 3.10: Pad multiplicity versus efficiency to 3 GeV electrons for 2 resistive and 1 non-resistive (or standard) Micromegas prototypes (left). Efficiency dependence on rate in a resistive prototype for 3 values of threshold (right). The electron beam spot is $\sim 2 \times 2 \text{ cm}^2$.

(3 GeV electrons) rates in excess of 10 kHz/cm^2 . This limit is compatible with the resistivity of the coated material. At lower rates, it could be shown that the linearity of a Micromegas calorimeter to electrons is not affected by the resistive coatings, up to 5 GeV, which was the maximum energy available during the testbeam campaign.

3.8.4 Engineering Challenges

3.8.5 Detector R&D plans for the coming years

Plans for the coming years include maintaining a commitment to linear collider detector R&D and possibly seek new applications. Despite a decline of resources, an R&D program to optimise resistive Micromegas for calorimetry is established. Linearity, rate capability and spark protection in dense electromagnetic showers will be checked up to high-energy and for detector designs with a large variety of resistivity and geometry. These measurements will be necessary to validate the resistive Micromegas technology for calorimetry at a future LC. Also, the on-going R&D for high-luminosity LHC (HL-LHC) detector upgrades are an appealing perspective to the LAPP group. In particular, the possibility to equip the backing part of the CMS forward calorimeter is being investigated. Such high-rate application will put strong stability constraints on resistive Micromegas, making the optimisation work mentioned above even more relevant.

On a longer term and if resources are sufficient, a Micromegas calorimeter prototype should be constructed so its performance can be compared to concurrent detector technologies. Some performance have already been studied with Monte Carlo simulation, the minimal prototype dimensions are known as well as its cost. This final step of the project naturally comes after optimisation of the resistive coating and would complete the R&D on Micromegas calorimetry.

3.8.6 Applications Outside of Linear Colliders

3.9 DualReadout

3.9.1 Introduction

The scientific goal of RD52 (previously the DREAM collaboration) is to understand the fundamental limitations to hadronic energy resolution and, in general, the limitations to achieving high-quality calorimetric performance in Gaussian energy resolution, mean response linearity, and ease and precision of calibration.

3.9.2 Recent Milestones

The essential features of our fiber dual-readout calorimeters are (a) near-perfect optical conduits (fibers) for read-out, (b) fine spatial sampling on the mm-scale, (c) dual measurement of scintillation light in scintillating fibers (all charged particles) and simultaneous Cerenkov light in clear fibers (only electromagnetic particles), (d) absolute fiber-absorber volume uniformity, and (e) low-noise readout with PMTs below 100 MeV per ton of calorimeter. This design achieves a Gaussian response, a linearity near 1% from 20-300 GeV, and excellent energy resolution. The calibration is by a direct electron beam into each calorimeter tower.

About 30 dual-readout papers are published in Nucl. Intrs. Meths., Rev. Sci. Instr., and JINST, including dual-readout in several crystals, a planar geometry, as well as fibers in several geometries. We have built and tested Pb-based and Cu-based dual-readout modules and are designing a W-based test module. Typical readout of the Pb-modules is shown in Figure 3.12 for 20, 60, and 100 GeV pion beams in the H8 beam of the North Area at CERN. Simple dual-readout yields a Gaussian and linear response, currently limited by lateral leakage fluctuations in the Pb-based modules of about 1 tonne. The record holder for linear, Gaussian energy resolution is still the SPACAL module of 20 years ago, built by Wigmans at CERN to demonstrate the newly understood concept of “compensation”. SPACAL was a Pb-scintillating fiber module of mass 20 tonnes that collected scintillation light for 100-200 ns to achieve compensation from the $np \rightarrow np$ recoils in the scintillating fibers. We show in Fig. 2 the hadronic energy resolutions for single pions for SPACAL, DREAM, and the new RD52 modules, plotted vs. $1/\sqrt{E}$, so that the slope is the stochastic term and the intercept is the constant term. A calorimeter with the ILC goal for hadronic energy resolution of $\sigma/E = 30\%/\sqrt{E}$ is shown as the thin red line. We have not yet achieved this goal, but we know we are limited merely by lateral leakage fluctuations which can be suppressed by a larger module. As shown in Fig. 2 we are closing in. There are several improvements over the results in Figure 3.13 for (a) Cerenkov photoelectron yield, (b) photocathode efficiency, (c) fiber quality, (d) optical uniformity and, finally, (e) absorber mass. All of these are planned for testing one year from now at CERN. We expect, based on our data, simulations, and our understanding, that we are likely to achieve a resolution of about $30\%/\sqrt{E}$ with a small constant term. This would result in 3% energy resolution at 100 GeV and about 2% energy resolution at the highest SPS beam energies available at CERN.

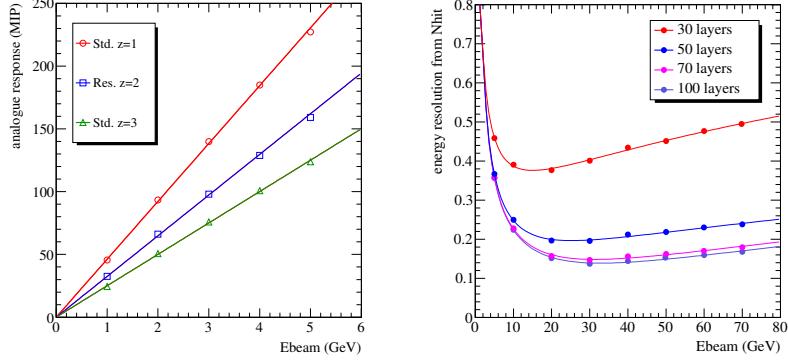


Figure 3.11: Electron response of a virtual Micromegas SDHCAL deduced from measurements of longitudinal shower profiles in non-resistive ($z=1$ and $z=3$) and resistive ($z=2$) Micromegas prototypes placed behind increasing thicknesses of passive material (left). Geant4 calculation of the energy resolution to pions of a Micromegas DHCAL of 30 to 100 layers based on simple hit counting (right).

Hadron detection with a dual-readout calorimeter

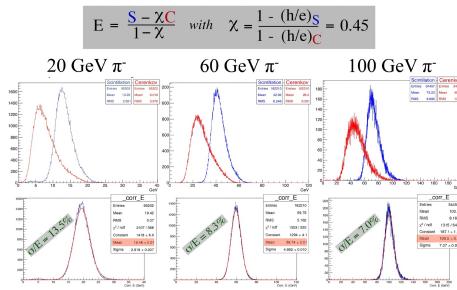


Figure 3.12: Raw scintillation and Cerenkov data for 20, 60, and 100 GeV pion beam, and the dual readout response below

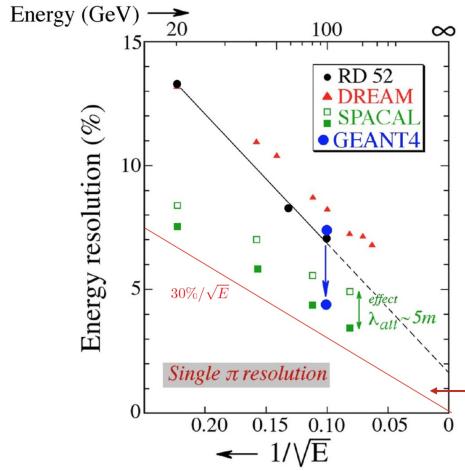


Figure 3.13: Hadronic energy resolution for SPACAL, DREAM, and RD52 modules

3.9.3 Engineering Challenges

Manufacturing of the high-precision absorber, whether Pb or Cu or W. Assembly of a large calorimeter involves a lot of fibers which can and must be automated. Control of the optics to 1% is a challenge. It should be emphasized that we do not have engineers working on RD52, but rather find simple solutions which achieve the physics goals without expending large funds. On a construction project, engineering design would improve all our results.

3.9.4 Future Plans

Solving the problems of projective geometry; implementation of SiPM readout; manufacture of a tungsten W-absorber with full dual-readout capability; test of a gaseous dual-readout calorimeter.

3.9.5 Applications Outside of Linear Colliders

High precision calorimetry is vital to many experiments, both collider and fixed target; dual-readout is considered for a space station experiment; and, a high-precision dual-readout calorimeter is being considered for an electron-ion col- lider.

3.9.6 References

Complete papers, figures, proposals, status reports, and photos are accessible at our website: <http://highenergy.phys.ttu.edu/dream/>.

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