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1.2 ChronoPix

1.2.1 Collaborating Institutions

The chronopixel sensor is been developed in the collaboration of the University of Oregon and Yale University. The silicon sensor engineering is performed by Sarnoff Corporation under contract with the two Universities.

1.2.2 Introduction

The chronopixel is the monolithic CMOS pixelated sensor with the ability to record time stamp of pixel crossing by charge particles in the pixel memory. Each pixel contains 2 memory cells (12 bits each), and can record 2 time stamps happening during the same bunch train. This information is read out in the time interval between bunch trains. Chronopixel option for ILC vertex detector was described in the ILC DBD. By the time of the DBD, 2 prototypes were built and tested, and summary of test results were also presented in the DBD. They are listed below:

- We have proven that we can record time stamps in every pixel with time resolution better than 300 ns (we have tested it down to 150 ns).
- We have tested sparse readout, allowing to read only pixels with hits, thus reducing readout time to the level allowing readout of all pixels in the sensor in the intervals between bunch crossings.
- We have tested pulsed power for analog part of the pixels and have proven that turning power ON in about 100 μs before bunch train and turning it off between bunch trains does not create any problems for threshold setting accuracy in the comparators.
- We have tested the idea of building all in-pixel electronics only from NMOS transistors, thus eliminating the need for special process (deep p-well) to protect signal charge from parasitical collection by in-pixel transistors. We have proven that all NMOS electronics can be built in this way, and that this does not significantly increase the power consumption compared to CMOS electronics.
- We have tested compensation of comparator offsets using analog calibration, when the value of the offset is stored as a voltage on the capacitor in each pixel. This have advantage over digital calibration (value of offset is stored as code in the special register) in that there are no discrete levels, and accuracy of such a calibration scheme is not affected by the size of such a register and the spread of the initial offsets.

1.2.3 Recent Milestones

- Test of prototype 2 revealed some problems. Possible solutions for these problems were discussed with Sarnoff engineers.
- New contract with Sarnoff for the design of prototype3 was signed in August 2013.
- The submission of prototype 3 to foundry for manufacturing is expected by the end of April 2014.

The most recent report on chronopixel status was presented by N.Sinev at LCWS13 on November 2013 at Tokyo

1.2.4 Engineering Challenges

- Achieving low capacitance of sensor diode in 65 nm and smaller feature size process. Following standard design rules for such process led to much higher than hoped for diode capacitance. There seems to be solution for this problem (using non-standard âĂIJnative diodeâĂİ from design library). But that need to be checked, and this is the main goal of the 3rd prototype.

- If low value of sensor diode capacitance will be achieved, the signal/noise ratio will improve. However, lower value of this capacitance will make it more sensitive to cross-talks through capacitive coupling. Reducing such coupling can be a challenge.

- Transition from small prototypes (few mm^2) to real ILC detector size ($10\,cm^2$) may meet additional problems. One of them will be effect of Lorentz forces on the power supply buses, especially in the case of pulsing power. Pulsing power is the only way to achieve acceptable power dissipation in the vertex detector. However, it will generate varying Lorentz forces, acting on power supply lines. This may produce vibrations, which are unacceptable for required spatial resolution of the detector.

1.2.5 Main directions of the R&D for the next 5 years

- Achieve signal/noise ratio required for close to 100% signal registration efficiency. So far we got a signal/noise of around 10 in prototype 2, and we would like at least 20. We know a few ways to improve it - increasing epitaxial layer thickness, increasing epitaxial layer resistivity, or reducing sensor capacitance. The most attractive would be reducing sensor capacitance, as it does not require special process, however there are some problems to be solved with this approach.

- Achieve required pixel size (prototype 3 will have 25 µm pixels, we would eventually like 15 µm). It may require going to technology with feature size less than 65 nm. There seems to be no problems in that, but both - good signal/noise and pixel size requirements may be challenging.

- Achieve acceptable level of inter-pixel and digital to analog circuit cross talks and parasitic feed backs.

- Depending on available funding, try to build complete sensor with large enough area and full feature readout.

1.2.6 Applications Outside of Linear Colliders

With some modifications (for example, adding time-time convertor) Chronopixel architecture can be applied for any experiment requiring time stamping of individual hits - it may be HL-LHC, CLIC and so on.

1.3 FPCCD

1.3.1 Collaborating Institutions

The following institutes are participating in this project:

- KEK, High Energy Accelerator Research Organization
- Tohoku University
- Shinshu University
- JAXA, Japan Aerospace Exploration Agency

1.3.2 Introduction

Fine pixel CCD (FPCCD) is one of the candidate sensor options for the vertex detector of ILD detector at ILC. In the present design, FPCCD sensors for the innermost layer of the vertex detector have the pixel size of 5 μm and the fully depleted epitaxial layer with a thickness of 15 μm. Because of the small size of the pixels, the pixel occupancy is acceptably low even if the hits are accumulated for one bunch train (1 ms). The efforts of the FPCCD collaboration are currently focused on pixel characterization and development, while we also pursue developments to the cooling system (led by KEK), electronics downstream of ASICs (led by Shinshu University) and the reconstruction software (led by Tohoku University).

1.3.3 Recent Milestones

R&D activity for the FPCCD vertex detector at present is mainly focused on FPCCD sensors and a detector cooling system using 2-phase CO_2. One of the achievements of FPCCD sensors after DBD is the fabrication of real size ($12.3 \times 62.4\,m^2$) sensors with 50 μm total thickness. Figure 1 shows the real size prototype sensor. It has 8 readout nodes, and each channel has different pixel sizes of 12 μm, 8 μm, and 6 μm. We have started neutron damage test using small (6 mm × 6 mm) FPCCD prototypes [1]. A prototype sensor was irradiated by a neutron beam of few tens of MeV at CYRIC in Tohoku University. Detailed analysis on the irradiated sensor is still on-going. In order to increase the radiation immunity of FPCCD sensors, particularly to reduce the transfer inefficiency due to radiation damage, the sensors should be cooled down to -40 °C. We have started R&D on two-phase CO_2 cooling system for this purpose. There are several examples of utilizing two-phase CO_2 cooling system for high energy physics experiments. For these cases, the CO_2 coolant is circulated using liquid pumps. This method is, however, not so efficient for very low temperature cooling of -40 °C. Therefore, we adopted CO_2 gas compressor for the circulation of CO_2 coolant. Figure 2 shows a simplified schematic diagram of the system. A prototype system has been constructed, and cooling between -40 °C and +15 °C has been successfully demonstrated using this system.

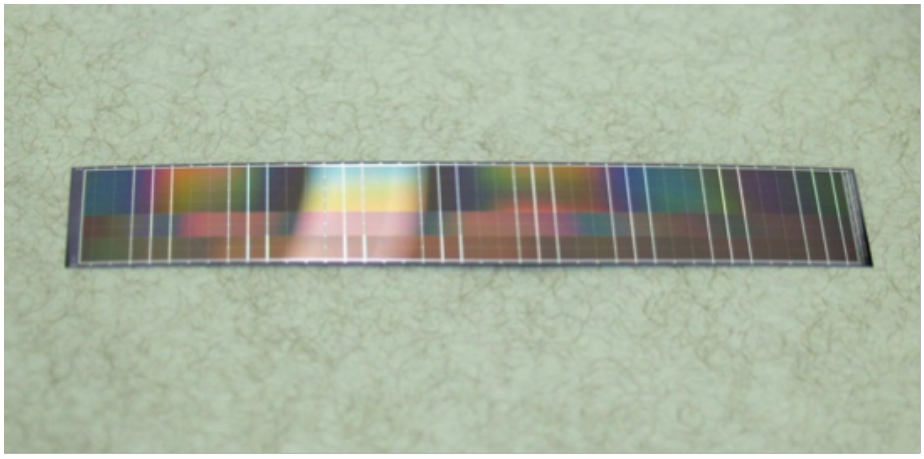

Figure 1: Real size FPCCD sensor thinned down to 50 µm

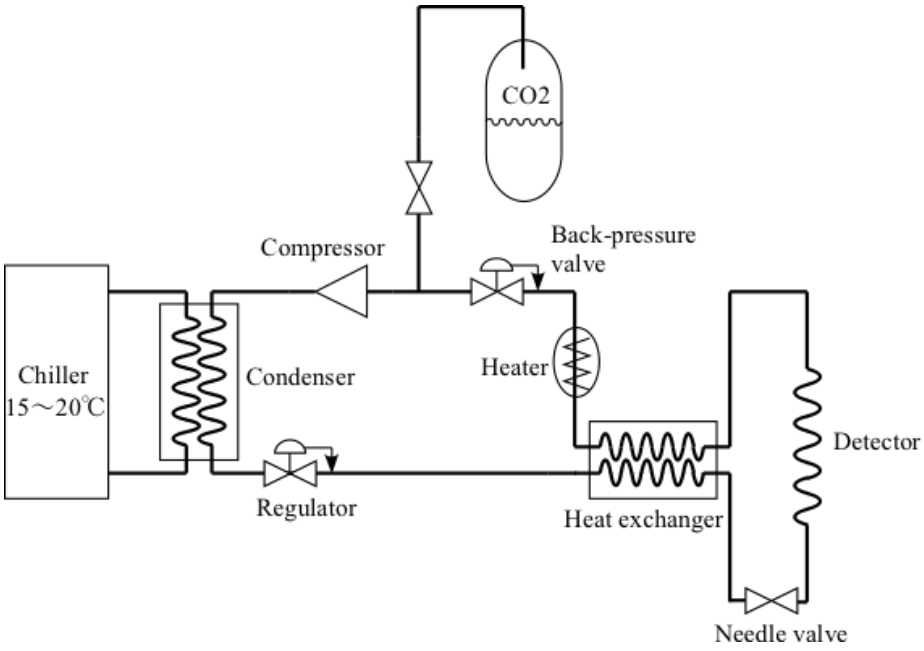

Figure 2: A simplified schematic diagram of the two-phase CO_2 cooling system

1.3.4 Engineering Challenges

In the present design of ILD vertex detector, two sensor layers are mounted on both sides of a light-weight ladder of 2 mm thick. Our goal of the material budget of this ladder is 0.3% X0/ladder = 0.15% X0/layer. This goal would not be so easy, and we need a lot of R&D effort. The ladders have to be cooled down to -40 °C. We plan to achieve this cooling by heat conduction to the end-plate on which thin cooling tubes for 2-phase CO_2 are attached. The design of this structure is not trivial, and we need R&D including thermal simulation. There are challenges both in mechanical structure and in electronics circuit for the ladder R&D. We have not started this effort yet.

1.3.5 Future Plans

We have been doing our R&D on the FPCCD vertex detector based on a Grant-in-aid for science research which expires at the end of FY2015. By that time, we plan to carry out the following R&D items:

- Characterization of FPCCD sensors including beam tests and radiation damage tests
- Development of FPCCD sensors with the pixel size of 5 μm, which is our ultimate goal
- Construction of prototype ladders for inner layers
- Development of readout electronics downstream of ASICs

If new funding is secured in future, the following R&D items have to be done:

- Development of larger FPCCD sensors and prototype ladders for outer layers
- Development of readout electronics which can fit in the small space of real experiment
- Construction of real size engineering prototype and its cooling test

1.3.6 Applications Outside of Linear Colliders

Because of the relatively slow readout speed, application of FPCCD sensors to other high energy physics would be limited. However, high spatial resolution of small pixel size must be applicable to measurements of X-ray imaging in material science. Two-phase CO_2 cooling system can be applied to any other detectors which require efficient cooling between -40 °C and near room temperature. Our system, which uses a CO_2 gas compressor, has great advantage for low temperature operation near -40 °C compared with systems using liquid pumps for circulation.

1.4 CMOS

1.4.1 Collaborating Institutions

1.4.2 Introduction

1.4.3 Recent Milestones

1.4.4 Engineering Challenges

1.4.5 Future Plans

1.4.6 Applications Outside of Linear Colliders

1.5 CLICPix

1.5.1 Collaborating Institutions

- CERN
- Spanish network for Future Linear Colliders
- University of Liverpool
- Institute of Space Science, Bucharest
- University of Bristol

The University of Glasgow and the University of Oxford also intend to be involved, but they have not yet contributed.

1.5.2 Introduction

To achieve the physics goals of flavour tagging at CLIC, a vertex pixel detector with high spatial precision (3 um single-point resolution), 10 ns time stamping and ultra-low mass (0.2% X0 per detection layer) will be required.

1.5.3 Recent Milestones

- Development of the CLICpix hybrid pixel readout ASIC with 25 µm pitch, analog readout, time stamping, and power-pulsing functionality, implemented in 65 nm CMOS technology
- Development of ultra-thin (50 um) planar pixel sensors, as well as active sensors with capacitive coupling
- Low-mass fine-pitch interconnects between sensor and ASIC
- Through-silicon via technology for powering, configuration and readout of the ASIC
- Low-mass powering infrastructure, including power-pulsing with local energy storage

- Low-mass carbon-fibre supports
- Detector cooling based on forced air-flow
- Concepts for mechanical integration and detector assembly
- Detector layout optimisation studies

1.5.4 Engineering Challenges

1.6 3D Pixel Development

1.6.1 Collaborating Institutions

- Brown University
- Cornell University
- Fermilab
- Northern Illinois University
- SLAC
- University of Illinois Chicago

1.6.2 Introduction

This R&D area covers sensors and electronics integrated utilizing 3-dimensional electronics technology. This technology is distinct from 3D sensors and builds on efforts in the electronics industry to stack multiple layers of electronics to form dense assemblies of complex devices. It is important for Particle Physics in that it allows very fine pitch (4 μm) integration of sensors with multiple layers of electronics, allows interconnection to both the top and bottom of devices, and provides techniques for low mass, thinned devices. The interconnection of top and bottom means that sensors can be bonded to complex electronics with no wasted area for interconnect and optimal delivery of power and ground.

1.6.3 Recent Milestones

Major R&D efforts and recent developments since ILC DBD (with publications/references to major results) We have completed our multi-year effort to demonstrate commercial 3D technology. This consists of two tiers of 0.13 μm CMOS interconnected with Direct Oxide Bonding (DBI) technology and access using Through-Silicon-Vias (TSV). The DBI bonds are at 4 μm pitch. Fermilab sponsored the first 3D multiproject run for Particle Physics. The wafers were delivered last summer. Fermilab had three chips on the run VICTR – a CMS track trigger chip, VIPIC – an X-ray imaging chip, and VIP – an ILC vertex chip. Test of the VIPIC and VICTR have shown working devices. Tests for the VIP chip were delayed due to lack of funding and personnel. We have recently

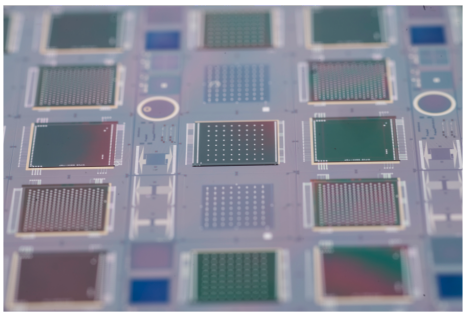

Figure 3: 3D chips placed on BNL sensor wafers. VIP is middle left and right

restarted this work and initial tests are promising with the readout token successfully passed through the VIP.

In addition to the development of the 3D chips we have also explored the use of DBI to connect the 3D electronics with sensors. Brookhaven Laboratory fabricated a sensor wafer with regions that mate to the VIP, VIPIC and VICTR chips. The chips are ground to expose the top TSVs and contacts are deposited. The assembly is then attached to a handle wafer and the TSVs which project from the other side are exposed. Wafers are then process for DBI bonding and individual die from the 3D wafer are bonded to the sensor wafer. Finally the top "handle" silicon is ground and etched to reveal the previously formed contacts. The total thickness of the readout at the end of this process is about 25 µm (Figure 3). These wafers were received at the end of March 2014 and are being tested.

Due to the fact that contacts to a 3D assembly can be made to the body of the die, rather than its edge space usually reserved for wirebond contacts at the edge can be eliminated. This raises the possibility of fabricating large, complex pixel detectors of arrays of 4-side butted devices using sensors with active edges. We are in the process of demonstrating this technology utilizing active edge sensors fabricated at VTT and using wafer-to-wafer bonding to a 3D readout wafer. The active edge wafers are based on a silicon-on-insulator stack and thus can be fabricated with essentially arbitrarily thin sensors, in this case 200 µm. Sensor and dummy readout wafers have been fabricated and a test wafer is being etched at SLAC. We expect to have DBI bonded assemblies this summer.

1.6.4 Engineering Challenges

Major engineering challenges include:

- Development of widely commercially available 3D technologies. Based partly on our development the silicon brokers CMP, CMC, and MOSIS now include 3D multiproject runs as part of their standard offerings.
- Development of high yield 3D bonded chip-to-wafer devices. This is the subject of our active edge project.

- This development shares with other vertexing technologies the problems of low mass mechanical support, power delivery, and cooling. An SOI-based device can be made thin without special effort. Such thinned devics will need low mass backing hybrid circuitry, presumably flex on carbon fiber or a similar technology

1.6.5 Future Plans

- Complete the 3D active edge project
- Apply our concepts to x-ray imaging devices
- ILC developments would await renewed funding in the US.

1.6.6 Applications outside of Linear Colliders

As stated above the technology is already being developed for CMS and x-ray imaging applications. The large area sensor concept is applicable for a variety of focal plane array concepts.

1.6.7 References

1. Results of Tests of Three-Dimensionally Integrated Chips Bonded to Sensors By Grzegorz W. Deptuch, Gabriella Carini, Terence Collier, Pawel GryboÅŻ, Piotr Kmon, Ronald Lipton, Piotr Maj, Marcel Trimpl et al.. Submitted to: IEEE Trans.Nucl.Sci.. 2. Recent Results for 3D Pixel Integrated Circuits using Copper-Copper and Oxide-Oxide Bonding By R. Yarema, G. Deptuch, R. Lipton. Submitted to: Proceedings of Science. 3. Tests of the First Three-Dimensionally Integrated Chip for Photon Science By P. Maj, G. Carini, G. Deptuch, P. Grybos, P. Kmon, D.P. Siddons, R. Szczygiel, M. Trimpl et al..m PoS Vertex2012 (2013) 027. 4. 3D Technologies for Large Area Trackers By G. Deptuch, U. Heintz, M. Johnson, C. Kenney, R. Lipton, M. Narian, S. Parker, A. Shenai et al.. arXiv:1307.4301. 5. Combining the two 3Ds By R. Lipton, G. Deptuch, U. Heintz, M. Johnson, C. Kenney, M. Narian, S. Parker, I. Planell-Mendez et al.. 10.1088/1748-0221/7/12/C12010. JINST 7 (2012) C12010. 6. Vertically Integrated Circuit Development at Fermilab for Detectors By R. Yarema, G. Deptuch, J. Hoff, F. Khalid, R. Lipton, A. Shenai, M. Trimpl, T. Zimmerman. 10.1088/1748-0221/8/01/C01052. JINST 8 (2013) C01052.

1.7 SOI

1.7.1 Collaborating Institutions

KEK

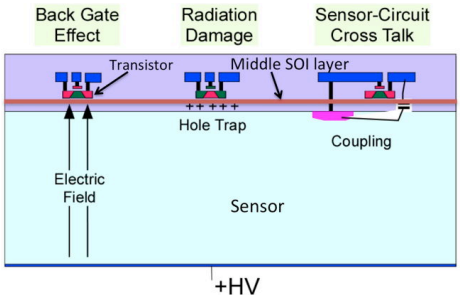

Figure 4: Major issues in the SOI pixel detector and introduction of a middle-SOI layer

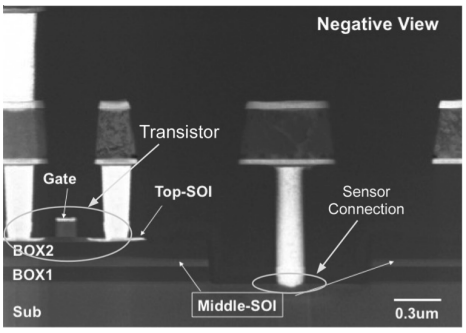

Figure 5: Cross section of the double SOI chip after processing

1.7.2 Introduction

1.7.3 Recent Milestones

At present, major issues in the SOI pixel development are “back-gate effect”, “hole trap under the transistors by radiation,” and “sensor-circuit cross talks” as shown in Figure 4. For these, we have been developing a double SOI technology. The developed double SOI wafer has an additional middle-SOI(Si) layer under the transistors. The conduction layer of the middle-SOI can solve all the three issues. We could successfully process the double-SOI wafer (Figure 5). Threshold shift by radiations is successfully recovered by applying compensating voltage to the middle SOI layer (Figure 6).

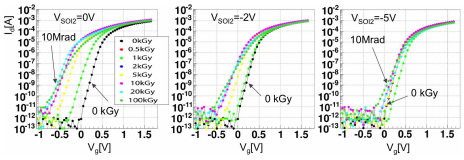

Figure 6: Threshold shift recovery by applying compensating voltage (Vsoi2) to the middle Si layer

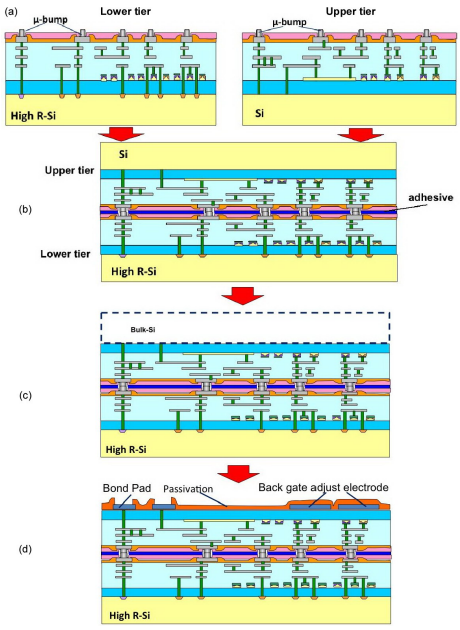

Figure 7: Micro-bump 3D integration process flow of the SOI pixel

1.7.4 Engineering Challenges

The resolution for the ILC vertex detector is required as better as a few μm. This means pixel size must be less than 20 μm square or so. On the other hand, each pixel must register arrival time of the hits during bunch train etc., so this requires many transistors and capacitors must be located in each pixel area. Natural solution to this is 3D vertical integration of circuit layer. SOI technology is very fit to the 3D integration since the thinning is stopped at the buried oxide (BOX). We already tried 3D SOI pixel chip in collaboration with T-Micro Co. Ltd. Process flow of micro-bump 3D connection is shown in Figure 7. We have confirmed low resistance (6 Ω/bump) between upper and lower tiers for 1,000 daisy chain (2,000 bumps) as show in Figure 8. However, we think much higher density digital circuit such as 32 nm technology may be necessary for the upper tier in the ILC. This requires bonding of two different technology wafers. The 3D integration of different technology wafers (or chips) is still engineering challenge.

1.7.5 Future Plans

Detector R&D plans for the coming years; We are planning following items for the coming year.

- Sep. 2014 : Complete architecture study for the ILC pixel detector.
- Mar. 2015 : Design and fabrication of first test chip for the ILC.

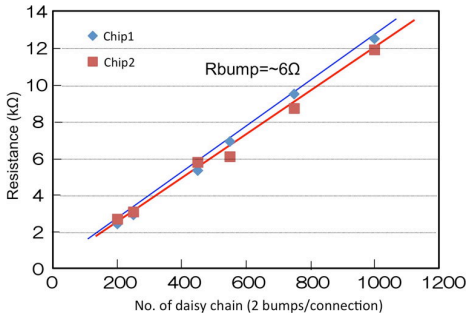

Figure 8: Resistance of micro-bump daisy chain between upper and lower tiers

- Dec. 2015 : Beam test of the test chip.

2 Tracking Detectors

2.1 SCIPP Tracking R&D

SCIPP has been involved in Linear Collider tracking R&D for a number of years, and its work has led to the development of a refined understanding of several generic tracking issues with potential applications for Linear Collider detectors. These include the use of resistive strips and dual-end readout for the determination of the longitudinal coordinate of the charge deposition on narrow electrodes [1] and limitations on silicon microstrip ladder length for precision narrow-strip sensors [2]. These studies are in fact dependent only on the properties of the electrode that collects the signal and propagates it to the readout electronics, and thus are independent of the sensor technology that generates the signals. Thus, this work may have relevance to detection issues across a wide array of fields. Ongoing tracking R&D is focused on the further development of the Long Shaping-Time Front End (LSTFE) microstrip readout ASIC. This properties of this ASIC have been explicitly optimized for the readout of long ladders of silicon strip sensors that are motivated by the need for precise low-mass central tracking for a Linear Collider Detector. With a small and straightforward change to the shaping properties of the ASIC, it could be reoptimized for use for the short strips and high occupancy that would be expected for ILC forward-tracking applications. Similar to most ILC-oriented readout designs, the LSTFE features a long shaping time optimized to reduce voltage-referenced readout noise, as appropriate for narrow-strip, long-ladder applications. Unique to the LSTFE design, however, is the use of time-over-threshold readout to estimate the analog pulse-height generated by through-going subatomic particles. A pule-development and readout simulation developed at SCIPP suggested that the intrinsic statistical fluctuations of the charge-deposition process in 300 Âţm of silicon obviate the need for a precise measurement of deposited charge. A simulation of the centroid-finding (position-resolution) uncertainty provided by time-over-threshold readout showed little degradation relative to that provided by an exact measurement of deposited charge. On the other hand, there

are several advantages offered by the use of time-over-threshold readout. It is very simple to implement within a digital back-end to the LSTFE's analog front end (the implementation would be on the same chip as the front-end readout), requiring only a measurement of the number of clock counts that the given channel is over threshold, and then the assembly and transmission of a single data word containing the time of the upward transition, the time over threshold after the transition, and the channel number. This happens in real time and is driven immediately off the chip into the DAQ, eliminating the need for buffering and ADC conversion. In particular, there is no limit to the rate at which particles can be detected other than the return-to-baseline of the analog signal, and so the data-accumulation rate capability of the device is very high. In addition, for forward tracking, for which short strips are envisioned, the shaping time can be shortened significantly. This will further improve the rate capability of the LSTFE readout, making it an excellent choice for the high-occupancy forward region. Figure 1 shows the measured fractional charge uncertainty for the LSTFE prototype ASIC; for depositions expected from minimum-ionizing particles (1-4 fC) the fractional charge measurement uncertainty is approximately 15%, which is small compared to the intrinsic fluctuations that arise from the deposition process.

References [1] J. K. Carman et al., Longitudinal Resistive Charge Division in Multi-Channel Silicon Strip Sensors, Nulcear Inst. and Methods in Physics Research A579 (2007), pp 595-598. [2] K. Collier et al., Microstrip Electrode Readout Noise for Load-Dominated Long Shaping-Time Systems, Nuclear Inst. and Methods in Physics Research, A729 (2013), pp. 127-132.

2.2 KPIX

2.2.1 Collaborating Institutions

- SLAC National Accelerator laboratory
- University of California, Davis
- University of California, Santa Cruz
- University of Oregon
- University of New Mexico

2.2.2 Introduction

KPiX is a 1024 channel "System on a Chip" intended for bump bonding to large area Si sensors, enabling low multiple scattering Si strip tracking and high density Particle Flow calorimetry for SiD at the International Linear Collider (ILC).

Each channel consists of a dynamically switchable gain charge amplifier; shaping; threshold discrimination; and 4 sample and hold capacitors and 4 timing registers. The chip permits 4 separate measurements of amplitude and time of threshold crossing during each train, and amplitude digitization and readout during the intertrain period. The dynamic range is from sub minimum ionizing particle (mip) (320 micron silicon)

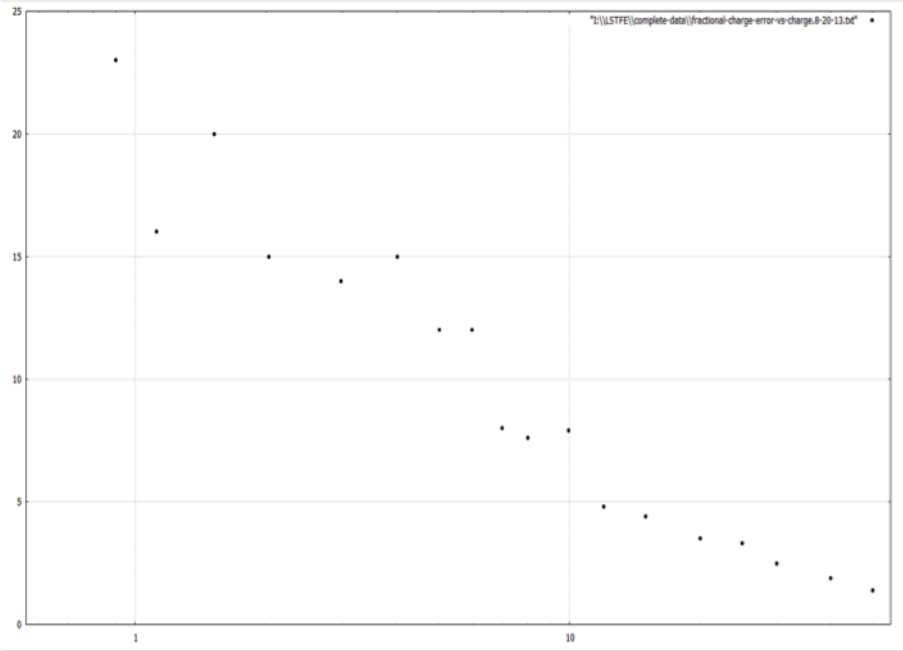

Figure 9: Fractional pulse-height uncertainty (percent) versus injected charge (fC) for the LSTFE front-end ASIC. The development of this ASIC has been done solely at the Santa Cruz Institute for Particle Physics (SCIPP) within the University of California at Santa Cruz, and while slowed significantly due to the loss of support for Linear Collider Detector R&D, continues within SCIPP. Tasks that remain in developing a chip suitable for use in a Linear Collider Detector include the development of the digital back end; significant progress has already been made in defining the architecture of this section of the chip and in implementing this architecture in prototype form on an FPGA. Power cycling (switching the chip into a low-power quiescent mode for most of the 199 ms between beam crossings) also needs to be implemented.

to more than 2000 mip. KPiX also has a calibration system for each channel, servos for leakage compensation, "DC" reset for asynchronous operation for testing with cosmic rays, and polarity inversion for use with GEMs and similar detectors. The noise floor is about 0.15 fC (1,000 electrons), and the maximum signal is 10 pC (utilizing the dynamic range switching). The full dynamic range corresponds to 17 bits.

2.2.3 Recent Milestones

ILC related R&D in the US is largely unfunded and small efforts are being kept alive on the margins. The KPiX R&D is such an example of necessary work for SiD that is marginally alive.

2.2.4 Engineering Challenges

At this time, KPiX is seen as the baseline readout system for the tracker and electromagnetic calorimeter. A stack of 13 EMCal sensors with bump bonded KPiX was assembled for a beam test at SLAC in the summer of 2013. That test discovered that two kinds of crosstalk are significant:

- In-time crosstalk occurs due to parasitic coupling of traces on metal 2 of the sensor to other pixels. The level of crosstalk increases with the size of the signal, and decreases with increased speed of the front end charge amplifier (meaning increased current and power dissipation). A new sensor design is being developed that uses metal 1 to shield the traces of metal 2, and these ideas will be tested in the next sensor prototype.

- Out-of-time cross talk occurs when many pixels are hit and reset simultaneously. The resets collectively cause other pixels to trigger, and a cascade builds up. This uses up all the KPiX buffers. The root cause of the problem appears to be some internal logic within KPiX that is not current limited, and will require design modification.

A more general issue is that both the EMCal and tracker sensors from Hamamatsu were ordered with Al pads, as it was believed that plating (by the zincate process) a stack of metals culminating with Au would be straightforward. This turns out to be wrong. After many attempts at University of California Davis (UCD) and local industry, IZM has Ar ion etched the pad surfaces and sputtered a base layer, permitting the buildup of a stack that ended with Au, and permitting the attachment with solder bumps that had been placed during KPiX manufacture by TSMC. Testing of these sensors revealed 10% pixel to pixel shorts and some opens of signal traces, that are suspected to be damage caused by the Ar ion etch. Future sensors will be ordered with Au pads. An additional issue is that the Tracker sensor was planned to be wire bonded to its (very thin) cable. The sensor oxide layer is not strong enough to allow wire bonding without damage, and so must be solder bumped. The pad pitch is small, and solder bumping the cable will be challenging. The trouble with the wire bonding to the sensor was unexpected. Another concern is that the current design of KPiX has deadtime after a pixel has accepted a trigger. Only the triggered pixel is affected;

all the other pixels are available for signals. This deadtime is different from the usual notion of data acquisition deadtime where the entire detector is unavailable, but the correction to the luminosity integral is easy. Finally, the buffer requirement (4 in the current version of KPiX) is being re-evaluated in SiD simulations. A possible new architecture for KPiX is in early stages of evaluation. A small mechanical engineering effort has started to study the structure of the EMCal. The Sid EMCal has emphasized thin gaps between the tungsten layers to minimize the Moliere radius, and this implies that the structure is connected by columns at the vertices of the sensors. The DBD design shows hexagonal sensors, which indeed are the most efficient way of tiling large areas, but no consideration was given to the edges of these arrays. The engineering work is leading to the realization that it is probably easier and cheaper overall to use two sizes of rectangular sensors, where the two sizes can be selected to tile to the edges of the layers and even tile the endcaps reasonably. Thus it is likely that the next round of EMCal sensor prototypes will be rectangles with square pixels. Tracker sensors are now at IZM for the pad plating and subsequent bonding of KPiX; they will then go to UCD for cable attachment and testing.

2.2.5 Future Plans

Assuming positive developments with Japan are announced soon, we expect the financial support to improve. It should be noted that an important effect of the withdrawal of support is that most of the US collaborators have been forced to move to other work.

- EMCal Sensors: A second round of prototypes will be designed and ordered with rectangular layout; shielded traces, and Au pads.
- Tracker Sensors: The current prototypes will be evaluated, and if appropriate tested in a beam.
- KPiX: A new architecture with little (or no) deadtime will be evaluated. A decision will be made to develop this new architecture or incrementally.
- improve the existing design.
- The EMCal mechanical structure will be pushed towards a conceptual design.

2.2.6 Applications Outside of Linear Colliders

This work represents a significant step in the aggressive integration of silicon sensors with readout electronics, just short of integrating the electronics directly into the sensors. It has prompted consideration of this approach by CMS for calorimetry and by ATLAS for a muon system. It may have applications in sensors for light sources as well as other particle physics detectors.

2.3 Time Projection Chamber – Bonn

2.3.1 Collaborating Institutions

- CEA Saclay

- NIKHEF
- Fraunhofer Institut IZM, Berlin

2.3.2 Introduction

The University of Bonn is studying the pixelized readout of a TPC for the ILD detector. The readout is based on the Timepix ASIC with a triple GEM or Micromegas based gas amplification.

2.3.3 Recent Milestones

The first studies were based on the triple GEM setup with a single Timepix chip. This readout was mounted in a small test detector in the Bonn laboratory. Here, the working principle was tested with a long drift distance. It could be demonstrated that the transverse spatial resolution of the reconstructed primary electrons was close to the expected diffusion limit of single electrons. The results are summarized in the following publications: âĂŞ C. Brezina et al., Operation of a GEM-TPC with pixel readout, IEEE TNS, Vol. 59, No. 6, December 2012, pp. 3221-3228 âĂŞ J. Kaminski et al., Time projection chamber with triple GEM and pixel readout, NSS Conference Record, 2008, 2926-2929 âĂŞ C. Brezina et al., A Time Projection Chamber with triple GEM and pixel readout, 2009 JINST 4 P11015 âĂŞ J. Kaminski et al., Time projection chamber with triple GEM and highly granulated pixel readout, LP 2009, Conf. Proc. C0908171 (2009) 533-535 âĂŞ P. Schade et al., A large TPC prototype for a linear collider detector, NIMA 628 (2011) 128-132

The new focus are GridPix based detectors, where the gas amplification stage is a Micromegas produced in a postprocessing technique, which guarantees a high quality grid well aligned with the readout pixels. This approach was pioneered by NIKHEF and the University of Bonn has modified the production process together with the Fraunhofer Institut IZM so that a wafer-based production of GridPix detectors is standard by now. The new GridPixes were tested on small prototype detectors and also assembled in an 8 GridPix module for the Large Prototype detector at DESY. A successful test beam campaign was performed last year. âĂŞ M. Lupberger, The Pixel-TPC: first results from an 8-InGrid module, 2014 JINST 9 C01033 âĂŞ W. Koppert, GridPix detectors: Production and beam test results, NIMA 732 (2013) 245âĂŞ249 The current work is focused on a new LP module with about 100 GridPixes. This module is a demonstrator that larger areas (400 cm2) can be produced and operated. It shall be tested in the LP at the beginning of next year. For this a number of challenges have to be coped with. In particular commercial readout systems are not easily scalable. This is why Bonn has developed a cheap and easily expandable system based on the Scalable Readout System (SRS) of the RD51 collaboration. In addition Bonn is developing the software for reconstructing and analyzing the test beam and simulation data. For this the LCTPC software framework of MarlinTPC is used. âĂŞ J. Abernathy et al., MarlinTPC: A Common Software Framework for TPC Development, NSS conference record, 2008, 1704-1708 Finally, Bonn also takes part in designing new pixel chips. To test the new digitization and readout techniques two test chips were designed in collaboration with N'IKHEF. Then Bonn also contributed to the design of the Timepix

successor chip, Timepix3, which is being tested now: âĂŞ A. Kruth et al., GOSSIPO-3: measurements on the prototype of a read-out pixel chip for Micro- Pattern Gaseous Detectors, 2010 JINST 5 C12005 âĂŞ C. Brezina et al., GOSSIPO-4: Evaluation of a Novel PLL-Based TDC-Technique for the Readout of GridPix-Detectors, IEEE Trans. Nucl. Sci. Vol. PP âĂŞ Y. Fu et al., The charge pump PLL clock generator designed for the 1.56 ns bin size time-to-digital converter pixel array of the Timepix3 readout ASIC, 2014 JINST 9 C01052

2.3.4 Engineering Challenges

The production of a module with 100 GridPixes requires 4 main components: The production of a large number of GridPixes with sufficiently good quality. This has been addressed by the new production method and a large batch is being produced. The challenge of the readout is being addressed by the new readout system. Finally the distribution of the LV power to all ASICs and the cooling of the ASICs still are unclear, but since both challenges are similar for most readout electronics, standard solutions are expected to be adequate.

2.3.5 Future Plans

On a short term the production of the 100 ASIC module is the main goal at Bonn. If this module has been successfully operated, we are interested in replacing the Timepix ASIC by the Timepix3 ASIC and produce GridPix detectors with this improved chip. There are also some ideas of how to improve the grid structure and make it more reliable. Finally, the reconstruction and analysis software needs further improvement and has to be extended, so that simulated data for the final TPC (i.e. 10,000 hits per track) can be studied.

2.3.6 Applications Outside of Linear Colliders

A single InGrid detector will be installed this year in the CAST experiment for axion search. For a CLIC-TPC a highly granular (i.e. pixelized) readout structure is mandatory to lower the occupancy.

3 Electromagnetic Calorimeter R&D

3.1 Scintillator Strips

3.1.1 Collaborating Institutions

Nihon Dental University, Shinshu University, Tokyo University (ICEPP), Tsukuba University

3.1.2 Introduction

3.1.3 Recent Milestones

- introducing a new scintillation light readout scheme, with different scintillator strip shape by having better homogeneity
- photo-sensor of increased number of pixels in 1mmx1mm, this leads larger dynamic range for the calorimeter
- more experience on the FE read out board and ASICs

They are not published yet, instead some proceedings

3.1.4 Engineering Challenges

- wrapping the scintillator strip and align them on the FE read out layer automatically
- mass test facility for the read out layer

3.1.5 Future Plans

- optimizing scintillator layer: shape of scintillator strip, how to read out scintillation light, the location of photo-sensor, size and shape of photo-sensor and mass production scheme
- developing photo-sensor with Hamamatsu photonics company, to have lager dynamic range and mass test scheme
- establish a detector fabrication plan

3.1.6 Applications Outside of Linear Colliders

- photo-sensor named MPPC from Hamamatsu photonics INC is employed for the T2K experiment, CMS upgrade (HC-CAL), BELLII detector (endocarp muon)
- PET and SPECT development

3.2 Silicon Pads

3.2.1 Collaborating Institutions

- LPNHE-Paris
- LAL
- Univ. of Tokyo
- Kyushu University

3.2.2 Introduction

3.2.3 Recent Milestones

ELECTROMAGNETIC Calorimeter

- First development of PFA for dedicated detector (TESLA Report)
- First prototype of High granularity electromagnetic calorimeter ("physics prototype", see publications in the CS report).
- First design of ECAL silicon–tungsten for a full scale detector (From TESLA report to DBD 2013)
- R&D on scalable technology for all the involved large detector aspects (integration of embedded readoud chips, on thin supporting electronics boards, in self-supporting tungsten–carbon mechanical elements ensuring the cooling and protection; all made of exchangeable elements with a quality control procedure; the associated DAQ).
- Realisation of a large self-supporting W–Carbon fiber structure with integrated stress monitoring (using Fiber Bragg Gratting)
- Recently: tests of 1st base sensor units of the technological prototype in beam

PFA:

- Development of Mokka an overlayer of the GEANT4 used for ILD, CLIC detectors, CALICE TB, ...
- Reconstruction tools adapted to the high granularity calorimeters (photon reconstruction [GARLIC], Advanced clustering [ARBOR], event displays [DRUID])

ILD integration & optimisation

- for the DBD: integration of all the ILD elements, placement of services, thorough estimation of total cost of the detector
- since DBD: re-optimisation of the ILD dimensionning, esp. for the Si-W ECAL using full PFA reconstruction.

3.2.4 Engineering Challenges

- Silicon wafer cost reduction when used for calorimetry; direct contact with producers established (Hamamatsu, On-Semi, ...).
- A chip with the good dynamic, noise, power dissipation (using power pulsing), etc.
- Integration in a compact device, ensuring all the requests (precision: electronic and mechanic, heat production, reliability)
- Industrialisability of solutions; scalability of tests for a 100M channel detector.

3.2.5 Future Plans

Impossible. No way to see beyond next year (see IN2P3 recommendation) To recall, all the R&D will stop at the end of 2016, if there is no decision in Japan

3.2.6 Applications Outside of Linear Colliders

- CEPC, TLEP and directly today on CMS upgrade
- The compact Silicon-W design has been used in the PAMELA satellite (very similar to physics prototype)

4 Hadronic Calorimeter R&D

4.1 Scintillator Tiles

4.1.1 Collaborating Institutions

4.1.2 Introduction

4.1.3 Recent Milestones

4.1.4 Engineering Challenges

4.1.5 Future Plans

4.1.6 Applications Outside of Linear Colliders

4.2 Resistive Plate Chambers

4.2.1 Collaborating Institutions

4.2.2 Introduction

4.2.3 Recent Milestones

4.2.4 Engineering Challenges

4.2.5 Future Plans

4.2.6 Applications Outside of Linear Colliders

4.3 GEM

4.3.1 Collaborating Institutions

4.3.2 Introduction

4.3.3 Recent Milestones

4.3.4 Engineering Challenges

4.3.5 Future Plans

4.3.6 Applications Outside of Linear Colliders

4.4 FCAL

4.4.1 Collaborating Institutions

- AGH-University of Science and Technology, Cracow, Poland
- CERN, Geneva, Switzerland
- DESY, Zeuthen, Germany
- IFIN-HH, Bukharest, Romania
- IFJPAN, Cracow, Poland

- ISS Bukharest, Romania
- LAL Orsay, France
- JINR Dubna, Russia
- NCPHEP Minsk, Belarus
- Pontificia Universidad Catolica de Chile, Santiago, Chile
- Tel Aviv University, Tel Aviv, Israel
- Tohoku University Sendai, Japan
- University of Colorado Boulder, USA
- University of California Santa Cruz, USA
- VINCA Institute of Nuclear Science & University of Belgrade, Belgrade, Serbia

4.4.2 Introduction

4.4.3 Recent Milestones

4.4.4 Engineering Challenges

4.4.5 Future Plans

4.4.6 Applications Outside of Linear Colliders