1 Collaborating institutes

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2 Introduction

CMOS Pixel Sensors (CPS) combine high granularity with low material budget and allow integrating the full signal processing circuitry on the sensor substrate. Being moreover cost effective because of the underlying industrial market, CPS are attractive for a wide range of applications. They are developed for the ILC since more than fifteen years and were shown to rather easily comply with the required spatial resolution and material budget of an ILC vertex detector and their radiation tolerance was observed to go well beyond the ILC requirements [1]. The state of the art of the technology is illustrated by the 400 ULTIMATE sensors operated in the STAR-PXL detector [2] at RHIC/BNL since 2014 and by the 10-100 times faster sensors developed for the upgrade of the ALICE Inner Tracker System (ITS) [3].

The achieved read-out speed of the CPS developed for an ILC vertex detector is already quite satisfactory [1], but is worth improving in ordre to facilitate track seeding at nominal ILC running conditions and to introduce a safety margin reflecting the uncertainties affecting the predicted beam related background rate.

The technology should in fact allow single bunch tagging, provided power consumption and, in turn, power cycling remain under control. The flexibility and detection performances of CPS are also indicating attractive perspectives for trackers, where relaxed constraints on the granularity may be exploited to find a well suited balance between speed, power saving and material budget. Ambitious goals for an ILC experiment may therefore be considered since their development may be carried out for numerous years until the design inputs of a vertex detector ought to be fixed.

The charged particle detection performances of CPS are currently essentially limited by manufacturing parametres. The latter evolve steadily since several years in a direction which makes them increasingly suited to the ILC vertexing and tracking. Besides achievements targetted with existing processes, the present R&D addresses also improvements expected from the evolution of the CMOS industry, mainly driven by the trend towards smaller feature sizes which would allow overcoming the conflict between the spatial resolution and the bunch tagging capability of CPS. This evolution is already well visible when comparing the performances achieved with the 0.35 μm process used for the STAR-PXL and the more recently addressed 0.18 μm process used for the ALICE experiment.

The R&D adresses presently four objectives :

- 2 or 3 CPS variants optimised for the different vertex detector layers :
  - inner layer : design privileging spatial resolution and read-out speed
  - outer layers : design privileging power saving, exploiting the less demanding spatial and time resolutions
- CPS adapted to tracking sub-systems, based on large pixels and privileging power saving
- ultra-light double sided ladders (called PLUME [4]) equipped with (identical or complementary) CPS on its two faces

3 Recent milestones

Specific CPS are being developed since 2011 to equip the Inner Tracking System (ITS) of the ALICE experiment in the framework of its upcoming upgrade. The surface to cover exceeds 10 square meters, i.e. nearly two ordres of magnitude more than the STAR-PXL or an ILC vertex detector.

Two CPS are being developed, differing by their read-out architectures. The most conservative of them, called MISTRAL-0, reproduces the ULTIMATE sensor equipping the STAR-PXL and is thus based on a synchronous, rolling-shutter, read-out. The concept underlying the other sensor, called ALPIDE, features an asynchronous read-out based on a token ring relying on a pre-amplifier/shaper/discriminator chain implemented in the pixel array. It allows for a few microsecond read-out time and for a power consumption below 50 mW/cm^2. These performances were demonstrated in 2014 [5] on a real scale prototype.

MISTRAL-O relies on large pixels to achieve a 20 μs read-out time and a power consumption below 100 mW/cm^2 while providing 10 μm resolution with its integrated binary encoding. Its read-out architecture was validated in 2014 with a real scale prototype [6] featuring 160,000 small (22x33 μm^2 large) pixels. More recently [7], prototypes composed of three times larger pixels were tested on beam and demonstrated satisfactory charged particle detection performances at 30°C and after radiation loads exceeding those expected at the ILC by several ordres of magnitude.

In summary, the full chain of the ULTIMATE sensor has been reproduced in a 0.18 μm process with twice faster read-out frequency and improved sensitive volume (epitaxial layer) characteristics. The optimisation of this design for tracking systems, using relatively large pixels, is validated.

Moreover, a small prototype of a sensor optimised for the vertex detector outer layers was realised in the 0.18 μm process mentioned earlier. Low power is achieved using enlarged, 35 μm pitch, square pixels and the spatial resolution is kept below 4 μm by integrating a 3-bit ADC in each pixel. The approach was validated in the former 0.35 μm process with the MIMOSA-31 prototype, but the ADCs had to be kept at the sensor periphery because of process limitations, translating into larger power consumption and slower read-out. Laboratory tests of the new prototype were performed since last Summer, showing satisfactory noise performances at nominal read-out speed, thus validating the concept.

4 Engineering challenges

Squeezing the material budget of the double-sided PLUME ladders below 0.3 % X_0 will the main engineering challenge, as the design has to account for the necessity to power pulse the ladders in the strong experimental magnetic field. Power pulsing seems mandatory in case of continuous read-out as the sensor design is unlikely to end up with a power density suppressed enough to avoid switching the sensors off inbetween consecutive trains. The possibility to introduce micro-channel cooling in the ladders will be studied in ordre to mitigate the power pulsing requirements.

5 Future plans

Several development directions will be pursued in the coming years, to improve the performances of the CPS and to assess the added value of the ultra-light double-sided ladder concept.

The development of CPS will mainly aim at realising a prototype of a new sensor series, called IBISCUS[1], composed of pixels with less than 20 μm pitch providing a read-out time of about 1 μs (using a token ring read-out).

[1] standing for **I**lc **B**unch **I**dentifying **S**ensor **C**ompatible with **U**ltraprecise **S**patial resolution

The R&D on the other CPS versions mentioned earlier (for the vertex detector outer layers and for tracking sub-systems) will be pursued with coarser priority. Besides these continuous read-out architectures, a sensor composed of 4 μm pitch square pixels with analog output, foreseen to be read out inbetween trains like FPCCDs, will also be studied.

Different versions of double-sided ladders will be realised and their performances evaluated in terms of spatial accuracy, including alignment issues, and in terms of stability against power pulsing, possibly in a high magnetic field.

The two main alternative design options are going to be compared to each other. One version is based on a high precision sensor (< 3 μm) on one side featuring $\lesssim 50$ μs integration time, while a fast sensor ($\sim$ 2-3 μs) equips the other side which provides ~ 5 μm resolution. The other version is based on a single sensor equipping both ladder sides, which offers ~ 4 μm spatial resolution and about 5 μs time resolution.

6 Applications outside of Linear Colliders

CPS developed at IPHC in perspective of the ILC are used in several devices, as illustrated by the non-exhaustive list below:

- Several high precision transparent beam telescopes, adapted to (< 1 GeV) electron beams, are equipped with the MIMOSA-26 or -28 (alias ULTIMATE) sensors
- The first generation of sensors with full on-chip signal processing developed at IPHC (in a 0.35 μm CMOS process) was applied to the STAR-PXL detector at RHIC, which completed successfully its first data campaign in 2014 and has started its 2015 run
- The upgraded ALICE ITS will be the next equipment based on CPS; it will provide insight of a token ring architecture pioneering the one considered for the IBISCUS chip mentioned above; it will also provide running experience with a tracker based on CPS
- The Micro-Vertex Detector of the CBM experiment at FAIR/GSI will also be based on the CPS presently developed for the ALICE-ITS upgrade
- The sensors were, or are, being applied outside of subatomic physics. They were for instance used in the FIRST experiment at GSI, for hadrontherapy monitoring; they are presently developed for soft X-Ray imaging and brain-imaging.

References

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