**3D Pixel Development**

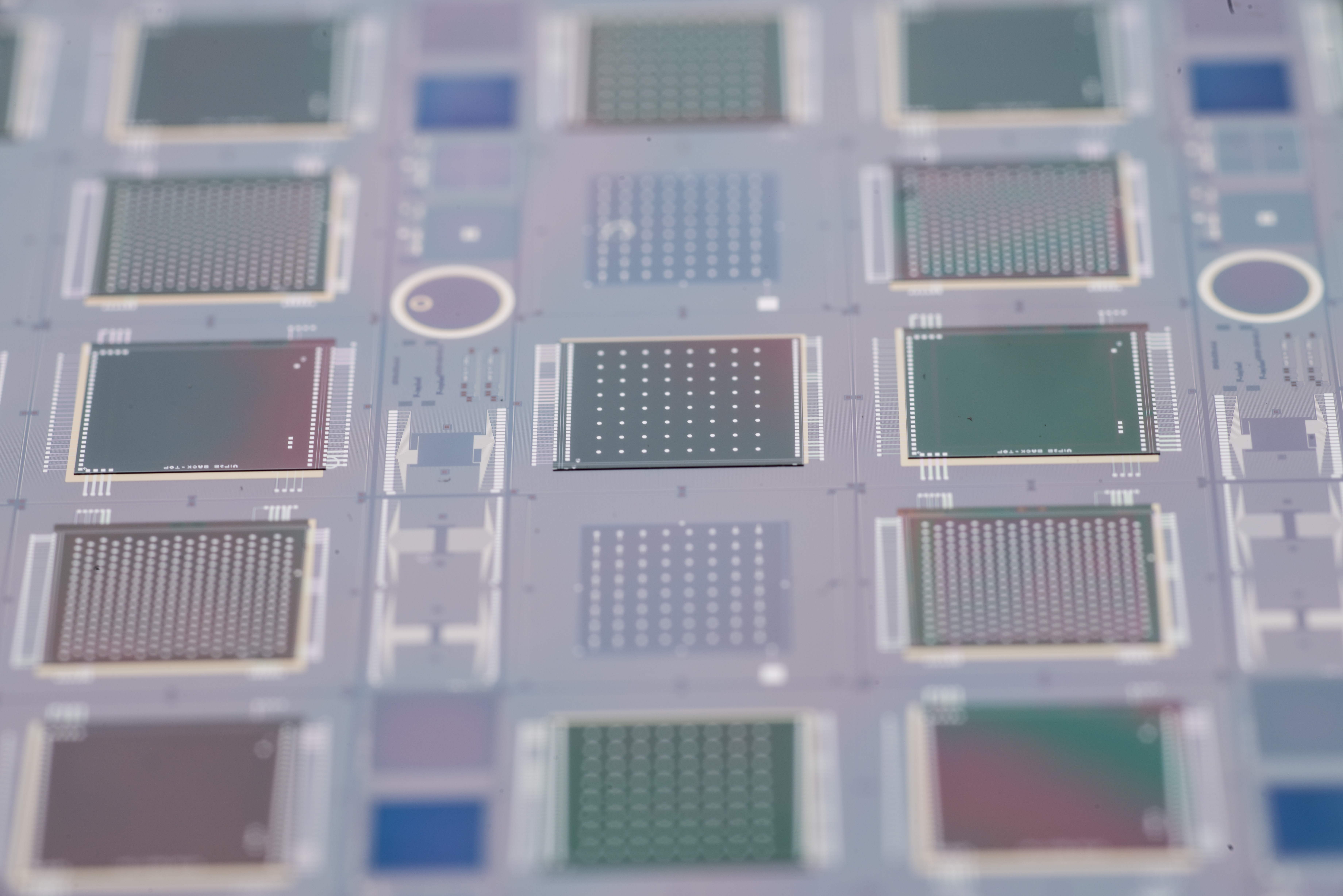
This R&D area covers sensors and electronics integrated utilizing 3-dimensional electronics technology. This technology is distinct from 3D sensors and builds on efforts in the electronics industry to stack multiple layers of electronics to form dense assemblies of complex devices. It is important for Particle Physics in that it allows very fine pitch (4 micron) integration of sensors with multiple layers of electronics, allows interconnection to both the top and bottom of devices, and provides techniques for low mass, thinned devices. The interconnection of top and bottom means that sensors can be bonded to complex electronics with no wasted area for interconnect and optimal delivery of power and ground.

* Major R&D efforts and recent developments since ILC DBD (with publications/references to major results)

We have completed our multi-year effort to demonstrate commercial 3D technology. This consists of two tiers of 0.13 micron CMOS interconnected with Direct Oxide Bonding (DBI) technology and access using Through-Silicon-Vias (TSV). The DBI bonds are at 4 micron pitch. Fermilab sponsored the first 3D multiproject run for Particle Physics. The wafers were delivered last summer. Fermilab had three chips on the run VICTR – a CMS track trigger chip, VIPIC – an X-ray imaging chip, and VIP – an ILC vertex chip. Test of the VIPIC and VICTR have shown working devices. Tests for the VIP chip were delayed due to lack of funding and personnel. We have recently restarted this work and initial tests are promising with the readout token successfully passed through the VIP.

In addition to the development of the 3D chips we have also explored the use of DBI to connect the 3D electronics with sensors. Brookhaven Laboratory fabricated a sensor wafer with regions that mate to the VIP, VIPIC and VICTR chips. The chips are ground to expose the top TSVs and contacts are deposited. The assembly is then attached to a handle wafer and the TSVs which project from the other side are exposed. Wafers are then process for DBI bonding and individual die from the 3D wafer are bonded to the sensor wafer. Finally the top “handle” silicon is ground and etched to reveal the previously formed contacts. The total thickness of the readout at the end of this process is about 25 microns (figure 1). These wafers were received at the end of March 2014 and are being tested.

Due to the fact that contacts to a 3D assembly can be made to the body of the die, rather than it’s edge space usually reserved for wirebond contacts at the edge can be eliminated. This raises the possibility of fabricating large, complex pixel detectors of arrays of 4-side butted devices using sensors with active edges. We are in the process of demonstrating this technology utilizing active edge sensors fabricated at VTT and using wafer-to-wafer bonding to a 3D readout wafer. The active edge wafers are based on a silicon-on-insulator stack and thus can be fabricated with essentially arbitrarily thin sensors, in this case 200 microns. Sensor and dummy readout wafers have been fabricated and a test wafer is being etched at SLAC. We expect to have DBI bonded assemblies this summer.

Figure 1 – 3D chips placed on BNL sensor wafers. VIP is middle left and right.

* Engineering challenges  
  Major engineering challenges include:
  + Development of widely commercially available 3D technologies. Based partly on our development the silicon brokers CMP, CMC, and MOSIS now include 3D multiproject runs as part of their standard offerings.
  + Development of high yield 3D bonded chip-to-wafer devices. This is the subject of our active edge project.
  + This development shares with other vertexing technologies the problems of low mass mechanical support, power delivery, and cooling. An SOI-based device can be made thin without special effort. Such thinned devics will need low mass backing hybrid circuitry, presumably flex on carbon fiber or a similar technology.
* Detector R&D plans for the coming years
  + Complete the 3D active edge project
  + Apply our concepts to x-ray imaging devices
  + ILC developments would await renewed funding in the US.
* List of participating institutes  
  Brown University, Cornell University, Fermilab, Northern Illinois University, SLAC, University of Illinois Chicago
* Perspectives of this R&D for applications beyond the ILC   
  As stated above the technology is already being developed for CMS and x-ray imaging applications. The large area sensor concept is applicable for a variety of focal plane array concepts.
* Recent references

1. Results of Tests of Three-Dimensionally Integrated Chips Bonded to Sensors

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1. Tests of the First Three-Dimensionally Integrated Chip for Photon Science

By P. Maj, G. Carini, G. Deptuch, P. Grybos, P. Kmon, D.P. Siddons, R. Szczygiel, M. Trimpl et al..m PoS Vertex2012 (2013) 027.

1. 3D Technologies for Large Area Trackers

By G. Deptuch, U. Heintz, M. Johnson, C. Kenney, R. Lipton, M. Narian, S. Parker, A. Shenai et al.. arXiv:1307.4301.

1. Combining the two 3Ds

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By R. Yarema, G. Deptuch, J. Hoff, F. Khalid, R. Lipton, A. Shenai, M. Trimpl, T. Zimmerman.

10.1088/1748-0221/8/01/C01052.

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