

Detector R&D Report

Editors
Jan Strube **Maxim Titov**
jan.strube@pnnl.gov maxim.titov@cea.fr

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Chapter 1

Vertex Detectors

1.1 Motivation and Constraints for Vertex Detectors at Linear Colliders

The reconstruction of displaced decays has been an important part of particle physics programs since the days of bubble chambers and the discovery of “V” particles. This is still true in today’s high-energy collider experiments. If long-lived particles, such as B or D mesons, or tau leptons, decay to at least one charged track in the detector, they can in principle be resolved from the interactions of the primary collision. Similarly, the possibility to distinguish several primary interaction points significantly improves the reconstruction of events. To this end, modern vertex detectors use silicon sensors with small pixels, assembled in support structures with as little material as possible to reduce multiple scattering. A driver for Linear Collider vertex detector R&D has been low power operation to reduce or completely avoid the need for active cooling.

The reconstruction of displaced vertices depends crucially on the resolution of the perigee, or *impact parameter* of a helical track from the interaction point, which can be parameterized as $\sigma_{\text{ip}} = \left(\frac{\alpha}{p^{3/2} \sin \theta} \right)$. The goal for the impact parameter resolution in an ILC experiment is $\approx 3 \mu\text{m}$. This puts stringent requirements on the pixel size and the distance of the innermost layer from the interaction point.

Machine-induced background processes at the ILC and CLIC include electron–positron pairs produced in beam–beam interactions. During collisions, vertex detectors accumulate hits from these processes, in addition to those from the primary physics events. In addition to small feature size and low power, it is the reduction of these backgrounds that drives the R&D for linear collider vertex detectors. Because of the close proximity to the beams, their design is heavily influenced by the beam structure of the accelerator.

In addition to the precise determination of decay vertices, the CLICdp detector and the SiD concept have integrated vertex detectors into their all-silicon tracking systems. This puts additional emphasis on high reliability and high hit detection efficiency.

Highly performing vertex detectors are essential for the success of the physics program at the ILC. Discovery channels for a large class of new physics models involve third-generation fermions: b quarks that form long-lived mesons, top quarks that decay predominantly to a b quark and a W boson, and long-lived tau leptons.

1.2 CMOS

Contact person: Marc Winter (email: Marc.Winter@IReS.in2p3.fr)

1.2.1 Introduction

CMOS Pixel Sensors (CPS) combine high granularity with low material budget and allow integrating the full signal processing circuitry on the sensor substrate. Being moreover cost effective because of the underlying industrial market, CPS are attractive for a wide range of applications. They are developed for the ILC since more than fifteen years and were shown to rather easily comply with the required spatial resolution and material budget of an ILC vertex detector and their radiation tolerance was observed to go well beyond the ILC requirements [1]. The state of the art of the technology is illustrated by the 400 ULTIMATE sensors operated in the STAR-PXL detector [2] at RHIC/BNL since 2014 and by the 10-100 times faster sensors developed for the upgrade of the ALICE Inner Tracker System (ITS) [3].

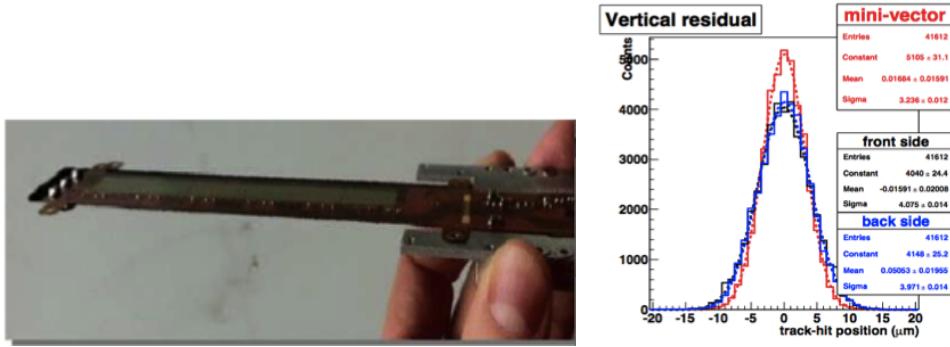


Figure 1.1: left: Photograph of a MIMOSA ladder for EUDET. right: A track resolution of $3\mu\text{m}$ has been achieved.

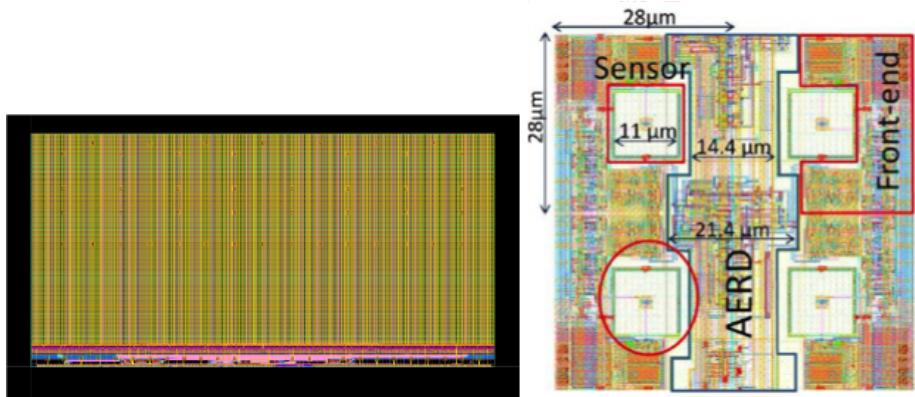


Figure 1.2: Two architectures are being developed: Left: synchronous readout in the MISTRAL chip. Right: asynchronous readout in the ALPIDE chip

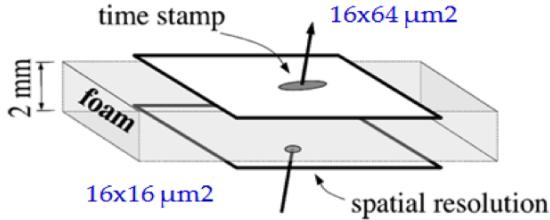


Figure 1.3: Double-sided ladders: mini-vectors providing high spatial resolution and time stamping

The achieved read-out speed of the CPS developed for an ILC vertex detector is already quite satisfactory [1], but is worth improving in order to facilitate track seeding at nominal ILC running conditions and to introduce a safety margin reflecting the uncertainties affecting the predicted beam related background rate.

The technology should in fact allow single bunch tagging, provided power consumption and, in turn, power cycling remain under control. The flexibility and detection performances of CPS are also indicating attractive perspectives for trackers, where relaxed constraints on the granularity may be exploited to find a well suited balance between speed, power saving and material budget. Ambitious goals for an ILC experiment may therefore be considered since their development may be carried out for numerous years until the design inputs of a vertex detector ought to be fixed.

The charged particle detection performances of CPS are currently essentially limited by manufacturing parametres. The latter evolve steadily since several years in a direction which makes them increasingly suited to the ILC vertexing and tracking. Besides achievements targetted with existing processes, the present R&D addresses also improvements expected from the evolution of the CMOS industry, mainly driven by the trend towards smaller feature sizes which would allow overcoming the conflict between the spatial resolution and the bunch tagging capability of CPS. This evolution is already well visible when comparing the performances achieved with the $0.35\text{ }\mu\text{m}$ process used for the STAR-PXL and the more recently addressed $0.18\text{ }\mu\text{m}$ process used for the ALICE experiment.

The R&D adresses presently four objectives :

- 2 or 3 CPS variants optimised for the different vertex detector layers :
 - inner layer : design privileging spatial resolution and read-out speed
 - outer layers : design privileging power saving, exploiting the less demanding spatial and time resolutions
- CPS adapted to tracking sub-systems, based on large pixels and privileging power saving
- ultra-light double sided ladders (called PLUME [4]) equipped with (identical or complementary) CPS on its two faces

1.2.2 Recent Milestones

Specific CPS are being developed since 2011 to equip the Inner Tracking System (ITS) of the ALICE experiment in the framework of its upcoming upgrade. The surface to cover exceeds 10 square meters, i.e. nearly two ordres of magnitude more than the STAR-PXL or an ILC vertex detector.

Two CPS are being developed, differing by their read-out architectures. The most conservative of them, called MISTRAL-0, reproduces the ULTIMATE sensor equipping the STAR-PXL and is thus based on a synchronous, rolling-shutter, read-out. The concept underlying the other sensor, called ALPIDE, features an asynchronous read-out based on a token ring relying on a pre-amplifier/shaper/discriminator chain implemented in the pixel array. It allows for a few microsecond read-out time and for a power consumption below 50 mW/cm^2 . These performances were demonstrated in 2014 [5] on a real scale prototype.

MISTRAL-0 relies on large pixels to achieve a $20 \mu\text{s}$ read-out time and a power consumption below 100 mW/cm^2 while providing $10 \mu\text{m}$ resolution with its integrated binary encoding. Its read-out architecture was validated in 2014 with a real scale prototype [6] featuring 160,000 small ($22 \times 33 \mu\text{m}^2$ large) pixels. More recently [7], prototypes composed of three times larger pixels were tested on beam and demonstrated satisfactory charged particle detection performances at 30°C and after radiation loads exceeding those expected at the ILC by several orders of magnitude.

In summary, the full chain of the ULTIMATE sensor has been reproduced in a $0.18 \mu\text{m}$ process with twice faster read-out frequency and improved sensitive volume (epitaxial layer) characteristics. The optimisation of this design for tracking systems, using relatively large pixels, is validated.

Moreover, a small prototype of a sensor optimised for the vertex detector outer layers was realised in the $0.18 \mu\text{m}$ process mentioned earlier. Low power is achieved using enlarged, $35 \mu\text{m}$ pitch, square pixels and the spatial resolution is kept below $4 \mu\text{m}$ by integrating a 3-bit ADC in each pixel. The approach was validated in the former $0.35 \mu\text{m}$ process with the MIMOSA-31 prototype, but the ADCs had to be kept at the sensor periphery because of process limitations, translating into larger power consumption and slower read-out. Laboratory tests of the new prototype were performed since last Summer, showing satisfactory noise performances at nominal read-out speed, thus validating the concept.

1.2.3 Engineering Challenges

Squeezing the material budget of the double-sided PLUME ladders below $0.3\% X_0$ will be the main engineering challenge, as the design has to account for the necessity to power pulse the ladders in the strong experimental magnetic field. Power pulsing seems mandatory in case of continuous read-out as the sensor design is unlikely to end up with a power density suppressed enough to avoid switching the sensors off in between consecutive trains. The possibility to introduce micro-channel cooling in the ladders will be studied in order to mitigate the power pulsing requirements.

1.2.4 Future Plans

Several development directions will be pursued in the coming years, to improve the performances of the CPS and to assess the added value of the ultra-light double-sided ladder concept.

The development of CPS will mainly aim at realising a prototype of a new sensor series, called IBISCUS¹, composed of pixels with less than $20 \mu\text{m}$ pitch providing a read-out time of about $1 \mu\text{s}$ (using a token ring read-out).

The R&D on the other CPS versions mentioned earlier (for the vertex detector outer layers and for tracking sub-systems) will be pursued with coarser priority. Besides these continuous read-out architectures, a sensor composed of $4 \mu\text{m}$ pitch square pixels with analog output, foreseen to be read out in between trains like FPCCDs, will also be studied.

¹standing for Ilc Bunch Identifying Sensor Compatible with Ultraprecise Spatial resolution

Different versions of double-sided ladders will be realised and their performances evaluated in terms of spatial accuracy, including alignment issues, and in terms of stability against power pulsing, possibly in a high magnetic field.

The two main alternative design options are going to be compared to each other. One version is based on a high precision sensor ($< 3 \mu\text{m}$) on one side featuring $\lesssim 50 \mu\text{s}$ integration time, while a fast sensor ($\sim 2 - 3 \mu\text{s}$) equips the other side which provides $\sim 5 \mu\text{m}$ resolution. The other version is based on a single sensor equipping both ladder sides, which offers $\sim 4 \mu\text{m}$ spatial resolution and about $5 \mu\text{s}$ time resolution.

1.3 DEPFET Pixel Sensors

Contact person: Marcel Vos (email: vos@ific.uv.es)

1.3.1 The DEPFET Collaboration

The DEPFET collaboration consists of nearly 100 members from 13 institutes. It currently takes responsibility for the following work packages:

Mechanics The DEPFET ladder integrates the support structure with the sensor wafer using state-of-the-art silicon processing technology. Read-out electronics and signal routing are integrated on the silicon wafer. The resulting all-silicon ladder is fully self-supporting. The mechanical properties of thin ladders in a realistic environment are studied in detail using detailed models (mock-ups) for Belle II and the ILC .

Cooling The DEPFET cooling concept for Belle II relies on two-phase CO₂ cooling for the end-of-ladder. The sensor is cooled moreover with a forced flow of cold gas. The CO₂ cooling plant is developed by KEK, while the design for the cooling block/support structure is performed within the collaboration. The impact of the linear collider cooling strategy - based on reducing the power dissipated using a pulsed power supply to the detector and cooling through a forced air flow - is studied. A novel cooling strategy for future applications based on mico-channels in the sensors is being evaluated in the collaboration. Solutions for monitoring of environmental parameters are being developed.

Ancillary ASICs The operation of a DEPFET detector requires ancillary electronics in the form of a read-out ASIC (the Drain Current Digitizer), a steering ASIC (SWITCHER) and on-detector ASICs for digital data processing (DHP). These ASICs are developed within the collaboration.

Data Acquisition and Trigger The development of off-detector electronics to process the data from the Belle II vertex detector.

Characterization of prototypes, laboratory and beam tests This work package has contributions from nearly all institutes involved in the DEPFET collaboration.

Currently, the construction of the Belle II vertex detector [8] is the main focus of the collaboration. The requirements of the Belle II vertex detector are similar to those of the ILC, and more stringent in some aspects. The Belle II construction project therefore has considerable synergy with developments for a future linear collider. The LC-specific effort is focused on the development of small-pixel devices and the design of a forward vertex detector. We envisage that after the installation of the Belle II detector (2016) the balance between both projects is restored.

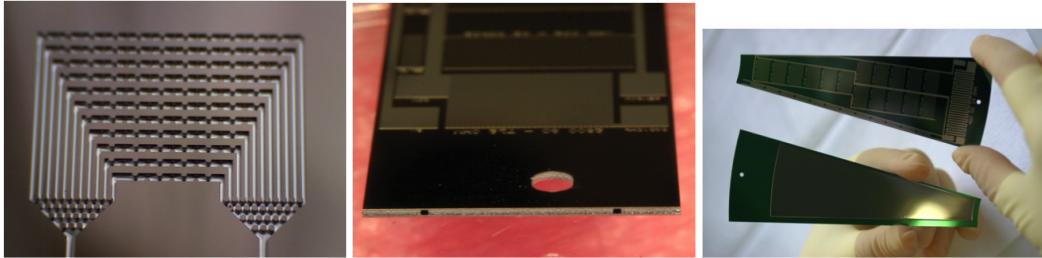


Figure 1.4: left: Microchannel cooling. center: Samples with cooling circuits. right: FTD mockup

Table 1.1: Comparison of ILC and Belle II requirements of a vertex detector

	ILC	Belle II
occupancy	$0.13 \text{ hits}/\mu\text{m}^2/\text{s}$	$0.4 \text{ hits}/\mu\text{m}^2/\text{s}$
radiation	$< 100 \text{ krad}/\text{yr}$	$> 1 \text{ Mrad}/\text{yr}$
	$10^{11} \text{ MeVn}_{\text{eq}}/\text{yr}$	$2 \times 10^{12} \text{ MeVn}_{\text{eq}}/\text{yr}$
duty cycle	1/200	1
frame time	$25 - 100 \mu\text{s}$	$20 \mu\text{s}$
momentum range	100 keV - 500 GeV	$\sim 1 \text{ GeV}$
angular acceptance	$6^\circ - 174^\circ$	$17^\circ - 150^\circ$
spatial resolution	excellent: $3 - 5 \mu\text{m}$	moderate
pixel size	$20 \times 20 \mu\text{m}$	$50 \times 75 \mu\text{m}$
material budget	$0.15\% X_0/\text{layer}$	$0.21\% X_0/\text{layer}$

1.3.2 Introduction

The DEPFET technology implements amplification within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted high-resistivity silicon wafer. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate. The amplified signal is extracted from the pixel matrix by a numbers of ASICs [9, 10] mounted directly on the sensor: The SWITCHER, Drain Current Digitizer (DCD) [11, 12] and Data Handling Processor (DHP) [13].

The DEPFET in-pixel amplification allows for a comfortable signal-to-noise ratio with a very thin active detector. The reduced sensor thickness of $75 \mu\text{m}$ for Belle II, $50 \mu\text{m}$ for the Linear Collider, is the key to remain within the material budget of 0.15% of a radiation length per layer. DEPFET prototypes with $20 \times 20 \mu\text{m}^2$, small enough to meet the stringent spatial resolution specifications of the ILC, have successfully been operated in beam tests [14, 15]. The DEPFET matrix is read out in rolling shutter mode at a rate of 100 ns/row. For the column depths relevant for the ILC and Belle II a frame rate of several tens of μs is achieved [16]. The expected performance of a DEPFET-based vertex detector meets the specifications drawn up by the ILD experiment. DEPFET is also considered as a back-up solution to the SiD concept, in case the single bunch crossing time stamping proves to be out of reach.

1.3.3 Recent Milestones

The concept of a DEPFET active pixel detector for vertex detection at collider experiments was initiated in the linear collider community (for TESLA). The operation principle was extensively proven [14, 15] on small-scale prototypes. A recent reassessment of the DEPFET potential for a linear collider at the energy frontier is found in [16] and in the report [17] for the ECFA detector R&D review in 2014. A large-scale, 75 μm thin Belle II ladder with the ancillary ASICs integrated on the sensor was successfully submitted to a test in an electron beam at DESY in January 2014[18].

The first full-scale DHP prototype was implemented in IBM 90 nm CMOS technology. As this technology was discontinued, more recent designs were submitted in the TSMC 65 nm CMOS process. DHPT v.1.0 comprises temperature independent current references, 11 bias 8-bit DACs with current output, an integrated temperature measuring system and JTAG control. This design has been successfully tested during early 2014[9].

1.3.4 Engineering Challenges

Vertex detector ladders with a thickness of several tens of microns and a spatial resolution of well below 10 μm require very robust mechanical properties. The power generated by the sensors and ASICs must be removed with the smallest impact on the detector material. Measurements on thin ladders under a realistic load, including pulsed powering according to the ILC beam structure, prove the excellent mechanical properties of the all-silicon ladder [19].

1.3.5 Future Plans

Currently, the construction of the Belle II vertex detector (to be installed by 2016 for the first physics run in 2017) implies a large effort of R&D, including:

- Develop the die-attach technology in a controlled atmosphere required for the mounting of passive components on the DEPFET active pixel detector ladders. The first milestone is a fully integrated electrical prototype based on the EMCM.
- First tests that will determine if all the ASICs on the ladder are fully functional
- The integration of read-out and steering ASICs on the pixel sensor to be performed using a flip-chip technique and so-called bump-bonding, using microscopic solder balls.
- The production of the Belle II vertex detector modules, a joint effort of the DEPFET collaboration
- The test of the last version of the DHP chips

In the near future we hope to characterize the performance of a thin ILC-design prototypes with pixels of $20 \times 20 \mu\text{m}^2$

- Perform an engineering design for a DEPFET all-silicon module with the required petal geometry
- A detailed characterization of the response of the device
- Design of the ancillary ASICs, taking full responsibility for future design cycles of the Front End read-out chip, the Drain Current Digitizer (DCD) that is relevant to the ILC and a Belle II upgrade. This chip converts the analog signal from the detector to digital and has a crucial impact on the detector performance.

In the longer term the DCD and DHP are envisaged to evolve into a single chip. Being large arrays of DEPFET pixels a promising technology for the vertex detector of the planned ILC, adaptation of the DCD and DHP chips must also be done.

In the near future we hope to characterize the performance of ILC design prototypes with pixels of $20 \times 20 \mu\text{m}^2$. Important experience is furthermore gained with the thermal and mechanical properties of ultra-thin ladders. Measurements on thin ladders under a realistic load, including pulsed powering according to the ILC beam structure, prove the excellent mechanical properties of the all-silicon ladder. A complete mock-up for the innermost disks is under construction.

1.4 FPCCD

Contact person: Yasuhiro Sugimoto (email: yasuhiro.sugimoto@kek.jp)

1.4.1 Introduction

Fine pixel CCD (FPCCD) is one of the candidate sensor options for the vertex detector of the ILD detector at the ILC [20, 21, 22]. In the present design, FPCCD sensors for the innermost layer of the vertex detector have a pixel size of $5 \mu\text{m}$ and a fully depleted epitaxial layer with a thickness of $15 \mu\text{m}$. Because of the small size of the pixels, the occupancy is acceptably low even if the hits are accumulated for one nominal ILC bunch train ($\approx 1 \text{ ms}$). The efforts of the FPCCD collaboration are currently focused on pixel characterization and development, while we also pursue developments to the cooling system, electronics downstream of ASICs and the reconstruction software [23].

1.4.2 Recent Milestones

R&D activity for the FPCCD vertex detector at present is mainly focused on FPCCD sensors and a detector cooling system using 2-phase CO_2 . One of the achievements of FPCCD sensors after DBD is the fabrication of real size ($12.3 \times 62.4 \text{ mm}^2$) sensors with $50 \mu\text{m}$ total thickness. Figure 1.5 shows the real size prototype sensor. It has 8 readout nodes, and each channel has different pixel sizes of $12 \mu\text{m}$, $8 \mu\text{m}$, and $6 \mu\text{m}$.

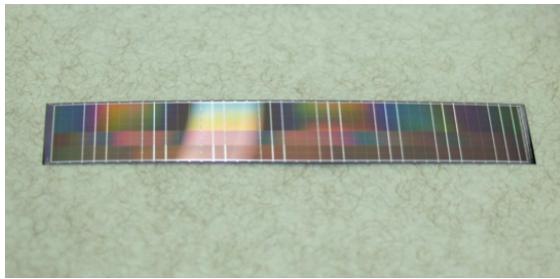


Figure 1.5: Real size FPCCD sensor thinned down to $50 \mu\text{m}$

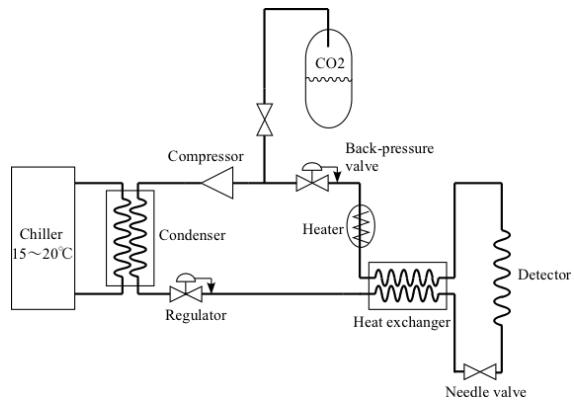


Figure 1.6: A simplified schematic diagram of the two-phase CO_2 cooling system

We have started a neutron damage test using small ($6\text{ mm} \times 6\text{ mm}$) FPCCD prototypes [24]. A prototype sensor was irradiated by a neutron beam of few tens of MeV at the CYRIC facility of Tohoku University. The detailed analysis on the irradiated sensor is still on-going. In order to increase the radiation immunity of FPCCD sensors, particularly to reduce the transfer inefficiency due to radiation damage, the sensors should be cooled down to -40°C . We have started R&D on a two-phase CO_2 cooling system for this purpose. There are several examples of utilizing two-phase CO_2 cooling systems for high energy physics experiments. For these cases, the CO_2 coolant is circulated using liquid pumps. This method is, however, not so efficient for very low temperature cooling of -40°C . Therefore, we adopted a CO_2 gas compressor for the circulation of CO_2 coolant. Figure 1.6 shows a simplified schematic diagram of the system. A prototype system has been constructed, and cooling between -40°C and $+15^\circ\text{C}$ has been successfully demonstrated using this system.

1.4.3 Engineering Challenges

In the present design of the ILD vertex detector, two sensor layers are mounted on both sides of a light-weight ladder of 2 mm thickness. Our goal of the material budget of this ladder is $0.3\% \text{ X}_0/\text{ladder} = 0.15\% \text{ X}_0/\text{layer}$. This goal would not be so easy to accomplish, and we need a lot of R&D effort. The ladders have to be cooled down to -40°C . We plan to achieve this cooling by heat conduction to the end-plate on which thin cooling tubes for 2-phase CO_2 are attached. The design of this structure is not trivial, and we need R&D including thermal simulation. There are challenges both with the mechanical structure and the electronics circuit for the ladder R&D. We have not started this effort yet.

1.4.4 Future Plans

We have been doing our R&D on the FPCCD vertex detector based on a Grant-in-aid for science research which expires at the end of FY2015. By that time, we plan to carry out the following R&D items:

- Characterization of FPCCD sensors including beam tests and radiation damage tests
- Development of FPCCD sensors with the pixel size of $5\text{ }\mu\text{m}$, which is our ultimate goal
- Construction of prototype ladders for inner layers
- Development of readout electronics downstream of ASICs

If new funding is secured in future, the following R&D items have to be done:

- Development of larger FPCCD sensors and prototype ladders for outer layers
- Development of readout electronics which can fit in the small space of real experiment
- Construction of a real size engineering prototype and its cooling test

1.5 ChronoPixel

Contact person: Jim Brau (email: jimbrau@uoregon.edu)

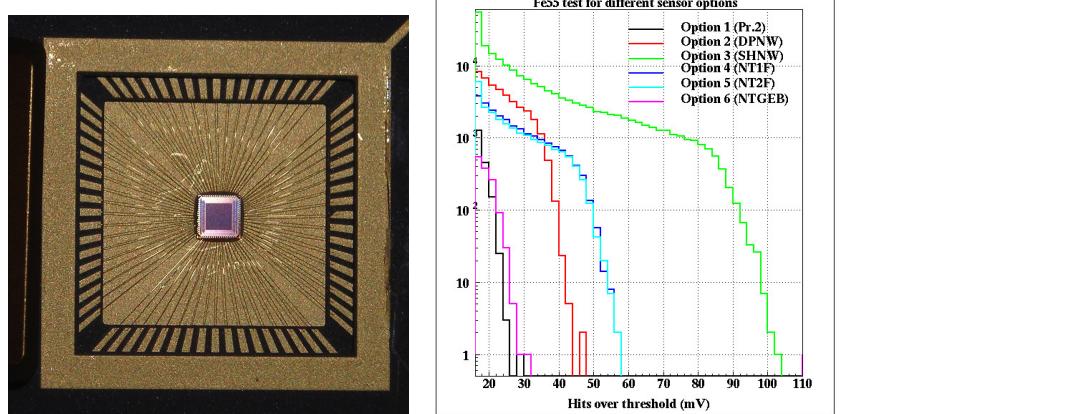


Figure 1.7: Photograph of the prototype 3 chip in its package. The chip has 48×48 pixels, each with a size of $25 \times 25 \mu\text{m}^2$.

Figure 1.8: ^{55}Fe signal over threshold counts for 6 different sensor diode options, implemented in prototype 3. For comparison, option 1 is the same as in prototype 2.

1.5.1 Introduction

The ChronoPixel is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps of pixel hits by charged particles in a nominal ILC bunch train. This information is read out in the time interval between bunch trains. The ChronoPixel option for the ILC vertex detector was described in the ILC DBD [25]. By the time of the DBD, 2 prototypes had been built and tested, and the summary of test results was also presented in the DBD. The main points are:

- We have proven that we can record time stamps in every pixel with time resolution down to 150 ns.
- We have tested sparse readout, allowing to read only pixels with hits, thus reducing readout time to the level allowing readout of all pixels in the sensor in the intervals between bunch crossings.
- We have tested pulsed power for the analog part of the pixels and have proven [26] that turning power ON about 100 μs before bunch train and turning it off between bunch trains does not create any problems for threshold setting accuracy in the comparators.
- We have measured sensor noise level, including all pick-up and cross-talk. It was 24 e- r.m.s in prototype 1 and 26 e- r.m.s. in prototype 3, sensor option 3. Our specification was 25 e- noise.
- We have tested the idea of building all in-pixel electronics only from NMOS transistors, thus eliminating the need for a special process (deep p-well) to protect signal charge from parasitic collection by in-pixel transistors. We have proven [27] that all NMOS electronics can be built in this way, and that this does not significantly increase the power consumption compared to CMOS electronics.
- We have tested the compensation of comparator offsets using analog calibration, when the value of the offset is stored as a voltage on the capacitor in each pixel. This has an advantage over digital calibration (where the offset value is stored as code in the special register) in that there are no discrete

levels, and the accuracy of such a calibration scheme is not affected by the size of the register or the spread of the initial offsets.

1.5.2 Recent Milestones

- Test of prototype 2 revealed some problems. Possible solutions for these problems were discussed with Sarnoff engineers.
- A new contract with Sarnoff for the design of prototype 3 was signed in August 2013.
- Prototype 3 was manufactured in September 2014. Tests have shown that problems revealed in prototype 2 were solved.

The most recent report [28] on the status of ChronoPixel was presented by N. Sinev in June 2015 at Vertex2015 in Santa Fe, New Mexico.

1.5.3 Engineering Challenges

- The Vertex Detector for ILC faces many engineering challenges. The sensors need to be thinned to about $50\text{ }\mu\text{m}$ to reduce the amount of material in the detector. Support structures also need to be very light, but provide enough stability. Power dissipation of the entire detector should be small to be able to use only air cooling.
- If acceptable levels of the sensor diode capacitance can be achieved, the signal-to-noise ratio will improve. However, a lower value of the capacitance will make the pixels more sensitive to cross-talk through capacitive coupling. Reducing this coupling can be a challenge.
- Transition from small prototypes (few mm^2) to ILC detector size ($\approx 10\text{ cm}^2$) may meet additional problems. One of them will be the effect of Lorentz forces on the power supply buses, especially in the case of power pulsing. Power pulsing is the only way to achieve acceptable power dissipation in the vertex detector. However, it will generate varying Lorentz forces, acting on power supply lines. This may produce vibrations, which are unacceptable for the required spatial resolution of the detector.

1.5.4 Future Plans

- To achieve signal-to-noise ratio required for close to 100% signal registration efficiency. We have achieved very low sensor capacitance in prototype 3, and the signal-to-noise ratio with such a sensor capacitance for ^{55}Fe signal is about 60, however, for minimum ionizing particles the signal will be much smaller, depending on epitaxial layer thickness and charge collection efficiency. The signal-to-noise ratio for standard $7\text{ }\mu\text{m}$ epitaxial layer will be 20 if the charge collection efficiency is 100%, which is unlikely (we have not measured it yet). So we probably will need to increase the epitaxial layer thickness.
- To achieve the required pixel size (prototype 3 has $25\text{ }\mu\text{m}$ pixels, we would eventually like $15\text{ }\mu\text{m}$). It may require going to a technology with feature size less than 65 nm. There seems to be no problems in that, but both – good signal-to-noise ratio and pixel size requirements may be challenging.

- To achieve acceptable level of inter-pixel and digital-to-analog circuit cross talks and parasitic feed-back.
- Depending on available funding, to build a complete sensor with a large enough area and full feature readout.

1.6 3D Pixel Development

Contact person: Ron Lipton (email: lipton@fnal.gov)

1.6.1 Introduction

This R&D area covers sensors and electronics integrated utilizing 3-dimensional electronics technology. This technology is distinct from 3D sensors and builds on efforts in the electronics industry to stack multiple layers of electronics to form dense assemblies of complex devices. It is important for Particle Physics in that it allows very fine pitch ($4\text{ }\mu\text{m}$) integration of sensors with multiple layers of electronics, allows interconnection to both the top and bottom of devices, and provides techniques for low mass, thinned devices. The interconnection of top and bottom means that sensors can be bonded to complex electronics with no wasted area for interconnect and optimal delivery of power and ground.

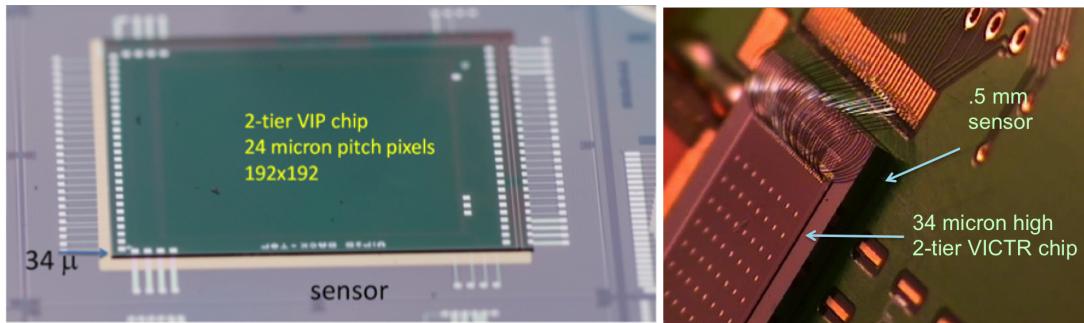


Figure 1.9: Left: ILC Chip. Right: CMS chip

1.6.2 Recent Milestones

We have completed our multi-year effort to demonstrate commercial 3D technology. This consists of two tiers of $0.13\text{ }\mu\text{m}$ CMOS interconnected with Direct Oxide Bonding (DBI) technology and access using Through-Silicon-Vias (TSV). The DBI bonds are at $4\text{ }\mu\text{m}$ pitch. Fermilab sponsored the first 3D multi-project run for Particle Physics. The wafers were delivered last summer. Fermilab had three chips on the run: VICTR – a CMS track trigger chip, VIPIC – an X-ray imaging chip, and VIP – an ILC vertex chip. Tests of the VIPIC and VICTR have shown working devices. Tests for the VIP chip were delayed due to lack of funding and personnel. We have recently restarted this work and initial tests are promising with the readout token successfully passed through the VIP.

In addition to the development of the 3D chips we have also explored the use of DBI to connect the 3D electronics with sensors. Brookhaven Laboratory fabricated a sensor wafer with regions that mate to the

VIP, VIPIC and VICTR chips. The chips are ground to expose the top TSVs and contacts are deposited. The assembly is then attached to a handle wafer and the TSVs which project from the other side are exposed. Wafers are then process for DBI bonding and individual die from the 3D wafer are bonded to the sensor wafer. Finally the top “handle” silicon is ground and etched to reveal the previously formed contacts. The total thickness of the readout at the end of this process is about 25 μm (Figure 1.10). These wafers were received at the end of March 2014 and are being tested. Due to the fact that contacts to a 3D assembly can

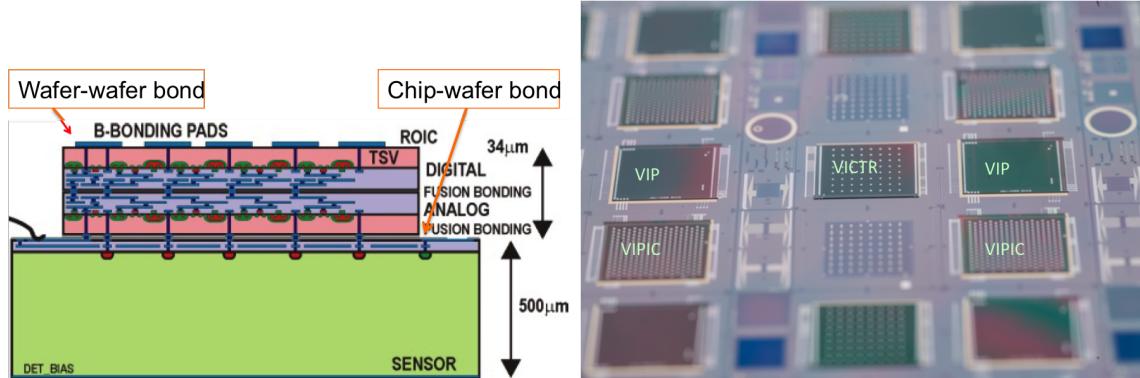


Figure 1.10: Left: Schematic view of the vertically integrated technology. Right: 3D chips placed on BNL sensor wafers. VIP is middle left and right

be made to the body of the die, rather than its edge, no space needs to be reserved for wire bond contacts at the edge. This raises the possibility of fabricating large, complex pixel detector arrays of 4-side butted devices using sensors with active edges. We are in the process of demonstrating this technology utilizing active edge sensors fabricated at VTT and using wafer-to-wafer bonding to a 3D readout wafer. The active edge wafers are based on a silicon-on-insulator stack and thus can be fabricated with essentially arbitrarily thin sensors, in this case 200 μm . Sensor and dummy readout wafers have been fabricated and a test wafer is being etched at SLAC. We expect to have DBI bonded assemblies this summer.

1.6.3 Engineering Challenges

Major engineering challenges include:

- Development of widely commercially available 3D technologies. Based partly on our development the silicon brokers CMP, CMC, and MOSIS now include 3D multi-project runs as part of their standard offerings.
- Development of high yield 3D bonded chip-to-wafer devices. This is the subject of our active edge project.
- This development shares with other vertexing technologies the problems of low mass mechanical support, power delivery, and cooling. An SOI-based device can be made thin without special effort. Such thinned device will need low mass backing hybrid circuitry, presumably flex on carbon fiber or a similar technology

1.6.4 Future Plans

- Complete the 3D active edge project
 - Apply our concepts to x-ray imaging devices
 - ILC developments would await renewed funding in the US.
1. Grzegorz W. Deptuch et al. “Results of Tests of Three-Dimensionally Integrated Chips Bonded to Sensors”. In: *IEEE Trans.Nucl.Sci.* (2013)
 2. R. Yarema, G. Deptuch, and R. Lipton. “Recent Results for 3D Pixel Integrated Circuits using Copper-Copper and Oxide-Oxide Bonding”. In: *Proceedings of Science* (2014)
 3. P. Maj et al. “Tests of the First Three-Dimensionally Integrated Chip for Photon Science”. In: *PoS Vertex2012* (2013), p. 027
 4. G. Deptuch et al. “3D Technologies for Large Area Trackers”. In: *ArXiv e-prints* (July 2013). arXiv: [1307.4301 \[physics.ins-det\]](https://arxiv.org/abs/1307.4301)
 5. R Lipton et al. “Combining the two 3Ds”. In: *Journal of Instrumentation* 7.12 (2012), p. C12010
 6. R Yarema et al. “Vertically integrated circuit development at Fermilab for detectors”. In: *Journal of Instrumentation* 8.01 (2013), p. C01052

1.7 SOI

Contact person: Yasuo Arai (email: yasuo.arai@kek.jp)

1.7.1 Introduction

1.7.2 Recent Milestones

At present, major issues in the SOI pixel development are “back-gate effect”, “hole trap under the transistors by radiation,” and “sensor-circuit cross talks” as shown in Figure 1.11. For these, we have been developing a double SOI technology. The developed double SOI wafer has an additional middle-SOI(Si) layer under the transistors. The conduction layer of the middle-SOI can solve all the three issues. We could successfully process the double-SOI wafer (Figure 1.12). Threshold shift by radiations is successfully recovered by applying compensating voltage to the middle SOI layer (Figure 1.13).

1.7.3 Engineering Challenges

The impact parameter resolution for the ILC vertex detector is required to be a few μm . This means the pixel size must be less than about $20 \mu\text{m}^2$. On the other hand, each pixel must register arrival time of the hits during bunch train, which requires many transistors and capacitors to be located in each pixel. A solution to this is 3D vertical integration of the circuit layers. SOI technology is ideally suited for 3D integration, since the thinning is stopped at the buried oxide (BOX). We already tried 3D SOI pixel chip in collaboration with T-Micro Co. Ltd. The process flow of micro-bump 3D connection is shown in Figure 1.14. This process achieves a resistance of ($\sim 6 \Omega/\text{bump}$) between upper and lower tiers for 1,000 daisy chain (2,000 bumps)

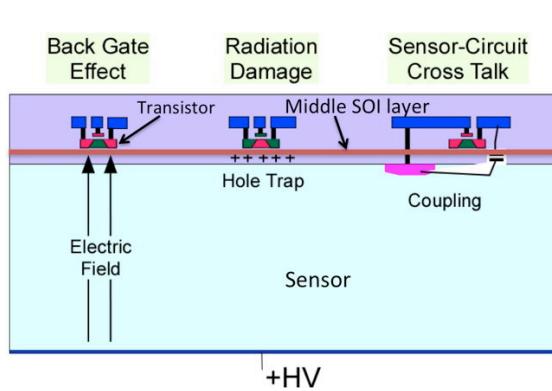


Figure 1.11: Major issues in the SOI pixel detector and introduction of a middle-SOI layer

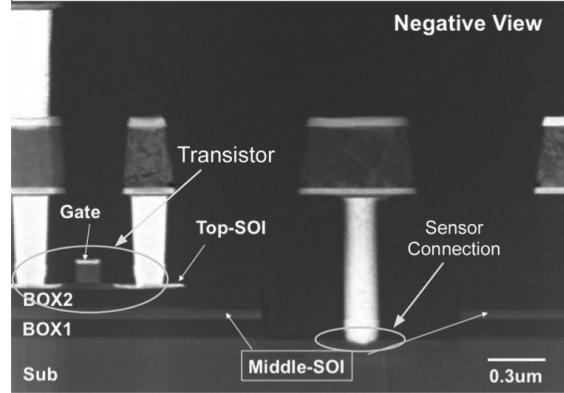


Figure 1.12: Cross section of the double SOI chip after processing

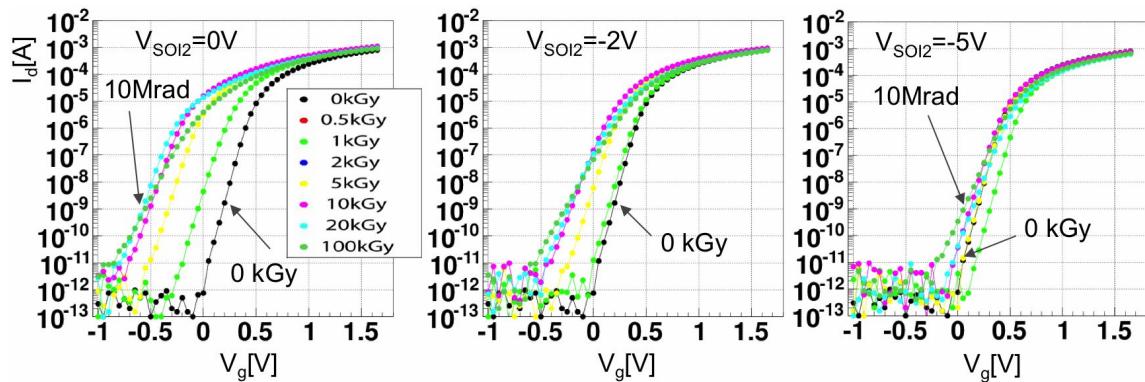


Figure 1.13: Threshold shift recovery by applying compensating voltage (V_{SOI2}) to the middle Si layer

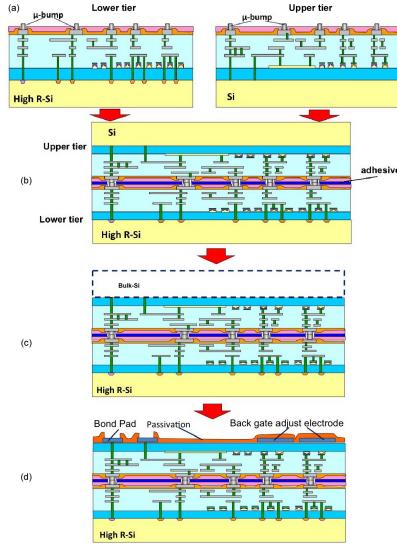


Figure 1.14: Micro-bump 3D integration process flow of the SOI pixel

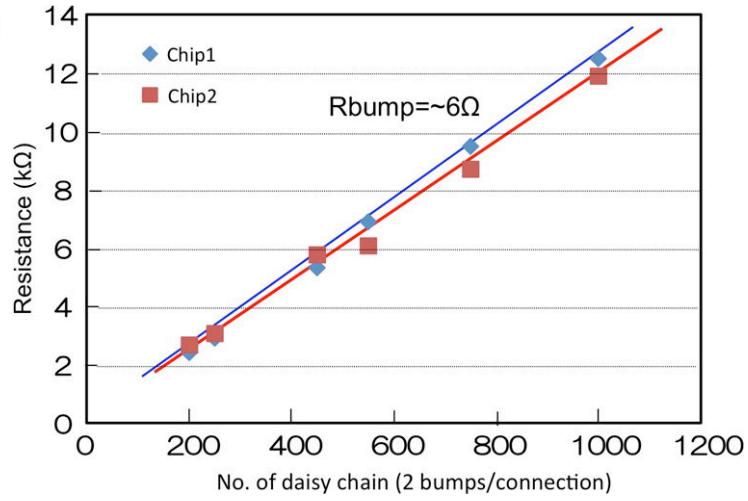


Figure 1.15: Resistance of micro-bump daisy chain between upper and lower tiers

as shown in Figure 1.15. However, to achieve the density of digital circuitry necessary for ILC operations, 32 nm technology may be necessary for the upper tier in the ILC. This requires bonding of two different technology wafers. The 3D integration of different technology wafers (or chips) is still an engineering challenge.

1.7.4 Future Plans

Detector R&D plans for the coming years; We are planning following items for the coming year.

- Sep. 2014 : Complete architecture study for the ILC pixel detector.
- Mar. 2015 : Design and fabrication of first test chip for the ILC.
- Dec. 2015 : Beam test of the test chip.

1.8 CLICpix

Contact person: Dominik Dannheim (email: dominik.dannheim@cern.ch)

1.8.1 Introduction

The precision physics needs at the CLIC TeV-scale linear electron-positron collider require a vertex-detector system with excellent flavour-tagging capabilities through a measurement of displaced vertices in an environment with high rates of beam-induced background events [35]. As a result, the CLIC vertex-detector system needs to have excellent spatial resolution ($3 \mu\text{m}$), full geometrical coverage extending to low polar angles, extremely low material budget ($0.2\% X_0$ per layer), low occupancy facilitated by time-tagging (10 ns

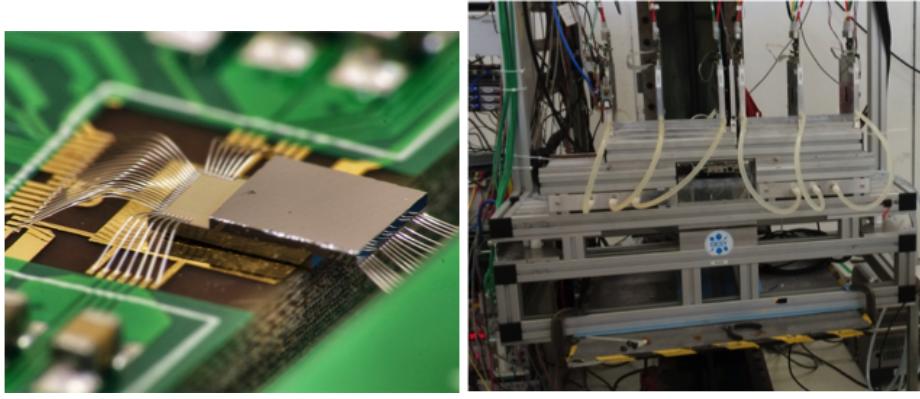


Figure 1.16: Left:CCPDv3 + CLICpix. Right: Timepix3 in the AIDA telescope (CERN PS-T9)

precision), and sufficient heat removal from sensors and readout. A concept based on hybrid pixel-detector technology is under development for the CLIC vertex detector. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin planar sensors or active HV-CMOS sensors via low-mass interconnects. The power dissipation of the readout chips is reduced by means of power pulsing, allowing for a cooling system based on forced gas flow. Through-Silicon Via (TSV) vertical interconnects remove the need for wire bonding connections on the side of the readout ASICs and therefore allow for an efficient tiling to form larger modules with minimal inactive areas.

1.8.2 Recent Milestones

A broad hardware R&D program is in place, addressing the challenges for the CLIC vertex detector in an integrated approach [36]. Recent achievements in the sensor and readout domain include:

Hybrid pixel assemblies with ultra-thin planar sensors Planar pixel sensors with 55 μm pitch and different thicknesses (50–300 μm) were procured from different vendors and bump-bonded to Timepix [37] readout ASICs (100 and 700 μm thickness). Slim-edge sensor designs are compared to designs with active edges. Preliminary beam-test results show very good efficiencies in both cases, extending beyond the edge pixels [38]. For 50 μm sensor thickness and nominal readout parameters, the fraction of multi-pixel clusters is approximately 20%. Single-point resolutions of approximately 3 μm have been extracted for clusters of two pixels using charge interpolation and taking into account non-linear charge sharing.

CLICpix demonstrator ASIC A CLICpix demonstrator chip has been produced in 65 nm CMOS technology, including a 64×64 pixel matrix and power-pulsing capability [39]. The pixel size is 25 $\mu\text{m} \times 25 \mu\text{m}$. Simultaneous 4-bit Time-Of-Arrival (ToA) and Time-Over-Threshold (ToT) measurements are implemented in each pixel, allowing for a front-end time slicing with approximately 10 ns and for measuring the charge to improve the position resolution through interpolation. The full chip can be read out in less than 800 μs (for 10% occupancy), using a 320 MHz readout clock and zero suppression. The power consumption of the chip is dominated by the analog frontend with a peak power corresponding to 2 W/cm². The total average power consumption can be reduced to a value below the target of 50 mW/cm² by means of power gating for the analog part and clock gating for the digital

part. Readout tests have confirmed that the CLICpix demonstrator chip is fully functional and the power consumption and performance are in agreement with simulations [40]. Hybrid modules of CLICpix ASICs with planar slim-edge sensor prototypes are currently in production.

Capacitively coupled active HV-CMOS sensors Hybrid assemblies of CLICpix prototype chips with CCPDv3 active sensors have been produced and tested. The sensors are implemented in a 180 nm high-voltage CMOS process [41]. A deep n-well above the low-resistivity (few Ωcm) p substrate surrounds low-voltage p-wells and acts as the signal collecting electrode. A nominal operation voltage of -60 V at the n-well results in a depletion layer of approximately 10–20 μm in the p substrate. The fast drift signal collected in this depletion layer passes through a two-stage transimpedance amplifier in each pixel and the resulting voltage signal is capacitively coupled to the CLICpix ASIC through a layer of glue a few microns thick. Laboratory tests with radioactive sources show a good signal-to-noise performance for the active sensor output. Preliminary test-beam results with CLICpix-CCPDv3 assemblies suggest a detection efficiency of > 99% for minimum ionising particles and a high fraction of single-pixel clusters with a position resolution of approximately 7 μm , as expected for 25 μm pixel pitch.

Through Silicon Vias (TSV) A “via last” TSV process developed in collaboration with CEA-LETI has demonstrated the feasibility of TSVs on functional readout ASICs from the Medipix/Timepix chip family [42]. The project uses Medipix3 readout wafers produced in 130 nm CMOS technology. The wafers are thinned to 120 μm and the resulting vias have a diameter of 60 μm . An ongoing continuation of the TSV project aims at producing TSVs in Timepix3 ASIC wafers thinned to 50 μm .

1.8.3 Engineering Challenges

The detector performance requirements lead to challenging constraints for the mechanical and electrical integration of the vertex-detector components and its cooling system. An integrated approach is followed, addressing several of the critical R&D issues in these domains:

Power delivery and power pulsing A low-mass power-pulsing and power-delivery system optimised for the small duty cycle of the CLIC machine has been developed [43]. Controlled current sources deliver a low and almost constant current (< 300 mA per ladder) into the vertex region through low-mass cables. The energy needed by the readout ASICs during the time of the collisions and detector readout is stored locally in silicon capacitors. Low-dropout regulators provide the necessary stability of the output voltage for the analog ($\Delta V \approx 16\text{mV}$) and the digital part ($\Delta V \approx 70\text{ mV}$) of the readout ASICs. Prototypes have been tested successfully with dummy loads emulating the power consumption of the 12 readout ASICs in a half ladder. The total contribution of the powering infrastructure to the material budget of each barrel layer is approximately $0.1\%X_0$. It is expected to decrease to less than $0.05\%X_0$ with evolving silicon-capacitor technology.

Cooling Even with power pulsing a total power of approximately 500 W will be dissipated in the vertex detectors alone. To limit the amount of material in the vertex-detector region, a cooling system based on forced air flow is under development [44]. Finite-element Computational Fluid Dynamics (CFD) simulations show that air cooling is feasible. For a mass flow of 20 g/s, the temperature increase in the vertex detector is limited to approximately 40 °C. The proposed cooling scheme is being validated in thermal mockups. Preliminary results confirm the validity of the simulations.

Mechanical supports The low overall material budget leaves only about $0.05\%X_0$ per detection layer for mechanical supports. Prototypes based on Carbon-Fibre-Reinforced Polymers (CFRP) are under study [45]. Bending-stiffness calculations have been validated in finite-element simulations and with bending tests. Measurements within an air-cooling mockup show that the air-flow induced vibrations are at an acceptable level of approximately $1 - 2 \mu\text{m}$ RMS amplitude for the direction perpendicular to the detector plane and at nominal flow conditions.

Assembly and access scenarios Assembly and access scenarios for in-situ testing have been developed, taking into account the constraints from the surrounding detector elements [45]. Realistic cabling layouts are proposed and evaluated in terms of their impact on the global and local material budget.

1.8.4 Future Plans

The technical development programme for the CLIC vertex detector aims at building demonstration modules for the main components of the vertex detector system in time for the next update of the European Strategy for Particle Physics in 2018/19. To reach this medium-term goal, several technology prototypes are under development. Ultra-thin edgeless hybrid pixel assemblies with Timepix3 readout ASICs (including ASICs thinned to $50 \mu\text{m}$ and processed with TSVs) are currently in production. The next version of the CLICpix demonstrator ASIC (CLICpix2) is foreseen to be produced in the second half of 2015. It contains a larger pixel matrix (128×128) and higher dynamic range (8-bit ToA and 5-bit ToT). Slim-edge and edgeless sensors matching the 128×128 CLICpix2 footprint have already been produced and an improved version of the CCPD active HV-CMOS sensor will be submitted for production by the end of 2015.

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
ChronoPix	University of Oregon Yale University Sarnoff Corporation	ChronoPix is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps per pixel during the bunch train. Hits are read out in the time between bunches.	April 2014: Device tests of prototype 2 inform the design of prototype 3 to be submitted to foundry	Prototype 3 was manufactured in September 2014. Tests have shown that problems revealed in prototype 2 were solved.
CMOS MAPS	IPHC Strasbourg DESY, Hamburg University of Bristol University of Frankfurt	The CMOS pixel sensor uses as a sensitive volume the 10–20 μm thin high-resistivity epitaxial Si-layer deposited on low resistivity substrate of commercial CMOS processed chips. The generated charge is kept in a thin epi-layer atop the low resistivity silicon bulk by potential wells that develop at the boundary and reaches an n-well collection diode by thermal diffusion.	2016 : production of CPS for the ALICE-ITS upgrade 2018/19 : production of CPS for the micro-vertex detector of the CBM experiment at FAIR/GSI 2018/19 : validation of light double-sided ladder concept combining highly granular sensors on one side with timestamping sensors on the other side < 2020 : validation of power pulsing of double-sided ladders inside a high magnetic field 2022/23 : finalisation of the R&D on various CPS adapted to the different layers of a very high performance vertex detector at the ILC	Until 2018-2019: Development and production of CPS for the ALICE-ITS and CBM-MVD Development of various CPS optimised for the different layers of a vertex detector at the ILC, with emphasis on bunch tagging Development of low material double-sided ladders
DEPFET	University of Barcelona, Spain University of Bonn, Germany Heidelberg University, Germany Giessen University, Germany University of Göttingen KIT Karlsruhe, Germany IFJ PAN, Krakow, Poland MPI Munich MPG HLL, Munich, Germany Charles University, Prague, Czech Republic IFIC, CSIC-UVEG, Valencia, Spain DESY, Hamburg, Germany IFCA, CSIC-UC, Santander, Spain	The DEPFET technology implements a single active element within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted, detector-grade bulk silicon. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate.	2014: Full-scale 75 μm thin Belle II ladder in beam test at DESY	Development of die-attach technology Full-scale test of all ASICs on ladder Integration of read-out and steering ASICs on pixel sensor using flip-chip technique and microscopic solder ball bump-bonding Production of Belle II vertex detector modules Tests of the last version of the DHP chips Engineering design for all-silicon module with petal geometry required for ILC Detailed characterization of device response Design of ancillary ASICs, taking full responsibility for future design cycles of the FE read-out chip, called Drain Current Digitizer
FPCCD	KEK Shinshu University Tohoku University JAXA, Japan Aerospace Exploration Agency	Fine Pixel CCD sensors have pixel sizes of 5 μm and a fully depleted epitaxial layer with a thickness of 15 μm	Fabrication of real size (12.3 mm \times 62.4 mm) sensors with 50 μm total thickness Neutron irradiation of a small (6 mm \times 6 mm) FPCCD sensor Construction of a prototype cooling system and demonstration of cooling between -40°C and $+15^\circ\text{C}$	Characterization of FPCCD sensors including beam tests and radiation damage studies Development of FPCCD sensors with a pixel size of 5 μm Construction of prototype ladders for the inner layers of a vertex detector Development of readout electronics downstream of ASICs Development of larger FPCCD sensors and prototype ladders for outer layers Development of readout electronics with a small footprint Construction of a real size engineering prototype and cooling test
3D Pixels	Brown University Cornell University Fermilab Northern Illinois University SLAC University of Illinois Chicago	3D technology allows very fine pitch (4 μm) integration of sensors with multiple layers of electronics, allows interconnection to both the top and bottom of devices, and provides techniques for low mass, thinned devices.	Completed multi-year effort to demonstrate commercial 3D technology, consisting of 0.13 CMOS interconnected with Direct Oxide bonding technology and access using TSV. Received readout wafers with thickness of 25 μm , processed with TSV and DBI to connect to 3D electronics Currently working on active edge demonstrator devices	Complete the 3D active edge project Apply concepts to x-ray imaging devices Re-start ILC developments pending renewed funding
SOI	KEK University of Tsukuba Tohoku University Osaka University	In the Silicon-On-Insulator (SOI) technology the sensing and processing functionalities are separated in different layers; the sensing is provided by a high-resistive substrate connected through an insulating layer with the processing layer.		Sep 2014: Complete architecture study for the ILC pixel detector Mar 2015: Design and fabrication of first test chip for the ILC Dec 2015: Beam test of the chip
CLICpix	Cambridge University CERN University of Geneva Karlsruhe Institute of Technology (KIT) University of Liverpool SLAC Institute of Space Science Bucharest Spanish Network for Linear Colliders	Hybrid pixel-detector technology comprising fast, low-power and small-pitch readout. ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin planar or active HV-CMOS sensors via low-mass interconnects.	Beam tests of prototype assemblies with ultra-thin sensors (50–300 μm) CLICpix demonstrator ASIC in 65 nm technology Beam tests of assemblies with capacitive coupling between CCPDv3 HV-CMOS active sensors and CLICpix ASICs Power-pulsing demonstrator with dummy loads Prototypes of carbon-fibre ladder supports Full-scale thermal mockup of the CLIC vertex-detector region	Demonstration modules for all major components in time for the next update of the European Strategy for Particle Physics in 2018/19

Chapter 2

Silicon Trackers

2.1 Long-Ladder and Charge Division Tracking R&D

Contact person: Bruce Schumm (email: baschumm@ucsc.edu)

2.1.1 Introduction

The SiD collaboration has done microstrip R&D in two directions that might provide attractive alternatives to the SiD baseline: the exploration of the long-ladder limit for precision microstrip tracking, and the exploration of the use of ‘charge division’ – reading out resistive electrodes from both ends – to glean information about the longitudinal position of the track along the length of the sensor.

Two activities have been undertaken for the exploration of the long-ladder limit: the development of an optimized, time-over-threshold readout ASIC (the LSTFE chip) and a lab-bench study of the noise limitations associated with reading out long, thin electrodes. The possibility of using charge division to determine the longitudinal coordinate of deposited charge with sub-centimeter precision was explored using a mock electrode network read out with an optimized amplification and shaping chain. Milestones have been achieved in all three areas.

2.1.2 Recent Milestones

The properties of this Long Shaping-Time Front End (LSTFE) microstrip readout ASIC have been optimized for the readout of long ladders of silicon strip sensors that are motivated by the need for precise low-mass central tracking for a Linear Collider Detector. With a small and straightforward change to the shaping properties of the ASIC, it could be re-optimized for use for the short strips and high occupancy that would be expected for ILC forward-tracking applications. The LSTFE features optimized initial-amplification characteristics and shaping time to reduce voltage-referenced readout noise, as appropriate for narrow-strip, long-ladder applications. Unique to the LSTFE design, however, is the use of time-over-threshold readout to estimate the analog pulse-height generated by subatomic particles passing through. A pulse-development and readout simulation developed for the purpose of the designing the LSTFE suggests that the intrinsic statistical fluctuations of the charge-deposition process in 300 μm of silicon obviate the need for a precise measurement of deposited charge. A simulation of the centroid-finding (position-resolution)

uncertainty provided by time-over-threshold readout showed little degradation relative to that provided by an exact measurement of deposited charge.

On the other hand, there are several advantages offered by the use of time-over-threshold readout. It is very simple to implement within a digital back-end to the LSTFE’s analog front end (the implementation would be on the same chip as the front-end readout), requiring only a measurement of the number of clock counts that the given channel is over threshold, and then the assembly and transmission of a single data word containing the time of the upward transition, the time over threshold after the transition, and the channel number. This happens in real time and is driven immediately off the chip into the DAQ, eliminating the need for buffering and ADC conversion. In particular, there is no limit to the rate at which particles can be detected other than the return-to-baseline of the analog signal, and so the data-accumulation rate capability of the device is very high. In addition, for forward tracking, for which short strips are envisioned, the shaping time can be shortened significantly. This will further improve the rate capability of the LSTFE readout, making it an excellent choice for the high-occupancy forward region.

The possibility of obtaining a longitudinal coordinate from silicon microstrip sensors has been explored [46], making use of the implant as a resistive electrode, with no overlain metallic electrode. A mock resistive microstrip-implant electrode network was constructed on a PC board out of discrete resistors and capacitors which was read out on both ends by an amplifying and shaping chain that was optimized to give the greatest precision in the longitudinal position of the charge deposition on the implant. For a 10 cm-long sensor, a longitudinal resolution of 6 mm was observed, achieving the resolution needed to aid in tracking reconstruction in dense jet environments. Finally, sources of readout noise were measured and modeled for sensors in the long, thin strip electrode limit [47]. The readout noise observed with the LSTFE ASIC was measured as a function of the length of a daisy-chained ladder of sensors, and the results modeled with a SPICE simulation. It was found that network effects due to the distributed resistance and capacitance of the electrode provide significant mitigation of the readout noise relative to the assumption of single, lumped elements. It was also found that reading out the ladder at its center rather than from one end provided further noise suppression. Attaching this noise model to the pulse-development simulation developed for the LSTFE design suggested that ladders of as much as 75 cm long could be made operation with end readout. Ladders approaching 1 m in length could be operated with center readout.

2.1.3 Engineering Challenges

The primary remaining engineering challenges are the implementation of LSTFE power-cycling with a $\approx 1\%$ duty cycle, and the transfer of the digital back-end processing of the LSTFE information from an off-chip FPGA directly onto the ASIC.

2.1.4 Future Plans

Because of this work, the possibility of a tracker making use of long ladders of silicon microstrip sensors, or shorter strips with time-over-threshold readout in the forward region, remains an option for the SiD detector. However, at this time resources are being directed towards the modular KPiX design.

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2.2 Resistive charge-division on thinned micro-strips sensors with low signal amplification

Contact person: Ivan Vila Alvarez (email: ivan.vila@csic.es)

2.2.1 Introduction and Motivation

In the context of the ILC, the relatively low occupancy environment and the power pulsing operation of the front-end electronics provide an opportunity for the implementation of ultra-lightweight silicon-based tracking systems where the dominant contribution to the material budget in the fiducial volume comes from the sensors. Reducing the material budget has a major impact on the hit position resolution and hence the momentum resolution of the tracker system; therefore, we have pursued during the last three years an RD program for the development of very thin micro-strips sensors able to provide two dimensional information of the hit position.

The ultimate goal of this R&D is the development of a micro-strip sensor which combines signal amplification — allowing the thinning of the sensor’s substrate — and resistive electrodes — allowing the implementation of the charge-division method for the determination of the hit position along the strip direction. In a first phase, we are aiming to demonstrate the feasibility of each of the above mentioned features independently and, in a second phase, to integrate both technological solutions into the same micro-strip sensor; the thinning of the sensor will be done using the anisotropic wet etching (TMAH process) used for the DEPFET fabrication [1.3](#).

2.2.2 Recent Developments and Milestones

The use of the charge-division method in long micro-strip sensors, with a length of several tens of centimeters, was proposed as a possible tracking technology for the International Linear Collider detector concepts a few years ago [\[48\]](#). More recently, we have demonstrated [\[49, 50, 51\]](#) the feasibility of the charge division concept on fully fledged micro-strip sensor with resistive electrodes made of poly-crystalline silicon achieving a spatial resolution along the strip direction of about 7% the strip length. One of the limitations of this technology is the attenuation of the signal along the resistive electrode; additionally, the position resolution along the strip is proportional to the signal-to-noise ratio. Therefore, to maintain or even increase the SNR without increasing the sensor substrate thickness we proposed the integration of signal amplification structures in the sensor itself. The Low Gain Avalanche Detector (LGAD) technology appears as a well suited technique for achieving the signal amplification. LGAD devices engineered as reach-trough avalanche detectors with a moderate gain where initially proposed and developed for timing application [Pellegrini 2014], the moderate signal amplification ensured that a relatively standard front-end readout electronics could be employed. As a spin-off of this original aim, we introduced the i-LGAD micro-strip concept for tracking, a LGAD device implemented in a p-type substrate where the ohmic electrode is strip-wise segmented; this design favors the uniform signal amplification over the sensors active volume overcoming the non-uniform gain in LGAD micro-strips sensors with a strip-wise segmented amplification layer that we recently characterized [\[52, 53\]](#). The former R&D line is complemented with the development

of a dedicated ASIC using a 180 nm AMS fabrication process which integrates a charge amplifier with long shaping time and time stamping functionalities; finally, we completed the study and testing of several pulsed power system topologies based on super-capacitors.

2.2.3 Engineering Challenges

Concerning the component aspects, the main challenges are to complete to proof-of-concept of the thinned micro-strips with charge amplification and resistive charge-division in a implementation suitable for the LC tracking needs, namely: proof the i-LGAD concept, integrating amplification and charge division, thinning of sensors substrate, large area sensors, manufacturing long ladder by daisy chaining of the sensors. Concerning the read out ASIC, the main challenge will be the design of the front-end with the required functionalities while keeping the power dissipation low enough. System wise, the main challenge is the design of an air-based cooling system and its integration on the CFRP supporting structure such that the material budget of the system remains acceptable from the point of view of it tracking performance.

2.2.4 Future detector R&D

During the next two years we will focus our activities on the testing of the i-LGAD devices and, if the results were positive, the integration of the low gain amplification and manufacturing of large area sensors (100 cm^2). Concerning the front-end electronics, the main goal will be to complete a few channel demonstrator integrating the long shaping time amplifier and power pulsing. A real scale thermo-mechanical mockup is of the FTD sub-detector at ILD is currently under construction to assess different air forced cooling options.

2.3 KPIX

Contact person: Marty Breidenbach (email: mib@slac.stanford.edu)

2.3.1 Introduction

KPiX is a 1024 channel “System on a Chip” intended for bump bonding to large area Si sensors, enabling low multiple scattering Si strip tracking and high density Particle Flow calorimetry for SiD at the International Linear Collider (ILC).

Each channel consists of a dynamically switchable gain charge amplifier; shaping; threshold discrimination; and 4 sample and hold capacitors and 4 timing registers. The chip permits 4 separate measurements of amplitude and time of threshold crossing during each train, and amplitude digitization and readout during the intertrain period. The dynamic range is from sub minimum ionizing particle (mip) (in $320 \mu\text{m}$ silicon) to more than 2000 mip. KPiX also has a calibration system for each channel, servos for leakage compensation, “DC” reset for asynchronous operation for testing with cosmic rays, and polarity inversion for use with GEMs and similar detectors. The noise floor is about 0.15 fC (≈ 1000 electrons), and the maximum signal is 10 pC (utilizing the dynamic range switching). The full dynamic range corresponds to 17 bits.

2.3.2 Recent Milestones

ILC related R&D in the US is largely unfunded and small efforts are being kept alive on the margins. The KPiX R&D is such an example of necessary work for SiD that is marginally alive.

2.3.3 Engineering Challenges

At this time, KPiX is seen as the baseline readout system for the tracker and electromagnetic calorimeter. A stack of 13 EMCal sensors with bump bonded KPiX was assembled for a beam test at SLAC in the summer of 2013. That test discovered that two kinds of crosstalk are significant:

- In-time crosstalk occurs due to parasitic coupling of traces on metal 2 of the sensor to other pixels. The level of crosstalk increases with the size of the signal, and decreases with increased speed of the front end charge amplifier (meaning increased current and power dissipation). A new sensor design is being developed that uses metal 1 to shield the traces of metal 2, and these ideas will be tested in the next sensor prototype.
- Out-of-time cross talk occurs when many pixels are hit and reset simultaneously. The resets collectively cause other pixels to trigger, and a cascade builds up. This uses up all the KPiX buffers. The root cause of the problem appears to be some internal logic within KPiX that is not current limited, and will require design modification.

A more general issue is that both the EMCal and tracker sensors from Hamamatsu were ordered with Al pads, as it was believed that plating (by the zincate process) a stack of metals culminating with Au would be straightforward. This turns out to be wrong. Future sensors will be ordered with Au pads.

An additional issue is that the Tracker sensor was planned to be wire bonded to its (very thin) cable. The sensor oxide layer is not strong enough to allow wire bonding without damage, and so must be solder bumped. The pad pitch is small, and solder bumping the cable will be challenging. The trouble with the wire bonding to the sensor was unexpected. Another concern is that the current design of KPiX has deadtime after a pixel has accepted a trigger. Only the triggered pixel is affected; all the other pixels are available for signals. This deadtime is different from the usual notion of data acquisition deadtime where the entire detector is unavailable, but the correction to the luminosity integral is easy. Finally, the buffer requirement (4 in the current version of KPiX) is being re-evaluated in SiD simulations. A possible new architecture for KPiX is in early stages of evaluation. A small mechanical engineering effort has started to study the structure of the EMCal. The SiD EMCal has emphasized thin gaps between the tungsten layers to minimize the Moliere radius, and this implies that the structure is connected by columns at the vertices of the sensors. The DBD design shows hexagonal sensors, which indeed are the most efficient way of tiling large areas, but no consideration was given to the edges of these arrays. The design is being re-evaluated to optimize the cost-effectiveness over the whole area taking into account geometric efficiencies and total wafer cost. Tracker sensors are now at IZM for the pad plating and subsequent bonding of KPiX; they will then go to UCD for cable attachment and testing.

2.3.4 Future Plans

Assuming positive developments with Japan are announced soon, we expect the financial support to improve. It should be noted that an important effect of the withdrawal of support is that most of the US collaborators have been forced to move to other work.

- EMCAL Sensors: A second round of prototypes will be designed and ordered with rectangular layout; shielded traces, and Au pads.
- Tracker Sensors: The current prototypes will be evaluated, and if appropriate tested in a beam.
- KPiX: A new architecture with little (or no) deadtime will be evaluated. A decision will be made to develop this new architecture or incrementally.
- improve the existing design.
- The EMCAL mechanical structure will be pushed towards a conceptual design.

R&D Techn

text

Chapter 3

Gaseous Trackers

LCTPC collaboration spokesperson: Jochen Kaminski (email : kaminski@physik.uni-bonn.de)

Detectors for a high energy linear electron positron collider have been discussed since the early 1990's. For the main tracking a TPC was proposed early on. The advantages of a TPC are its ability to detect track elements in 3 dimensions while introducing very small amounts of dead material. A potential disadvantage could be the appearance of distortions due to $E \times B$ effects in the drift region, originating from possibly inhomogeneous magnetic or electric fields, which could be a consequence of the construction or from space-charge build-up as a result of ion back-flow.

In 1996, the first Linear Collider detector conceptual report [54] considered the possibility to read out the end-cap chambers with MSGC, Micromegas and GEMs. Several advantages of the MPGDs were recognized immediately: the ion back-flow could be very limited by a suitable choice of the field configuration, and the $E \times B$ effects present close to the wires of a MWPC are very limited in the case of the microscopic structure of a MPGD. However it was also recognized that, to profit from the excellent resolution allowed by a limited diffusion and a very localized avalanche, either sufficiently small pads would be needed, to share the charge among several pads, or a mechanism for spreading the avalanche was needed. Without such a sharing, the only information obtained would have been which pad received the charge, and the hit position would have a flat probability over the pad width, limiting the resolution along a pad row to $p/\sqrt{12}$, p being the pitch over a pad row. It was also understood that for a multi-stage GEM, the amount of natural spreading by diffusion in the gas amplification device itself, about 300 μm r.m.s., was sufficient to obtain enough charge spreading with $\sim 1\text{ mm}$ wide pads. For Micromegas, where the avalanche has typically a 15 μm r.m.s., an additional charge-spreading mechanism was necessary, even for 1 mm pads. Such a method was introduced by the Carleton group, using a superposition of an insulator and a resistive cover. This arrangement provides a continuous Resistor-Capacitance (RC) network over the surface which spreads the charge around the avalanche. The induced signal is measured, shaped and digitized by the electronics connected to each pad. Note that this technique is applicable also to GEMs and allows pad widths of 2, 3 or more mm.

At the beginning of the years 2000, several small prototypes were built in Aachen, Amsterdam, Saclay-Orsay with a Berkeley electronics, DESY, Munich, Karlsruhe, Carleton, Victoria, Saga, KEK, Tsinghua, to study various aspects of the GEM and Micromegas technology. Ion feed-back was studied, resolution was measured in various prototypes, and the possible gases were studied. The fundamental proof was made that a TPC with MPGD readout can be operated stably, and can reach intrinsically the anticipated resolutions.

Then, in 2004, part of the nascent collaboration gathered around a 5 GeV pion beam and cosmic-ray

tests at KEK. The detector was immersed in a 1 T magnetic field from a permanent-current superconducting magnet. The 25 cm drift field cage was designed in Munich and electronics was recuperated from ALEPH. Several endplates were adapted to this cage with wires, Micromegas (without resistive foil) and GEM technologies. In 2006 the Carleton 16 cm drift length prototype with a Micromegas resistive foil took data simultaneously with the Munich prototype.

At the same time other developments took place in other institutes. Noteworthy was the use of 2 parallel laser beams in Victoria and later at DESY to study 2-track separation. This study showed that a separation of two tracks was possible down to 1 pad size distance between the laser beams.

Several groups carried out tests in a 5 T magnet at DESY in the years 2003-2007. The operation in such high fields could be established for both Micromegas and for GEMs, and the extrapolation of the resolutions previously measured at lower fields could be demonstrated.

The next step then was the construction and operation of a common large prototype. The European Union - funded project EUDET allowed a facility to be built at DESY, with a 1T SC magnet offered by KEK, a field cage designed at DESY, an endplate brought by Cornell, a cosmic trigger with SiPMs built by Saclay, a beam trigger from Nikhef, a gas system from DESY and Rostock, high density readout electronics by Saclay and Lund, etc..

The endplate has 7 openings to receive up to 7 identical modules. The “keystone” shape of the modules is chosen to be as close as possible to the anticipated real configuration of a disc paved by concentric rows of modules. Data taking started in 2008 in the fixed magnet. At this time, to shoot the beam at a given z position along the drift axis was possible only by sliding the TPC in the magnet; this way, the large drift distances could only be obtained by taking the TPC in a very inhomogeneous field. This was solved the following years by the installation of a moving stage allowing horizontal and vertical translations, as well as rotations in the horizontal plane. Rotation of the TPC around the magnet axis could be performed by hand.

Since then beam tests took place nearly every year, alternating between GEMs from Japan, Micromegas, GEMs from DESY, and pixels.

3.1 GEM based Readout

Gas Electron Multipliers (GEMs) [55] have been invented in the mid 90's. They consist of a thin polyamide foil, covered with Copper on both sides. Holes are produced into the foil on a regular pattern. Typical dimensions are a hole pitch of $140\text{ }\mu\text{m}$ and a hole diameter of $70\text{ }\mu\text{m}$. If an electric field is applied between the two sides of the foil, high fields form inside the holes, and provide avalanche gas amplification. Since the high fields are constrained inside the holes, many of the high-voltage problems connected to traditional wire based chambers are not relevant. GEM foils can be stacked to provide tailored gas amplification. During the years a number of different types of GEM foils have been developed. They differ for example in the cross section of the holes, in the material of the foil, and in the pitch and hole sizes. For application in the ILC TPC currently two main options are being pursued. The first one is based on a GEM where a laser is used to "drill" each hole. The resulting holes are strictly cylindrical. The second option is based on a chemical etching process. The resulting holes have a double conical shape.

In addition to the different types of GEM foils two different schemes to build readout modules for the TPC are investigated. Scheme one (called module type A in the following) relies on a sturdy aluminum frame where the GEM foils are stretched between the bottom and the top of the readout module. This scheme allows to build a module which has essentially no dead area on the side of the module, but where some dead space is needed on the top and the bottom. The second option (called module type B in the following) relies on an assembly of a stiff but thin ceramic frame which when glued to the GEM provides a self-supporting stiff assembly. The width of the frame is around one millimeter, so that in this approach a small dead area is present all around the module. Both approaches allow the stacking of GEM foils, and both are compatible with the installation of a gating GEM on top.

3.1.1 Module Type A, "Asian Module"

Contact person: Akira Sugiyama(email: sugiyama@cc.saga-u.ac.jp)

The Asian modules use GEM stacks as a gas amplification stage and are optimised to reduce the insensitive area on the sides of the modules which point towards the detector center. A module can be seen in figure 3.1.

Particles from the interaction point passing between the modules may not be detected if they have very high momenta. Therefore, the Asian module foresees no frame along the sides and extends the sensitive area up to the edge of the backframe. To ensure a flat mounting of the GEMs, they are stretched on both the upper and lower arcs (as seen in figure 3.1) which are made of a stiffer material: GEMs with an insulator of $100\text{ }\mu\text{m}$ Liquid Crystal Polymer (LCP) covered with $5\text{ }\mu\text{m}$ copper on both sides were produced by a company named SciEnergy. The holes were produced by CO₂-laser drilling after which they were carefully cleaned by dry etching to remove potentially conductive residuals from the insides of the holes. The hole pattern is identical to standard CERN GEMs. Because of the thicker material also higher gas gains per GEM can be reached and a double GEM structure is used and considered to be sufficient. The two GEMs are mounted with an induction gap of 2 mm and a transfer gap of 3 mm.

The pad size is $1.2 \times 5.4\text{ mm}$ and there are 28 pad rows with a total of 5152 pads. From the beginning the use of an ion gate (see subsection 3.5) was envisaged and, thus, the level of the first GEM was designed to be 1 cm below the nominal module height allowing for a later addition of the gate. To absorb the strength necessary to stretch the GEMs and the gate, strong metal poles were implemented at the top and bottom arc.

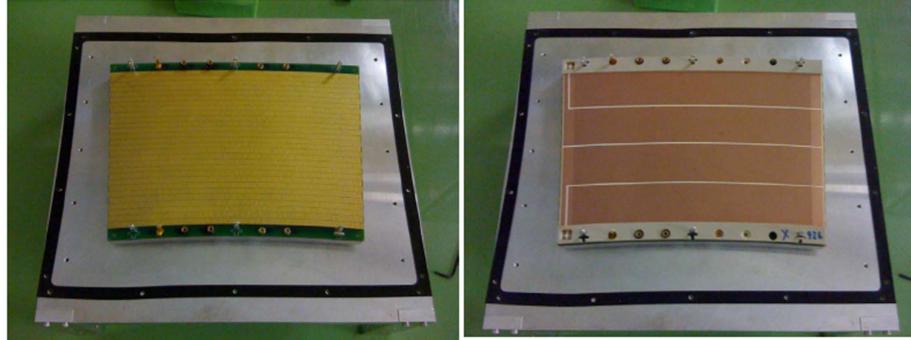


Figure 3.1: Asian GEM picture: left - anode pad plane; right - segmented cathode.

3.1.2 Recent Milestones

All modules have been tested in the Large Prototype at DESY. The experience gained during all test beam periods as well as the best transverse spatial resolution is described next. The testbeam measurements have used the gas mixture of Ar-CF₄(3%)-isobutane(2%). The electric drift field was set in most cases to E=230 V/cm, which is close to the maximum of the drift velocity, and alternatively to E=130 V/cm, which is the minimum of the transverse diffusion. The Asian modules were also measured using a laser system, in order to analyze the distortions. The laser beam was scanned across the module, and the deviations were compared with calculations and are understood.

The Asian groups built three modules and made several test beam measurements at DESY (2009, 2010, 2012). The first campaigns were dominated by very strong field distortions because of the mounting pins and the bare frames. After introducing the field shaper, the distortions are comparable to the ones of other techniques used for modules. The transverse spatial resolution is shown in figure 3.2, where the measured spatial resolution of a single row in the middle of a module can be seen.

In this context an analytical formula was developed to predict the spatial resolution of a TPC. This formula includes not only the effect of diffusion, angle, noise and a finite pad-size, but also the influence of the electronics threshold, number of effective primary electrons, the Polya-parameter of the gas amplification, cross talk between pads and signal lines, charge loss because of attachment and the pad response

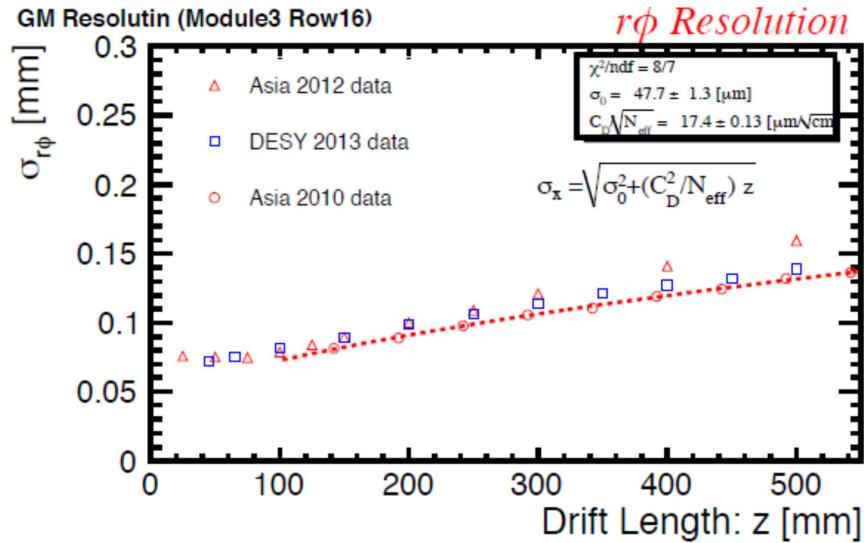


Figure 3.2: Resolution measured for the Asian GEMs, and compared with a result for the DESY GEMs.

function are taken into account. All these parameters can be varied and, if correctly chosen, describe well the measured data.

Finally, one other important observation was the HV micro-discharges on the Asian GEMs, with associated gain drops, and investigations of this problem are summarized here.

To minimize the energy released in a discharge, the GEMs were segmented into four arcs, each with an area of about 100 cm^2 (figure 3.1, right). Studies of the micro-discharges for the various types of GEMs were measured under a controlled environment. The $100 \mu\text{m}$ Asian GEMs discharged frequently, while the DESY $50 \mu\text{m}$ GEMs (made by CERN) had little or no discharges. For the $50 \mu\text{m}$ GEMs, there is no significant difference of the discharge rate between different types of GEMs. It is noteworthy that, at low gain, the $100 \mu\text{m}$ GEMs had a discharge rate which is almost the same as for the $50 \mu\text{m}$ GEMs. The water content in the gas does not seem to influence the discharge rate, and long-term measurements are in progress.

3.1.3 Future Plans

In the future, it is planned to:

- understand better the reasons for the micro discharges and eliminate them, and
- construct a full scale Asian module with gate.

3.1.4 Module type B, “DESY Module”

Contact person: Ties Behnke (email: ties.behnke desy.de)

The goal of module type-B is a maximal coverage of the endplate with minimal dead area and a low material budget. It relies on thin ceramic frames to support the GEM foils on top of the readout plane [56, 57], see figure 3.3. The high stiffness of the ceramic frame allows the construction of very thin frames, which in turn minimize the dead areas of the module. With the current design only $\sim 5\%$ of the active area is taken by the support structure and gaps between modules, the rest is sensitive area. The design of the system allows the simple stacking of GEM foils to build up compact, light weight self supporting multi-GEM modules. The development of this module type is led by DESY.

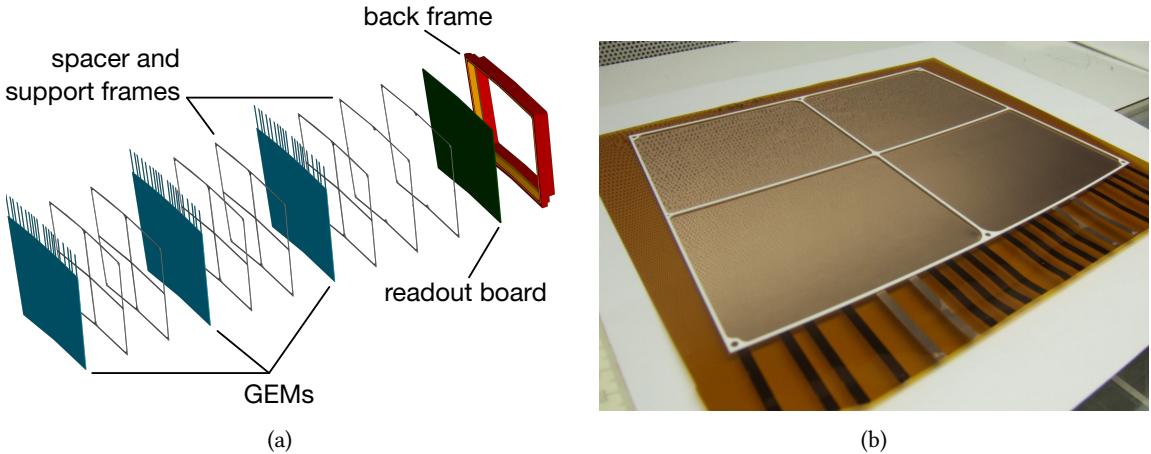


Figure 3.3: a) Exploded view of one module showing the sequence of GEM foils and ceramic frames. b) GEM foil with ceramic frame support used in the construction of the modules.

3.1.5 Recent Milestones

Over the last years several test-beam campaigns took place and exposed three GEM based modules to test beam. Extensive data sets were collected with and without magnetic field, at different working points, and at different angles between the TPC and the beam.

For the first time the data taken were used in a global attempt to determine and correct field distortions. The Millepede-II [58, 59] program was used to perform this global fit. First results indicate that distortions as large as several millimeters can be well corrected, see figure 3.4a. The resolution obtained both in $r\varphi$ and z behave as expected, and, if extrapolated to the running conditions at the ILC, meet the requirements, see figure 3.4b.

The field homogeneity was in addition studied in dedicated laser runs [60]. A UV laser illuminates the cathode plane in the TPC, on which dots are placed made from a material with a small work function. The laser light extracts electrons at the position of the dots. These electrons are then drifted towards the anode, and are measured. From the dislocations of the dots relative to the known position on the cathode, the integrated effect of field distortions in the TPC volume can be measured.

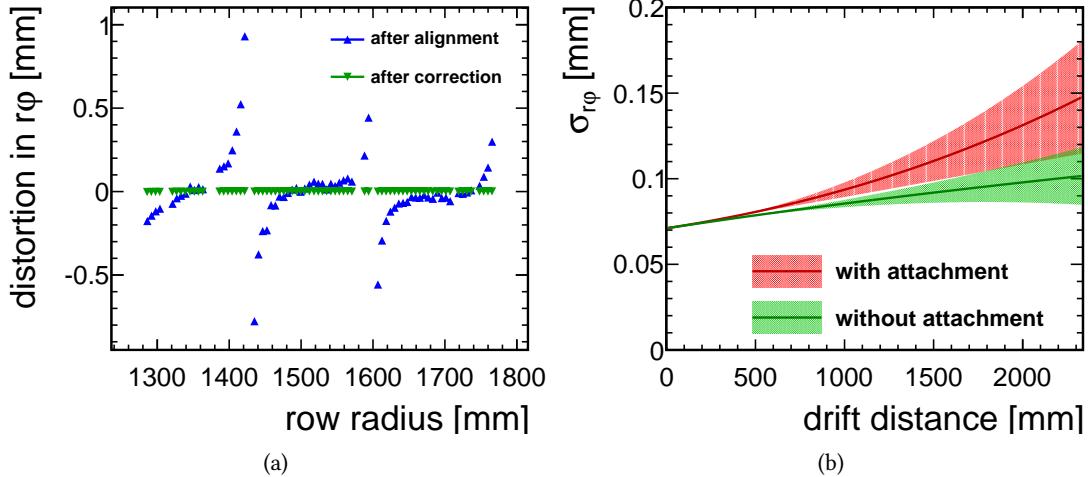


Figure 3.4: a) Alignment and distortion correction: mean hit position in $r\phi$ with respect to the track position at 1 T versus pad row radius. In blue after alignment correction, in green after distortion correction. b) Point resolution: extrapolation to a magnetic field of 3.5 T based on parameters measured with the Large TPC Prototype at 1.0 T. Plotted over the full ILD TPC drift length of 2.35 m including 1σ error bands. In red with the measured attachment rate, in green without any attachment.

Extensive simulations of the behavior of the GEM foils in case of electrical breakdown were performed. They showed that a strong coupling exists between the different regions of the GEM foil. In some cases these couplings can trigger secondary trips in the module, which in rare cases can damage the GEM. A protection circuit is currently under development and will be tested in the near future.

3.1.6 Future Plans

By now two generations of these modules have been developed and successfully tested. The main issues which are going to be addressed in the next 1-2 years are

- re-optimisation of the support structure for maximum mechanical strength and minimal interference with the readout
- development of a protection scheme which will ensure safe operation of the module even in case of high-voltage trips.
- optimization of the field-shaping integrated into the module, to minimize field distortions close to the module and at module boundaries.
- integration of a GEM based gate on top of the current amplification structure, based on the recent developments at KEK.

It is planned that within the next six months a third generation module design will be developed and several modules built which will address these challenges.

3.1.7 Engineering Challenges

A detailed study is ongoing to understand and quantify the mechanical behavior of the ceramic frame GEM system. Bending tests have been performed, and compared to simulations. The interference between the mechanical properties and the electrical properties are studied. Measurements of the flatness of the module are being done, and will provide input for the next design iteration. The fabrication of the ceramic frames which is currently done by laser cutting from solid sheets of ceramic will be studied. Possible alternatives are 3D printing of the frames. Improvements in the laser cutting technology might allow thinner frames, without loosing stiffness.

Another open question is the distribution of the high voltage from the endplate to the different GEM layers. The current solution is rather labour intensive, and relies heavily on the skills of the person doing this connection. Faults are difficult to find, and even more difficult to repair. Here new solutions are being sought, which are more easily to produce, more reliable, and will give better high voltage security. Connected to this are the protection schemes against accidental high voltage discharges, which are still not perfect.

As discussed in section 3.5, a gating GEM will be implemented as part of the amplification scheme. This gating GEM needs to be mechanically integrated into the module.

Currently a gap of about 2 mm exists between neighboring modules. This gap introduces significant field distortions [60]. They are partially compensated by a field shaping strip on the outside of each module. However a better and more robust solution would be to further minimize the gap between modules. Doing so will need improvements of the high voltage distribution, as discussed above, but also of the overall mechanical integration of the modules into the endplate.

3.2 Resistive Micromegas

Contact person: Paul Colas (email: paul.colas@cea.fr)

3.2.1 Introduction

First Micromegas prototypes were built with a micro-mesh stretched on a frame, and kept on top of a segmented anode at a fixed distance of 50 μm . The gap is defined by spacers manufactured by photolithographic techniques. Early tests confirmed that, due to “hodoscope effect” a resolution down to 100 μm could not be reached [61]. This triggered studies with charge spreading developed at Carleton University [62]. The first resistive material was an AlSi CERMET deposited on a Mylar foil and glued at 90 °C with layer of melting polymer [63]. Later on, a more robust resistive material was used: the Dupont-de-Nemours Carbon-loaded Kapton. Novel way to manufacture the Micromegas detector were perfected by the Saclay group in partnership with CERN.

3.2.2 Recent Milestones

From 2008 onward, tests with resistive Micromegas were performed in the Large Prototype. From 2008 to 2010 a single module sitting in the middle of the endplate was tested, with dummy modules all around. The 1726 pads, each about 3 mm wide and 7 mm long, were arranged in 24 lines and 72 radial columns, with 2 pads sacrificed to bring the high voltage to the mesh through the PCB. The standard electronics from the T2K/ND280 neutrino experiment based on the AFTER chip was used, connected through 20 to 40 cm long flat cables [64]. To minimize the dead area, the so-called “bulk” [65] process was used to fix the mesh on the PCB: in this process a stainless-steel mesh is held by polyimide pillars sandwiching the mesh, melt together through the mesh. This makes a robust and dust-proof detector, with only 2 mm taken by a grounding ring at the periphery of the module. This ring is used to fix the potential of the resistive anode all around.

Data taken in this 1-module configuration allowed several resistive coatings to be tested. Resistive pastes were discarded, as their electrical properties were not uniform enough and lead to distortions on the hit position. Carbon-loaded Kapton gave very good results, with a resolution down to 70 μm at zero drift distance.

Starting in 2011, a completely new integration of the electronics has been carried out to allow the simultaneous operation of 7 modules. Naked chips were directly wire-bonded on cards. All the protection of the electronics was removed, this functionality being fulfilled by the resistive coating. The ADC was moved from the front-end to a mezzanine card, all the electronics fitted just behind the module. At the same time the noise and the power consumption were lowered by 25%. To connect a module with 1726 channels, only 3 cables need to be connected: a High Voltage cable for the gaseous amplification, a low voltage cable to supply the electronics, and an optical fiber to transport the data and the command parameters to the mezzanine card. The production of 9 modules (including 2 spares) and their electronics followed a quasi-industrial scheme.

Data with 7 modules were taken in 2014 and 2015, allowing new topics to be addressed, as module alignment and distortions. ExB effect induces distortions for tracks reconstructed near the module boundary causing shifts of almost 1 mm for pad hits located at the extremity of the module.

This is in agreement with the simulations carried out in the Kolkata group and which can be corrected down to 20 μm .

In 2014 and 2015, a two-phase CO₂ cooling was provided to the 7 Micromegas modules. The two-phase coolant, under a pressure of 50 bar, circulates at a temperature close to the ambient. It consists presently of a serpentine running on the back of the modules, in good thermal contact with Aluminum heat sinks, themselves in contact with the chips. The pipe diameter is less than a millimeter, giving a moderate contribution to the material budget. The unit which provides the pressurized CO₂ was funded by KEK and designed by a Nikhef-CERN collaboration. An efficient cooling was observed for more than 80 hours continuously.

In 2015, two new modules were inserted on the endplate. The resistive material of the new modules was Diamond-Like Carbon obtained by sputtering on a Kapton foil. This gives a very robust resistive anode, and the procurement of this material, made in Japan, is more reliable than the Dupont Carbon-loaded Kapton. These two modules showed identical performance as the other modules.

3.2.3 Engineering Challenges

First paragraph to be moved to electronic section... A higher density of the electronics might be necessary, to mitigate the background at small radius and to improve two-track separation where the track density is highest, as well as the fake hit density. This can be done by switching to the 65 nm technology for the chip design. Though the present consumption is rather moderate (15 mW/channel), a suitable power-pulsing operation should be adapted. Early estimates show that such a system can be designed, but requires a careful balance between power saving and increased complexity.

Special care will have to be given to the design of the edge of the modules, to have a uniform potential on the exposed surface of the pad while the boarders of the modules must be grounded.

The adaptation of a gating device at a few cm from the end-plate, or integrated to each module, is a difficult engineering challenge if a minimal degradation of the performances is to be obtained.

3.2.4 Future Plans

The time structure of the beams will produce positive ion backflow disks moving slowly (at a few 1 m/s) towards the cathode. To experimentally address the question of the effect of these ion disks on the drifting electrons, it is projected to produce such ions by casting UV light to the cathode for a ms every 100 ms or so, while observing distortions on cosmic-ray or beam tracks. Last but not least, the momentum resolution should be evaluated with long tracks from a particle beam, which requires a silicon tracker inside the magnet to measure precisely the track position and momentum. For the cooling, further integration work is needed, using micro-channels in the detector board and new material choices for the sink.

In summary, the Micromegas TPC R&D successfully underwent its proof-of-principle phase and the main integration questions are now addressed. They now request targeted design to progress, thus specific project funding.

3.3 Pixelized Readout

Contact person: Klaus Desch (email: desch@physik.uni-bonn.de)

3.3.1 Introduction

To make the most of the fine pitches of the Micropattern Gaseous Detectors the readout structure should be adapted to the same feature size. Therefore, readout ASICs of silicon pixel detectors such as the Timepix ASIC [37, 66] can be placed directly below the gas amplification stage. In this setup, the bump bond pads normally used to connect the readout chip to the Si-sensor are used as charge collection pads. In some studies a triple GEM was used as a gas amplification stage [67], [68], while in others a Micromegas has been built directly on the ASIC [69]. The latter detector type is called GridPix and is produced with a post-processing technique, which guarantees a high quality grid well aligned with the readout pixels. This alignment ensures that the complete charge avalanche initiated by a primary electron is collected on one pixel. Because of the high signal to noise ratio both tracking and dE/dx measurement benefit from distinguishing and detecting single primary electrons with a high efficiency. This type of detector was pioneered by Nikhef/University of Twente (NL) and the University of Bonn has modified the production process together with the Fraunhofer Institut IZM so that a wafer-based production of GridPix detectors is standard by now [70]. First tests were done with both gas amplification stages by using single ASICs with an active area of about 2 cm². The detectors were operated in laboratories at Nikhef, Saclay, Bonn, Freiburg and Siegen to test the working principle. It could be demonstrated that the transverse spatial resolution of the reconstructed primary electrons was close to the expected diffusion limit of single electrons.

3.3.2 Recent Milestones

At the University of Siegen new types of GEMs are being tested in combination with the Timepix ASIC: GEMs with a carbon coating on the copper electrodes and GEMs with a ceramic insulator. Both types have been successfully tested and promise an improved stability and better handling.

At Nikhef, Saclay and Bonn several projects were done to demonstrate multi-module operation and large area coverage of modules with GridPix detectors. The new GridPixes were also assembled in 8 GridPix modules for the Large Prototype detector at DESY. Successful test beam campaigns were performed in 2010 with a single module and in 2013 and 2014 with two modules [71]. The latest work was focused on three LP modules with a total of 160 GridPixes. The central module is equipped with 96 GridPixes and the two outer modules have 32 GridPixes arranged to maximize the lever arm.

This setup serves a demonstrator that larger areas (~ 400 cm²) can be produced and operated. It was tested in the Large Prototype in March/April of 2015 and operated for more than one week permanently in the test beam. A total of about 200 runs with more than 1.5 million events were recorded.

Nikhef and Bonn have also taken part in designing a successor ASIC of the currently used Timepix. The new Timepix-3 features several improvements, which promises a much better performance. In particular it is multi-hit capable, can record both time and charge of each signal, has a much faster digitization frequency (640 MHz) and can be read out quasi continuously. A first beam test of two single Timepix-3 ASICs covered with a Micromegas grid took place in August 2015 at CERN SPS.

3.3.3 Engineering Challenges

The production of modules with large area coverage requires to solve four technical challenges:

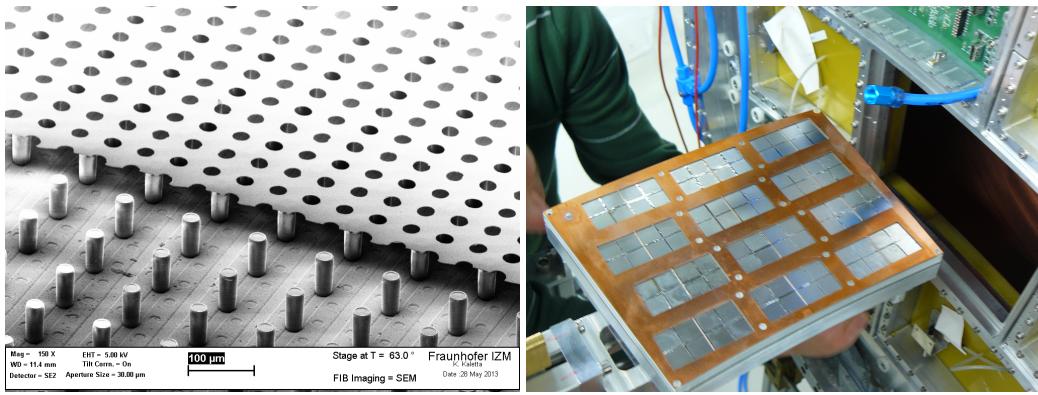


Figure 3.5: Left: SEM picture of an InGrid detector with a partially removed grid, right: Fully equipped LP module with 96 GridPix detectors is being mounted in the LP.

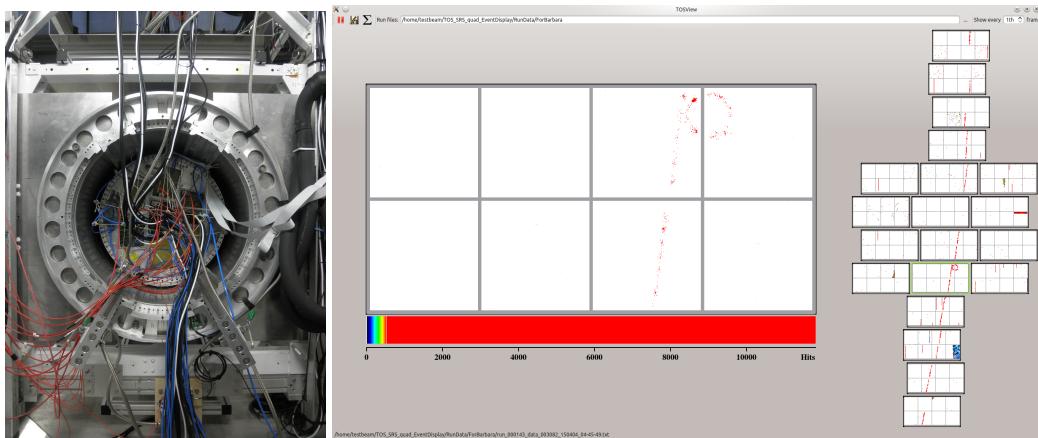


Figure 3.6: Left: Three modules with 160 GridPix detector mounted on the Large Prototype, right: Online event display of a 2 track event recorded with 160 GridPixels.

1. The production of a large number of GridPixels with sufficiently good quality. This has been addressed by the new production method, which is based on complete wafers. The process was developed in collaboration with the Fraunhofer institute IZM at Berlin and yields up to 428 GridPixels per batch (4 wafers).
2. In particular commercial readout systems are not easily scalable. This is why Bonn has developed a cheap and easily expandable system based on the Scalable Readout System (SRS) of the RD51 collaboration. Nikhef developed (partially funded by the AIDA FP7 project) the SPIDR fast readout system for Timepix-3 ASICs.
3. The distribution of the LV power to all ASICs which can reach peak values of 85 A at 2.2 V was designed.
4. Cooling of the ASICs was done by cold water. However in future also 2-phase CO₂ cooling will be

implemented.

3.3.4 Future Plans

Currently the main focus is on the analysis of the test beam data. The challenge of finding and fitting tracks with several thousand hits is quite different from the standard pad-based TPC analysis. For this a group of people from Nikhef, DESY, Siegen and Bonn are testing new ideas. On a longer term all participating institutes are working on software to simulate, reconstruct and analyze data of the ILD-TPC (i.e. about 10,000 hits per track) so that the difference in performance between a pad and a pixel-based TPC can be studied. On the hardware side the replacement of the Timepix ASIC with the Timepix-3 ASIC is most important. An improved grid structure using ceramic materials is under development. The construction of a few fully equipped, engineering modules with Timepix-3 GridPix detectors is being planned.

3.4 Time Projection Chamber – GridPix, Bonn

3.4.1 Introduction

The project studies the pixelized readout of a TPC for the ILD detector. The readout is based on the Timepix ASIC with a triple GEM or Micromegas based gas amplification.

3.4.2 Recent Milestones

The first studies were based on the triple GEM setup with a single Timepix chip. This readout was mounted in a small test detector in the Bonn laboratory. Here, the working principle was tested with a long drift distance. It could be demonstrated that the transverse spatial resolution of the reconstructed primary electrons was close to the expected diffusion limit of single electrons. The results are summarized in the following publications:

- C.Brezina et al. “Operation of a GEM-TPC With Pixel Readout”. In: *Nuclear Science, IEEE Transactions on* 59.6 (Dec. 2012), pp. 3221–3228. ISSN: 0018-9499
- J.Kaminski et al. “Time projection chamber with triple GEM and pixel readout”. In: *Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE*. Oct. 2008, pp. 2926–2929
- C Brezina et al. “A Time Projection Chamber with triple GEM and pixel readout”. In: *Journal of Instrumentation* 4.11 (2009), P11015
- Jochen Kaminski et al. “Time projection chamber with triple GEM and highly granulated pixel readout”. In: *Conf.Proc. C0908171* (2009), pp. 533–535
- Peter Schade and Jochen Kaminski. “A large {TPC} prototype for a linear collider detector”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 628.1 (2011). {VCI} 2010 Proceedings of the 12th International Vienna Conference on Instrumentation, pp. 128–132. ISSN: 0168-9002

The new focus are GridPix based detectors, where the gas amplification stage is a Micromegas produced in a postprocessing technique, which guarantees a high quality grid well aligned with the readout pixels. This approach was pioneered by NIKHEF and the University of Bonn has modified the production process together with the Fraunhofer Institut IZM so that a wafer-based production of GridPix detectors is standard by now. The new GridPixels were tested on small prototype detectors and also assembled in an 8 GridPix module for the Large Prototype detector at DESY. A successful test beam campaign was performed last year.

- M Lupberger. “The Pixel-TPC: first results from an 8-InGrid module”. In: *Journal of Instrumentation* 9.01 (2014), p. C01033
- W.J.C. Koppert et al. “GridPix detectors: Production and beam test results”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 732 (2013). Vienna Conference on Instrumentation 2013, pp. 245–249. ISSN: 0168-9002. doi: <http://dx.doi.org/10.1016/j.nima.2013.08.010>. URL: <http://www.sciencedirect.com/science/article/pii/S0168900213011364>

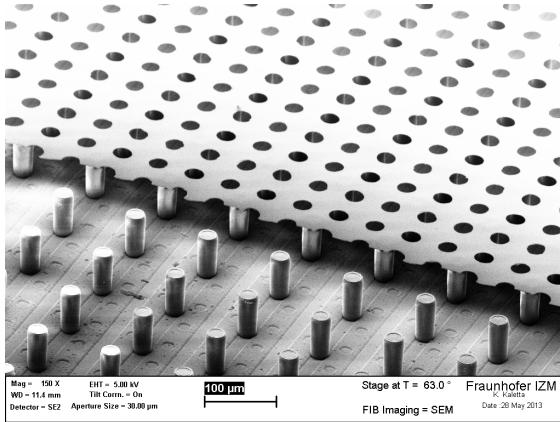


Figure 3.7: GridPix detector with a partially removed grid

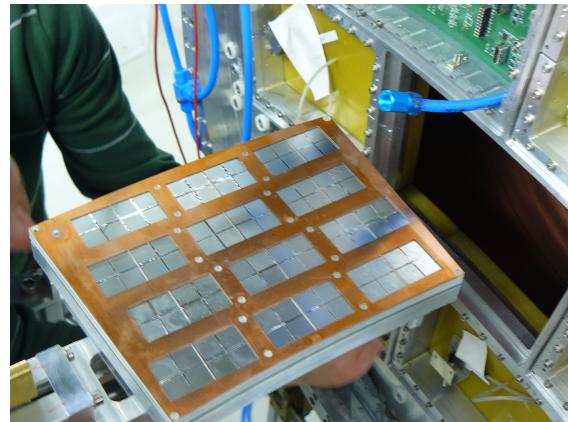


Figure 3.8: Fully equipped module as it is being mounted

The current work is focused on a new LP module with about 160 GridPixels. The central module is equipped with 96 GridPixels and the two outer modules have 32 GridPixels arranged to maximize the lever arm. This setup serves a demonstrator that larger areas (400 cm^2) can be produced and operated. It was tested in the Large Prototype of the LCTPC collaboration in March/April of 2015 and operated for more than one week permanently in the test beam. A total of about 200 runs with more than 1.5 million events were recorded. For this a number of challenges had to be overcome. In particular commercial readout systems are not easily scalable. This is why Bonn has developed a cheap and easily expandable system based on the Scalable Readout System (SRS) of the RD51 collaboration.

In addition Bonn is developing the software for reconstructing and analyzing the test beam and simulation data. For this the LCTPC software framework of MarlinTPC is used.

- Jason Abernathy et al. “MarlinTPC: A common software framework for TPC development”. In: *Nuclear Science Symposium Conference Record, 2008. NSS ’08. IEEE*. Oct. 2008, pp. 1704–1708

Finally, Bonn also takes part in designing new pixel chips. To test the new digitization and readout techniques two test chips were designed in collaboration with NIKHEF. Then Bonn also contributed to the design of the Timepix successor chip, Timepix3, which is being tested now:

- A Kruth et al. “GOSSIPO-3: measurements on the prototype of a read-out pixel chip for Micro-Pattern Gaseous Detectors”. In: *Journal of Instrumentation* 5.12 (2010), p. C12005
- C. Brezina et al. “GOSSIPO-4: Evaluation of a Novel PLL-Based TDC-Technique for the Readout of GridPix-Detectors”. In: *Nuclear Science, IEEE Transactions on* PP.99 (2014), pp. 1–1. ISSN: 0018-9499
- Y Fu et al. “The charge pump PLL clock generator designed for the 1.56 ns bin size time-to-digital converter pixel array of the Timepix3 readout ASIC”. in: *Journal of Instrumentation* 9.01 (2014), p. C01052

3.4.3 Engineering Challenges

The production of a module with 160 GridPixels requires 4 main components:

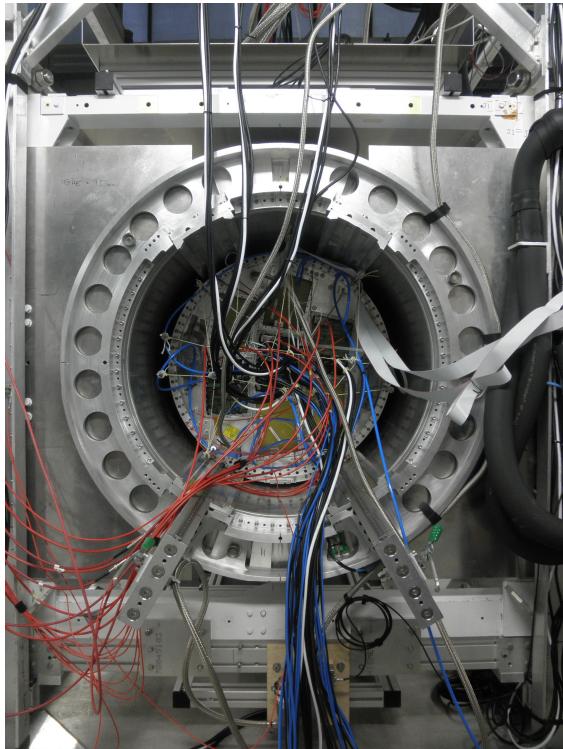


Figure 3.9: Fully cabled end plate

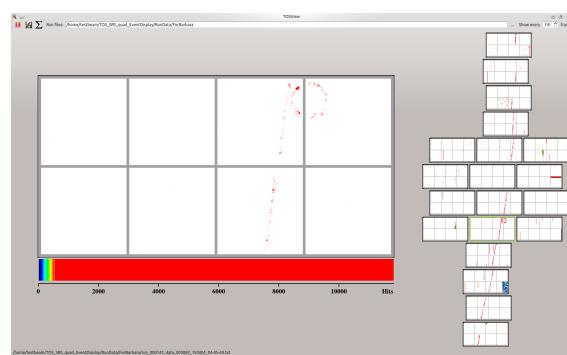


Figure 3.10: Online display of an example track

1. The production of a large number of GridPixels with sufficiently good quality. This has been addressed by the new production method, which is based on complete wafers. The process was developed in collaboration with the Fraunhofer institute IZM in Berlin and yields up to 400 GridPixels per batch. Figure 3.7 shows a GridPix detector with a partially removed grid.
2. The challenge of the readout is being addressed by the new readout system as described above.
3. The distribution of the LV power to all ASICs which can reach peak values of 85 A at 2.2 V was studied in a Master thesis.
4. Cooling of the ASICs was done by cold water.

3.4.4 Future Plans

Currently, the main focus is on the analysis of the test beam data. The challenge of finding and fitting tracks with several thousand hits is quite different from the standard pad-based TPC analysis. On a longer term all participating institutes are working on software to simulate, reconstruct and analyze data of the ILD-TPC (i.e. about 10,000 hits per track) so that the difference in performance between a pad and a pixel-based TPC can be studied. On the hardware side we are interested in replacing the Timepix ASIC by the Timepix3 ASIC and produce GridPix detectors with this improved chip, which promises a much better performance, since it is multi-hit capable, can record both time and charge of each signal and has a much faster digitization frequency. There are also some ideas of how to improve the grid structure and make it more reliable.

3.5 Ion Backflow and Gating

Contact person: Akira Sugiyama (email: sugiyama@cc.saga-u.ac.jp)

3.5.1 Introduction

The distortion of particle tracks due to the accumulation of positive ions in the drift space is the well-known issue for TPCs, whereby the ions are generated in the gas amplification region and drift back into the TPC drift volume. Although this ion back flow is much suppressed for the MPGD technology, compared to the earlier MWPC TPCs, it can still cause significant distortion of tracks when the particle density is high.

Because of the bunch-train structure of the ILC beams (i.e., a train of ca. 1300 to 2600 bunches during about 1 ms and a train-repetition rate of 5 Hz), the ions flow back from the gas amplification and will form a few discs of about 1 cm thickness in the TPC drift volume where they slowly drift toward the TPC central cathode. There will be three such ion discs during one train of normal ILC operation, and each disk will modify the trajectory of the drifting electrons, resulting in the distortion of tracks. The simulations of this distortion at ILC were made by several people, details can be found in [80, 81]. Figure 3.11 shows the azimuthal displacement of drift electrons by the ion disks for different radial positions of TPC with three ion disks in the drift space at the drift distances indicated by the red lines.

In Fig. 3.11 it is assumed that for every drift electron one positive ion drifts back. The actual amount of displacement should therefore be multiplied by the ratio of the gas amplification factor to the suppression factor of the ion backflow of the MPGD system. Since the suppression factor by the MPGD system has been measured to be in the order of order 10^{-3} at best [81], the ratio will be larger than one for a gas gain of a few thousand, and distortions larger than 60 μm in some parts of TPC would be expected.

At the ILC a TPC point resolution of 100 μm or better is required by the physics. Thus it is necessary to either install an efficient gating device to block the ions from the gas amplification, or to correct the track distortion. Because the machine backgrounds at ILC may not be stable enough to make a reliable correction possible, an efficient gating device will be needed. Fortunately the bunch-train configuration of ILC has an ideal time structure for ion gating. The positive ions drift back around 5 mm during the 1 ms bunch-crossing period, and can be absorbed by the ion gate which is ‘closed’ (explanation below) during next 200 ms between the bunch trains.

For the expected particle density at ILC, the track distortion by the *primary* ions produced in the LCTPC volume is small and has negligible effect.

3.5.2 Engineering Challenges: a Wire Gate or a GEM Gate

Ion gates used for TPCs in past collider experiments consisted of a wire grid. The operation and structure of the wire gate is well known and can be used for the LCTPC. Figure 3.12 shows a simple mechanical prototype of such a wire gate mounted on an Asian GEM module.

The disadvantage of a wire gate for the LCTPC module is to deteriorate the advantages of an MPGD TPC: the material and space budgets are increased because of the mechanical structure needed to support the many stretched wires on the module. Therefore, the wire gate is kept as a backup option for the LCTPC, and efforts are focused on the development of the gate using a GEM foil.

The idea of the GEM gate was proposed by F. Sauli in 2006 [82]. The ions from the gas amplification have to be absorbed by the electrode of the gate-GEM in the gate-closed condition. ‘Closed’ is where the electric field across the gate-GEM is reversed by changing the potential of the bottom electrode of the gate

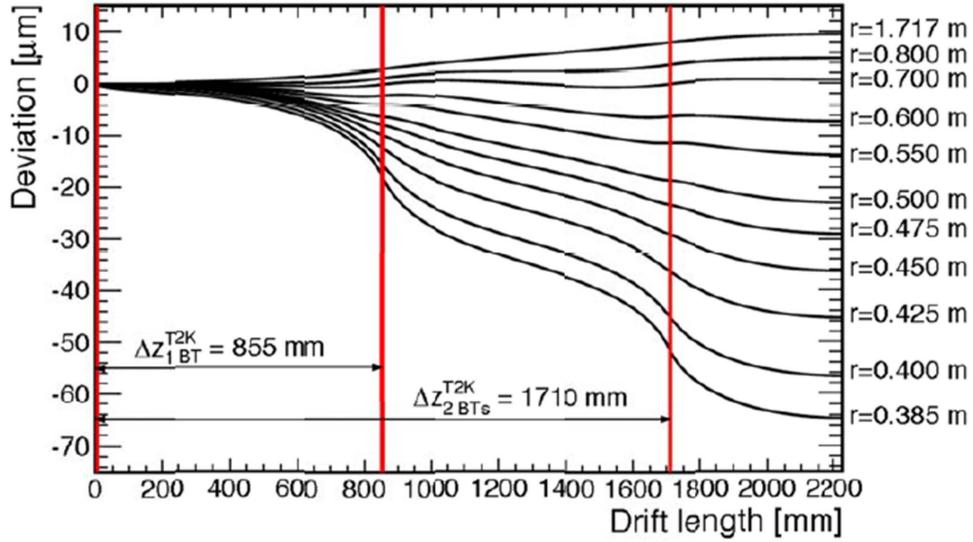


Figure 3.11: Displacement due to the positive-ion discs.

by about 10 V. In the gate-open condition the drift electrons need to reach to the gas amplification region with a high efficiency in order to not deteriorate the LCTPC resolution due to loss of signal.

Details of the simulation of GEM gate using the Garfield++ may be found in [80]. Experience was that it is easy to stop the ions with the necessary suppression factor of 10^{-4} or smaller. On the other hand, it is more of a challenge to keep a very high efficiency of the drift electrons passing through the gate-GEM in the gate-open condition. This is because the efficiency is limited by the optical transparency of the gate-GEM when a TPC is used in a high magnetic field (as in the 3.5 T field of ILD) and with a high- $\omega\tau$ gas mixture, such as the T2K gas [1, 83, 84, 85] foreseen for the LCTPC. In this condition the drift electron tends to follow the magnetic field lines rather than the electric field lines, which makes the optical transparency an important parameter .

The first GEM gate prototype for the Asian GEM module for the TPC large prototype (LP) beam test at DESY in 2009 was 14 μm thick with the round GEM holes of 90 μm diameter and 140 μm pitch. It had a maximum electron transmission of 50% in the magnetic fields of 1 T and 0 T. It was clear that a GEM with bigger holes and a narrow rim was needed, that is with larger optical transparency. Simulations found that

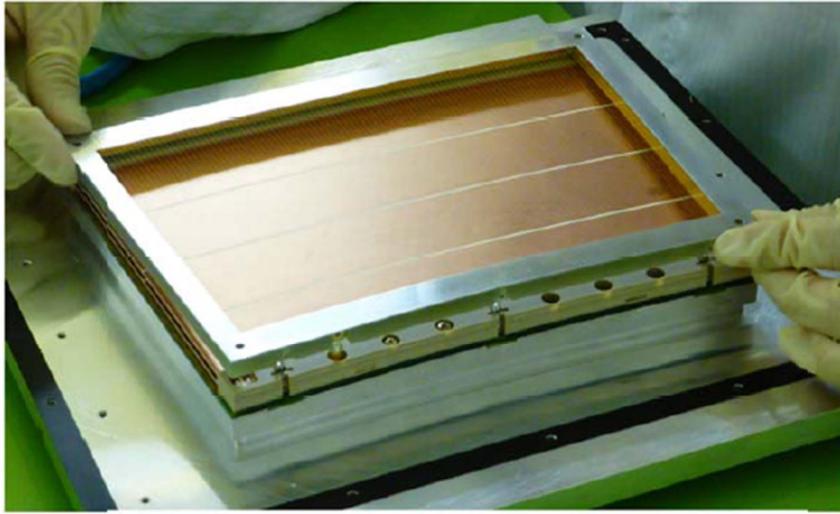


Figure 3.12: Prototype wire gate installed on the Asian GEM module.

GEM holes of the honeycomb shape with very thin rims would maximize the optical transparency.

As is seen the simulation results shown in Fig. 3.13, the thin gate GEM with honeycomb-shaped holes of 100 μm pitch and 10 μm rim width is shown to reach an electron transmission of 80%. However, a rim width of 10 μm turns out to be very difficult to produce; an alternative is presented in the next subsection.

3.5.3 Recent Milestones

In 2013 the Japanese LCTPC group started the actual fabrication of the GEM gate with the large optical transmission. With the limitations of the available processes of GEM, the specifications were set using Fig. 3.14(lower) which are summarized in the Table 1. The target is to fabricate a gate GEM with honeycomb shape holes of around 300 μm diameter and rim-width of 35 μm or smaller. The immediate goal of this study is to test the Asian LP module with this GEM gate in the DESY test beam in 2016.

Prior to the fabrication of a large, module-sized gate, many small samples of 10cm \times 10cm were produced to test different processing techniques. Although some samples by the standard single-mask chem-

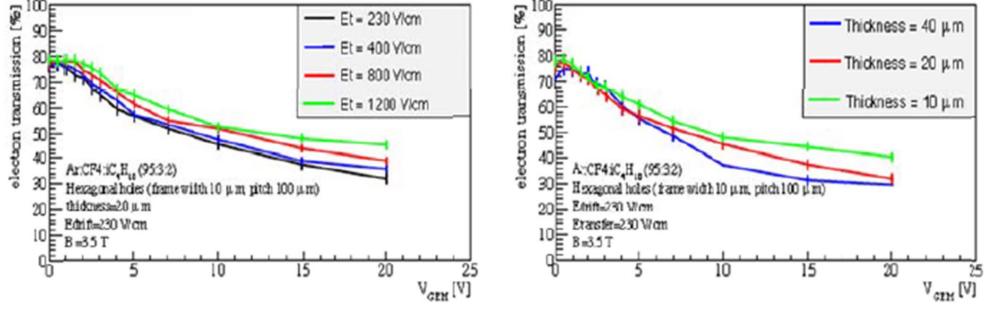


Figure 3.13: The electron transmission simulated for a gate-GEM with the honeycomb-shaped holes of pitch 100 μm and rim width 10 μm .

ical process were promising, limited resources required that a major effort be continued with Fujikura Ltd. [86] using their laser-chemical hybrid technology to produce FPCs (flexible printed circuits). Details of the Fujikura process for the gate-GEM were presented at MPGD2015 [87]. Figure 3.14(upper) shows the structure of one of the gate-GEM small samples made by Fujikura according to the specifications in Table 3.1.

The electron transmission was measured for these samples, and Fig. 3.14(lower) shows the results of the measurement compared to the simulation in magnetic fields of 0, 1 and 3.5 T. In the left panel, the results for the sample with round holes, and in the right panel for the sample with honeycomb-shaped holes. The electron transmissions at 0 and 1 T were confirmed to be better than 80% while the optical transmission was calculated to be 82% for the honeycomb-shaped-hole sample.

Having established the best configuration and the best process for the gate GEM with the small samples, the focus has now moved to the fabrication of the gate-GEM with the size of the Asian GEM module (Fig. 3.15). Here the major issue for the fabrication is to minimize any defects in the electrode circuit of the

Item	Specification
Optical aperture ratio	80%
Hole size	300 μm
Hole pitch	335 μm
Rim size	35 μm
Insulator thickness	25 μm
Foil size	170 \times 220 mm

Table 3.1: Specification of the gate-GEM in the current study.

gate-GEM so that there is 100% stopping power of the ions.

Figure 3.16(left) shows the test mounting of the gate-GEM on the module. As can be seen, the pattern of the amplifier GEM below the thin gate-GEM can be seen clearly, indicating a high optical transparency. Figure 3.16(right) is a picture of a test assembly of the gate-GEM on the module.

3.5.4 Future Plans

The production process for the large gate-GEM has been essentially established, and a few of the good samples for the Asian GEM module have been delivered for testing. The preparations for measuring the electron transmission by using a laser beam are under way. Although the Asian model is designed to have a GEM gate mounted on it, there may be more issues coming up, and some optimization of the mounting method and the module structure might become necessary for the design of the LCTPC. Beside some difficulties to stretch such a thin GEM stably, some consideration on the possible ion leak through the module boundaries for the Asian GEM modules may be needed.

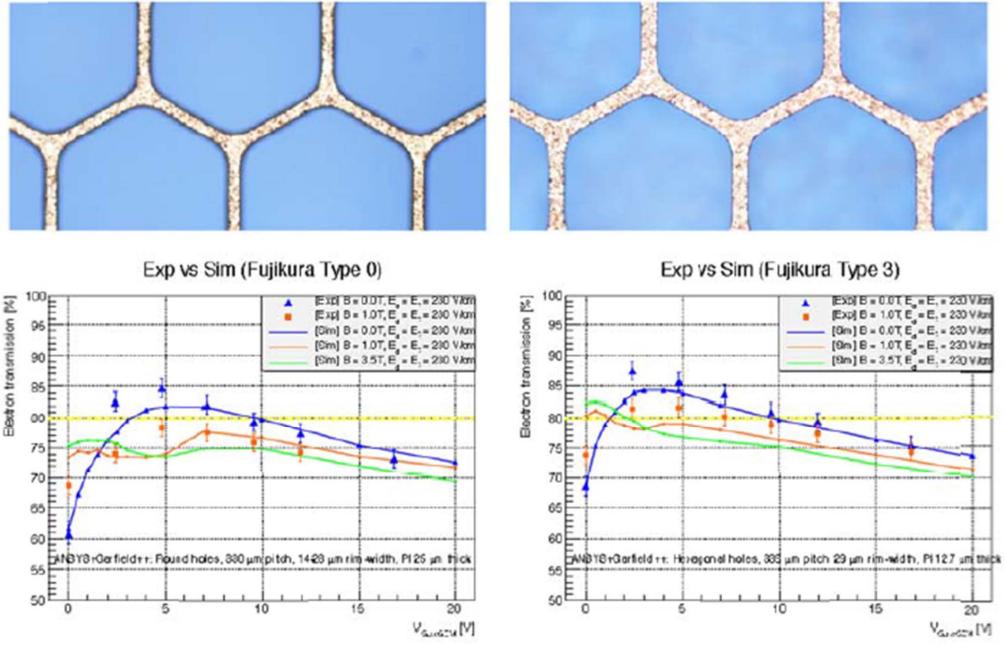


Figure 3.14: Upper: Honeycomb hole structure of the gate-GEM. The pitch of the holes is 335 μm , the rim width 29 μm . The polyimide insulator is 12.7 μm thick. Lower: Preliminary results of the electron transmission measurement are compared to simulation as functions of the GEM voltage for two types of gate-GEMs. In the left panel are results for gate-GEM with round holes; in the right panel results for the gate-GEM with honeycomb-shaped holes.



Figure 3.15: A sample gate-GEM for the Asian module.

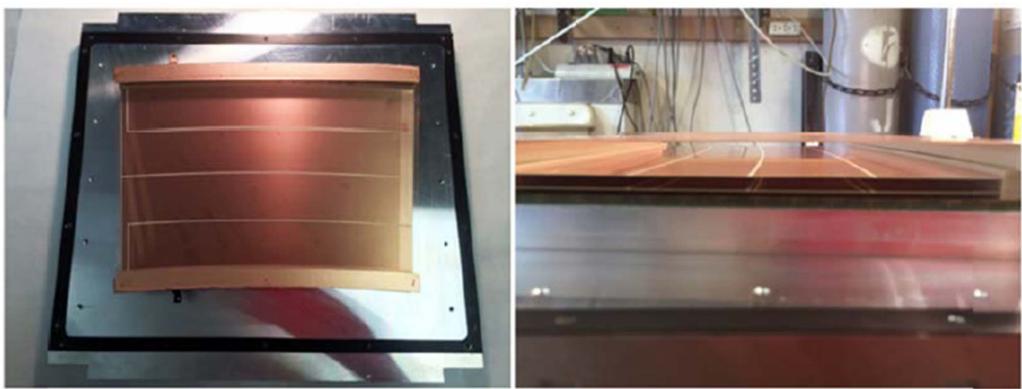


Figure 3.16: Left panel: Test mounting of the gate-GEM. Right panel: Test assembly of the gate GEM on the Asian GEM module.

3.6 Electronics, DAQ and Cooling

Contact person: Leif Jönsson (email: leif.jonsson@hep.lu.se)

3.6.1 Introduction

The readout electronics for the TPC has to be adapted to the design of the tracking chamber and the beam structure of the collider. The physics goals of the ILC requires high momentum resolution and two-track separation, which drive the track reconstruction in the $r\text{-}\varphi$ -plane to pad sizes of small dimensions. For the $r\text{-}z$ -plane a short shaping time and a high sampling rate is necessary to provide the best possible timing information. However, at the same time the noise level has to be kept at a manageable level. The sampling depth has to match the sampling frequency in order to cover the full drift length. The front end electronics has to be accommodated within pad modules, with a channel occupancy that is smaller than the pad size to allow space for the mounting frame, the voltage supply and the cooling system.

The power consumption of the front-end electronics should be kept low such that the heat dissipation does not lead to a temperature increase in the TPC-gas of more than typically 1 °C and in order to minimize the cooling requirements. In this respect, power pulsing, where the front-end electronics is switched off for about 199 ms between the bunch trains, helps significantly.

The readout electronics presently under development aims to demonstrate that the channel occupancy can be made compatible with the small pad size foreseen. It is based on the CERN SALTRO16-chip, which integrates the analogue and digital signal processing of the incoming signals within the same compact circuit. The size of the chip itself is $8.7 \times 6.2 \text{ mm}^2$ and it contains 16 readout channels. The chip is programmable with respect to gain, rise time, decay time and polarity. The sampling can be clocked at frequencies 5, 10, 20 and 40 MHz and it allows for power pulsing.

The chips are bonded onto carrier boards of size $12.0 \times 8.9 \text{ mm}^2$, also offering space for passive components along the edges. Each board contains more than 200 bonding wires, which considering the small size of the board requires a very accurate bonding procedure. The upper surface is covered by an epoxy glob protecting the chip, the bonding wires and the passive components. The bottom side contains small tin balls organized in a BGA pattern for soldering of the carrier board on so called Multi-Chip Modules (MCM). Eight carrier boards are mounted on an MCM, which also contains a CPLD (Complex Programmable Logic Device) controlling the data flow. The MCM-board is the smallest unit in the front end electronics and it is attached to the pad plane via four micro-connectors, whereas on the opposite side of the board there are two connectors, via which the low voltage is distributed and the signals are transmitted. The MCM-board is designed in High Density Interconnect (HDI) technology, by which the number of layers is significantly reduced compared to conventional PCB design. The dimensions of the MCM-board are $32.5 \times 25 \text{ mm}^2$ and serves 128 readout channels. This corresponds to a channel occupancy of about 6.4 mm^2 , although some space is also required for the high voltage connectors of the gas amplification system (GEMs and Micromegas) and the cooling system.

A serial readout system is used for the signal transfer to the DAQ computer. The MCM-board and the Scalable Readout Unit (SRU) communicate directly via the Data Trigger Control (DTC) link. Communication, data transfer and control, between the SRU and a DAQ computer is done via Ethernet.

Cooling of the front end electronics is a challenge since the size of the cooling system must match the smallness of the electronics and still provide efficient cooling. The total power consumption of an MCM-board in continuous operation is 3203 mW on the top side and 3028 mW on the bottom side. In power pulsing mode, with a bunch train of 725 μs, containing 1312 bunches, the power dissipation is reduced to

about 223 mW per MCM-board on the top side and 48 mW on the bottom side. A cooling system with cooling pipes that run on top of the MCM-boards, using two-phase CO₂ coolant, is considered. Another possibility would be to use micro-channel cooling, which has been developed by the semiconductor community. Such systems are presently further developed within the AIDA2020 project, for applications in high energy physics experiments. The ILC cycle is not realistic in a test beam environment as at e.g. DESY. To get a reasonable trigger rate is e.g. a cycle with 5 ms beam at 10 Hz more useful, which corresponds to 343 mW per MCM-board on the top side and 168 mW on the bottom side, in power pulsing mode.

3.6.2 Recent Milestones

A test system has been built and a few mounted carrier boards have been produced, which are both under debugging. The design of the MCM-board in HDI-technology is ready and the production is awaiting the full characterisation of the carrier board. The design of the low voltage board is essentially ready. An MCM-development board, containing only one packaged SALTRO-chip, has been produced and has been used in the tests of the serial readout system. The tests were successful, although some further firmware development is needed for the full functionality. A cooling system using micro-channel cooling is under discussion within AIDA2020.

3.6.3 Engineering Challenges

The final aim is to produce front end electronics, high voltage supply and a cooling system which are compatible with a pad size of $1 \times 6 \text{ mm}^2$. The compactness of the electronics and the space limitations are major challenges, as well as designing a suitable and efficient cooling system. An elegant solution for the low voltage supply has to be found and due to space limitations the design of the mechanical support for the electronics is also a challenge.

3.6.4 Future Plans

In the next future the characterisation of the carrier board will be completed, followed by the production of the MCM-board. One fully mounted MCM-board with eight carrier boards will be produced and tested. The firmware for the serial readout will be further developed and tested. Discussions concerning micro-channel cooling will continue and we hope to get help with the design and production of a prototype system by AIDA2020.

3.7 Mechanics and Calibration

Contact person: Ties Behnke (email: ties.behnke desy.de)

3.7.1 Introduction

A key component of the TPC at a future collider will be the design and construction of the field cage. The cage should be light weight, yet mechanically and electrically stable. It should provide support for the cathode and the anode systems, and allow excellent field shaping in between. To test the concept for such a field cage a prototype has been built as part of the LCTPC test infrastructure [88]. The field cage is made from a light weight composite sandwich structure. The mechanical structure is given by a honeycomb layer, which is covered on the inside and the outside by a glass fibre reinforced epoxy layer. On the inside a Kapton foil provides electrical insulation, and field shaping through a system of copper ring electrodes. On the outside a thin aluminum layer provides grounding. Integrated into the field cage a laser based calibration system is foreseen.

The prototype field cage has been constructed in 2008 and has been used with all different readout technologies since. It is equipped with an aluminum based endplate, which can host up to seven identical readout modules. It is designed to fit into the PCMAG magnet [89] infrastructure, which is installed at the DESY test beam facility [90].

A large system like the TPC poses particular challenges to calibrate the system and to maintain the calibration. Currently several systems are under consideration.

An important part of the calibration will be done based on data recorded, without special hardware. Tracks will be used to align the different modules relative to each other, and to measure and correct field distortions.

While tracks are an excellent method to derive relative corrections, and to equalise the response, it might be difficult to reach the ultimate absolute resolution without an external unbiased reference. This reference can come from different sources. Within the ILD detector design silicon detectors are foreseen before and after the TPC, which will provide an external reference. These systems can be used to calibrate the field distortions, and to set the scale for the momentum measurement. Another system will be based on laser beams. Laser beams will be used in two ways. Well focused small cross section beams can be inserted into the drift volume, and serve as fake tracks. The ionization along the laser beams is recorded as for normal tracks, and can be used to calibrate the response of the TPC. A wide laser beam can be used to illuminate the cathode of the TPC. Dots or lines of a low work-function material like e.g. aluminium on the surface of the cathode would then provide well defined spots where the laser light can liberate electrons. These electrons then drift towards the anode and sample any inhomogeneities on their way. Thus, they can be used to monitor and –to some extent—determine the field properties inside the drift volume. Both types of laser beams need to be inserted into the TPC, and will require the design and implementation of sophisticated hardware.

Engineering Challenges

The current field cage has been successfully used in numerous test beam campaigns. However, it has failed to deliver the ultimate mechanical precision which is needed for the demonstration of the anticipated momentum resolution of the TPC system. In particular, the manufacturer has failed to deliver the needed alignment between the anode and the cathode, and has introduced a small overall skew into the field cage. The main challenge will be to develop and build a second generation field cage which fulfills the

precision requirements. For this an entirely new tooling is being developed, which should help to ensure the mechanical precision.

The results from this prototype field cage will then be applied to a study of the design of the full field cage for the ILD TPC. A central and so far unsolved engineering challenge is the support of the TPC in the overall detector. Here a combination of light weight, space saving support structures combined with superb mechanical stiffness need to be found. Particular attention will also need to be payed to the behaviour of the system in case of earth quakes, given that the proposed site of the ILC in Japan is located in an earthquake prone region.

An open and as yet unsolved issue is the design of the central cathode of the TPC. This system is located in the centre of the detector, very difficult to access. It needs to be light weight, yet dimensionally very stable. It will be supplied with high voltage of close to 100 kV. The supply of this very high potential in a safe and reliable way is under study and represents significant challenges.

As described above laser beams will be used to calibrate the system. The insertion and guidance of these laser beams present significant challenges. Ways will need to be found to bring the laser beams to the TPC. The laser will have to be installed on the outside of the detector, so that transport ways of several meters through a very crowded environment are needed.

3.7.2 Future Plans

Over the next few years a full engineering design of the ILD TPC will be developed. This will include a detailed simulation of the TPC system, and its mechanical properties, and its integration into the ILD detector as a whole.

Detailed problems which will need to be addressed are:

- Finite Element Method (FEM) calculations of the field cage and the endplate
- Optimisation and final decision on the layout of the endplate: size of modules, number of modules, etc.
- Design of the support system of the TPC in the ILD detector
- Study of the mechanical properties of the TPC support in view of vibrations and overall stability
- Design and implementation of a system of laser beams in the TPC drift volume
- Design and implementation of a system to illuminate the TPC cathode with a laser beam.

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
Asian GEM	Saga, KEK, Hiroshima, Kindai, Kogakuen, Iwate, Nagasaki IAS, Tsinghua	Design of an endcap readout module with a stack of two thicker laser etched polymer-based GEMs and pads	2010-2013: Several test beam campaigns were performed with three readout modules.	During test beam activities the stability of the HV was not as good as in lab tests. The origin of the discharges is being investigated. A modified module with a gating device will be designed and constructed in the next step, and pad plane adapted for the SALTRO is also planned. (2016/17)
GEM	DESY, Hamburg Bonn Siegen	Design of an endcap readout module with a stack of three standard CERN GEMs and pads	2009-2013: Several test beam campaigns were performed with three readout modules.	Though no problems occurred during the test beam, the HV-stability is still being investigated. A new module with gating device, reduced local field distortions and pad plane adapted for the SALTRO is planned. (2016/17)
Resistive Micromegas	CEA Saclay, Carleton	Design of an endcap readout module with a Micromegas gas amplification stage, a resistive layer for charge dispersion and integrated readout. Construction of 11 modules.	2010-2015: Several test beam campaigns were performed with up to seven readout modules, covering the complete LP-endplate.	New materials as resistive layer are being investigated. A module with lower local field distortions is planned.
GridPix ConceptGEM + pixel readout	Bonn, NIKHEF, CEA Saclay Bonn, Siegen	Design of an endcap readout module with a highly pixelized readout with GridPixels. These devices consist of a Micromegas mesh built by postprocessing technology on a pixel ASIC. Alternatively a GEM-stack is used as a gas amplification stage.	2009-2015: Several test beam campaigns with up to three modules were performed. The three modules featured a total of 160 GridPixels and this test beam was performed in March/April 2015. This demonstrated that a large area could be covered with GridPixels and about 100 GridPixels per module could be operated.	2017: The successor chip Timepix3 will be implemented in the readout chain and a test beam with several Timepix-3 chips is planned. This new chip fulfills basic requirements for an operation in an ILD environment.
Field cage	DESY	Design and construction of a TPC field cage	2009: A first prototype has been built and is used as a test device at DESY	A new field cage with improved geometrical precision is under construction at DESY. (2017)
Electronics	Lund, CERN, CEA Saclay	Design of a readout electronics fit for test beam operation at T24/1 at DESY and for investigation the requirements of the ILD-TPC electronics.	2009: Sofar, readout systems based on the AFTER and the ALTRO chip have been used with 10,000 channels each.	A new system based on the SALTRO-16 chip is being prepared (2017). Simulations on the impact of key electronics parameters on the TPC-performance are planned.
DAQ	Lund, ULB-VUB, Hubei	Design of a data acquisition system fit for test beam operation at T24/1 at DESY.	Sofar, DAQ systems for both readout systems (AFTER and ALTRO) have been set up.	A new DAQ system for the SALTRO-16 based readout electronics is being prepared and will be available soon.
Endcap	Cornell	Study of different endplate designs for an ILD-TPC with CAD programs and production of smaller endplates fit for operation at test setup at T24/1 at DESY.	A detailed model of the endplate was implemented in a CAD program and in 2009 a first endcap for the test beam setup has been produced several years ago. A new version also fulfills the requirements of the material budget and will be used from 2015 onwards.	Simulations optimizing the module size are planned.
	CEA Saclay, DESY	Mechanical studies for ILD-TPC regarding the effect of pressure, weight, hanging/support schemes on the mechanical deformation of the endplate and field cage.	First studies have been done.	More detailed studies are planned
Calibration	BNL, CERN, Indiana, Kolkata	Laser calibration system, Alignment/calibration of the TPC, Integration with other tracking systems		
Study of systematic effects	Victoria, Kolkata	Field distortions are a major source uncertainties in track reconstruction. The sources of these distortions are studied and minimized.		
Analysis software	DESY, Carleton, CEA Saclay, KEK, Saga, Siegen, Tsinghua	Development of a software package MarlinTPC, which serves all groups for reconstructing and analyzing the test beam data and for simulation, reconstruction and analysis of ILD events.	MarlinTPC is well developed and the key analysis tool for all analyses.	Further improvements are continually made.
Ion backflow/Gating	Japanese Univers., KEK, Tsinghua, Kolkata, DESY	The ion back flow from gas amplification stages is a major source for time dependent field distortions and has to be suppressed as much as possible. With simulations and experimental setups the minimization of ion production and the reduction of the back flow by a gating device are under study. Field distortions are a major source uncertainties in track reconstruction. The sources of these distortions are studied and minimized.	Simulations have shown, that all gas amplification stages release too many ions into the drift volume and a gating device is necessary. 2014: A first MPG-based device, a Gating-GEM, has been produced and is being compared to a standard wire gate.	2016: module sized GEM-gates will be available. Then the impact of the gate on the TPC-performance will be studied by using a UV-laser facility at KEK, and in test beams.
Cooling	KEK, Saga, NIKHEF, Saclay, Kolkata	Cooling is important to divert the heat produced by the readout electronics at the endplate. The temperature influences the gas gain and drift properties in the gas and has to be kept as stable as possible to achieve a reliable measurement.	2014: A CO ₂ cooling plant has been purchased and setup at the test beam site. First results show a significantly reduced temperature gradient due to heating at the endplate.	Cooling of the SALTRO-16 based module will be studied with a mockup which emulates heat and mechanical conditions of the module. Then, the SALTRO-16 based module will be built with the CO ₂ cooling pipes.

Chapter 4

Calorimeters

4.1 Scintillator Strips

Contact person: Tohru Takeshita (email: tohru@shinshu-u.ac.jp)

4.1.1 Introduction

The CALICE scintillator strip-based ECAL (ScECAL) uses a scintillator strip structure to deliver the granularity and resolution required of an ILC detector. Each strip is individually read out by a Multi Pixel Photon Counter (MPPC, a silicon photon detector produced by Hamamatsu Photonics KK [91]). Although plastic scintillators have been widely used in calorimeters, this is the first time that a highly granular calorimeter has been made using scintillator strips. Such an ECAL has a smaller cost than alternative technologies using silicon sensors (e.g. [92]). The MPPC has promising properties for the ScECAL: a small size (active area of $1 \times 1 \text{ mm}^2$ in a package of $2.4 \times 1.9 \times 0.85 \text{ mm}^3$), excellent photon counting ability, low cost and low operation voltage (70 V), with disadvantages of temperature-dependent gain, saturation at high light levels, and the dark noise rate. The use of tungsten absorber material minimises the Moliere radius of the calorimeter, an important aspect for the effective separation of particle showers required by PFA reconstruction. The chosen strip geometry allows a reduction in the number of readout channels, while maintaining an effective granularity given by the strip width, by the use of appropriate reconstruction algorithms. One such algorithm, known as the Strip Splitting Algorithm [93], has been developed and demonstrated to perform well in jets expected at ILC.

4.1.2 Recent Milestones

- introducing a new scintillation light readout scheme, with different scintillator strip shape by having better homogeneity
- photo-sensor of increased number of pixels in $1 \text{ mm} \times 1 \text{ mm}$, this leads larger dynamic range for the calorimeter
- more experience on the FE read out board and ASICs

They are not published yet, instead some proceedings

4.1.3 Engineering Challenges

- wrapping the scintillator strip and align them on the FE read out layer automatically
- mass test facility for the read out layer

4.1.4 Future Plans

- deciding on the scintillator layer: shape of scintillator strip, how to read out scintillation light, the location of photo-sensor, size and shape of photo-sensor and mass production scheme
- developing photo-sensor with Hamamatsu photonics company, to have larger dynamic range and mass test scheme
- establish a detector fabrication plan

4.2 Silicon-Tungsten ECAL in ILD

Contact person: Jean-Claude Brient (email: brient@llr.in2p3.fr)

4.2.1 Introduction

The group of the silicon-tungsten electromagnetic calorimeter for ILD aims to develop a highly granular detector optimized for particle flow measurements. The calorimeter uses a sandwich architecture of silicon sensors with $5 \times 5 \text{ mm}^2$ pixels as active elements embedded in an alveolar structure made of tungsten and carbon fiber. The group is active in the development of simulation software and algorithms for calorimeter reconstruction, as well as in the design of readout chips, front-end electronics boards, mechanical structures, cooling and in ILD integration.

4.2.2 Recent Milestones

The work is now focusing on the construction of a technological prototype. This is a new milestone after the successful operation of the “Physics Prototype” in the years 2004–2011, including large scale beam tests at DESY, CERN and FNAL and data analysis [92, 94, 95, 96, 97].

In the technological prototype and in the ILD design the front end SKIROC chips [98, 99] are embedded into the calorimeter layers and mounted on multi-layer printed circuit boards (PCBs). Four silicon sensors are glued with a conductive epoxy to the readout PCB. Depending on the ILD and the silicon sensor sizes, up to about ten of these PCBs will be connected together in-line and read out from one end by a data acquisition (DAQ) electronics. The sandwich of the silicon sensors with PCBs on both sides of the absorber layer represents one active module, called “slab”. It is slid in the tungsten – carbon fiber alveolar structure. The slab absorber layer is also made of tungsten wrapped in carbon fiber. In this way, half of the absorber layers are in the structure and half are in the slabs.

A series of tests with simplified PCBs have been carried out starting from 2012: several beam tests at DESY, cosmic calibrations and infrared laser tests. Each simplified PCB served one silicon sensor. The power pulsing operation of the SKIROC chips has been demonstrated. The bias currents of the chips were shut down and raised with a frequency between 1 – 20 Hz. It was shown that the SKIROC currents should be switched on at least 600 μs before physical events, so that all transition processes are finished. Mechanical rigidity of electrical interconnections under changing Lorentz force and also, the stability of pedestals was

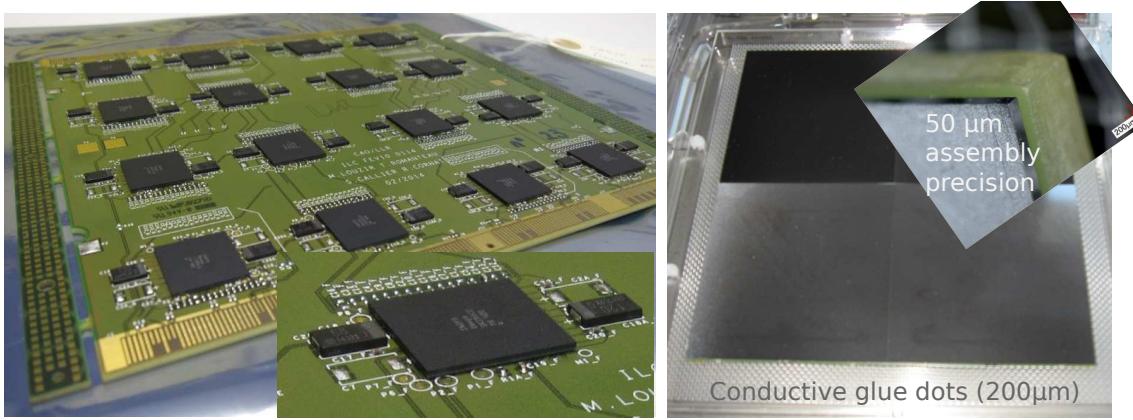


Figure 4.1: Left: new PCB with 16 SKIROC chips and 1024 channels, right: 4 sensors aligned and prepared for robotic gluing to PCB.

checked in the power pulsing mode in the magnetic fields of up to 2 T. The continuous cosmic data taking during 24 hours allowed to calibrate each pixel with 3% statistical accuracy. The variation of cosmic MIP signals across all channels was measured at 3-4% level. It was found to be dominated by the spread between the chips and by the variation of electronic channel gains within a chip. The same spread is measured by a calibrated charge injection into SKIROC preamplifiers. In cosmic and test beam data the signal-over-noise ratio for MIP signals was measured at the level of 8 – 20. It depended on the SKIROC gain, the better values were obtained for the gain 5 times higher than nominal.

The infrared laser tests have been used to study the so-called “square” events. They are caused by a capacitive coupling (cross-talk) between a silicon sensor guard ring and its boundary pixels. The guard ring ensures low dark currents of the sensor under high voltage. For technological reasons it is not grounded. High local signals at the sensor periphery may, therefore, propagate to all boundary pixels, fire them and produce “square” events. With an improved segmented guard ring design, the cross-talk is reduced to $\leq 0.5\%$ per outer pixel side, as it was measured with the laser induced signals. Hamamatsu HPK company also developed a new “no guard ring” design, their small sensors demonstrated both the lowest guard ring cross-talks and sufficiently low dark currents. Another activity which has been started in 2015, is the study of dark current dependence on neutron irradiation dose at a nuclear reactor.

Generally, the analysis of accumulated beam test, cosmic and infrared laser data validated the concept of the front end electronics. It will also allow for correcting an observed shortcomings of the SKIROC chips and the first PCB. A new version of PCB serving four sensors as required for ILD, has been designed and produced, see Figure 4.1. To increase a channel density, a ball grid array (BGA) packaging of the SKIROC chips was chosen. The gluing of four fragile silicon sensors with a gap in between of only $100\text{ }\mu\text{m}$ has been successfully performed with a robot. The first detectors have been assembled in 2015 and the first tests with the cosmics and the laser have shown a good performance. An assembly procedure together with quality controls is formalized and well documented. Further improvement and production of the new version of SKIROC chips is planned for both ILD and for a CMS phase-2 endcap calorimeter upgrade project (HGCAL). The combined with HGCAL beam tests at SPS in CERN are planned in November 2015 and in 2016.

The mechanical design of ILD ECAL is well advanced. A full scale prototype of a barrel tungsten –

carbon fiber alveolar module with three towers of 15 alveoli has been successfully produced with required tolerances. A full scale absorber part of the barrel slab has been also manufactured with tungsten substituted by carbon to reduce the cost. The mechanical simulations of one alveolus structure have been verified with the measurements using a special prototype with molded Bragg grating fibers. When elongated under loads, such fibers change a frequency of reflected light, allowing very precise measurements. The same technique is used in constructing buildings, bridges etc. A long 2.5 m endcap carbon structure with 3 alveoli is also successfully produced. The rails supporting ECAL on the HCAL face in ILD, and also the transport and handling tools for future ECAL assembly have been designed and mechanically simulated.

Thermal simulations have shown that a passive cooling inside alveoli should be sufficient. Outside water cooling will be performed with leakless loops, first prototypes exist.

In addition to the hardware development, there is a big activity on ILD optimization and on PFA algorithms. In particular, it was shown that the big ILD ECAL with fine longitudinal segmentation which was chosen in DBD on the basis of a physical performance, may be not optimal in terms of a cost effectiveness [100, 101]. In particular, the number of ECAL layers may be reduced, eg. 19 layers provide only $\leq 10\%$ worse jet energy resolution than the nominal 29. Even bigger cost savings may be achieved by reducing ECAL sizes. Eg. with an inner ECAL radius of 1400 mm instead of the nominal 1843 mm and a proportional reduction of an ECAL length, the 45–250 GeV jet energy resolution is degraded by 8–19%. It may be partially compensated by an increase in a magnetic field. In addition to the jet resolution, the performance of a smaller ILD for a reconstruction of tau decay modes has been studied [102]. It is essential for a measurement of CP violation in $H^0 \rightarrow \tau^+ \tau^-$ Higgs decays, where τ polarization is extracted from its decay products. It was shown, that the τ mode reconstruction efficiencies change by $\leq 1\%$ when the ECAL radius is reduced to 1450 mm and the magnetic field is increased from 3.5 to 4 T. Based on these studies and taking into account the ECAL silicon sensor size, two new ILD models have been proposed for ILD community [103], with the ECAL inner radii of 1615 (“Khephren”) and 1480 mm (“Mykerinos”, by the name of the third ancient Egyptian pyramid). The ECAL engineering models for these sizes are under development.

Another important activity is a continuous improvement of PFA programs GARLIC [104] and ARBOR [105]. The former is specialized on a photon reconstruction in the highly granular ECAL, the latter is a PFA program approaching PANDORA [106] in performance. Both programs are under active development.

A shower fractal dimension measured in the highly granular calorimeter has been studied in [107]. It was demonstrated, in particular, that the fractal dimension could be effectively used to distinguish electromagnetic and hadronic showers. The performance of PANDORA, ARBOR and GARLIC to separate two electromagnetic or electromagnetic – hadronic showers is being verified with the physical prototype data collected in 2007 – 2011. Such a separation is crucial for reducing a PFA confusion. A good agreement between Monte Carlo and data has been observed. In another analysis, a detailed study of hadronic interactions recorded in ECAL physical prototype has been compared with GEANT4 models [108].

PANDORA jet energy resolution has been studied in DBD geometry [109] as a function of several ECAL parameters, including PCB thickness, guard ring size and fraction of dead channels and chips. It was demonstrated that the PCB thickness with BGA packaging already achieved in the technological prototype is sufficiently small (about $\sim 3\%$ degradation of jet energy resolution compared to zero thickness). The standard guard ring thickness of $500 \mu\text{m}$ is also sufficiently small (1-2% degradation compared to zero). The dependence on the fraction of randomly distributed dead channels is rather weak, even at 10% the jet energy resolution degrades by $\leq 4\%$.

4.2.3 Plans of the near future

The ILD slab has on each side several PCBs connected in-line. Both supply voltages, clock and readout signals should be well propagated along the slab through the PCBs and interconnections between them. The assembly of in-line PCBs partially equipped with sensors (at least at the ends) is an important R&D activity for the future. For this purpose, we plan to develop an assembly line, incorporating the reception and the test of the material, the alignment of the PCBs, sensors and the interconnections, with a continuous monitoring for quality control purposes. First, a manual assembly line capable for a small production will be realized. Based on it, we will propose an automatized system for mass assembly together with industrial partners. A survey to search for such partners is a part of the proposal. A goal is to design the system such that it can be duplicated at other sites.

When built, the long slab will be tested at beams and with cosmics. The detailed characterization of channel responses will be obtained with the calibrated charge injection. A special study of various types of cross-talks is foreseen (across channels of one SKIROC chip, especially in high occupancy events, noise pick-up from PCB digital lines etc.).

Like this was done for the ECAL physical prototype, we plan common beams with other CALICE calorimeters, when our DAQ systems are sufficiently well integrated to acquire common data.

Hamamatsu HPK produces sensors from 6 inches wafers with the typical thicknesses in the range 300–500 μm . Another company, LFoundry in Europe, may produce in large scale the sensors from 8 inches wafers with the thickness of about 700 μm . Larger sensors have less fraction of guard ring dead area, while thicker sensors provide slightly better ECAL photon resolution. The LFoundry sensors which have been already ordered, will be tested in the future. In parallel, the tests of existing Hamamatsu prototypes will continue, in particular, the cross-talk studies with the infrared laser and the neutron irradiation measurements. The radiation hardness measurements of other slab components is also planned. The sensors from other companies (not only Hamamatsu) may also be tested in the same way. One may expect a future growth of a market of large area silicon detectors due to a future mass production of sensors for CMS HGCAL.

Other ECAL R&D may also greatly benefit from the synergy with the HGCAL project. It is expected that a new improved version of SKIROC chip will be manufactured for both HGCAL beam tests and for ILD. After that, when the SKIROC performance is proved to be sufficiently stable, a new chip generation will be designed and produced which will have zero (pedestal) suppression. Alternatively, if a new chip with superior characteristics will be developed for CMS HGCAL, it may be tested and adapted for ILD purposes (note, that HGCAL does not have the power pulsing and its bunch spacing is 25 nsec).

A continuous development of DAQ electronics is another important activity. In addition to the optimization of the baseline PCB with BGA packaging which should at least closely follow the SKIROC development, there is a R&D on embedding naked dye SKIROC chips inside the PCB. This option may provide ~ 1.5 mm thinner active ECAL layer, but is technologically challenging because of the constraints on the required PCB flatness. Further R&D on improvement and miniaturization of DAQ electronics placed at the end of the slab, and also, on low and high voltage distribution systems is also foreseen.

All activities mentioned above also imply the search for industrial partners where the future mass production may be realized. This also means a continuous work on a cost estimation and optimization of all ECAL elements.

The work on physics – cost optimization of ILD ECAL will continue, together with the optimization of PFA algorithms. ECAL endcap ring should be designed taking into account high backgrounds closer to the beam pipe. The questions of ECAL integration in ILD, its assembly and safety will be further elaborated.

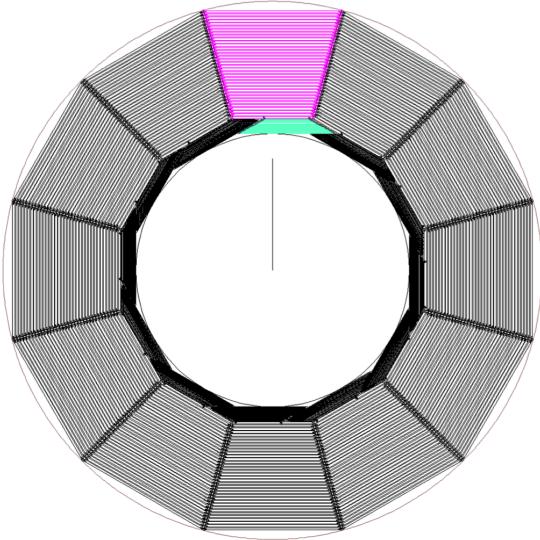


Figure 4.2: Outer HCAL and inner ECal barrel

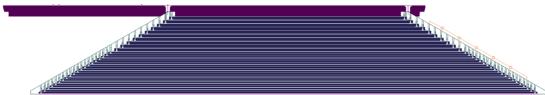


Figure 4.3: ECal module

4.2.4 Engineering Challenges

The following challenges will have to be addressed when proposing this technology for ILD:

- cost reduction of calorimetric silicon sensors, direct contact with producers is already established (Hamamatsu, LFoundry, On-Semi, . . .).
- A chip with the good trigger stability, dynamic range, low noise and power dissipation, power pulsing etc.
- Integration in a compact device, satisfying all the requirements (mechanical tolerances, readout signal quality, heat dissipation / cooling, reliability).
- Industrialization of solutions, scalability of all elements for O(10M) or 100M channel detector.

4.3 Silicon Tungsten SiD ECAL

Contact person: Marty Breidenbach (email: mib@slac.stanford.edu)

This note describes the theory of the mechanical aspects of the E-Cal system for SiD. The E-Cal barrel consists of stacks of tungsten heavy metal plates which are arranged in modules surrounding the beamline. Full cylindrical coverage of the baseline design is attained with twelve modules (see Figure 4.2) occupying a radial envelope from 1265 mm to 1409 mm. The total barrel length is 3.53 m. Each module uses 20 inner plates which are 2.5 mm thick followed by ten 5 mm thick plates. Gaps between adjacent plates are 1.25 mm and house the silicon detectors with their associated cables (see Figure 4.3). These hexagonal silicon detectors are electrically connected to each other with thin, flexible circuits which are read out on both ends of a module (see Figure 4.4). Panels of detectors increase in width as they get closer to the beamline. To minimize silicon waste and to maximize coverage, fractions of hexagons complete the panel edges (see

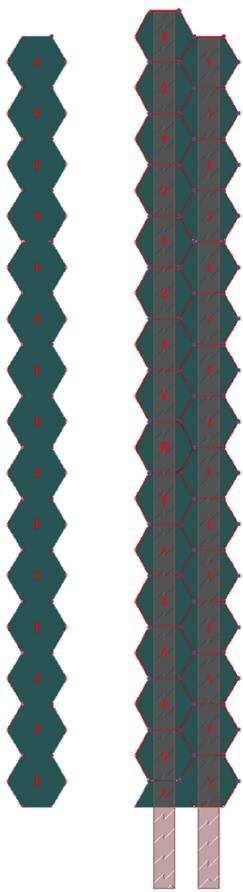


Figure 4.4: Hexagonal silicon detectors with flexible circuit interconnects

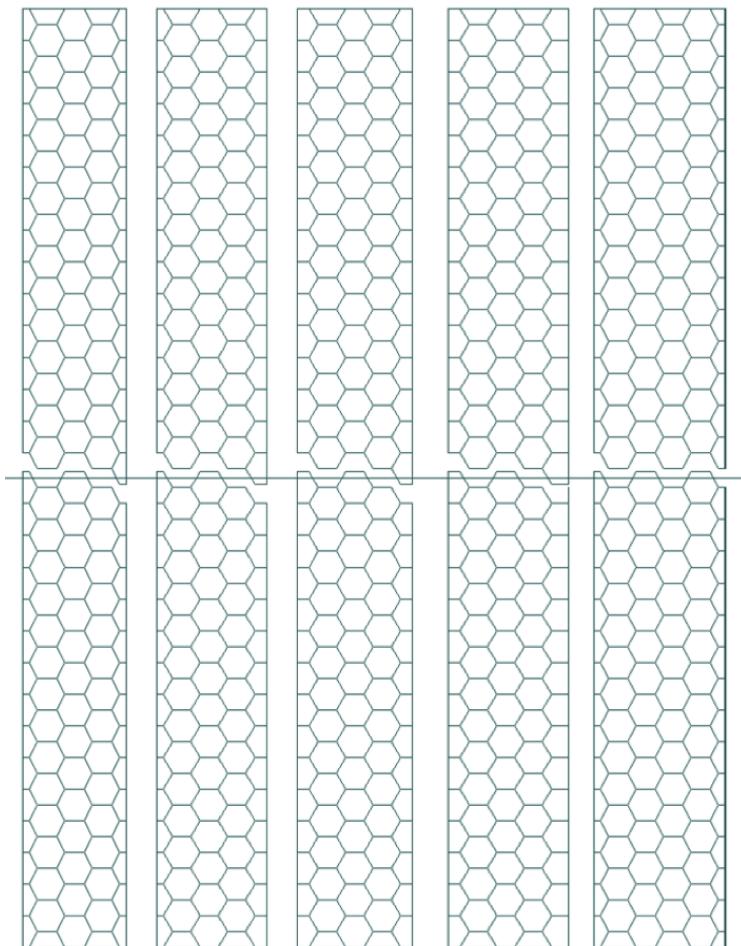


Figure 4.5: Silicon layout for five outer layers

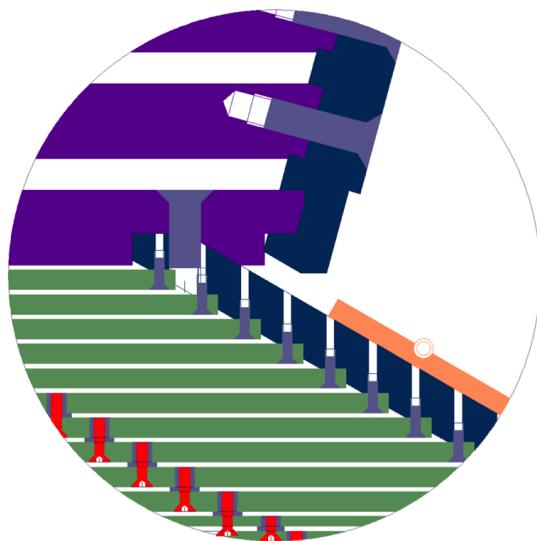


Figure 4.6: Edge and field fasteners

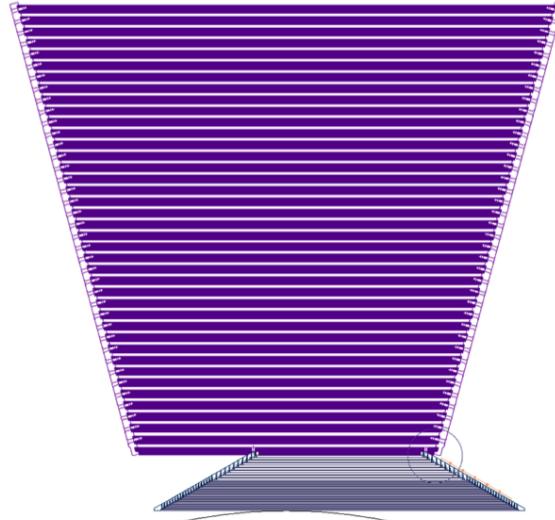


Figure 4.7: ECal to HCal mounting

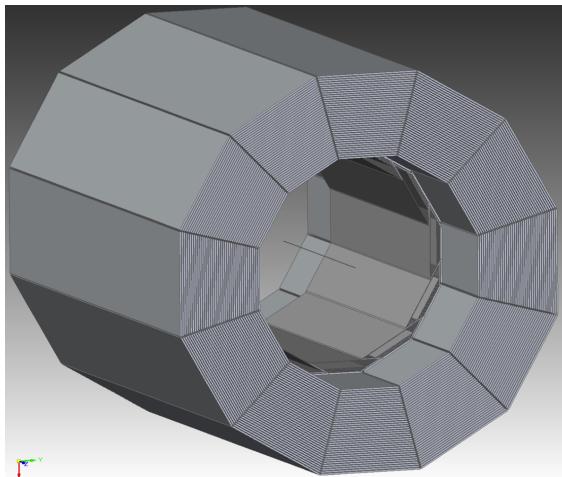


Figure 4.8: HCal with integral ECal detector

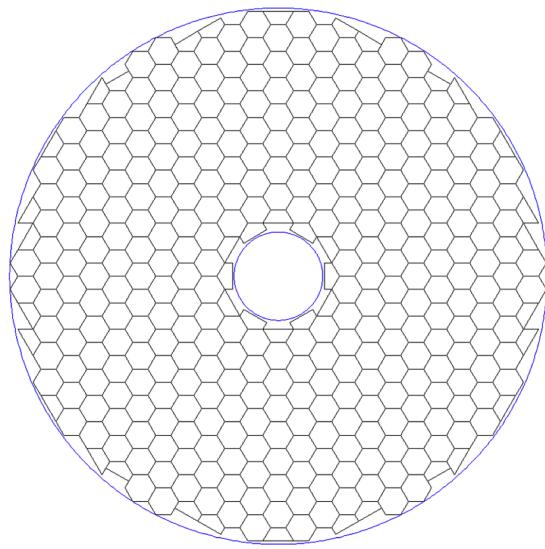


Figure 4.9: Endcap detector layout

Figure 4.5). By cutting the silicon in strategic locations, only a few different silicon shapes may be needed to achieve the 31 different panel widths. The tungsten plates are connected together on their longitudinal edges as well as in the field of detectors. Space for fasteners in the field is achieved by chamfering the corners of the hexagonal detectors. The field fasteners hold the plates together, provide a uniform 1.25 mm standoff height, and assist with inter-plate shear. The fasteners near the edges of the plates close the module profile and lend torsional rigidity to the structure. An FEA simulation of the proposed configuration should be done to properly size the fasteners (see Figure 4.6). The modules, which weigh about 5 tons each, are mounted to stainless plates which are used as the first layer of the next detector system (H-Cal). This first H-Cal plate is unique in that its two longitudinal edges form a guide system to locate the E-Cal to the H-Cal system. The H-Cal modules are first bolted together to form the H-Cal barrel. Interleaving structural side battens maintain spacing for the H-Cal plates and extend inward to the E-Cal support plates. The inner ends of these battens act in concert as the female portion of the E-Cal guide system. The E-Cal modules are slid into place in the inner H-Cal bore. Extension plates complete the inner H-Cal first layer, since the E-Cal barrel is shorter. H-Cal detector panels are installed after this structure is complete (see Figure 4.8). Only simple detector layouts have been done for the E-Cal endcaps so far. These layouts show that using full and partial hexagons could yield fairly good coverage with only a few shapes. (see Figure 4.9).

4.3.1 Introduction

KPiX is a 1,024 channel “System on a Chip” intended for bump bonding to large area Si sensors, enabling low multiple scattering Si strip tracking and high density Particle Flow calorimetry for SiD at the International Linear Collider (ILC).

Each channel consists of a dynamically switchable gain charge amplifier; shaping; threshold discrimination; and 4 sample and hold capacitors and 4 timing registers. The chip permits 4 separate measurements of amplitude and time of threshold crossing during each train, and amplitude digitization and readout during the intertrain period. The dynamic range is from sub minimum ionizing particle (mip) (320 μm silicon) to more than 2,000 mip. KPiX also has a calibration system for each channel, servos for leakage compensation, “DC” reset for asynchronous operation for testing with cosmic rays, and polarity inversion for use with GEMs and similar detectors. The noise floor is about 0.15 fC (\approx 1,000 electrons), and the maximum signal is 10 pC (utilizing the dynamic range switching). The full dynamic range corresponds to 17 bits.

4.3.2 Recent Milestones

ILC related R&D in the US is largely unfunded and small efforts are being kept alive on the margins. The KPiX R&D is such an example of necessary work for SiD that is marginally alive. At this time, KPiX is seen as the baseline readout system for the tracker and electromagnetic calorimeter . A stack of 13 EMCal sensors with bump bonded KPiX was assembled for a beam test at SLAC in the summer of 2013. That test discovered that two kinds of crosstalk are significant:

- In-time crosstalk occurs due to parasitic coupling of traces on metal 2 of the sensor to other pixels. The level of crosstalk increases with the size of the signal, and decreases with increased speed of the front end charge amplifier (meaning increased current and power dissipation). A new sensor design is being developed that uses metal 1 to shield the traces of metal 2, and these ideas will be tested in the next sensor prototype.
- Out-of-time cross talk occurs when many pixels are hit and reset simultaneously. The resets collectively cause other pixels to trigger, and a cascade builds up. This uses up all the KPiX buffers. The

root cause of the problem appears to be some internal logic within KPiX that is not current limited, and will require design modification.

A more general issue is that both the EMCal and tracker sensors from Hamamatsu were ordered with Al pads, as it was believed that plating (by the zincate process) a stack of metals culminating with Au would be straightforward. This turns out to be wrong. After many attempts at University of California Davis (UCD) and local industry, IZM has Ar ion etched the pad surfaces and sputtered a base layer, permitting the buildup of a stack that ended with Au, and permitting the attachment with solder bumps that had been placed during KPiX manufacture by TSMC. Testing of these sensors revealed $\approx 10\%$ pixel to pixel shorts and some opens of signal traces, that are suspected to be damage caused by the Ar ion etch. A new round of sensors has been ordered with the Metal 1 layer used to shield the Metal 2 traces from the diodes that they cross on the way to the KPiX bump pads, and with the Au pads being built by Hamamatsu.

An additional issue is that the Tracker sensor was planned to be wire bonded to its (very thin) cable. The sensor oxide layer is not strong enough to allow wire bonding without damage, and so must be solder bumped. The pad pitch is small, and solder bumping the cable will be challenging. The trouble with the wire bonding to the sensor was unexpected. Recent attempts with both bump bonding a cable and utilizing electrically conductive epoxy have failed. The best explanation is that the $150\text{ }^{\circ}\text{C}$ thermal cycles associated with these attachments increased the stress on the KPiX bonds and caused the sensor pads to separate from the sensor. It is believed that something went wrong with the Hamamatsu process on both types of sensors, and is related to the wire bonding problem.

Another concern is that the current design of KPiX has deadtime after a pixel has accepted a trigger. Only the triggered pixel is affected; all the other pixels are available for signals. This deadtime is different from the usual notion of data acquisition deadtime where the entire detector is unavailable, but the correction to the luminosity integral is easy. Finally, the buffer requirement (4 in the current version of KPiX) is being re-evaluated in SiD simulations. A possible new architecture for KPiX is in early stages of evaluation. Another approach is the development of Monolithic Active Pixel (MAP) sensors for both SiD sensors using thinned HVCMS. The sensors would be approximately the same size as the current sensors. The tracker would have $40 \times 500\text{ }\mu\text{m}$ pixels, and would only need one buffer. A prototype to evaluate the pixel performance is being designed now. The EMCal sensor will have $1 \times 1\text{ mm}$ pixels which should limit the required dynamic range and eliminate range switching, but would still need 16 buffers.

A small mechanical engineering effort has started to study the structure of the EMCal. The SiD EMCal has emphasized thin gaps between the tungsten layers to minimize the Moliere radius, and this implies that the structure is connected by columns at the vertices of the sensors. This work has been carried out to the level of a pre-conceptual design.

4.3.3 Engineering Challenges

4.3.4 Future Plans

Assuming positive developments with Japan are announced soon, we expect the financial support to improve. It should be noted that an important effect of the withdrawal of support is that most of the US collaborators have been forced to move to other work.

- EMCal Sensors: A second round of prototypes will be designed and ordered with rectangular layout; shielded traces, and Au pads.
- Tracker Sensors: The current prototypes will be evaluated, and if appropriate tested in a beam.

- KPjX: A new architecture with little (or no) deadtime will be evaluated. A decision will be made to develop this new architecture or incrementally improve the existing design.
- The EMCal mechanical structure will be pushed towards a conceptual design.

4.4 DECAL

Contact person: Jan Strube (email: jan.strube@pnnl.gov)

The studies of a digital ECAL (DECAL) continue in the UK, in spite of very significant funding difficulties. In December 2008, the STFC Executive recommended sufficient funding to allow the SPiDER Collaboration to construct a full physics prototype DECAL, as outlined in [110]. By December 2009, the funding for SPiDER had still not been issued and STFC informed the Collaboration that they would not do so.

The UK groups in SPiDER have demonstrated that the INMAPS technology developed specifically for the DECAL application is viable in terms of basic pixel efficiency. INMAPS is implemented as a $0.18\text{ }\mu\text{m}$ CMOS process in which a deep P-well implant stops signal charge from being absorbed in N-well circuits, and therefore allows the use of both NMOS and PMOS within the pixel, as well as (optionally) high resistivity silicon in the thin epitaxial layer to reduce the charge collection time.

4.4.1 Test Beams in 2010

Following a successful test beam run at CERN in September 2009 using 120 GeV pions, two further data taking runs have been carried out. The first of these was at DESY in March 2010, for which the primary goal was to quantify the peak electromagnetic shower density observed downstream of specific absorber materials. A secondary goal was to make further pixel efficiency measurements. Data were recorded with the 1-5 GeV electron beam, using a configuration in which four TPAC 1.2 sensors were aligned precisely along the beam direction using the same custom-built mechanical frame as at CERN. Absorber material (W, Fe, Cu) was placed downstream of these, followed immediately by a further pair of TPAC sensors, to study the shower density.

To complement the DESY run, similar, additional data was recorded at CERN in September 2010, using the EUDET telescope alone as it has finer pitch than the TPAC sensor, with positrons between 10 and 100 GeV. The same slabs as those at DESY were used together with new slabs due to the higher energies available at CERN. Initial results of shower multiplicities are presented in [111].

4.4.2 Pixel efficiency results

The studies of pixel efficiency from CERN 2009 testbeam and DESY were performed using a set of six TPAC 1.2 sensors aligned along the beam direction, in which the outer four sensors served as a beam telescope, while the two innermost sensors were considered as the devices under test. The trajectory of the beam particle was projected onto the plane of both of these sensors, and each pixel of the test sensors was examined for the presence of hits as a function of the distance from the projected track. The MIP hit efficiency was determined by fitting the distribution of hit probability to a flat top function, convoluted with a Gaussian of the appropriate resolution to allow for finite tracking performance. This efficiency, folded for all pixels together, is illustrated in Figure 4.10

The MIP efficiency was determined per pixel for both the DESY and CERN data, and for each of the four pixel variants tested. The variants (and corresponding marker color in Figure 4.10) are:

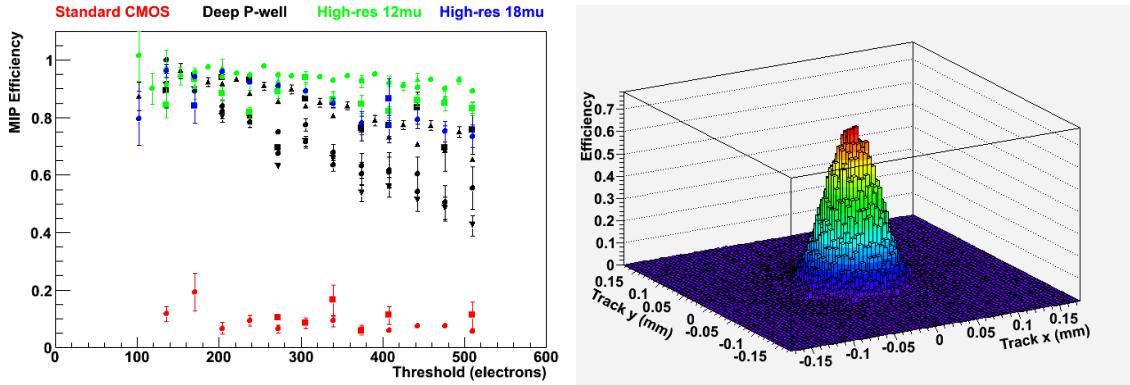


Figure 4.10: (left) Distribution of the probability of a pixel registering a hit in response to a MIP, as a function of distance to the projected track, and (right) MIP efficiency as a function of the sensor digital threshold, for all four sensor variants studied.

1. (red) in 12 μm standard (non-INMAPS) CMOS;
2. (black) 12 μm deep P-well CMOS;
3. (green) deep P-well within a 12 μm high resistivity epitaxial layer;
4. (blue) deep P-well within an 18 μm high resistivity epitaxial layer.

The results [112] are summarized in Figure 4.10, for a range of the sensor digital thresholds representative of the signal levels expected in DECAL pixels due to charge spreading. (A typical MIP signal in a 12 μm epitaxial layer of silicon is 1200 electrons and a single pixel absorbs at most 50% of this due to charge spreading.)

From the results shown in the figure, it is observed that the standard, non-INMAPS sensors have markedly low efficiencies, which is attributed to signal charge being absorbed by in-pixel PMOS transistors. In contrast, the use of the deep P-well reduces the absorption of signal charge by N-wells in the circuitry, improving very substantially the pixel efficiency by a factor of ≈ 5 . The addition of the high resistivity epitaxial layer further improves the pixel efficiency to $\approx 100\%$.

4.4.3 Future plans

It is no longer an option to plan for a physics prototype DECAL and the short-term future of the DECAL project is extremely uncertain at present. A program of radiation hardness has been conducted on 2011 and the results are summarized in [111, 113]. This is in part to understand how the TPAC sensor would satisfy the requirements of ALICE ITS and SuperB. The studies which have been carried out so far are in the process of being finalized, and a series of papers, e.g. [114], are in preparation to document what has been achieved. The technology development has been taken over by the Arachnid collaboration who are testing the CHERWELL chip (designed and manufactured by the SPiDeR collaboration but never used due to money constraints) to evaluate the performance for ALICE and SuperB.

4.5 Resistive Plate Chambers

Contact person: Jose Repond (email: jose.repond@anl.gov)

4.5.1 Description of the DHCAL

The Digital Hadron Calorimeter or DHCAL uses Resistive Plate Chambers (RPCs) as active elements. The chambers are read out with $1 \times 1 \text{ cm}^2$ pads and 1-bit (digital) resolution. A small-scale prototype was assembled and tested in the Fermilab test beam in 2007 to validate the concept. Based on the success of the small-scale test [1-6], a large prototype with up to 54 layers and close to 500,000 readout channels was built in 2008 – 2011. Each layer measured approximately $96 \times 96 \text{ cm}^2$ and was equipped with three chambers, stacked vertically on top of each other. For tests with particle beams the DHCAL layers were inserted into a main stack of 38 or 39 layers, followed by a tail catcher with up to 15 layers. For the tests performed at Fermilab the main stack contained steel absorber plates. At CERN the absorber plates were made of a Tungsten based alloy. In both cases the tail catcher featured steel absorber plates. In the various test beam campaigns combined, spanning the years 2010 – 2012, the DHCAL recorded around 14 Million muon events and 36 Million secondary beam events, where the latter contained a mixture of electrons, muons, pions, and protons.

4.5.2 Current R&D activities

The analysis and publication of the test beam results are currently the highest priority of the DHCAL group. Major challenges, such as the calibration (or equalization) of the response of the RPCs and the detailed simulation of the response of RPCs, are very close to having been overcome [7-11]. Parallel to the analysis of test beam data, the group is pursuing the following R&D activities:

Development of 1-glass RPCs

The DHCAL prototype featured a standard chamber design based on RPCs with two resistive plates. It is possible to eliminate one of the glass plates in future applications. The advantages are: close to unit pad multiplicity with significant simplification of the calibration and monitoring procedure, reduced thickness of the active element, higher rate capability, and insensitivity of the response to the surface resistivity of the resistive layer (used to apply the High Voltage). To date several 1-glass RPCs have been assembled. The chambers tested very well with cosmic rays. Tests in particle beams are planned for future test beam campaigns.

Development of high-rate RPCs

Due to the high bulk resistivity of glass (and Bakelite), RPCs are notoriously rate limited [115]. The DHCAL group is addressing this shortcoming with the developments of semi-conductive glass (in cooperation with COE college) and low-resistivity Bakelite (in co-operation with USTC). First chambers with samples of low-resistivity glass plates have been assembled and have been tested in the Fermilab test beam.

Development of a High-Voltage distribution system

With up to 50 layers in a single calorimeter module, a cost-effective way to distribute the High-voltage to individual layers is required. A system capable to regulate the voltage within a few 100 V, to monitor both

the current and the voltage, and to switch off individual channels, is being developed. A first prototype controlling a single channel has been assembled and tested successfully with an RPC. The development is currently on hold due to lack of funding.

Development of a gas recycling system

The operation of RPCs requires a gas mixture, which is both costly and environmentally harmful. To limit the effect of releasing gas into the environment, the DHCAL group is developing a gas recycling system. The system is based on a new approach, appropriately labeled Reference “Zero Pressure Containment”. A prototype of the gas collection subsystem is currently being assembled; however, progress is again slow due to lack of funding.

Development of the next generation front-end readout system

The next generation front-end readout system will contain several upgrades compared to the current system: higher channel count, token ring passing, low power operation, power pulsing, and improved internal charge injection systems. To proceed, the project is awaiting funding from both US and Chinese agencies.

4.5.3 Engineering challenges

Several engineering challenges remain to be addressed before an RPC-based DHCAL can be proposed as an option for a colliding beam detector. Following is an (incomplete) list of the major issues:

- Industrialization of the construction of RPCs.
- Design of the readout boards, covering the entire area of the layer (with varying width). The design is expected to feature only a minimum number of different boards.
- Design of the gas distribution system, which ensures equal pressure in all layers of a given module, independent of its orientation.
- Development of a cooling strategy for the front-end boards, which will include power pulsing, as well as active cooling.
- Development of a module assembly procedure.

4.5.4 Plans for the coming years

The activities of the coming years depend strongly on the progress with the Japanese intentions to host the ILC. Assuming the ILC project goes ahead, the DHCAL group will a) Complete the analysis and publication of the test beam data, b) Complete the R&D projects listed above, and c) Start the development of the design of calorimeter modules. In case, the ILC is not going forward, the group plans on completing the data analysis and to continue the tests of high-rate RPCs. Other R&D projects, such as the development of distribution systems, will be put on hold.

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4.6 GEM

Contact person: Andy White (awhite@uta.edu)

4.6.1 Introduction

The High Energy Physics group at UTA has been developing a new type of calorimetry, based on the Particle Flow technique, for experiments at the future International Linear Collider. White proposed the application of GEM [55] technology to digital hadron calorimetry. Basic requirements include, the ability to achieve a high level of transverse and longitudinal segmentation, a MIP signal well separated from the noise level, a high density front-end readout to handle the large number of channels, and flexibility in the design and implementation of a variety of active layer sizes in realistic size modules. GEM technology offers a viable and attractive solution to these requirements. Our proposed digital hadron calorimeter (Figure 4.11) comprises a stack of steel absorbers, of sufficient thickness to contain hadronic showers, interlaced with active gaseous sampling-elements.

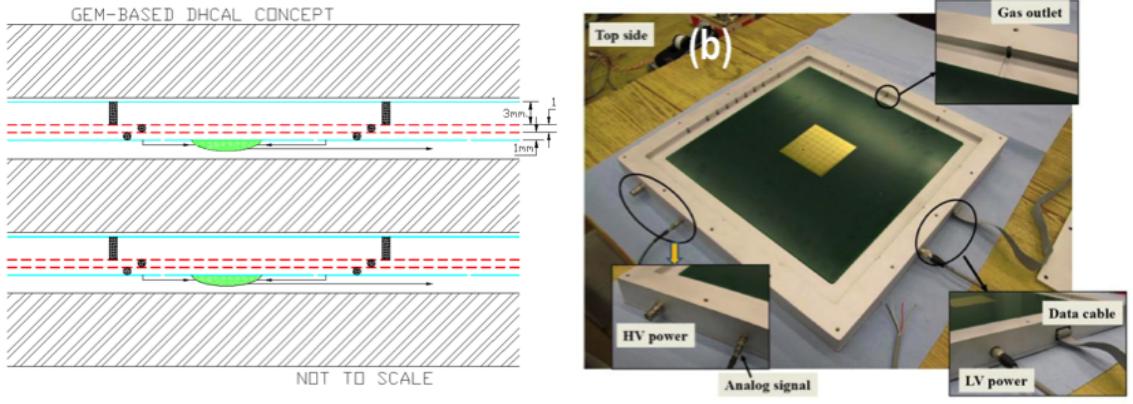
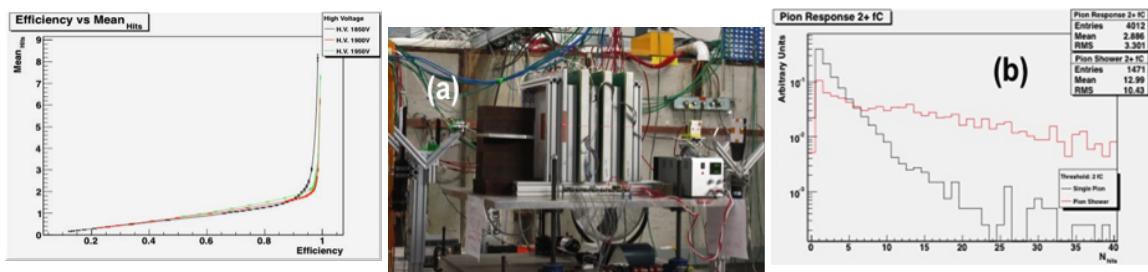


Figure 4.11: Concept for a Digital Hadron GEM-based Calorimeter

Figure 4.12: Concept for a Digital Hadron GEM-based Calorimeter



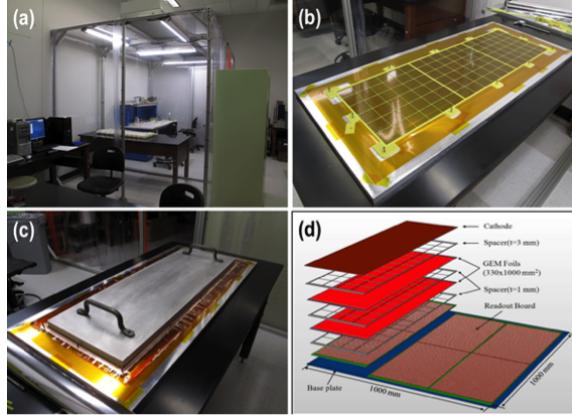


Figure 4.16: Large scale GEM chamber activity at UTA: (a) Purpose-built clean room for handling large foils, (b) partially assembled 33 cm × 100 cm double-GEM chamber, (c) glue curing stage under pressure plate, (d) schematic view of three 33 cm × 100 cm chambers integrated in a 1 m² chamber.

4.6.2 Recent Milestones

A series of prototype detectors (Figure 4.12) has already been constructed and tested using 10 cm × 10 cm GEM foils from CERN and 30 cm × 30 cm GEM foils from 3M Corporation and CERN [128]. The KPiX chip from SLAC was used for the readout. KPiX has a four-deep pipeline, on-board DAC charge injection calibration, and a Wilkinson 13-bit ADC for each of its 1024 channels. Results from exposure to cosmic rays, and an external, scintillator trigger, yielded MIP detection efficiency of 95%, in agreement with simulation predictions. The corresponding hit multiplicity, the average number of hits seen in a single active layer when one particle passes through, was measured to be 1.7 (Figure 4.13). This predicts only little confusion in track following and energy cluster definition in a final calorimeter system. A gas mixture of Argon 80%, CO₂ 20% was used throughout these initial studies, and for which a most probable signal size of 10 fC was measured for a MIP. The detector gain was about 3,500. Various chambers (Figure 4.14) were also exposed to a test beam at Fermilab, with satisfactory stable performance for single pions (non-interacting) and showers induced by steel absorber in front of the chambers [129].

4.6.3 Engineering Challenges

CERN has demonstrated that large area GEM foils can be successfully produced using the single-side etching technique. This technology would need to be available from a commercial manufacturer for large quantity production. The main challenges would then be the assembly of many different size double-GEM chambers, for the 40 layers of a DHCAL, the longitudinal division of the barrel chambers, with solutions to the provision of high voltage and gas through multiple chambers and the extraction/readout of the signals from the large number of small pads.

4.6.4 Future Plans

The next stage in the development of GEM-based DHCAL is the construction of large area chambers. We have received and qualified five 33 cm × 100 cm large GEM foils. We are developing the mechanical

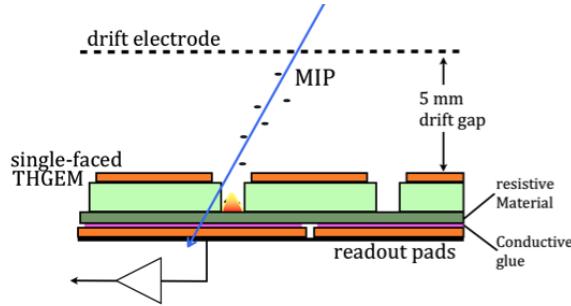


Figure 4.17: The RPWELL configuration with a resistive anode and a readout electrode. The WELL, a single-faced THGEM, is coupled to a readout anode (e.g. with strips or pads) via a resistive plate.

structure, the electronic readout board schemes and the schemes for integrating the three unit chambers ($33\text{ cm} \times 100\text{ cm}$) into one $1\text{ m} \times 1\text{ m}$ plane (Figure 4.16). We plan to construct and test two of these $33\text{ cm} \times 100\text{ cm}$ unit chambers initially. Work on the large chambers is currently waiting the resumption of support for ILC detector activities in the U.S.

4.7 THGEM-based sampling elements for DHCAL

Contact person: Shikma Bressler (email: shikma.bressler@cern.ch)

4.7.1 Introduction

Digital Hadronic Calorimetry (DHCAL) for future experiments (e.g. ILC-SiD) requires robust thin sampling elements with high detection efficiency at low pad multiplicity. The large detection area foreseen requires cost-effective solutions. In the past two years, a Weizmann-Aveiro-Coimbra team has shown that sampling elements based on Thick Gaseous Electron Multipliers (THGEM) [130] could meet DHCAL requirements. The THGEM concept has evolved from a cascade of double-sided electrodes coupled to a pad-anode through an induction gap [131], to thinner single-sided WELL detectors - coupled to the pads with and without resistive films [132, 133]. The most recent and presently leading candidate is the Resistive Plate WELL (RPWELL). It was tested extensively in the laboratory [134, 135] and at muon and high-rate pion beams at CERN-SPS. This very thin single-stage detector yielded a discharge-free operation in different gas mixtures, including Ne- and Ar-based ones, providing high detection efficiency at low pad multiplicity.

The Resistive Plate WELL

The Resistive Plate WELL (RPWELL) is a single-sided THGEM (with copper clad on one side only), coupled to the readout pads through a material sheet with high bulk resistivity (see Figure 4.17). Materials with bulk resistivity in the $10^9\text{ }\Omega\text{cm}$ scale prevent significant gain-, and hence efficiency drops, at high particle flux [134].

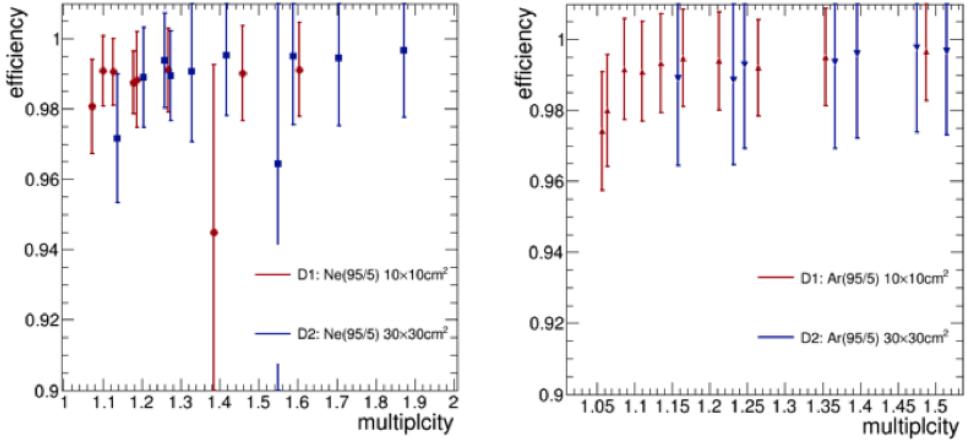


Figure 4.18: Efficiency as a function of the average pad multiplicity measured with the $10 \times 10 \text{ cm}^2$ and $30 \times 30 \text{ cm}^2$ detectors in muon beam. Left: Ne/5%CH₄ gas mixture. Right: Ar/5%CH₄ gas mixture

4.7.2 Recent Milestones

Small ($10 \times 10 \text{ cm}^2$) and medium size ($30 \times 30 \text{ cm}^2$) RPWELL detector prototypes were built and tested in the laboratory and at the CERN-SPS. The 0.8 mm thick WELL electrodes were coupled to $1 \times 1 \text{ cm}^2$ copper pads through 0.4 mm thick Semitron ESD225 resistive polymer ($\approx 10^9 \Omega\text{cm}$ bulk resistivity). With a 5 mm drift gap the sampling element had a total thickness of 6.2 mm (excluding readout electronics – here SRS-APV [136, 137]). The detection efficiency as a function of pad multiplicity (with low rate muons) is shown for the two prototypes in Figure 4.18. Both detectors reached high detection efficiency at low pad multiplicity when operated in our traditional Ne/5%CH₄ (Figure 4.18 left; operation voltage, V, in the range 800 – 930 V) and in the cost-effective Ar/5%CH₄ (Figure 4.18 right; V in the range 1500 – 1720 V) gas mixtures. Figure 4.19 shows the measured gain as a function of the particle flux; the same operation voltage of 880 V was maintained throughout the measurements (with low rate muons as well as high rate pions). A moderate gain-drop of $\approx 30\%$ was measured while the flux was increased by 3 orders of magnitude (from 50 to 10^5 Hz/cm^2). It resulted in negligible efficiency drop, since the pulse-over-threshold was sufficiently high. Most importantly, during the two weeks of in-beam operation (which included also long time operation under high rate, 10^5 Hz/cm^2 , pion beam), with both Ne-based and Ar-based gas mixtures, the small prototype was completely discharge-free. The resulting discharge probability is therefore below 10^{-8} . Occasional discharges occurring in the medium-size prototypes were traced to be associated with defects in some support pins within the active area; these can be avoided in the next prototypes. The RPWELL laboratory and test-beam results are the subject of two articles in preparation.

4.7.3 Engineering Challenges

The novel design of a large RPWELL detector prototype (without the present support pins) is completed. Assembly and tests are foreseen in the coming year. Upon success, we are confident that future chambers could be fully industrially produced. We are currently investigating, with industry, alternative materials

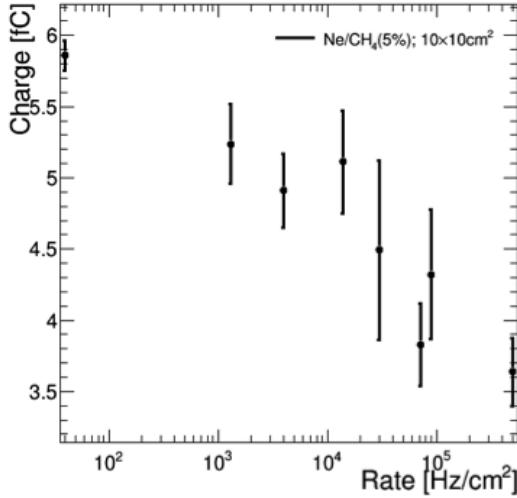


Figure 4.19: The charge (estimated from the spectra most probable value) as a function of the incoming particle flux. All the measurements were conducted at Ne/5%CH₄ gas mixture at the same operation voltage of 880 V. A pion beam was used to generate the high incoming fluxes.

and production technologies of THGEM electrodes; similarly, we are considering different resistive-plate materials, with of appropriate bulk resistivity.

4.7.4 Future Plans

As mentioned earlier, in the forthcoming year we intend to build a new medium-size detector prototype, to be followed by a prior to our square-meter one. Both prototypes will be tested in the laboratory and in muon and pion beams (CERN). We foresee investigating the properties of several RPWELL layers in a fully-equipped DHCAL prototype; in particular their performance in measuring Hadronic showers.

4.8 Analog HCAL

Contact person: Felix Sefkow (email: felix.sefkow@desy.de)

4.8.1 Introduction

With the advent of silicon photo-multipliers (SiPMs), the scintillator tile technology became a candidate for highly granular particle flow calorimetry. With analog read-out, energy and spatial resolution can be optimized independently. The particle flow performance is well understood; all published studies using PandoraPFA are based on this technology.

The CALICE AHCAL was the first large LC hadron calorimeter prototype to be exposed to test beams. Analysis is nearly complete and mostly published; the results validate the technology and the simulations.

The development of engineering solutions for a realistic detector is on its way. The integration of read-out electronics and calibration system into the detector layers has been demonstrated. The next step, an integrated stack, is being prepared. In parallel, as improved photo-sensors become available from industry, the design of the basic read-out cell – the tile with SiPM – is optimized with regard to mass production procedures.

4.8.2 Recent Milestones; past and present R&D

Test beam data analysis

The following results using data taken with the first AHCAL “physics” prototype in 2006 – 2011 at CERN and Fermilab have been published in peer-reviewed journals:

1. Detector construction, noise and aging studies [138]
2. Electromagnetic linearity and resolution [139]
3. Hadronic linearity and resolution, software compensation [140]
4. Test of particle flow algorithms (AHCAL with SiW ECAL) [97]
5. Studies using a scintillator SiPM based tail catcher [141]
6. Geant 4 validation with pion showers [142]
7. Geant 4 validation with tungsten absorber (low energy) [143]
8. Imaging capabilities, track segments [144]
9. Time structure of showers in Fe and W [145]
10. Geant 4 validation with protons [146]
11. Geant 4 validation with tungsten absorber (high energy) [147]

We consider all of them as critical for validating a given HCAL technology. Papers [142], [143], [144], [145], [146] and [147] appeared after the ILC TDR was handed over.

Preliminary results have been made public in the form of *CALICE Analysis Notes* after thorough internal reviewing on the following topics:

1. Combined performance SiW ECAL + AHCAL + Tail Catcher [148]
2. Leakage estimation using shower topology [149]
3. Parameterization of pion and proton shower shapes [150]
4. Analogue, Digital and Semi-Digital Energy Reconstruction [151]
5. Extraction of h/e from the longitudinal shower profiles [152]

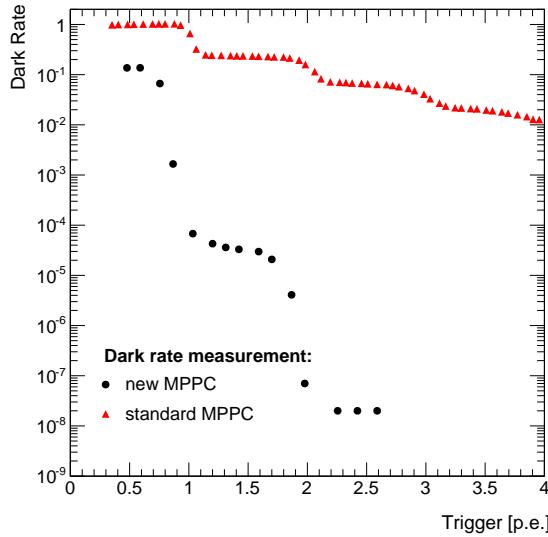


Figure 4.20: Dark count rate of recent SiPMs, MPPC devices by Hamamatsu, without (standard) and with (new) inter-pixel cross talk suppression. (*Courtesy MPI for Physics, Munich*)

Notes [150], [151] and [152] appeared in the time since the release of the ILC TDR. The studies are actively being followed up towards final publication; only the leakage study is presently uncovered due to lack of manpower.

Studies of the combined performance of the AHCAL in conjunction with the scintillator tungsten ECAL with MPPC readout are on-going. Results are expected later this year and will make the analysis of the first generation test beam data complete.

Data taking with a first, partially instrumented stack of the second generation has started at DESY continued in fall 2014 with electrons and hadrons at CERN. A framework for analysis software exists, but calibration and correction procedures for timing measurements still need to be developed.

The CALICE test beam results are nowadays the primary source of validation for hadron shower simulation, according to Geant 4 representatives, and extremely valuable for other HEP experiments, e.g. at the LHC, as well.

We finally note that test beam analysis plays an important role in training our students. Roughly speaking, each paper or note corresponds to one or several PhD theses. It is a distributed effort, the corresponding editors of the papers are from about 10 different groups.

Optimization of the scintillator SiPM read-out cell

As a consequence of the wide success of SiPM applications in other fields, e.g. in medical imaging, the development of improved sensors is dynamically pursued in industry, and several groups are in close contact with leading producers. Progress has been made in terms of dark rate (see Figure 4.20), noise above MIP threshold and dynamic range. For comparison, typical SiPMs in the first generation prototype at an the first generation had a dark rate of about 2 MHz and a cross talk probability of about 25%. In addition, the samples are much more homogeneous than at the time of the first prototype, which results in a simplification of commissioning and calibration procedures.

In the time since the TDR, tile SiPM cells without wave-length shifting fiber have been developed. One is based on machined, individually wrapped scintillator plates, the other one on injection-molded tiles. Both are using sensors from KETEK, those on the molded tile have a very large dynamic range. 300 devices have been produced and tested, and more than thousand devices have been produced and tested with semi-automatic procedures at Hamburg and Heidelberg. They been integrated into the test beam set-up and tested at DESY and CERN in 2014 and 2015. This version is a good candidate for a baseline design for a full detector, but more data taking and analysis is needed.

Industrialisation of the SiPM and tile design and production procedures is now actively being addressed, and first assemblies with industrial facilities such as automatic pick-and-place machines have been made. This needs to be continued in the coming years, fed back into the cell optimization, and awaits a feasibility demonstration at larger scale.

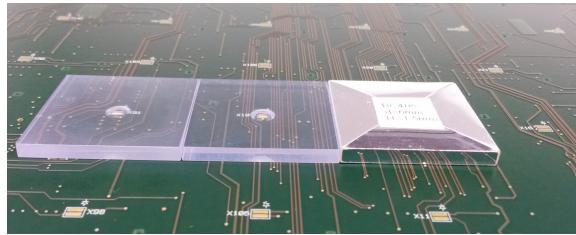


Figure 4.21: AHCAL read-out board with surface-mounted SiPMs and tiles. (*Courtesy University of Mainz*)

An alternative cell design, with photo-sensors integrated in the read-out electronics board, has been proposed some time ago, and the detailed development of the corresponding sensor and scintillator configuration is now being pursued. It has the potential to result in further simplifications (which should be read as cost and time savings), but poses higher performance requirements to the SiPM – which can now be met – and raises new issues in the quality assurance and integration chain. The goal is to fully develop such an alternative solution in the next 2 years. A prototype of this design is shown in Figure 4.21 and has already been successfully operated in the 2014 and 2015 test beam campaign.

Electronics and active layer integration

The design of the active layers with integrated read-out ASICs and calibration system has been basically validated in beam tests of a single HCAL layer consisting of four base units (HBUs) at CERN in 2012 and reported in the TDR. An HBU reads 12×12 tiles with 4 ASICs. The present ASIC belongs to the 2nd generation ROC family used also in ECAL and SDHCAL. An HCAL layer carries interfaces for DAQ, calibration and power supply, which already have a compact design fulfilling space constraints at an ILC detector.

The main difference between the integrated electronics and that of the physics prototype is the self-triggered operation and on-detector zero-suppression, which implies much higher demands on controlling the noise behavior and ensuring a stable detector response. It is thus mandatory to re-establish the calorimeter performance with a full-scale beam test, including the operation with fast power cycling. However, this is out of reach with present funding levels.

Further R&D in the next years has to be done both on the ASIC and on the PCB. For the ASIC, development of a 3rd generation ROC chip will start after fixing open issues with the 2nd generation. The 3rd will have a more robust slow control architecture and possibly channel-wise buffer management which



Figure 4.22: AHCAL stack with integrated read-out electronics and data concentrator for two complete modules.(Courtesy DESY)

improves rate capabilities. In parallel, an alternative design of the analog part, which can handle a larger range of sensor gain needs to be complemented with a digital part.

The PCB with integrated photo-sensors, as counterpart of the corresponding tile design (see 4.8.2), has been developed, taking automatic production and quality assurance into account. The PCB is also one of the main cost drivers of a particle flow HCAL. Dedicated R&D, in close cooperation with industrial manufacturers, is necessary to bring the cost down. First contacts have been made, and new prototype boards have been manufactured in Korea.

System integration

While the integration of layers is well advanced, that of entire stacks or modules has only begun. Since the TDR release, efforts concentrated on developing a multi-layer DAQ capable of reading larger systems. This was ready for beam tests at CERN in fall 2014 (see Figure 4.22). It involves integration of a dedicated module data concentrator, which collects signals from all layers for sending them to the off-detector data receiver.

Further work will be required to integrate the HCAL DAQ into a higher level system for the purpose of combined beam tests, for example with a tracking device for uniformity studies, or with an ECAL for inter-calibration and combined performance. The same is true for slow control data.

A power supply system with optimized channel density per module is being developed.

It has been demonstrated that temperature-induced variations of the SiPM gain can be compensated by adjusting the bias voltage. The approach has the potential to stabilise the detector response and trigger efficiency and thus simplify operations significantly. Automatic procedures based on this principle need to be developed and implemented for a test at system level.

On the mechanical side, a cooling system needs to be developed. The ASICs integrated in the detector layers are power-pulsed and do not need active cooling, but the interfaces, in particular the power regulators, do. A simple solution for beam tests exists, but a leak-less under-pressure based system for a large detector still needs to be prototyped.

Infrastructure for production, quality assurance and characterisation

The AHCAL is probably the sub-detector with the largest number of individual components. While the number of electronics boards, layers and interfaces is similar to other ECAL or HCAL options, the large

quantity of tiles and SiPMs deserves special attention. This affects production and quality assurance, but also characterisation, i.e. test bench measurements of parameters to be used later for calibration purposes.

While it would be premature to discuss building up full production infra-structure, conceptual solutions need to be developed and exercised using demonstrators, which could be seen as prototypes of future installations. The demonstration requires reasonably large samples of detector elements, in the order of 10000, as they would be needed for a next generation full prototype.

A semi-automatic test stand for SiPMs and tiles has been developed at Heidelberg and used for the elements of the early 2014 beam test. It needs to be adapted for future designs, e.g. with SiPMs integrated in the PCB.

Automatic assembly of HBUs, i.e. of placing and soldering tiles and SiPMs on the PCB, needs to be demonstrated in practice, too. First encouraging tests with individual samples have been reported, but obviously only larger scale tests can validate the concept. A versatile cosmic test stand for the characterisation of several complete active HBUs is under development.

Absorber structure

The absorber structure bears more challenges than for conventional hadronic calorimeters. Due to the much finer longitudinal segmentation and the imperative to minimize the total radius inside the coil, there are many active gaps with tight tolerances. A design has been developed and prototyped, which achieves the required tolerances with a cost-effective roller-leveling process without machining off excess material. Two test structures have been built; one covers the full transverse cross section of a barrel module, the other the full lateral extension. The cassettes housing the active elements have the final design and are used in beam tests.

These structures need to be investigated with respect to their robustness against earthquakes. Simulations of the whole ILD structure have been made, and measurements on the test structures exposed to accelerating forces should be done in order to check the simulations.

As enough active elements become available for instrumenting several active layers at full size, the thermal simulations should be verified with measurements, too. This will constitute an important step in system integration, as it addresses the issues associated with large layers and in particular power distribution, power cycling and heat dissipation.

4.8.3 Summary

The AHCAL effort has produced a number of significant results in the time since the ILC TDR:

- Publication of 6 journal papers and 3 preliminary results in the form of internally reviewed notes, on Geant 4 validation with pions and protons in steel and tungsten, including new observables like track segments
- Development, production and beam test of a new, simplified tile SiPM system without wave-length shifting fibers and improved sensor performance
- Test with electron and hadron beams of a partially instrumented realistic absorber structure with second generation electronics, DAQ and services

4.8.4 Future Plans

The AHCAL is ready to make the next step towards a realistic full-scale prototype and a technical design report. In order to achieve this, coordinated R&D is required in the following areas:

Software and analysis:

- Completion of physics prototype test beam analysis
- 2nd generation prototype reconstruction and simulation software
- Development of timing reconstruction
- Analysis of 2nd generation test beam data

Tile SiPM system:

- Development of scintillator SiPM system with SiPM on the PCB
- Development of associated assembly, quality assurance and characterization procedures
- Development of associated PCB

4.8.5 Engineering Challenges

Electronics:

- establish power-pulsed operation of large layers
- 3rd generation ASIC of ROC family
- ASIC for larger range of SiPM gains
- PCB cost optimization

System integration:

- Integration of DAQ and slow control into higher level system
- Implementation of temperature compensation scheme
- Power supply system
- Cooling system

Mass production concepts:

- Semi-automatic test stands
- Automatic placement and soldering of tiles and SiPMs

Absorber structure:

- Earthquake stability calculations and tests
- Thermal tests with full-scale instrumented and powered structures

There are ample opportunities for new groups to join into any of these fields, depending on the special competences they wish to contribute.

Particular engineering challenges are

- Assess and ensure earthquake stability of the absorber structure whilst maintaining a minimum of dead material
- Developing an active layer element consisting of tiles, SiPMs and readout electronics that can be automatically assembled, including production and quality assurance procedures

4.9 Micromegas SDHCAL

[Engineering Challenges missing](#) Contact person: Max Chefdeville (email: chefdevi@lapp.in2p3.fr)

4.9.1 Introduction

The Micromegas R&D is primarily intended for Particle Flow calorimetry at future linear colliders. It focuses on hadron calorimetry with large-area Micromegas segmented in very small readout cells of $1 \times 1 \text{ cm}^2$. This granularity provides unprecedented imaging capability which can be exploited to improve the measurement of jet energy. Past and current R&D efforts are described with emphasis on achievements since the publication of the ILC Detailed Baseline Design.

4.9.2 Hadron calorimeter design

The design of calorimeters at a future linear collider is optimised for the reconstruction of jets with a Particle Flow method. The SiD HCAL will be segmented in cells of $1 \times 1 \text{ cm}^2$. With a total instrumented area of 3000 m^2 , the number of readout channels will reach 30×10^6 . This unprecedented granularity can be achieved with gas detectors, thin PCBs and embedded front-end ASICs.

In addition, calorimeters will be placed inside the solenoid magnet to insure good matching of electron and charged hadron tracks with their energy deposits in the ECAL and HCAL. To limit cost, a very compact mechanical design is mandatory: e.g. the SiD HCAL would feature 40 layers within $\sim 110 \text{ cm}$. This design relies on very thin active layers to achieve fine sampling ($\sim 0.1 \lambda_{\text{int}} / \text{layer}$) and good hadron energy resolution ($\sim 50\%/\sqrt{E}$). The targeted active layer thickness and length in the barrel HCAL modules are 8 mm and 3 m respectively. To minimise dead zones, readout boards will be placed at the two ends of the barrel modules. Along the beam direction, ASIC will be daisy chained and PCBs connected together with flat connectors and cables.

Active cooling of the active layers is extremely challenging with this design. Instead, it is considered to limit heat dissipation and gradients inside the calorimeters by power-pulsing the front-end circuitry. Power-pulsing is possible because of the particular time structure of the ILC beam. This structure also drives the design of the ASICs which will be self-triggered. During collisions, signals will be processed and stored in memory with a timestamp synchronous to the ILC clock. Between bunch trains, memories are first read out, then the ASIC are turned off. With an ILC duty-cycle of 0.5%, the power consumption can be reduced down to $10 \mu\text{W} / \text{channel}$.

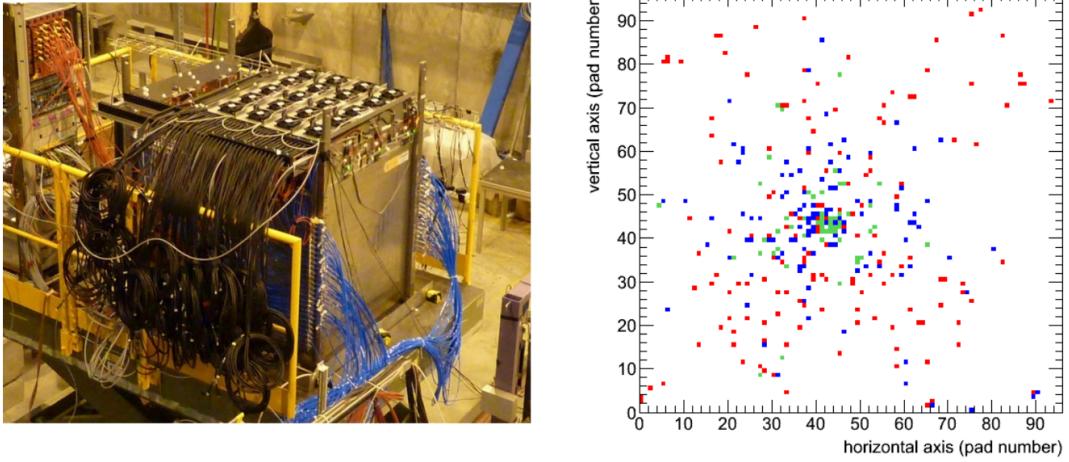


Figure 4.23: SDHCAL prototype in a beam line at the SPS at CERN (left). Event display of a 150 GeV pion shower measured in a Micromegas prototype after $2 \lambda_{\text{int}}$ of steel (right), the color indicates the threshold passed: red for 1, blue for 2 and green for 3.

4.9.3 Recent Milestones

The SDHCAL

The SDHCAL is a prototype of imaging hadron calorimeter equipped with 50 layers of gaseous detectors of $1 \times 1 \text{ m}^2$ interleaved by steel absorbers (Figure 4.23 (left)). Each detectors is segmented in pads of $1 \times 1 \text{ cm}^2$ and the processed pad signal is coded over 2-bits (Figure 4.23 (right)). The number of readout channels per layer imposes to integrated the front-end electronics directly on the gaseous detector printed-circuit-boards (PCB). Several CALICE groups are involved in this project.

The $1 \times 1 \text{ m}^2$ Micromegas prototype

Mechanics The Micromegas layers for the SDHCAL are made out of 6 high-voltage units installed together inside a gaseous chamber (Figure 4.24 (right)). Each unit is an 8 layer PCB with a Bulk Micromegas mesh, readout pads and front-end ASICs; it is dubbed Active Sensor Unit (or ASU). A drift gap of 3 mm is defined by spacers and a frame. Spacers are inserted in between ASUs, resulting in an inactive area of 2%.

Electronics Electronics connections to the DAQ as well as services (power cables, gas pipes) are provided on one side of the prototype. ASU-to-ASU connections are therefore mandatory and are made with dedicated connectors and flexible cables (Figure 4.24 (left)). They are used to distribute clocks and supply power to the ASICs, high voltage to the meshes, to configure the ASICs and read out data. Prior to assembly, 4 ASUs were chained and functional electronic tests were successfully performed. These key features make the design of the $1 \times 1 \text{ m}^2$ Micromegas prototype fully scalable to the required size of a HCAL module at a future LC (at most 2 m in the SiD detector concept).

Noise and detection efficiency A few prototypes were constructed [153] and extensively tested in beam at CERN [154]. Noise conditions were excellent both during standalone tests and inside the CALICE

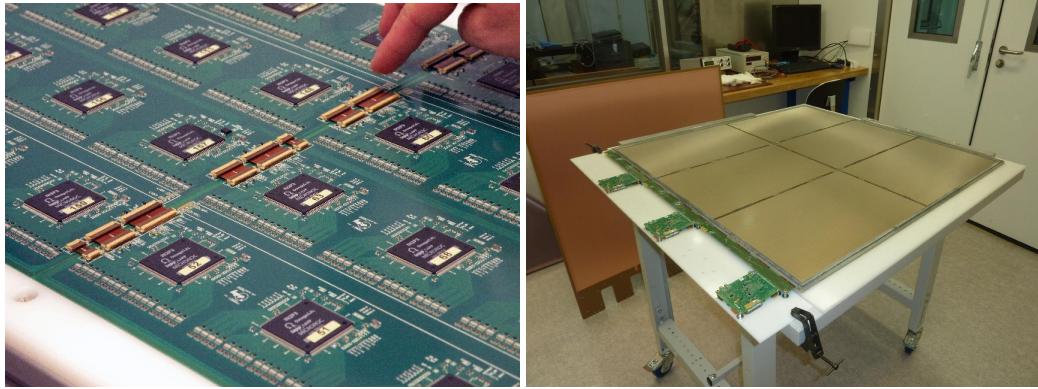


Figure 4.24: Photographs of interconnections between 2 Active Sensor Units (left) and a $1 \times 1 \text{ m}^2$ Micromegas prototype during assembly showing 6 of these units and a drift cover (right).

SDHCAL. ASIC thresholds can be lowered down to about 20% of a minimum ionising particle (MIP) signal at a typical running gas gain of 1500. Efficiency in excess of 95% are easily reached while keeping a pad multiplicity below 1.1 for MIPs. The actual charge threshold is as low as 1–2 fC; it is achieved on ASIC test-boards as well as once mounted on ASUs. The contribution of the PCB internal capacitances to the overall detector noise is therefore negligible.

Standalone performance Thanks to a precise control of the gas gaps and electronics settings, ASIC-to-ASIC variations of efficiency are below the percent in all tested prototypes. Although the statistics is low, the construction process seems reproducible. Stability with rate in high-energy hadron showers is excellent. Except occasional sparks, no effect of beam rate was observed on the pion response up to roughly 30 kHz beam rate; which was the highest rate during the tests. The measured spark probability lies in the range of $10^{-6} \dots 10^{-5}$ per showering pion at a running gas gain of 1500.

Resistive prototypes

While the Bulk Micromegas mesh is made of steel wires and is very resistant to sparking, sensitive front-end ASICs can suffer irreversible damage. Protections in the form of current-limiting diodes networks soldered on PCB were proved so far efficient. To simplify the PCB design and possibly reduce the overall detector cost, it is however desirable to get rid of diodes. It is well known that sparks can be suppressed by means of resistive coatings on the anode pad plane. This solution is used with great success in tracking detectors. Because it modifies the signal development, it needs some adaptation to calorimetry so as to preserve linearity and keep a narrow pad response function for Particle Flow reconstruction.

First resistive designs using resistive strips and pads were implemented on small size prototypes. In a mixture of Ar/CO₂, full suppression of sparking was demonstrated up to gas gain in excess of 10^4 . At comparable gas gains, resistive and non-resistive prototypes show similar response to traversing charged particles, reaching high efficiency and low pad multiplicity. Compared to non-resistive ones, the evacuation of charge is slowed down in resistive prototypes which are thus subject to rate-dependent drops of gas gain. Expected efficiency losses have been observed at (3 GeV electrons) rates in excess of 10 kHz/cm². This limit is compatible with the resistivity of the coated material. At lower rates, it could be shown that the linearity

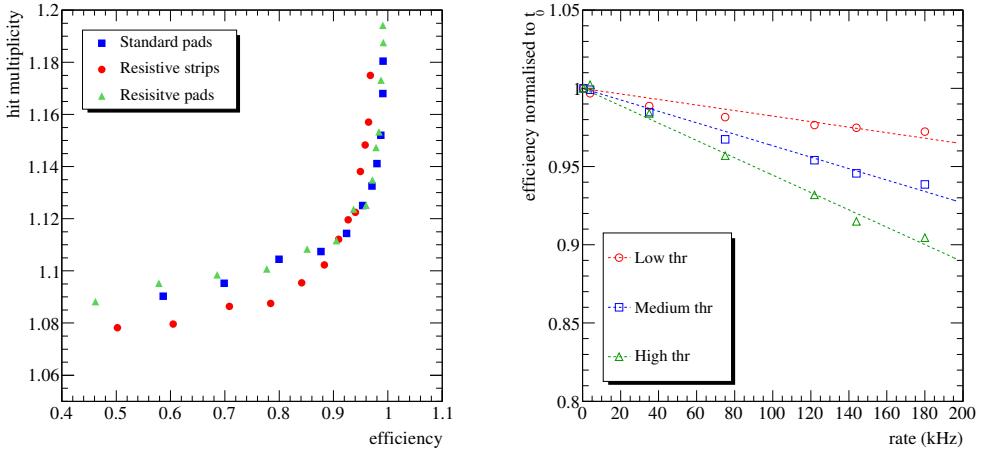


Figure 4.25: Pad multiplicity versus efficiency to 3 GeV electrons for 2 resistive and 1 non-resistive (or standard) Micromegas prototypes (left). Efficiency dependence on rate in a resistive prototype for 3 values of threshold (right). The electron beam spot is $\sim 2 \times 2 \text{ cm}^2$.

of a Micromegas calorimeter to electrons is not affected by the resistive coatings, up to 5 GeV, which was the maximum energy available during the testbeam campaign.

4.9.4 Engineering Challenges

4.9.5 Detector R&D plans for the coming years

Plans for the coming years include maintaining a commitment to linear collider detector R&D and possibly seek new applications. Despite a decline of resources, an R&D program to optimise resistive Micromegas for calorimetry is established. Linearity, rate capability and spark protection in dense electromagnetic showers will be checked up to high-energy and for detector designs with a large variety of resistivity and geometry. These measurements will be necessary to validate the resistive Micromegas technology for calorimetry at a future LC. Also, the on-going R&D for high-luminosity LHC (HL-LHC) detector upgrades are an appealing perspective. In particular, the possibility to equip the backing part of the CMS forward calorimeter is being investigated. Such high-rate application will put strong stability constraints on resistive Micromegas, making the optimisation work mentioned above even more relevant.

On a longer term and if resources are sufficient, a Micromegas calorimeter prototype should be constructed so its performance can be compared to concurrent detector technologies. Some performance have already been studied with Monte Carlo simulation, the minimal prototype dimensions are known as well as its cost. This final step of the project naturally comes after optimisation of the resistive coating and would complete the R&D on Micromegas calorimetry.

4.10 Glass RPC SDHCAL

Contact person: Imad Laktineh (email: laktineh@IPNL.IN2P3.FR)

4.10.1 Introduction

Hadronic calorimeter (HCAL) plays an essential role in PFA-based experiments as those proposed for the ILC. It allows to separate the deposits of charged and neutral hadrons and to precisely measure the energy of the neutrals. The contribution of the neutrals to the jet energy, around 10% on average, fluctuates in a wide range from event to event, and the accuracy of the measurement is the dominant contribution to the particle flow resolution for jet energies up to about 100 GeV. For higher energies, the performance is dominated by confusion, and both topological pattern recognition and energy information are important for correct track cluster assignment. High-granularity hadronic calorimeter is thus needed to achieve excellent jet energy resolution.

HCAL proposed for both projects of ILC (ILD and SiD), are sampling calorimeters with steel as absorber and scintillator tiles or gaseous devices with embedded electronics for the active part. The steel was chosen due to its rigidity which allows to build self-supporting structure without auxiliary supports (dead regions). Moreover, the moderate ratio of hadronic interaction length ($\lambda_I = 17$ cm) to electromagnetic radiation length ($X_0 = 1.8$ cm) of iron, allows a fine longitudinal sampling in terms of X_0 with a reasonable number of layers in λ_I , thus keeping the detector volume and readout channel count small. This fine sampling is beneficial both for the measurement of the sizable electromagnetic energy part in hadronic showers as for the topological resolution of shower substructure, needed for particle separation.

For the ILD project we propose gaseous detectors for the HCAL active layers: The Resistive Plate Chamber (RPC). This is motivated by the excellent efficiency and very good homogeneity the gaseous detectors could provide. Another important advantage of gaseous detectors is the possibility to have very fine lateral segmentation. Indeed, in contrast to scintillator tiles, the lateral segmentation of gaseous devices is determined by the electronics readout used to read them. Active layer thickness is also of importance for what concerns the ILC hadronic calorimeter to be placed inside the magnetic field. Highly efficient gaseous detectors can indeed be built with a thickness of less than 3 mm.

To obtain excellent resolution of hadronic shower energy measurement using a binary readout, a lateral segmentation of few millimeters is needed. This however leads to a huge number of electronics hardly affordable for the future ILC hadronic calorimeters. $1 \times 1 \text{ cm}^2$ cells were found to be a good compromise that still provides very good resolution at moderate energies. However, simulation studies show that saturation effects are expected to show up at higher energies (> 50 GeV). This happens when many particles cross one cell in the center of the hadronic shower. To reduce these effects, the choice of multi-threshold electronics (Semi-Digital) readout was envisaged to improve on the energy resolution by exploiting the particle density in more appropriate way.

High-granularity calorimeters imply however a huge number of electronics channels to operate them. This has two important consequences. The first is the power consumption and the resulting increase of temperature which affects the behavior of the active layers. The other consequence is the number of service cables needed to power, read out these channels. These two aspects can deteriorate the performance of the HCAL and destroy the principle of PFA if they are not addressed properly.

The R&D pursued by the SDHCAL-GRPC groups has succeeded to pass almost all the technical hurdles of the PFA-based HCAL. The SDHCAL-GRPC groups have succeeded to build the first technological prototype of these new-generation calorimeters with 48 active layers of GRPC, 1 m^2 each. The prototype validates the concept of high-granularity gaseous detector and permits to study the energy resolution of hadrons one can obtains with such calorimeter.

4.10.2 Readout Electronics

The readout electronics of the two Semi-Digital HCAL (SDHCAL) projects were developed in common. An ASIC called HARDROC was first developed to read out the G_RP_C detectors proposed for the ILD project. To solve the problem of connections related to the high number of electronics channels, the option of a detector embedded electronics using the DAISY chain scheme was chosen and Printed Circuit Board (PCB) were conceived for the readout of large detectors G_RP_C.

Front-end ASIC

The HARDROC chip (HR) implements a multi-threshold readout which integrates the functionalities of amplification, shaping, digitization, internal triggering and local storage of the data. Each of its 64 channels consists of a fast low impedance current preamplifier with 8-bit variable gain (in the [0, 2] range) followed by 3 fast shapers (15 ns shaping time). A low offset discriminator is present on each path and the three corresponding thresholds establish the multi-level readout. The thresholds are set using three integrated 10-bit Digital to Analog Converters (DAC). The outputs of the three discriminators are then encoded 3-to-2 bit and stored in an internal digital memory latched by a trigger event.

A trigger is generated when one of the lowest level discriminators is fired but can also be configured on the other thresholds. A frame consists of the 64 encoded discriminator outputs, plus a 24-bit time-stamp and a chip identifier is stored after a trigger is received. Noisy channels could be easily masked via the configuration parameters control. In order to avoid fake triggers produced by noisy channels, the output of each discriminator can be switched off from the trigger generator logic via the configuration parameters control (Slow Control hereafter) commands. The response of all the channels can be calibrated by injecting an analog signal through an integrated 2 ± 0.02 pF input test capacitor; this is a useful tool to make the response of the different channels as uniform as possible [155].

The ASIC contains a 127-frame long digital memory. This allows to work in a triggerless mode and keep all the data accumulated during the bench crossing. Once the memory is full the acquisition is stopped, the readout is performed and the ASIC can start acquisition again. The Gray-coded time-stamp is derived from an external 5 MHz clock.

An essential feature of the HR is the possibility to be operated in the power-pulsing mode (PP) that consists of switching off almost all power-consumption functionalities in between the bench crossings (BC) of the ILC electron beams. With the ILC duty cycle of one 1 ms of BC every 200 ms, this mode allows a reduction factor of more than 100 of power consumption. Thanks to this reduction, the temperature increase of the HCAL is moderate and only simple cooling system is needed to operate it efficiently.

Active Sensor Units

To read out the 1 m² detector of the SDHCAL, an electronic board with the same size is needed. This electronic board is an important piece in the present design. It hosts both the pick-up pads and the ASICs in addition to the connections linking the pads to the ASICs and those among the different ASICs. To ensure good transmission qualities and low cross-talk, 8-layer Printed Circuit Board (PCB) is designed. Feasibility constraints, make the tasks of circuit production, components soldering, testing and handling of the assemblies, exceedingly difficult in the case of a single board of one square meter. The solution of dividing that circuit into 6 smaller but more manageable PCB was adopted. Each of these small ASUs hosts 24 chips to read out 48×32 pads of 1 cm² each. This dressed PCB is dubbed Active Sensor Unit (ASU). The base pattern connecting 64 pads arranged in a 8×8 matrix to the ASIC's pins is shown in Figure 4.27. This is identical to the one used in the ASUs of the small G_RP_C chambers described in reference [155]. The

routing of each input signal from its own pad up to chip pin has been carefully optimized to reduce the cross-talk. All input signals are laid out in the same analog signal layer which is sandwiched between two GND layers. The routing of digital signals was kept well separated from the vias connecting signals from one layer to another. In the case of the GRPC related ASU, the HARDROC base pattern is replicated 4×6 times in the $33.33\text{ cm} \times 50\text{ cm}$ board. 4 1.6 mm diameter holes are present on the four angles of a PCB to be used for fixation purposes as will be explained later. The routing was conceived so two of the ASUs can be associated to form one slab hosting 48 ASICs. Each slab is then connected to one Detector Interface board (DIF). The connection between the DIF and the slab as well as the connection of the two ASUs is performed thanks to tiny connectors allowing the different clocks, signals as well as the power to circulate between the two ASUs. Three slabs are then assembled to form the required electronics board. To ensure the same electric reference level for the six ASUs, the GND layer of the six ASUs is connected thanks to a copper gasket on all the common sides. Similar schemes could be proposed for GRPC detectors with larger size.

Front-end and back-end boards

The interface between the ASUs and the data acquisition system (DAQ) is realised by the detector interface board called DIF. The main elements of the DIF is an FPGA and USB, HDMI and SAMTEC connectors. It manages the control signals (e.g. clock, busy/ready, external/internal trigger, power-pulsing) and supply power to the ASICs and also performs the readout of the ASIC memories. DIFs are read out by other FPGA-based boards called Data Concentrator Cards (DCC). They can be connected up to 9 DIFs through HDMI links and are controlled by a synchronous DCC (or SDCC). The SDCC can connects to up to 9 DCCs to which it distributes the clock and the commands. It is also connected to the computer network for the user to control the DAQ.

In the case of Micromegas ASUs, a small additional board called inter-DIF is used between the DIF and ASU to provide the high voltage to the meshes and drift electrode.

Acquisition Software

To exploit the data collected by the SDHCAL detectors an acquisition software was developed. This software is organized in three parts. The first one allows to access the hardware devices (DIF, SDCC) through an FTDI chip associated to each of these devices. It transmits the configurations parameters to ASICs through these devices and collect the data as well. The second part is the configuration data base. It gives the possibility to store and retrieve all parameters needed by the DAQ system. The database itself is hosted on an Oracle server at CC IN2P3 (Villeurbanne, France). To interface this SQL database with the DAQ software and to allow users to insert and query data without knowledge of SQL, a C++ library has been written. A special care was taken to allow to download the parameters associated to a given parameters of the prototype (roughly 550000 parameters) in few seconds. The third part concerns the data collection. Data from different DIFs may be readout at a different times but will have the same Bench Crossing IDentifier (BCID) for a given trigger. The logical way to keep synchronicity is to store in a BCID indexed map the buffers of all read DIFs but it requires to manage memory allocation, access and cleaning. This was achieved thanks to the abilities offered by recent Linux kernels to use file based shared memory. In addition, whenever several computers are involved in the data taking, as it is the case for the SDHCAL prototype, a communication framework is needed. The CMS data acquisition XDAQ framework was chosen. This provides communication tools with both binary and XML, an XML description of the computer and software architecture, a web-server implementation of all data acquisition application and a scalable event builder. A monitoring system was also developed to have an online follow-up of the acquisition during data collection.

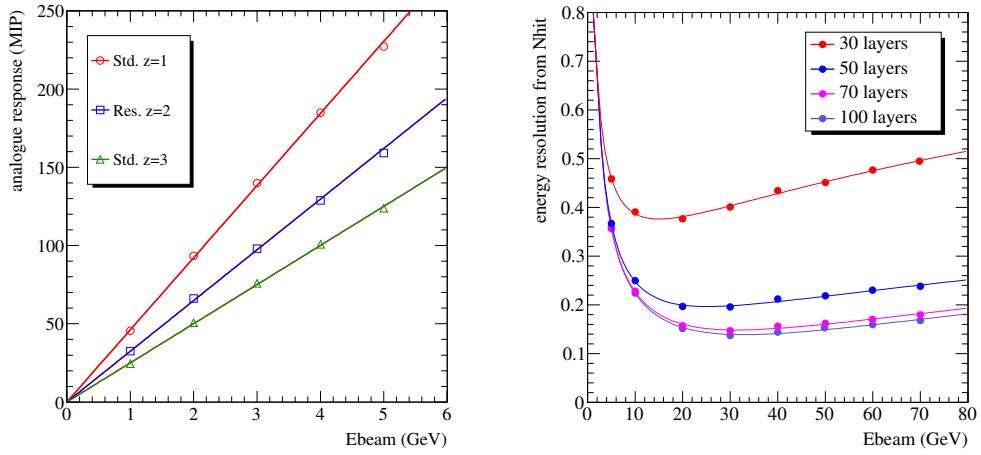


Figure 4.26: Electron response of a virtual Micromegas SDHCAL deduced from measurements of longitudinal shower profiles in non-resistive ($z=1$ and $z=3$) and resistive ($z=2$) Micromegas prototypes placed behind increasing thicknesses of passive material (left). Geant4 calculation of the energy resolution to pions of a Micromegas DHCAL of 30 to 100 layers based on simple hit counting (right).

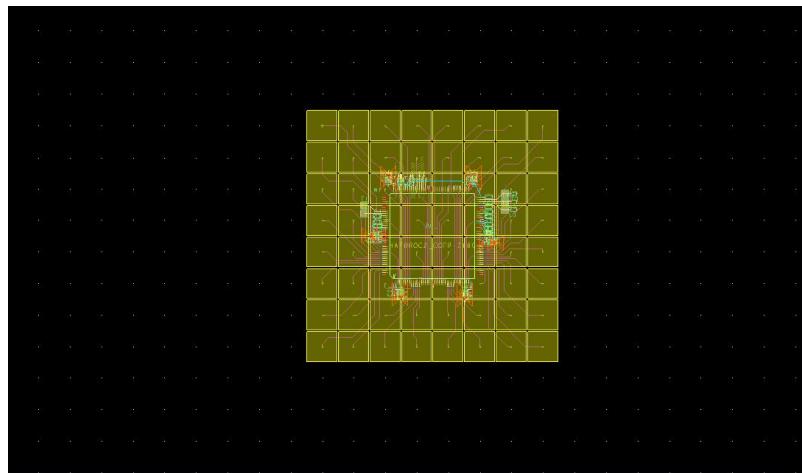


Figure 4.27: Pads connection to the ASIC's pins

4.10.3 GRPC-SDHCAL for ILD

Detector Development

The structure of GRPC proposed as an active layer of the HCAL proposed for ILD is shown in Figure 4.28. It is made out of two glass plates of 0.7 mm and 1.1 mm thickness. The thinner is used to form the anode while the thicker forms the cathode. Ceramic balls of 1.2 mm diameter are used as spacers between the glass plates. The balls are glued on only one of the glass plates. In addition to those balls, 13 cylindrical fiber-glass buttons of 4 mm diameter are also used. Contrary to the ceramic balls the buttons are glued to both plates ensuring thus a robust structure.

Special spacers (ceramic balls) were used to maintain uniform gas gap of 1.2 mm. Their number and distribution were optimized to reduce the noise and dead zones (0.1%). The distance between the spacers (10 cm) was fixed so that the deviation of the gap distance between the two plates under the glass weight and the electric force does not exceed 45 microns. The choice of these spacers rather than fishing lines was intended to reduce the dead zones (0.1%). It was also aimed at reducing the noise contribution observed along the fishing lines in standard GRPC chambers. The gas volume is closed by a 1.2 mm thick and 3 mm wide glass-fiber frame glued on both glass plates. The glue used for both the frame and the spacers was chosen for its chemical passivity and long term performance.

The resistive coating on the glass plates which is used to apply the high voltage and thus to create the electric field in the gas volume was found to play important role in the pad multiplicity associated to a mip [155]. To find the best coating for GRPC chambers many products were tested. Finally, a new product based on two components was chosen. By changing the two components ratio one can obtain the needed surface resistivity. Commercial products like Licron™ and Statguard™ which are used for Electro-Static Discharge (ESD) applications were tried and few 1 m^2 chambers were built using those products and intensively tested. Both products failed to satisfy our application either for long term stability under the high voltage (Licron using those products) or due to the impossibility to obtain the surface uniformity needed for our application (Statguard using those products). Eventually, two products were identified, both of which are based on colloids containing graphite. Both can be applied using the silk screen print method, which ensures very uniform surface quality. One of these products is a single component paint with a dry surface resistivity of $1 - 10\text{ M}\Omega/\square$. The second product comes as two components which must be mixed by the user. The surface resistivity may be adjusted over a wide range by changing the mix ratio. Both products require baking at around 170° C to attain a stable surface resistivity. One product based on colloids containing graphite was finally selected. The product can be applied using the silk screen print method, which ensures very uniform surface quality. In addition, the product is made of two components and it was found that by changing the mix ratio the surface resistivity may be adjusted over a wide range.

The measured surface resistivity at various points over a 1 m^2 glass coated with the previous paint showed a mean value of $1.2\text{ M}\Omega/\square$ and a ratio of the maximum to minimum values of less than 2. A study was also made of the repeatability of the surface resistivity between different mix batches. It was found that surface resistivity in the range $0.5 - 2\text{ M}\Omega/\square$ could be reliably reproduced. For 1 m^2 GRPCs the painting is applied on the whole glass plate except for 3 mm from the edges. This distance, corresponding to the frame width, was optimized so the dead zone of the detector is reduced while external sparks due to the presence of the metallic cassette in the vicinity is completely eliminated.

Another important aspect of this development concerns the gas circulation within the GRPC taking into account that for ILD SDHCAL gas outlets should all be on one side. A genuine system was proposed. It is based on channeling the gas along one side of the chamber and releasing it into the main gas volume at regular intervals. A similar system is used to collect the gas on the opposite side. A finite element model has been established to check the gas distribution [156]. The simulation confirms that the gas speed is

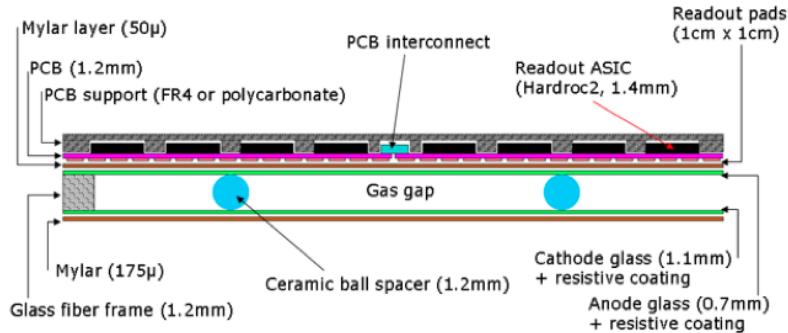


Figure 4.28: Cross-section through a 1m^2 chamber

reasonably uniform over most of the chamber area.

In order to improve on the gas distribution in large chambers taking into account the requirement that both gas outlets should be on the same side of the detector to satisfy all possible mechanical structures proposed for ILD hadronic calorimeter, new schemes were studied. The one we finally adopted allows us to improve the gas distribution by channeling the gas along one side of the chamber and releasing it into the main gas volume at regular intervals thanks to 1.2 mm diameter PEEK™tubes fixed 2 cm from the chamber side. A similar system is used to collect the gas at the other side of the chamber. A finite element model has been established to check the gas distribution [156]. The simulation confirms that the gas speed is reasonably uniform over most of the chamber area. as can be seen in Figure 4.29.

The GRPC and its associated electronics are housed in a special cassette which protects the chamber and ensures that the readout board is in intimate contact with the anode glass. The cassette is a thin box consisting of 2.5 mm thick stainless steel plates separated by 6 mm wide stainless steel spacers. Its plates are also a part of the absorber.

The electronics board is assembled thanks to a polycarbonate spacer which is also used to fill the gaps between the readout chips and to improve the overall rigidity of the detector. The electronics board is fixed on the small plate of the cassette. Thanks to tiny screws and the new set is fixed on the other plate which hosts the detector and the spacers. The whole width of the cassette is 11 mm with only 6 of them corresponding to the sensitive medium including the GRPC detector and the readout electronics.

4.10.4 Prototype

A technological prototype corresponding to the SDHCAL option proposed in the ILC LOI was built. 48 cassettes as the one described above were built. They fulfilled a stringent quality control. It is worth mentioning that 10500 HR ASICs were produced and tested using a dedicated robot for this purpose. The yield was found to be higher than 92%. The ASICs were then fixed on the PCBs to make a 1m^2 and itself fixed on the cassette cover once successfully tested.

The cassettes were inserted in a self-supporting mechanical structure that was conceived and built in collaboration with the Spanish group of CIEMAT. The structure is made of Stainless Steel plates of 1.5 cm each. The plates were machined to have an excellent flatness and well controlled thickness. The flatness of the plates was measured using a laser-based interferometer system. It was found that the flatness of the plates are less than 500 microns. This results guarantees that for the SDHCAL V structure proposed for ILD, a tolerance of less than 1 mm is achievable.

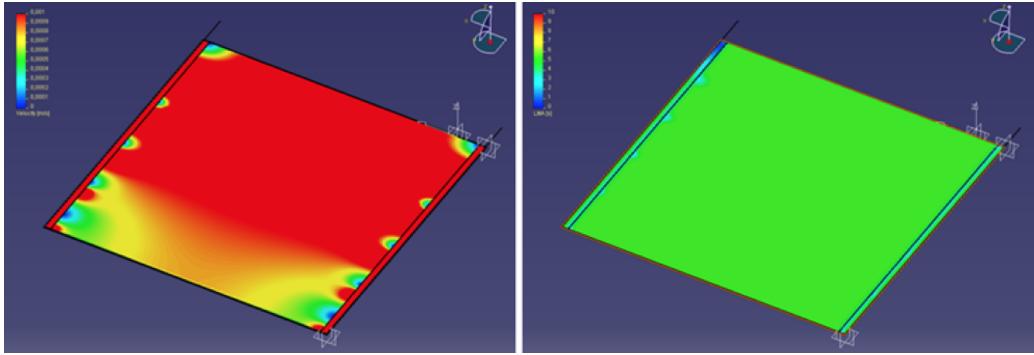


Figure 4.29: Left: Gas speed profile in the range 0–1 mm/s; Right: Least mean age profile in the range 0–10 s

The first cassettes were extensively tested using a cosmic-rays bench and later particles beam at CERN. Both the efficiency and the multiplicity of the GPC cassettes were studied. These studies showed high efficiency and good homogeneity and validated the cassette concept.

The prototype construction lasted less than 6 months. A commissioning test at CERN in 2011 allowed to understand the whole system behavior. More precisely a problem related to the acquisition system of the more than 430000 channels was found and fixed.

In parallel a single cassette was tested in a magnetic field of 3 Tesla (H2 line at CERN) applying the power-pulsed mode. The TB results indicated clearly that the use of the power-pulsed mode in such a magnetic field is possible. The behavior of the detector (efficiency, Figure 4.31, multiplicity, Figure 4.32) was found to be similar to those obtained in the absence of both the magnetic field and the power-pulsed mode.

In April 2012 the prototype was exposed to pion, muon, electron beams of both the PS and the SPS of CERN (Figure 4.30). Power-pulsed mode was applied to the whole prototype using the beam cycle structure (0.3 ms time duration for the PS beam and 9 s for the SPS beam every 45 s). A basic water-based cooling system was used to keep under control the temperature increase particularly in the case of the SPS where the consumption reduction is only 5 (to compare with a factor of more than 100 in the ILC case). An acquisition mode similar to that of the ILC was operated. The data were collected continuously in a triggerless mode. The DAQ stops when the memory of one ASIC is full. Data are then transferred to a storage station and then the acquisition starts again. Figures 4.33 and 4.34 show the efficiency and pad multiplicity of the prototype GPC chambers measured using the muon beam.

The SDHCAL prototype results obtained with a minimum data treatment (no gain correction) show clearly that excellent linearity and good resolution could be achieved on large energy scale as can be shown in Figures 4.35 and 4.36. Useless to mention that the high granularity of the SDHCAL allows one to study thoroughly the hadronic showers topology and to improve on the energy resolution by, among others, separating the electromagnetic and the hadronic contribution. The separation between close-by showers will also get big benefit thanks to the high granularity on the one hand and to the very clean detector response ($< 1 \text{ Hz/cm}^2$) on the other hand. These two points are being worked and recent results confirm this.

The quality of data obtained during three weeks of data taking validates completely the SDHCAL concept as proposed in the LOI. This is especially encouraging since no gain correction was applied to the electronics channels to equalize their response. However a gain correction mode is elaborated and tested during the TB. It will be applied in the future to assess the effect of such correction on the energy

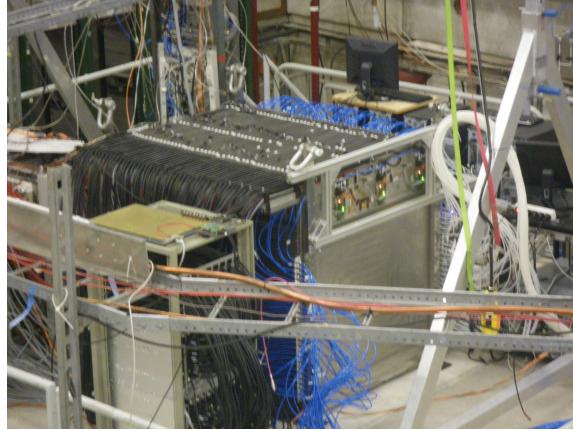


Figure 4.30: Cross-section through a 1 m^2 chamber.

resolution.

4.10.5 ILD Preparation

The expertise acquired with the construction and the commissioning of the technological prototype and the obtained results were used to implement a realistic simulation of the ILD HCAL. Physics channels such as the $t\bar{t}H$ were studied using the SDHCAL option and results were found identical to those obtained with the scintillator tile option despite the fact that the jet energy reconstruction code was optimized for the latter.

In addition, the French groups participated actively in the HCAL part of the ILC TDR (ILD part) by proposing a genuine mechanical structure for the hadronic calorimeter (called V-structure). The V structure was conceived to eliminate the projective holes and cracks so none of the particles produced close to the detector centre could escape detection. The V structure has additional advantages. It eliminates in principle the space between the barrel and the Endcaps avoiding the shower deformation which results not only because of this space but also of the different cables and services needed in CMS-like mechanical structures. In this structure the different services such as the gas tubes, data collection and electric cables of both the barrel and the Endcaps are taken out from the outer radius side. Detailed studies have shown that the deformation of this structure is extremely low and its robustness was verified experimentally with the SDHCAL technological prototype built with a self-supporting structure respecting the spirit of the V one. Services and Integration issues were also worked out. Besides, realistic costing was performed , based on the prototype experience.

4.10.6 Recent Milestones

4.10.7 Engineering Challenges

4.10.8 Detector R&D plans for the coming years

Large GRPC of 1 m^2 were developed and built for the technological prototype. However, larger GRPC are needed in the future DHCAL with the largest one being $290 \times 91\text{ cm}^2$. These large chambers with gas inlet

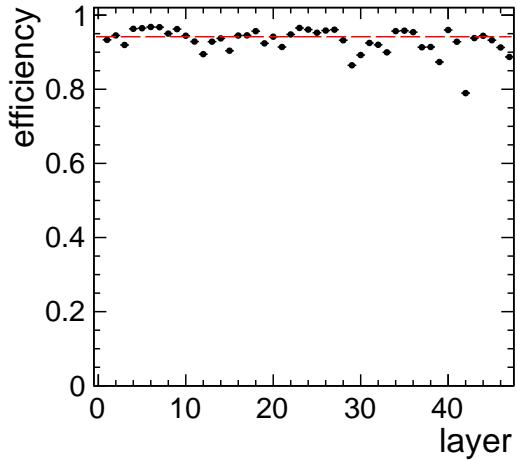


Figure 4.31: Efficiency of the GRPC prototype

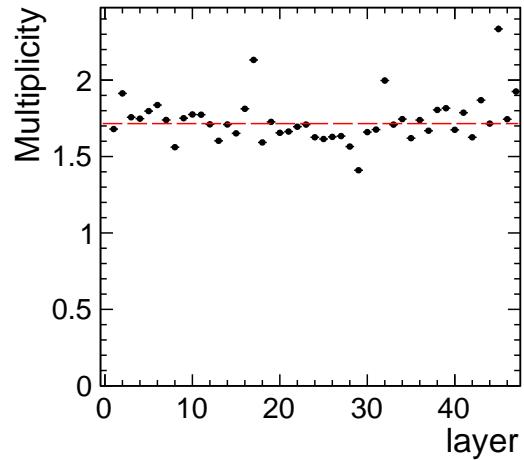


Figure 4.32: Pad multiplicity of the GRPC prototype.



Figure 4.33: GRPC setup in the CERN SPS-H2 line magnetic field.

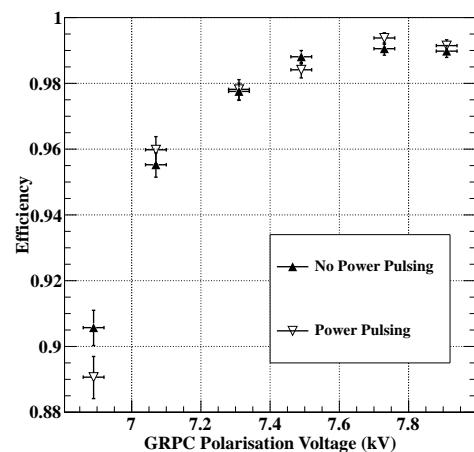


Figure 4.34: Efficiency scan over high voltage, with and without power pulsing.

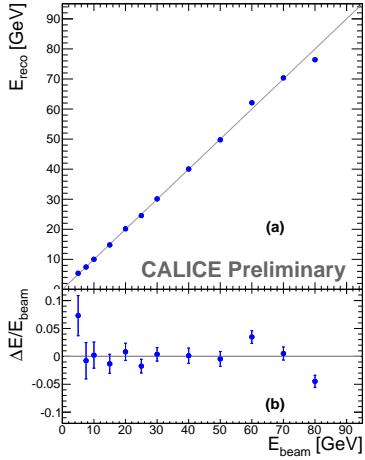


Figure 4.35: (a): Mean reconstructed energy for pion showers and (b): relative deviation of the pion mean reconstructed energy with respect to the beam energy.

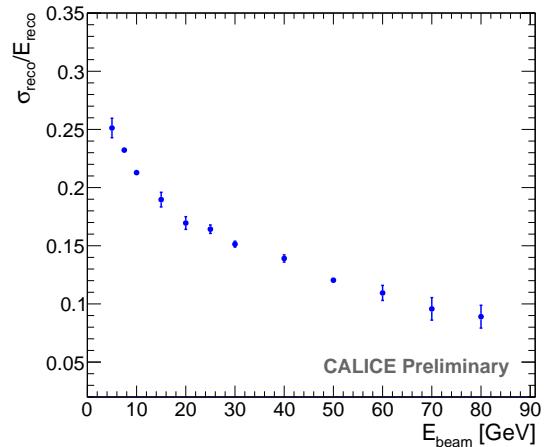


Figure 4.36: $\frac{\sigma_{reco}}{E_{reco}}$ of the reconstructed pion energy E_{reco} as a function of the beam energy.

and outlet on one side need a dedicated study to guarantee a uniform gas gap everywhere notwithstanding the angle of the plate. It is necessary also to ensure an efficient gas distribution as it was done for the 1 m^2 chambers. To obtain this different gas distribution systems were studied. A new scheme with two gas inlets and one outlet was found to ensure an excellent homogeneity of the gas distribution. This system will be used in the near future to build large detectors exceeding 2 m^2 . The readout of such chambers needs also to be as efficient as the one of the technological prototype 1 m^2 . An upgrade of the HR ASIC allowing larger dynamic range was conceived, produced and successfully tested 4.37. The new ASIC (HR3) allows to be directly addressed and easily bypassed in case of failure thanks to the I2C protocol. In addition and contrary to the HR2, the 64 channels of the new ASIC are independent which allows a better calibration procedure. In addition to the previous challenges we need to improve on the interface boards (DIF) needed to control the ASICs synchronization and data transfer. Indeed, the space left between the active layer of one module and the cryostat is only 5 cm. This means that the DIF components should be optimized to cope with the volume availability. A new design with new functionalities of the DIF is proposed. A TPC/IP protocol is adopted for data transfer and a TTC one for the clock synchronisation. A microprocessor implemented on the new DIF is in charge of the communication between the ASICs and the DIF's FPGA. The new DIF is capable to address up to 432 ASIC. New PCB design that allows to assemble few boards to cover up to 3 m^2 GRPC detector is being conceived. Care is taken to ensure robust and flexible but still tiny connection between the different PCB to build large one. Finally a new technique based on electron beam welding is being tested to build a mechanical structure. This intends to reduce the steel quantity used to assemble the absorber plates while guaranteeing a minimum deformation. First attempts have taken place at CERN recently 4.38 and more study is ongoing to determine the best protocol one should follow to obtain optimal results.

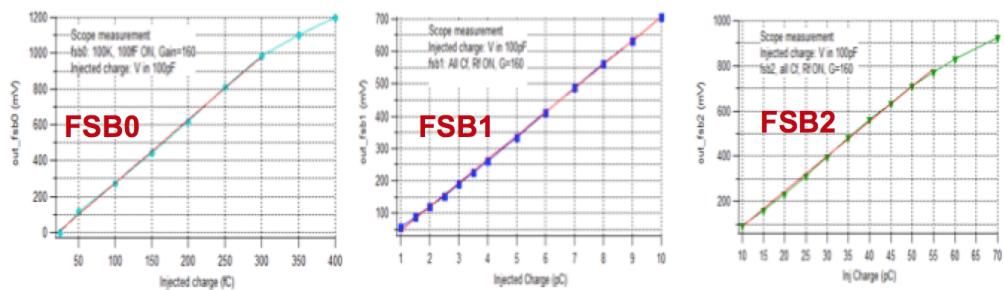


Figure 4.37: Dynamic range of the fast shapers associated to the three thresholds of the new version of HARDROC.



Figure 4.38: A prototype of an SDHCAL mechanical structure assembled using the electron beam welding technique.

4.11 DualReadout

Contact person: John Hauptman (email: hauptman@fnal.gov)

4.11.1 Introduction

The scientific goal of RD52 (previously the DREAM collaboration) is to understand the fundamental limitations to hadronic energy resolution and, in general, the limitations to achieving high-quality calorimetric performance in Gaussian energy resolution, mean response linearity, and ease and precision of calibration.

4.11.2 Recent Milestones

The essential features of our fiber dual-readout calorimeters are (a) near-perfect optical conduits (fibers) for read-out, (b) fine spatial sampling on the mm-scale, (c) dual measurement of scintillation light in scintillating fibers (all charged particles) and simultaneous Cerenkov light in clear fibers (only electromagnetic particles), (d) absolute fiber-absorber volume uniformity, and (e) low-noise readout with PMTs below 100 MeV per ton of calorimeter. This design achieves a Gaussian response, a linearity near 1% from 20-300 GeV, and excellent energy resolution. The calibration is by a direct electron beam into each calorimeter tower.

About 30 dual-readout papers are published in Nucl. Intrs. Meths., Rev. Sci. Instr., and JINST, including dual-readout in several crystals, a planar geometry, as well as fibers in several geometries. We have built and tested Pb-based and Cu-based dual-readout modules and are designing a W-based test module. Typical readout of the Pb-modules is shown in Figure 4.39 for 20, 60, and 100 GeV pion beams in the H8 beam of the North Area at CERN. Simple dual-readout yields a Gaussian and linear response, currently limited by lateral leakage fluctuations in the Pb-based modules of about 1 tonne. The record holder for linear, Gaussian energy resolution is still the SPACAL module of 20 years ago, built by Wigmans at CERN to demonstrate the newly understood concept of “compensation”. SPACAL was a Pb-scintillating fiber module of mass 20 tonnes that collected scintillation light for 100-200 ns to achieve compensation from the $np \rightarrow np$ recoils in the scintillating fibers. We show in Fig. 2 the hadronic energy resolutions for single pions for SPACAL, DREAM, and the new RD52 modules, plotted vs. $1/\sqrt{E}$, so that the slope is the stochastic term and the intercept is the constant term. A calorimeter with the ILC goal for hadronic energy resolution of $\sigma/E = 30\%/\sqrt{E}$ is shown as the thin red line. We have not yet achieved this goal, but we know we are limited merely by lateral leakage fluctuations which can be suppressed by a larger module. As shown in Fig. 2 we are closing in. There are several improvements over the results in Figure 4.40 for (a) Cerenkov photoelectron yield, (b) photocathode efficiency, (c) fiber quality, (d) optical uniformity and, finally, (e) absorber mass. All of these are planned for testing one year from now at CERN. We expect, based on our data, simulations, and our understanding, that we are likely to achieve a resolution of about $30\%/\sqrt{E}$ with a small constant term. This would result in 3% energy resolution at 100 GeV and about 2% energy resolution at the highest SPS beam energies available at CERN.

4.11.3 Engineering Challenges

Manufacturing of the high-precision absorber, whether Pb or Cu or W. Assembly of a large calorimeter involves a lot of fibers which can and must be automated. Control of the optics to 1% is a challenge. It should be emphasized that we do not have engineers working on RD52, but rather find simple solutions which achieve the physics goals without expending large funds. On a construction project, engineering design would improve all our results.

Hadron detection with a dual-readout calorimeter

$$E = \frac{S - \chi C}{1 - \chi} \quad \text{with} \quad \chi = \frac{1 - (h/e)_S}{1 - (h/e)_C} = 0.45$$

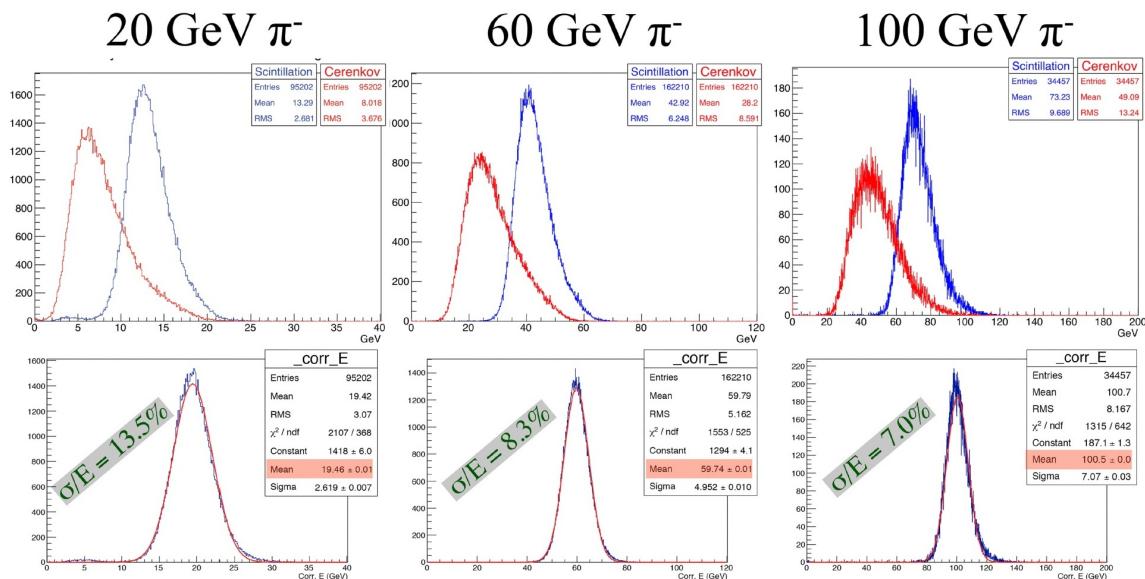


Figure 4.39: Raw scintillation and Cerenkov data for 20, 60, and 100 GeV pion beam, and the dual readout response below

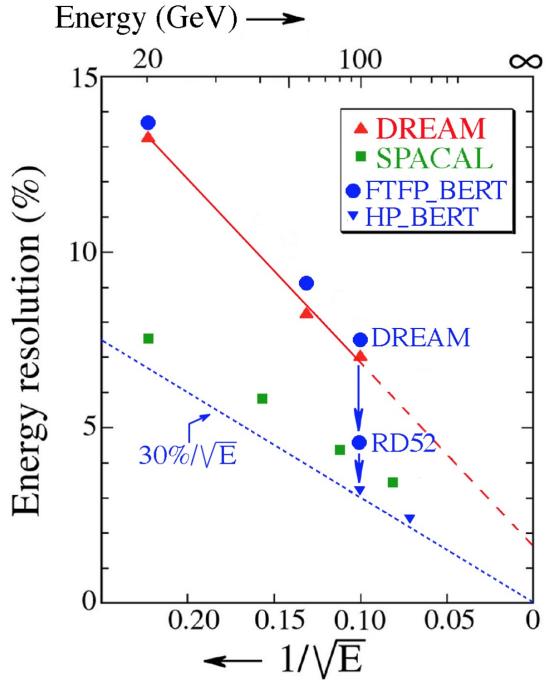


Figure 4.40: The Gaussian-fitted energy resolution of compensating and dual-readout fiber calorimeters. The RD52 copper-fiber dual readout energy resolutions at 100 GeV and 200 GeV energies for incident pions are shown as the inverted blue diamonds with the label caption HP_BERT. The dotted line is a resolution of $\sigma/E = 30\%/\sqrt{E}$ with zero constant term. The grant result seems to have a constant term of about 0.5%.

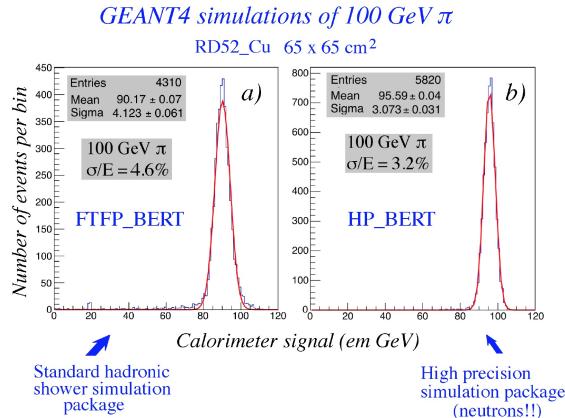


Figure 4.41: The raw pulse height distribution simulated from two GEANT4 physics lists. The latter one does a more correct treatment of the neutrons in the hadronic cascade and, therefore, better represents the dual-readout response of a hadronic calorimeter. Left: Standard hadronic shower simulation package. Right: High precision hadronic shower simulation package (neutrons!!).

4.11.4 Future Plans

Solving the problems of projective geometry; implementation of SiPM readout; manufacture of a tungsten W-absorber with full dual-readout capability; test of a gaseous dual-readout calorimeter.

4.11.5 References

Complete papers, figures, proposals, status reports, and photos are accessible at our website:
<http://highenergy.phys.ttu.edu/dream/>.

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
Scintillator ECAL	Nihon Dental University Shinshu University Tokyo University, ICEPP Tsukuba University			
SiliconECAL ILD	LLR / Palaiseau LAL / Orsay LPNHE / Paris University of Tokyo Kyushu University SKKU / Suwon, Korea LPSC / Grenoble OMEGA / Palaiseau	High granularity ECAL (≈ 4000 channels/dm 3). Active sensor: square matrix of about 5×5 mm 2 PIN diode pixels produced from one high resistivity Si wafer. 4 sensors are glued to PCB holding fully integrated readout electronics and passive cooling. Absorber: self-supporting modular tungsten in carbon-fiber structure.	2013-: tests of several layers of technological prototype with one sensor per PCB. 2014-2015: Design, production and first tests of prototypes with 4 sensor PCBs. Sensors are glued to PCB by a robot. Design of a distributed, quality controlled assembly chain of detector elements.	2015- SPS beam tests of a new several layer prototype. Each layer has one PCB with 4 sensors (1024 pixels of 5.5×5.5 mm 2). Documentation of prototype production steps for future industrial mass production. Tests of sensors of various designs / manufacturers. Optimization of DAQ electronics. Design, production and tests of ILD-like detector element with several PCBs connected consecutively and readout from one end.
SiliconECAL SiD				
AHCAL	DESY Hamburg Heidelberg MPI Munich Wuppertal Mainz Omega CERN ITEP MEPHI Dubna Prague NIU Tokyo University, ICEPP Bergen Shinshu	The analog hadron calorimeter is based on small plastic scintillator tiles read out with SiPM. It uses fully integrated electronics with power pulsing, auto-trigger and time-stamping capability.	2014 - multi-layer test beam campaign at CERN with technical prototype electronics, including large-size layers (4 HBUs) 2015 - First beam tests of full HBU with SMD SiPMs fabricated with automated assembly procedure	2015 Test beams at DESY and SPS with >15 HBUs 2016/17 Test beam at SLAC with 15 layer EM stack, power-up & ILC time structure, tests in magnetic field. Further develop SMD SiPM HBUs, explore "mega-tile" options Hadronic beam tests with a prototype with 1 m^3 fully instrumented volume (depends on pending funding request)
DECAL	University of Birmingham (inactive) University of Bristol (inactive) Imperial College London (inactive) Queen Mary, University of London (inactive) Rutherford Appleton Laboratory (inactive)	The digital electronic calorimeter (DECAL) proposes to use monolithic active pixel sensors (MAPS) for the readout of the silicon-tungsten ECAL. The pixels are small enough to count the number of secondary particles of the particle shower, hence the digital calorimeter.	Four TPAC 1.2 sensors were tested at CERN (2009) and DESY (2010). The tests validated the INMAPS process and demonstrated that sensors with a high-resistivity epitaxial layer can meet the required MIP efficiency.	DECAL efforts are currently dormant. The Arachnid collaboration continues some of the work on MAPS chips.
DHCAL (RPC)	Argonne National Laboratory Boston University COE College (Iowa) University of Iowa Shanghai Jiao Tong University – SJTU (in discussion) University of Science and Technology of China – USTC (in discussion)			
SDHCAL (RPC)				
SDHCAL(micromegas)	CALICE (LAPP) CEA Saclay Institute of Nuclear and Particle Physics, Demokritos Weizman	Micromegas is a thin steel micromesh that separates the gas volume in a region of charge conversion and a region of charge multiplication. It is interesting for EM and H calorimetry because its signal is proportional to the energy deposit in the gas. To avoid discharge upon very large energy deposits, it now incorporates resistive elements in the readout electrodes.	<ul style="list-style-type: none"> Study of different resistive configurations to suppress sparking (ANR SPLAM) Test in e-beam of 3 prototypes with integrated ASIC, show charge-up effect and spark suppression Systematic study of a resistive configuration for spark suppression and high rate capability Vary the RC-constant with 6 small prototypes with external electronics Rate capability and in-beam spark study to determine the optimal RC 	<ul style="list-style-type: none"> Implement the best resistive configuration on an ASU (with integrated ASIC) Build several layers, number depending on funding If sufficient number of layers, build and operate a small calorimeter prototype equipped with resistive Micromegas and possibly also THGEM-based elements. Full characterization in-beam of Micromegas calorimetry: response, resolution, profiles, multi-threshold compensation, MC validation.
GEM DHCAL	University of Texas, Arlington			
Thick Gems	Weizmann Institute, Rehovot Coimbra University Aveiro University	Cost-effective sampling element based on the a novel concept derived from the Thick gaseous electron multiplier	2014: 10×10 cm 2 discharge free (Ne/CH ₄) single stage RPWELL 2015: 30×30 cm 2 discharge free (Ar-based gas mixture)	Early 2016: new design of 30×30 cm 2 detector 2016: 1×1 m 2 prototype 2017- testing RPWELL layer in a fully equipped (S)DHCAL
Dual Readout RD52	Texas Tech University Iowa State University INFN (Pavia, Pisa, Cagliari, Rome, Cosenza, Lecce) LIP Lisbon CERN Tufts University	Measure scintillation and Cerenkov light independently in optical fibers and measure neutron content event-by-event. Current small modules are dominated by lateral leakage.	Twenty-nine papers published in NIM on all aspects of dual readout calorimetry, including crystal dual readout. GEANT (FTFP HP) simulations of a large copper module yield an energy resolution approximately represented by $\sigma/E \approx 30\%/\sqrt{E}$ for pion-induced showers.	Measure the difference between pion-induced and proton-induced hadronic showers; measure the time history of light at 5 GHz. Build a large module 4 ton for final test of hadronic performance.

Chapter 5

Forward Calorimeters

5.1 FCAL

Contact person: Wolfgang Lohmann (email: Wolfgang.Lohmann@desy.de)

5.1.1 Introduction

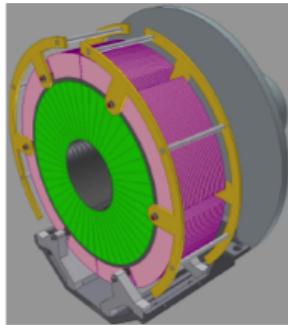
Two special electromagnetic calorimeters are foreseen in the very forward regions of a linear collider detector, denoted hereafter as LumiCal and BeamCal. These calorimeters will deliver both a fast and a precise measurement of the luminosity and extend the detector coverage to low polar angles, important e.g. for new particle searches with missing energy signature. In addition, a LHCAL extends the hadron calorimeter to very small polar angles. Detailed Monte Carlo studies have been performed to optimize the design of the calorimeters, estimate the background from physics processes and understand the impact of beam-beam interactions on the luminosity measurement [157]. A sketch of the design is shown in Figure 5.1 (left). To ensure a high efficiency for single high energy electron detection on top of the large and widely spread background from beamstrahlung, calorimeters with a small Molière radius are needed. Such compact calorimeters facilitate also the reconstruction of Bhabha scattering events. Due to the high occupancy originating from beamstrahlung and two-photon processes, both calorimeters need a dedicated fast readout. In addition, the lower polar angle range of BeamCal is exposed to a large flux of low energy electrons, resulting in depositions up to one MGy per year. Hence, radiation hard sensors are needed.

5.1.2 Mechanical Concept

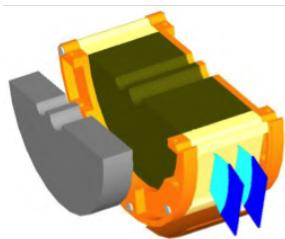
Since in both calorimeters a robust electron and photon shower measurement is essential, a small Molière radius will be preferable. Compact cylindrical sandwich calorimeters using tungsten absorber disks of one radiation length thickness, interspersed with finely segmented silicon (LumiCal) or GaAs (BeamCal) sensor planes, as sketched in Figure 5.1 (right), are found to match the requirements from physics [157]. LHCAL will be designed with a small hadronic interaction length, to fit into the limited space available.

5.1.3 Recent Milestones

Recent milestones were the publication of the performance of fully instrumented detector planes, and the beam-test of a four sensor-layer stack. The results on the performance are briefly summarized below. The



LumiCal: precise luminosity measurement 10^{-3}
500 GeV ILC; 10^{-2} – 3 TeV
CLIC



BeamCal: inst. lumi measurement / beam tuning,
beam diagnostic

LumiCal: Two Si6W sandwich EM calo at a ≈ 2.5 m from the IP (both sides) 30/40 (ILC/CLIC) tungsten disks of 3.5 mm thickness.

BeamCal: very high radiation load (up to 1 MGy / year) \rightarrow similar W6absorber, but radiation hard sensors (GaAs, CVD diamond)

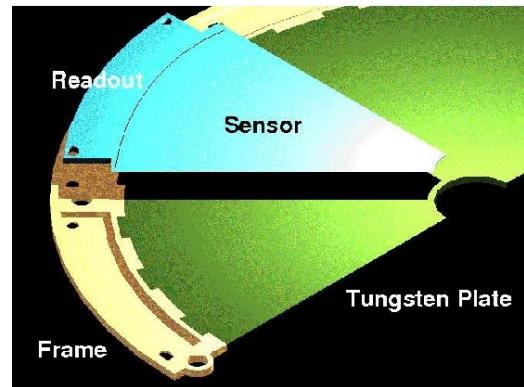
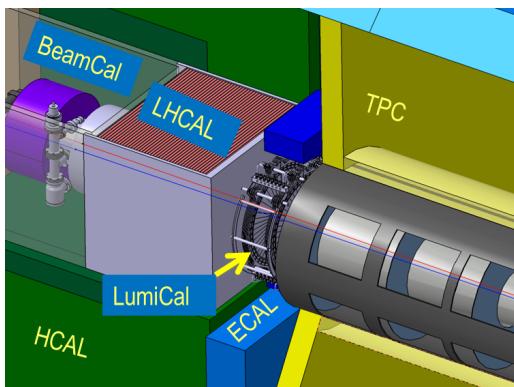


Figure 5.1: Left: The very forward region of the ILD detector. LumiCal, BeamCal and LHCAL are carried by the support tube for the final focusing quadrupole QD0 and the beam-pipe. TPC denotes the central track chamber, ECAL the electromagnetic and HCAL the hadron calorimeter. Right: A half layer of an absorber disk with a sensor sector and front-end electronics.

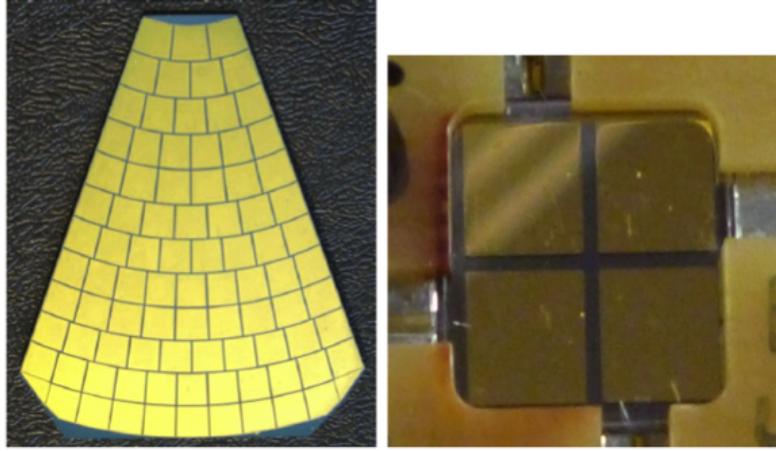


Figure 5.2: *Caption missing*

data analysis for the four sensor-layer stack is still ongoing.

Currently used Sensors and ASICs

Large area GaAs sensors, as shown in Figure ??, were developed and produced in collaboration with partners in industry. The Liquid Encapsulated Czochralski technology is used. The sensors were doped by a shallow donor (Sn or Te), and then compensated with Chromium. This results in a semi-insulating GaAs material with a resistivity of about $[10^7]\Omega m$. The sensors are 0.5 mm thick with pads of a few mm^2 area. The operation voltage is about 100 V with leakage current per pad less than 500 nA.

Prototypes of LumiCal sensors have been designed and manufactured by Hamamatsu Photonics. Their shape is a ring segment of 30°. The thickness of the n-type silicon bulk is 0.320 mm. The pitch of the concentric p⁺ pads is 1.8 mm and the gap between two pads is 0.1 mm. The bias voltage for full depletion ranges between 39 and 45 V, and the leakage currents per pad are below 5 nA [158].

Dedicated ASICs were designed choosing an architecture [159, 160] comprising a charge sensitive amplifier and a shaper. ASICs, containing 8 front-end channels, were designed and fabricated in $0.35\mu\text{m}$ CMOS technology. A variable gain in both the charge amplifier and the shaper is implemented by a mode switch. The peaking time of the shaper output signal is 60 ns. More results of the measurements of the performance were published elsewhere [161]. A dedicated low-power, small-area, multichannel ADC is designed and produced [162]. It comprises eight 10-bit power and frequency (up to 24 MS/s) scalable pipeline ADCs and the necessary auxiliary components.

5.1.4 Test-beam Results

Performance of a Fully Instrumented Detector Plane

Several test-beam campaigns were done to investigate the performance of single fully instrumented detector planes, both for LumiCal and BeamCal. Prototypes of sensor planes assembled with FE and ADC ASICs, as shown in Figure 5.4, were built using LumiCal and BeamCal sensors [163]. The detector plane prototypes were installed in an electron beam and the trajectories of beam particles were measured by four

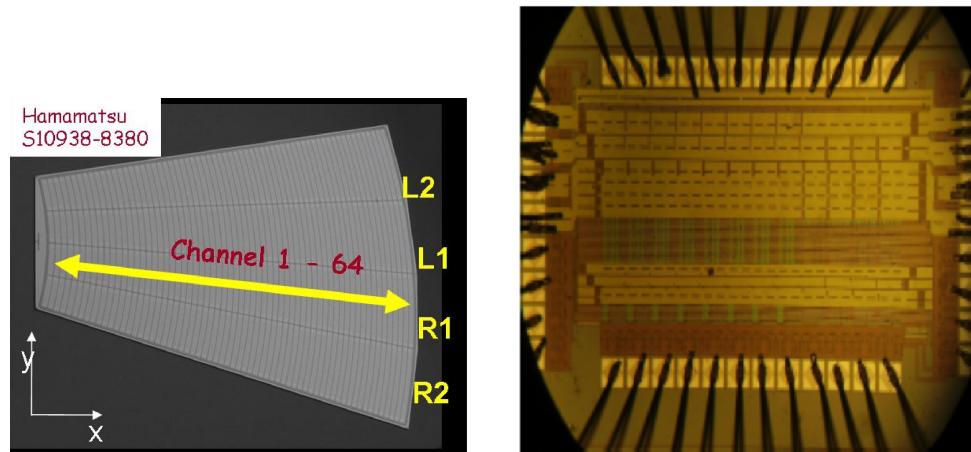


Figure 5.3: Caption missing



Figure 5.4: Photograph of a fully instrumented detector plane for FCAL.

planes of a silicon strip telescope. The front-end electronics outputs were sampled synchronously with the beam clock, a mode used at the ILC. Data were taken for different pads and also for regions covering pad

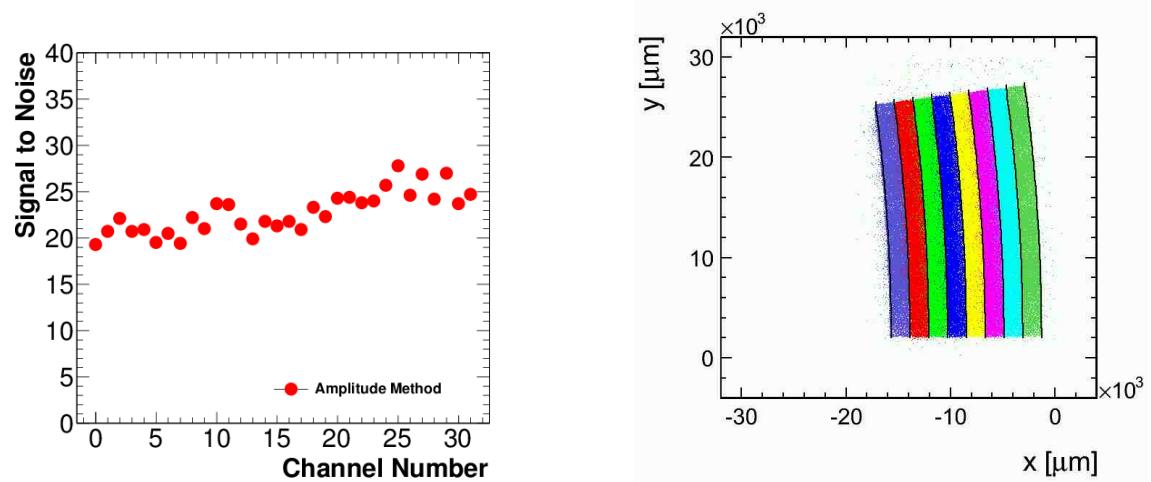


Figure 5.5: Left: The signal-to-noise ratio of all readout channels. Right: Distribution of the predicted impact points on pads with a color coded signal.

boundaries. Signal-to-noise ratios of better than 20 are measured for beam particles both for LumiCal and BeamCal sensors, as illustrated in Figure 5.5 (left). The impact point on the sensor is reconstructed from the telescope information. Using a color code for the signals on the pads the structure of the sensor becomes nicely visible, as seen in Figure 5.5 (right). The sensor response was found to be uniform over the pad area and to drop by about 10% in the area between pads.

Preliminary results from a Multilayer Stack

In two test-beam campaigns at CERN and at DESY a stack instrumented with 4 detector planes was investigated in an electron and in a mixed particle beam. Different numbers of uniform absorber plates were positioned in front and in between the detector planes in each run, allowing to study the longitudinal and lateral shower development. The data were compared to a GEANT4 simulation. A preliminary result is shown in Figure 5.6.

5.1.5 Engineering Challenges

Engineering challenges within the current and future research within FCAL are the following:

- A slim assembled sensor plane. The space between absorber planes must be kept as small as possible. The fan-out to move the signals from the sensor pads to the outside radius must be very thin and hence a new connectivity technology must be applied.
- Multichannel front-end and ADC ASICs for the prototype. A compromise must be found between integration, miniaturization and costs.
- Operation using power pulsing to avoid active cooling.

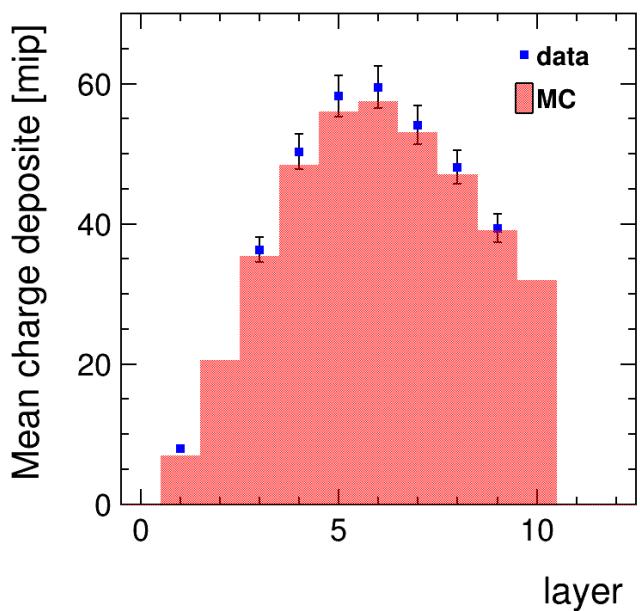


Figure 5.6: The mean charge read out for an electron shower as a function of the shower depth for data and Monte Carlo simulation. The mean charge is given in units of a mip response and the depth in units of a radiation length.

- A dedicated solution for data concentration, data reduction and transmission, allowing read out of the full calorimeters after each bunch crossing.
- Precise alignment and position monitoring. the inner radius of LumiCal has to be controlled within about $10\text{ }\mu\text{m}$, and the distance between the calorimeters on both sides of the IP within $100\text{ }\mu\text{m}$.
- Montage and demontage of the calorimeters must be done when the beam-pipe is installed. The calorimeters must be segmented at least in two half cylinders, and corresponding auxiliary mechanics has to be developed.

5.1.6 Future Plans

Radiation Damage Studies

Two studies Two studies of the radiation tolerance of potential BeamCal sensors have been carried out. The radiation tolerance of prototype GaAs sensors has been explored by exposing the sensors to direct irradiation from a high-intensity electron beam of about 10 MeV [164], which is an energy expected from beamstrahlung remnants at the ILC. It was found that the sensors can be operated at room temperature up to approximately 1 MGy without a significant increase in the leakage current [165]; however, significant loss in the response to ionizing particles was observed. In addition, several different silicon-diode sensor technologies were exposed to varying levels of radiation induced by the SLAC End Station A Test Beam (ESTB). For this study, the ESTB test beam, with energies varying between 3 and 11 GeV, was directed into a tungsten beam stop. The beam stop was split at the depth of the shower maximum and the sensor inserted, leading to an exposure incorporating the full spectrum of particle species that will irradiate the BeamCal sensors. Both n-type bulk oxygenated float-zone and magnetic Czochralski detectors were explored, with exposures varying from 0.2 to 2.2 MGy. It was found that, after allowing for a short period of controlled annealing, all sensor types withstood the maximum dose that they received with little loss in response to ionizing particles [166], but with some increase in leakage current. However, the sensors have to be operated at temperatures below $-10\text{ }^{\circ}\text{C}$. Further irradiation studies in the ESTB are planned for the future. The apparatus to measure the charge-collection efficiency at the Santa Cruz Institute for Particle Physics is being adapted for the evaluation of pad sensors, which will allow for radiation damage studies of the prototype GaAs sensors in this realistic electromagnetic shower environment. Studies to push the silicon diode sensors to higher levels of irradiation are also planned.

Novel Sensor Materials

The performance of single crystal Sapphire sensors to detect minimum ionising particles has been studied for the first time [167]. Sapphire sensors are a promising alternative for GaAs to instrument the region near the beam-pipe where a high radiation field is expected.

With Hamamatsu Photonics the design of edgeless silicon sensors is under preparation. Using edgeless sensors in LumiCal would avoid performance losses in gaps between sensor segments.

Mechanical Stack

A flexible mechanical structure, as shown in Figure 5.7, has been built as part of the AIDA I project at CERN, to compose a technological calorimeter prototype instrumented both with LumiCal and BeamCal sensors. Tungsten absorber plates, glued on a permaglass frame, are precisely positioned on a rod assembly, and interspersed with fully assembled sensor planes. The flatness of the absorber plates is better than $50\text{ }\mu\text{m}$

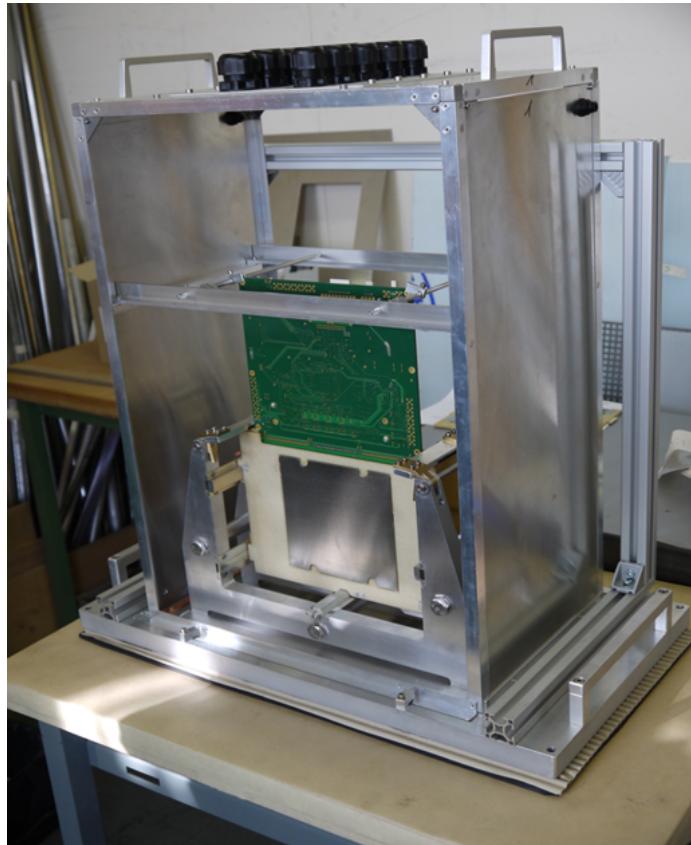


Figure 5.7: Photograph of the flexible mechanical structure. Tungsten absorber plates, glued on permaglass frames, are put into slots of the rod assembly.

to allow for highly compact packing of sensor and absorber planes. This stack will be completed with absorber plates of the necessary quality up to a total thickness of 30 radiation length. JINR Dubna compares the quality of samples from different suppliers using a highly precise 3D position measuring device and X-rays.

Technological Calorimeter Prototype

Currently the goal of FCAL is to prepare a calorimeter prototype for test-beam measurements. These measurements are essential firstly to develop and test engineering solutions to build a very compact calorimeter and secondly to verify the results of Monte Carlo studies. Depending on the test beam results the calorimeter may be redesigned. For the prototype calorimeter a mechanical structure, a sufficient amount of front-end and ADC ASICs, FPGAs for data concentration and a data acquisition system are needed. In addition, two-planes of a pixel tracker in front of LumiCal will be prepared to improve the polar angle resolution.

Alignment and Position Monitoring

A laboratory set-up for position monitoring has been constructed by IFJPAN Cracow using semi-transparent silicon sensors. Test measurements demonstrated that position monitoring with μm precision is possible.

Front-End and ADC ASICs

To match the requirements of extremely low power consumption and taking into account possible radiation fields in the very forward region, a new development of the front-end and ADC ASICs in deep sub-micron 130 nm CMOS technology has been pursued within AIDA by UST Cracow. These ASICs will be sufficiently fast to be used both in LumiCal and BeamCal. The overall readout architecture, so far successfully produced in 350 nm CMOS technology and used in the test-beam measurements as described above, has not been changed and comprises separated front-end and ADC ASICs for each readout channel. For both FE and ADC ASICs prototypes, shown in Figure 5.8, are under test. A dedicated ASIC development is ongoing for BeamCal [168] with a special option for a fast readout of a reduced amount of information from each bunch-crossing to be used for a fast feedback system for beam-tuning [169]. A prototype of a pixel sensor readout for the pair monitor, positioned in front of BeamCal was designed in SoI technology [170].

Data Concentrator and DAQ

In order to operate a large amount of sensor planes the readout has to be orchestrated. For this purpose a FPGA based data concentrator is foreseen which may deliver data in the so called AIDA protocol. The design of this device is currently under discussion. The higher level DAQ will depend on the functionality of the data concentrator. For the readout of test-beam data software is developed, mainly by the University of Tel Aviv, which can be easily adopted. For a final device FCAL will follow the developments of a common DAQ for all detectors.

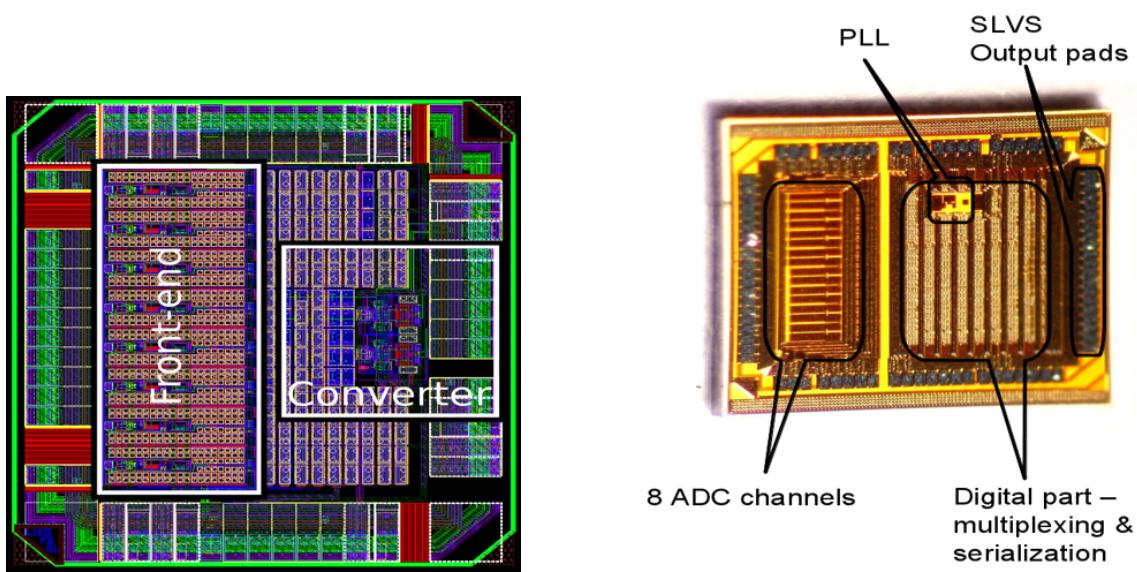


Figure 5.8: Left: 8 channel FE ASIC in 130 nm technology. Right: ADC ASIC in 130 nm technology.

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
LumiCal SiW Sandwich EM calorimetry	AGH-University of Science and Technology, Cracow, Poland	FE and ADC ASIC development in 130 nm CMOS technology, integration and data analysis	submission December 2015	Performance measurements, test-beam preparation
	CERN, Geneva, Switzerland	Mechanics frame, simulations for design optimization	test-beam infrastructure	
	DESY, Zeuthen, Germany	sensor qualification, connectivity scheme, integration, test-beam infrastructure, simulations	prototype of a thin fan-out 2016	conceptual design studies
	IFIN-HH, Bucharest, Romania	Data analysis and simulation		
BeamCal GaAs on CVD diamond tungsten calorimeter	IFJPAN, Cracow, Poland	laser based position monitoring, physics performance studies		FPGA programming for DAQ system, semi-transparent sensor studies
	ISS Bucharest, Romania	Data handling and analysis		
	JINR Dubna, Russia	GaAs sensor production and qualification, absorber plate production and qualification	delivery of absorber plate prototypes 2016	
	NCPHEP Minsk, Belarus	test-beam preparation, diamond sensor studies		
	Pontificia Universidad Catolica de Chile, Santiago, Chile	FE and ADC ASIC development in 180 nm TSMC technology	prototype performance results 2017	
	Tel Aviv University, Tel Aviv, Israel	sensor qualification, assembly of detector planes, data analysis and simulations	sensor plane prototype end 2015	
	Tohoku University Sendai, Japan	pixel sensor in SoI technology	prototype 2017	
	University of Colorado Boulder, USA	simulations		
University of California Santa Cruz, USA				
		radiation hardness studies for silicon and GaAs sensors		
VINCA Institute of Nuclear Science & University of Belgrade, Belgrade, Serbia		data analysis, simulations, physics performance studies		Test-beam measurements and data analysis

Chapter 6

Muon Detector

6.1 Muon / Tail Catcher Detector

Contact person: Valeri Saveliev (email : saveliev@mail.desy.de)

References not referred to in text

6.2 Introduction

The main goals of the Muon System in the ILC Detector are the identification and reconstruction of the muons from inelastic e^+e^- interactions over the largest possible energy and angular range and recover the energy leakage out of the hadron calorimeter (Energy Tail Catcher).

The physics goals set for the ILD detectors require that muons momentum are reconstructed with high precision of about $\Delta p_T/p_T^2 = 2 \times 10^{-5}$. Due to the large amount of material muons have to traverse before reaching the muon detection system, it cannot provide the required momentum resolution and will be optimized mainly to the high efficiency and purity of muon identification. A momentum resolution of this precision planned to be achieved with an excellent tracking system at ILC detector and important aspect is efficient linking of track candidates from the inner detectors with tracks in the muon detection system.

In addition to its muon identification ability, the first layers of the muon detection system will be optimized to act as a tail catcher for showers developing late in the calorimeters. This will improves the energy measurement in the hadron calorimeter, especially for the highest energy.

Another aspect of the muon system is the stand-alone identification and reconstruction of beam-halo muons. This requirement has an impact on the muon system granularity and time resolution, which shall be better than 1 ns.

6.3 Conceptual Design of the Muon / Tail Catcher Detector

Important constraints for the design of the muon system at ILC as for many other experiments is the instrumentation of the detection elements inside the Iron return yoke, needed for the magnetic flux return of the detector solenoids. The muon system/tail catcher detector instruments the Iron return yoke in the barrel and in the forward regions with maximal coverage. The needed mechanical stability requires that

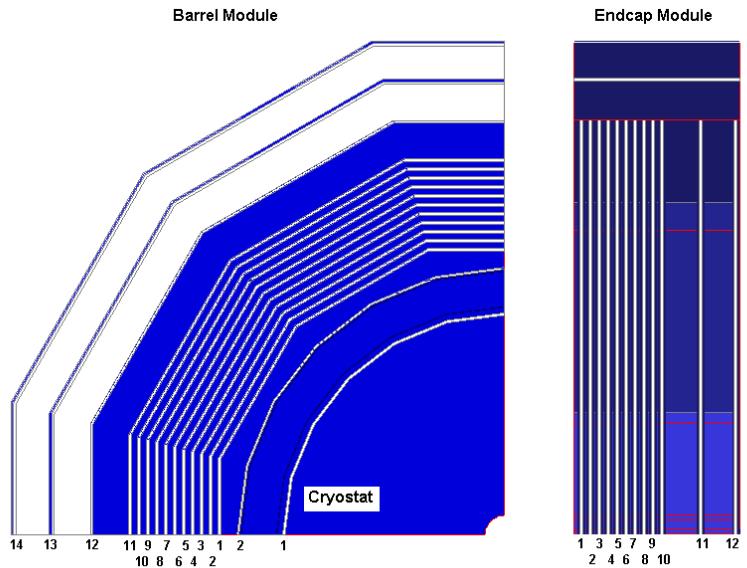


Figure 6.1: Sensitive Layers of ILD Muon /Tail Catcher Detector

the iron return yoke layer thickness is at least 10 cm. The muon detectors will be interleaved between such Iron plates are used as muons absorber.

The requirement that the muon system/tail catcher serves both as a muon identification and as a tail catcher impacts its layout design. The first section of the system provides ten relatively closely spaced layers, to act as a reasonable continuation of the hadron calorimeter. As mentioned above the mechanical constraints limit between readout stations to be at least 10 cm.

At the rear of the muon system the distance between stations can be much increased, since they only need to act as for the muon identification and reconstruction. Last three layers in the barrel, and two in the endcap are spaced 60 cm apart.

The fact that the magnet coil adds about two interaction lengths of material in front of the muon detection system limits the effect of the tail catcher. To maximize its impact the first sensitive layer is placed in front of the iron yoke, directly behind the coil and the first 10 layers are spaced more closely to improve the calorimetric performance of the muon system.

Finally the yoke barrel part is equipped with one sensitive layer in front of the Iron yoke, 10 layers spaced 14 cm apart, followed by three sensitive layers spaced by 60 cm apart. The forward part of the yoke is equipped with 10 layers spaced by 14 cm, followed by two sensitive layers spaced by 60 cm. The overall layout of the muon system/tail catcher is shown in Figure 6.2.

Two main options are investigated for the muon detection elements: scintillator strips equipped with wave-length shifting fibers and readout with silicon photomultipliers (Sc/SiPM), or resistive plate chambers (RPC).

6.4 Scintillator/Silicon Photomultiplier

Contact person: Valeri Saveliev (email : saveliev@mail.desy.de)

6.4.1 Introduction

The main option for the sensitive layers will use extruded plastic scintillation strips, composed of polystyrene doped with 1.0% PPO and 0.03% POPOP. The extruded scintillator a width of 25 – 30 mm and thickness of 7-10 mm.

A 1 mm wide extruded groove running along the centre of the strip will take a commercially available wave length shifting (WLS) fibers. The groove was filled with a white epoxy made of DER 332 resin and Jeffamine.

The scintillator strips will be covered on the outside by a layer of TiO_2 , that is co-extruded alongside the scintillator during the extrusion process.

The maximal length of strips required for ILD is 200 – 250 cm.

The signals will be readout from both sides of the strips by Silicon photomultipliers, coupled to the wave length shifting (WLS) fibres. Reading out both sides of a strip offers the possibility to define the position of the hits along the strip, which will help in reducing the fake rate in the muon system.

Figure 6.2 (left) shows the design of the scintillator strip. The right picture presents the signal (number of photons) of the scintillation strip with WLS and SiPM readout from both sides.

6.4.2 Recent Milestones

The major R&D effort of the Muon / Tail Catcher Development was concentrated on the optimization of the overall structure of the Muon System/ Tail Catcher:

1. Detailed Full Monte Carlo Simulation of the Muon System/Tail Catcher, it is concern to choose the geometry of detection plane, geometry of the stereo layers, number of the layers of the detection system and their position, especially concern to the energy leakage,
2. Study of the performance of the Muon System/Tail Catcher with framework of PFA,
3. Optimization of the detection elements of the Muon System/Tail Catcher. The first priority is the design of the main detection elements a scintillation strips with the SiPM readout,
4. Development of the Digital options of the SiPM for the Muon /Tail Catcher System, which will dramatically simplify the readout electronics and data processing.

6.4.3 Engineering Challenges

The main engineering challenge is the build the Distributed Large Scale of the Muon /Tail Catcher System and their embedment in the Solenoid Magnet Yoke. Several layouts for the muon system have been tested. This year will start the study of the integration of the large scale distributed Muon System/Tail Catcher Detectors in the Structure of the Solenoid Magnet Yoke.

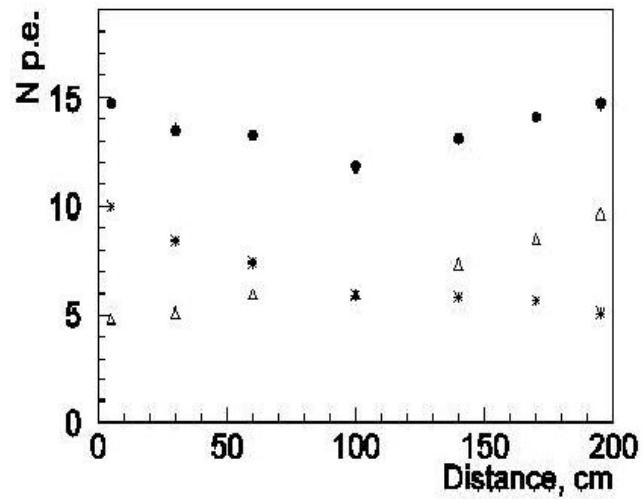
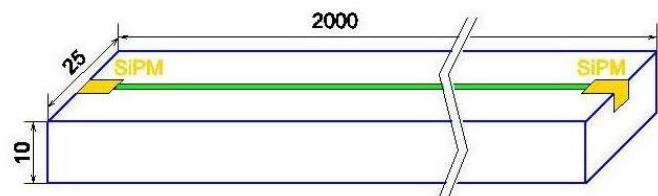


Figure 6.2: Sensitive Layers of ILD Muon /Tail Catcher Detector and number of detected photons

6.4.4 Future Plans

Continue of the optimization of the Muon System/Tail Catcher on base detailed Monte Carlo Simulation and Reconstruction Chain,

- The performance of the muon system has been evaluated by simulating events in the ILD concept. To determine the optimal layout, a geometry was created in MOKKA [3] with 19 layers in the barrel and 18 layers in the endcap, at equal distances of 140 mm. After simulating the detector response in MOKKA once, different layouts could be studied by including or excluding layers in the reconstruction phase. For this study the muon layers have been segmented in pads of $30 \times 30 \text{ mm}^2$.
- Study of the Integration of the Muon System/Tail Catcher in to Solenoid Yoke,
- Build of the prototypes of the Muon System/Tail Catcher detection elements on base of the Scintillator Strip/Wavelength Shifter and Analog SiPMs for the study of the main elements as thickness, length, reflection coating, wavelength shifters light yield and other. For this purposes will be develop the test setup for the cosmic muons detection,
- Design and Technology development of the Analog SiPMs on base CMOS technology as preliminary options for the Muon System/Tail Catcher optimization,
- Technology Development of the Digital option of the SiPMs on base innovative 3D interconnection (3D-IC) technology with fully digital readout and processing electronics.

6.4.5 Applications Outside of Linear Colliders

The development of the Digital SiPMs will have strong impact on the many application areas

One of the important application of practically full design and technology of the Muon /Tail Catcher System in the Homeland Security is the Muon Tomography for the security checking of the transport containers. The checking of the millions of the transport container in present time is one of the crucial and urgent problems, which don't have the efficient solution. The muon tomography, based on the HEP Muon System could be solution.

The development of the Digital SiPMs will have strong impact in Nuclear Medicine, in particular development of Positron Emission Tomography (PET). The new generation of the PET scanners will be developed on base of the All Digital SiPM Readout with more advanced performance.

6.5 Resistive Plate Chamber

Contact person: Valeri Saveliev (email : saveliev@mail.desy.de)

6.5.1 Introduction

Resistive plate chambers (RPC) are considered as an alternative sensitive elements for the Muon/Tail Catcher Detector. Main features are excellent granularity up to $1 \times 1 \text{ cm}^2$ pads and one threshold (1-bit), i.e. digital readout or semi-digital readout

Several types of RPCs have been successfully constructed and tested in the worldwide HEP community and within the ILC R&D program [4].

Resistive Plate Chambers (RPCs) are likely technology choices for the SiD ILC hadron calorimeter (HCAL) and MUON systems due to their low cost. RPCs have often been used as muon detectors (BaBar and BELLE). RPCs are inexpensive to build and can be easily constructed in a variety of shapes and sizes.

The major concern with RPCs has been their aging characteristics (BaBar was forced to replace its original RPCs and BELLE had startup problems). Despite the significant progress made in recent years in RPC *R&D*, a full understanding of all aging mechanisms has not been reached. For example, the precise role of gas contaminants such as HF (acid produced by the breakdown of the Freon used in RPC gases) in initiating of hot spot and increased current remains to be understood. A thorough understanding of the physics and chemistry of RPCs is needed if this technology is to be chosen for use in an ILC detectors.

Glass RPCs running in saturated avalanche mode are being considered for the HCAL. A large (40 m^2 of RPCs) prototype system is being proposed for beam tests in FY08. The construction schedule for the prototypes is ambitious and leaves little time for further studies of possible aging effects or of alternative gas mixes. A smaller parallel effort could focus solely on these details and would broaden the US expertise in this potentially vital technology.

Recently an attractive alternative to glass has emerged from *R&D* for the BESIII muon system. The BESIII have developed Bakelite RPCs that have thin plastic films covering the inner Bakelite surfaces which eliminate the need for the traditional linseed oil coating. This new material has intrinsically lower noise than the Bakelite/melamine electrodes used in both the LHC and BABAR detectors. Over 1000 chambers were built and installed for BESIII. The bulk resistivity of the Bakelite can be adjusted to allow higher rate capability than glass. The BESIII chambers operate in streamer mode. Studies of these chambers in saturated avalanche mode while monitoring the humidity and HF content of the output gas may prove this design to have significantly superior aging properties than standard RPCs.

Development of the RPC readout is going in collaborate with the SLAC KPIX group [].

The test prototypes of the KPIX front end data acquisition chip in the readout of RPCs operating in the saturated avalanche mode. The SLAC group will provide several KPIX chips for testing and aid in the design of a chip carrier that will mate to the 3 cm wide pickup strips of the RPCs. Initial tests of the device with existing Bakelite RPC chambers will establish the compatibility and robustness of the present design with actual RPC signals. If successful, the tests will be extended to glass RPCs as used in the HCAL prototype and to chambers constructed from BESIII Bakelite. A second study will examine the production and absorption of $F - (HF)$ in glass and BESIII RPCs and compare them to standard RPCs with linseed oil. Previous studies have found clear correlations between contaminants such as HF and increased noise rates and currents. Bakelite RPCs have been found to be sensitive to both the input gas and environmental humidity. A study of the humidity sensitivity of RPCs constructed from BESIII Bakelite will help determine the optimal operating conditions for these chambers.

6.5.2 Future Plans

1. Measure and predict the aging characteristics of the Bakelite RPCs to establish them as alternatives to standard glass or Bakelite RPCs,
2. Gain experience with glass RPCs while studying possible aging mechanisms. Study of alternative RPC gases could identify gas mixes that would minimize the production of harmful contaminants which lead to premature chamber aging,
3. Validate the use of the KPIX front-end chip for RPC readout.

Chapter 7

Software Tools

7.1 Introduction

Software for the simulation and reconstruction of detectors at Linear Colliders addresses the following needs of the community:

- Studies of detectors with several technology options within the same framework.
- Reconstruction in highly granular calorimeters with a goal of 3-5% jet energy resolution.
- Flavor tagging of b-, c-, and gluon jets in multi-jet events.
- Support of beam tests of detector prototypes as well as large-scale physics and detector simulation studies.

The center piece of the Linear Collider software infrastructure is the LCIO event data model and persistence format. The well-controlled evolution of the data format enabled the creation of reconstruction packages that can be shared by all collaborations in the Linear Collider community.

The software packages are well adapted to studying a variety of different detector models, as necessary for thorough detector optimization studies. The detector description facilitates quick changes to the detector layout, such as different sizes or positions for a given sub-detector. At the same time, it allows the addition of new readout schemes, sensitive materials, or geometries.

Starting from simple algorithms borrowed from previous experiments, the reconstruction packages have been incrementally improved on an as-needed basis, in parallel with improvements to the detail of the detector simulation. They now feature sophisticated strategies and state-of-the-art algorithms for pattern recognition and track and vertex reconstruction, and the most advanced particle flow algorithms available.

The following packages have been developed:

- LCIO – Event data model and file format
- Mokka – Detector simulation
- LCSim – Detector simulation and reconstruction
- LCFIPlus – Vertex reconstruction and flavor tagging

- PandoraPFA – Pattern recognition, calorimeter reconstruction and particle flow algorithms
- Marlin – Event reconstruction framework
- DD4HEP – Detector description for simulation and reconstruction

7.2 LCIO

7.2.1 Introduction

The LCIO software toolkit [171] provides an event data model (EDM) and persistency format for physics and detector simulations. It was developed as a joint effort and has been adopted by all of the detector concepts for both ILC and CLIC. Many of the sub-detector R&D groups (e.g. CALICE and LCTPC) have also adopted LCIO for both their simulation needs and for testbeam data. The software toolkit consists of an Application Programming Interface (API) with implementations in Java and C++ and a binding to python.

7.2.2 Recent Milestones

Please provide

7.2.3 Engineering Challenges

What are the engineering challenges *that will need to be solved* when the ILC becomes real.

7.2.4 Future Plans

Continued development of LCIO will be driven by user demand and developers' resources.

7.2.5 Applications Outside of Linear Colliders

The Heavy Photon Search experiment at Thomas Jefferson National Laboratory has adopted LCIO as its event data model and data persistency format. Physics and detector studies for CLIC and the Muon Collider have also used LCIO. The Whizard [172] event generator uses LCIO as a possible output format for Monte Carlo events. This could lead to its integration into other experiments. Because of its simple and well-documented persistency format LCIO is a perfect candidate for HEP data archiving applications.

7.3 LCSim

7.3.1 Introduction

The lcsim physics and detector response simulation and event reconstruction toolkit provides a suite of software programs to allow studies of multiple detector designs for the ILC. These tools include the Geant4-based detector response simulation program (slic), and the Java-based reconstruction and analysis tools (org.lcsim) [173].

7.3.2 Recent Milestones

Mile stones since the DBD

7.3.3 Engineering Challenges

What are the challenges for using this when the ILC becomes real?

7.3.4 Future Plans

The core functionality is being kept current by upgrading to the latest versions of Geant4, etc. Due to lack of funding, the project is currently primarily responding to user requests for additional functionality.

7.3.5 Applications Outside of Linear Colliders

The flexibility and power of this simulation package make it not only useful for the application domain for which it was developed (viz. HEP collider detector physics), but also for other physics experiments, and could very easily be applied to other disciplines, e.g. biomedical or aerospace, to efficiently use the full power of the Geant4 toolkit to simulate the interaction of particles with fields and matter. The Heavy Photon Search experiment at Thomas Jefferson National Laboratory has adopted slic as its detector response simulation package and the org.lcsim toolkit for its event reconstruction needs. Physics and detector studies for CLIC and the Muon Collider have also used both slic and the org.lcsim software. The software could be easily used for physics and detector studies at detectors at future circular colliders.

7.4 DD4HEP

7.4.1 Introduction

DD4hep[[174](#), [175](#)] provides a generic, consistent and complete detector description, including geometry, materials, visualization, readout, alignment and calibration. It supports the full experiment life cycle: from detector concept development over detector optimization and construction to the operation phase. A single source of information is used for simulation, reconstruction and analysis, where different interfaces and formats are provided as needed. DD4hep is implemented using the ROOT geometry package TGeom.

7.4.2 Recent Milestones

The core of DD4hep provides the necessary code and tools for a complete and flexible detector description, based on C++ classes per sub detector and corresponding XML files holding parameters. It provides a palette of simple and generic sub detector geometry classes, which allows new users to get started very quickly with using DD4hep by simply adapting the XML parameters files to define a new particle physics detector. Advanced users can write their own detector descriptors to incorporate any level of detail that is needed. A complete toolkit (DDG4)[[176](#)] for running a Geant4 based detector simulation based on a DD4hep detector model has been developed. It provides software modules for fully configuring and running a simulation application, including reading of generator files in various formats, overlaying several events, linking Monte Carlo truth information to hits and creation of the final output files in the LCIO file

format. The programs can either be run as a python application or a C++ application with XML configuration files. The current Mokka simulation models for ILD have been fully ported to DD4hep (in the lcgeo package) and the CLICdp group describes their new detector model exclusively in DD4hep/lcgeo.

7.4.3 Engineering Challenges

One of the most challenging aspects in the implementation of DD4hep lay in hiding some of the complexity and technicalities involved in detailed geometry models from the user in order to facilitate the development of maintainable experiment detector description code. A considerable fraction of the complexity is created by the fact that ROOT and Geant4 have independent implementations of the geometry classes, which partly differ in constructor arguments (meaning and order) as well as in a different set of units used in the two systems. Another challenge will be to make DD4hep compatible with multi-threading applications for simulation and reconstruction/analysis.

7.4.4 Future Plans

The improvement of the core functionality as well the development of new features in DD4hep will continue over the next years. Besides addressing the multi-threading needs of the community, an interface to conditions and alignment data is on the list of extension projects already identified. for DD4hep. Additional requirements and requests brought forward by the user community will have to be addressed.

7.4.5 Applications Outside of Linear Colliders

DD4hep has been designed from the start as a generic tool that can be applied to any particle physics experiment. It is currently used by the ILD and CLICdp detector concepts as the main source of detector geometry information and simulation application (based on DDG4). The three FCC studies (FCC-ee, FCC-hh, FCC-eh) have recently also decided to base their software chain on DD4hep and will use it for the conceptual design reports in the next years.

7.5 Marlin

7.5.1 Introduction

Marlin[177] is a C++ application framework for processing LCIO event data files. Marlin applications are configured with XML files. Software modules – called processors – have their own section in the configuration file, where all parameters local to the processor are defined. By design every parameter has to be registered by the author including a short documentation, which allows a Marlin application to provide a complete and fully documented example configuration file. The LCIO event data model is used as a so called internal data bus (or whiteboard), i.e. every Marlin processor can read its input collection(s) from the LCIO file and create one or more output collections.

7.5.2 Recent Milestones

As Marlin is at the core of the the data processing software for the Linear Collider community, an effort has been made to keep it stable and robust. It is used by ILD, CLICdp and SiD, as well as by almost all test beam collaborations in the context of the Linear Collider. Wherever possible, new features have been

added in a backwards compatible way, such that existing steering files would work as before. Some of the improvements that have been recently added to Marlin are:

- The addition of command line parameters, where every parameter present in the XML file can be overwritten on the command line – useful for scripting and bulk processing;
- optionally the LCIO collections that are read from the file can be limited, possibly resulting in greatly improved processing speed;
- introduction of the global flag `AllowToModifyEvent` to allow corrections or additions to input data collections.

7.5.3 Engineering Challenges

There were no major engineering challenges involved in the development and maintenance of Marlin. As pointed out above, the main challenge laid in keeping Marlin stable, usable and robust. Adopting Marlin to parallel processing and multithreading, which is planned for the near future, will however be a very complex and challenging process, where we will need to learn from the work done by the LHC experiments in this context.

7.5.4 Future Plans

The improvement of the core functionality as well as the development of new features in Marlin will continue over the next years. Making Marlin capable of processing several events in parallel in order to make better use of new multi-core hardware will be the most demanding new development in the near future. Additional requirements and requests brought forward by the user community will be addressed.

7.5.5 Applications Outside of Linear Colliders

Even though Marlin as well as LCIO have Linear Collider in their names, both are rather generic software tools that can and actually are used outside of the LC community. For example the EUTelescope software framework is based on Marlin and is used by Atlas and CMS groups in the context of the detector upgrade R&D program.

7.6 PandoraPFA

7.6.1 Introduction

The PandoraPFA software package [106, 178] consists of a C++ software development kit (SDK) and libraries of reusable pattern-recognition algorithms that exploit functionality provided by the SDK. Algorithms have been developed to provide a particle flow reconstruction of events in fine-granularity detectors, such as those proposed for use at the ILC or CLIC. The reconstruction uses over 60 algorithms in order to carefully trace the paths of visible particles through the detector. The output is a complete list of the particles in an event, each with a reconstructed four-momentum and an identified particle-type. The algorithms represent the state-of-the-art in particle flow calorimetry at a Linear Collider.

7.6.2 Recent Milestones

The Pandora Linear Collider algorithms have recently been used for extensive detector optimization studies, assessing the physics performance of the ILD_o1_v06 detector model with different configurations of the electromagnetic and hadronic calorimeters. A selection of the key plots is shown overleaf.

7.6.3 Engineering Challenges

The implementation of large numbers of pattern-recognition algorithms in C++ can be extremely difficult. Algorithms must work as intended, be easy to maintain/extend and have tight control of memory management. The Pandora SDK addresses these issues directly: it provides a sophisticated Event Data Model and performs all event memory- management. Access to event objects and modification of these objects can only occur via algorithms requesting services provided by the Pandora SDK. A key remaining challenge is to ensure algorithms are efficient and scale kindly with the number of input objects in an event. This is a matter for the algorithm author, rather than the framework, but the Pandora SDK provides a number of constructs to help address performance. These include KD-trees, which provide $\log(n)$ look-up of e.g. hits within a search-volume around a specified space-point. There is a cost associated with constructing KD-trees, but the reduction in e.g. hit-hit permutations can be enormous.

7.6.4 Future Plans

Continued development of Pandora SDK and pattern-recognition algorithms, plus provision of support to users of Pandora. On-going Linear Collider work includes improvement of π^0 reconstruction and efforts to further improve the ability to identify and separate neutral hadrons from nearby charged hadrons. Detector optimization studies will continue and will include full examination of performance of Pandora algorithms with digital and semi-digital HCAL detector models.

7.6.5 Applications Outside of Linear Colliders

The Pandora SDK has been designed to aid development of pattern-recognition algorithms in generic fine-granularity detectors. As such, its use is not limited to the ILC. Pandora algorithms now provide a successful particle flow reconstruction in an upgrade model of the CMS detector, even in dense pile-up conditions. Algorithms have also been developed for reconstruction of cosmic ray and neutrino-induced events in liquid argon time projection chambers, having significant impact in the neutrino-physics community.

7.7 LCFIPlus

7.7.1 Introduction

The LCFIPlus package [179] builds upon the previous heavy flavor identification software, LCFIVertex [180] to offer algorithms for jet clustering, secondary vertex reconstruction, and heavy quark flavor tagging. With respect to the previous version, specifically the reconstruction of multi-jet signatures, such as those encountered in the Higgs self-coupling analysis has been improved. This is achieved partly by first reconstructing secondary vertices, then clustering the event into jets taking into account the reconstructed objects. This strategy effectively prevents the splitting of secondary decays across multiple jets. LCFIPlus uses multivariate classifiers for the flavor tagging.

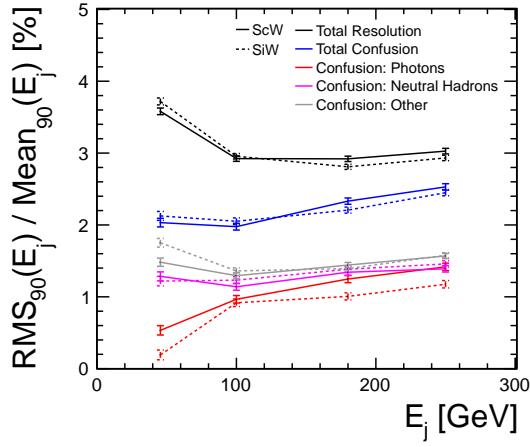


Figure 7.1: Jet energy resolution as a function of jet energy, including a breakdown of the resolution into contributing “confusion” terms. Illustrates performance of Pandora algorithms for ILD_o1_v06 with Silicon (Si) or Scintillator (Sc) as ECAL active material.

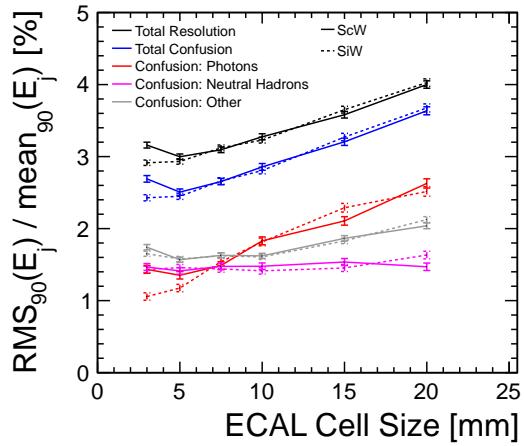


Figure 7.2: Jet energy resolution as a function of the ECAL cell size, for 250 GeV jets in ILD_o1_v06. As expected, the photon confusion term (ability to separate photons from nearby hadrons) drives performance changes.

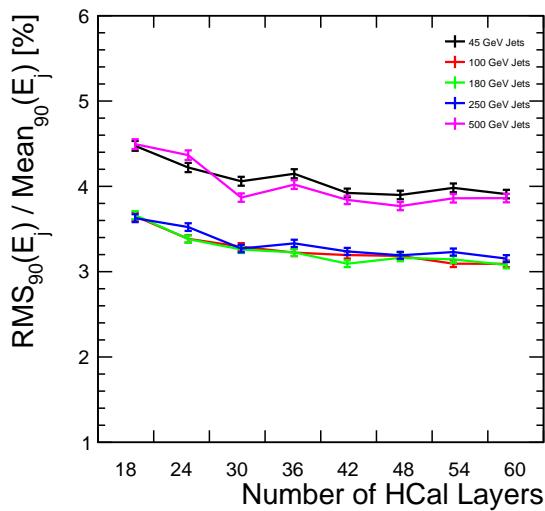


Figure 7.3: Jet energy resolution as a function of the number of layers in the HCAL, for a range of different energy jets in ILD_o1_v06.

7.7.2 Recent Milestones

Recent major developments have focused on improving statistical methods for flavor tagging. Other developments include improvements to the interface to simplify the performance tuning for different detectors. Additionally, the development infrastructure was modernized to facilitate collaboration; the code is now hosted on github.

7.7.3 Engineering Challenges

Future challenges include integration with new geometry descriptions. Additionally, improvements are needed to the CPU performance, particularly the scaling behavior for large number of tracks.

7.7.4 Future Plans

Current developments focus on further improving the flavor tagging performance by using advanced reconstruction methods. Adaptive vertex fitting methods can further increase the efficiency of finding secondary vertices. Additionally, incorporating particle identification information from the tracking detectors, and adding information from π^0 reconstruction allow to improve the vertex mass and hence the flavor tagging performance.

Technology	Institutes	Description / Concept	Milestones	Future Activities
LCIO	SLAC	Event data model (EDM)		
	DESY	and persistency format		
LCSim	SLAC	Physics and detector response simulation and event reconstruction toolkit		
DD4HEP	CERN	Detector description, including geometry, materials, visualization, readout, alignment and calibration.		
Marlin	DESY	C++ application framework for processing LCIO event data files.		Parallelization and adaptation to multi-core hardware
PandoraPFA	Cambridge	Particle Flow reconstruction package, consisting of a software development kit and reconstruction libraries		- improvement of π^0 reconstruction - improve the ability to identify and separate neutral hadrons from nearby charged hadrons.
LCFIPlus	Kyushu	Vertex reconstruction,	Development of a vertex-aware jet finder	Improvements to vertex reconstruction
	Tokyo	jet clustering, and flavor tagging toolkit	Efficient flavor tagging in 6-jet events	Addition of particle ID to flavor tagging
	PNNL			Better integration with geometry description
Arbor				
Garlic				
ILCDIRAC				
Mokka				

Chapter 8

Spinoffs

8.1 Vertex Detectors

8.1.1 CMOS

CPS developed at IPHC in perspective of the ILC are used in several devices, as illustrated by the non-exhaustive list below:

- Several high precision transparent beam telescopes, adapted to (< 1 GeV) electron beams, are equipped with the MIMOSA-26 or -28 (alias ULTIMATE) sensors
- The first generation of sensors with full on-chip signal processing developed at IPHC (in a $0.35\text{ }\mu\text{m}$ CMOS process) was applied to the STAR-PXL detector at RHIC, which completed successfully its first data campaign in 2014 and has started its 2015 run
- The upgraded ALICE ITS will be the next equipment based on CPS; it will provide insight of a token ring architecture pioneering the one considered for the IBISCUS chip mentioned above; it will also provide running experience with a tracker based on CPS
- The Micro-Vertex Detector of the CBM experiment at FAIR/GSI will also be based on the CPS presently developed for the ALICE-ITS upgrade
- The sensors were, or are, being applied outside of subatomic physics. They were for instance used in the FIRST experiment at GSI, for hadrontherapy monitoring; they are presently developed for soft X-Ray imaging and brain-imaging.

Sensors featuring pixels about 5 times larger than those equipping the STAR-PXL were fabricated in 2014, with different pixel design optimisations. Such large pixels are more exposed to the effects of signal charge recombination. The purpose of the paper is, among others, to show that the charge particle detection efficiency is not degraded, even after radiation loads representative of upcoming trackers, such the upgraded ALICE Inner Tracking System. The charged particle detection performances of these large pixel CPS prototypes with integrated signal processing and binary outputs were studied by exposing the sensors to a 450 MeV electron beam. The results obtained will be exposed and shown to validate the concept for its evolution towards large area tracking devices, with the perspective of integrating logical strips in the sensor.



Figure 8.1: Pixel detector for the STAR experiment

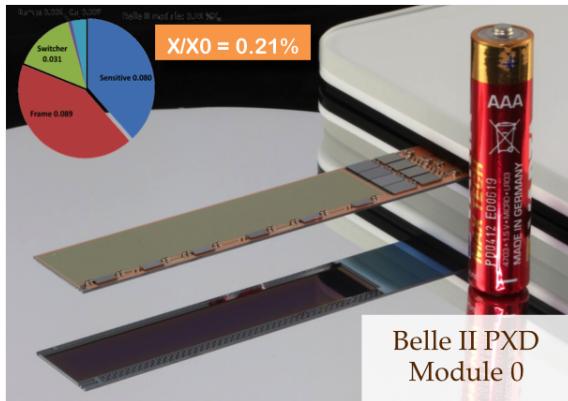


Figure 8.2: A DEPFET ladder for the Belle II vertex detector

8.1.2 DEPFET

The concept of a DEPFET active pixel detector for vertex detection at collider experiments was initiated in the linear collider community (for TESLA). The election of DEPFET technology for the Belle II detector therefore represents an important spin-off of linear collider detector R&D. DEPFET is also considered a strong candidate technology for the vertex detector at a future circular collider (<http://cepc.ihep.ac.cn/preCDR/volume.html>). DEPFET detectors are furthermore used for X-ray imaging at the XFEL [181]. Future space missions envisage the use of DEPFET sensors [182]. Their use in microscopy is being studied.

8.1.3 FPCCD

Because of the relatively slow readout speed, the application of FPCCD sensors to other high energy physics experiments would be limited. However, high spatial resolution of small pixel size must be applicable to measurements of X-ray imaging. Two-phase CO₂ cooling system can be applied to any other detectors which require efficient cooling between -40 °C and near room temperature. Our system, which uses a CO₂ gas compressor, has a great advantage for low temperature operation near -40 °C compared with systems using liquid pumps for circulation.

8.1.4 Chronopix

With some modifications (for example, adding time-time converter) ChronoPixel architecture can be applied for any experiment requiring time stamping of individual hits – it may be HL-LHC, CLIC and so on.

8.1.5 SOI

8.1.6 3D Pixel Development

As stated above the technology is already being developed for CMS and x-ray imaging applications. The large area sensor concept is applicable for a variety of focal plane array concepts.

8.1.7 CLICpix

The CLIC vertex-detector R&D shares its main challenges of simultaneously achieving small pixel pitch, low material budget and fast timing with other future pixel detector projects, such as the developments for the upgrades of the LHC detectors for high-luminosity operation or for future circular colliders. Synergies with these projects are exploited for example in the context of the RD53 collaboration for 65 nm hybrid readout ASICs [183] and via the AIDA2020 project for Advanced European Infrastructures for Detectors at Accelerators [184]. Moreover the CLICpix ASIC is derived from the Timepix/Medipix family of hybrid readout ASICs [185], which have a wide range of applications in medical imaging and material science.

8.2 Silicon Tracking

8.2.1 Long-Ladder and Charge Division Tracking R&D

It should be noted that the exploration of noise limitations for long, thin electrodes apply independently of the sensor technology that generates the signals. Thus, this work may have relevance to detection issues

across a wide array of fields.

8.2.2 Resistive charge-division on thinned micro-strips sensors with low signal amplification

The application of LGAD devices to the LC tracking is a spin-off of its original aim as timing devices for high radiation environments, this technology is being proposed as vertex locator technology for the LHC experiments: AFP2 and HGTD (ATLAS); and CT-PPS (CMS) [186].

8.2.3 KPIX

This work represents a significant step in the aggressive integration of silicon sensors with readout electronics, just short of integrating the electronics directly into the sensors. It has prompted consideration of this approach by CMS for calorimetry and by ATLAS for a muon system. It may have applications in sensors for light sources as well as other particle physics detectors.

8.3 Gaseous Tracking

8.3.1 Resistive Micromegas

The ND280 TPC at KEK uses the technology developed for ILC. A strong effort is pursued to develop detectors with similar technology for other applications such as the study of low energy neutrinos and the search for Dark Matter. Several TPCs for Nuclear Physics experiments are based on these developments. They are specifically discussed in a conference held every two years in Paris [187].

8.3.2 Pixelized Readout

A single GridPix detector is taking data for more than 1 year in the CAST experiment for axion search. For the LHCb VELO upgrade project a particle tracking telescope was constructed based on the Timepix-3 ASIC. In collaboration with KVI-CART in Groningen (NL) a system for proton radiography is being developed using small (gaseous) TPCs based on GridPix detectors, for accurate 3D proton tracking.

8.3.3 InGrid

A single InGrid detector will be installed this year in the CAST experiment for axion search. For a TPC in a CLIC detector, a highly granular (i.e. pixelized) readout structure is mandatory to lower the occupancy.

8.3.4 Electronics, DAQ and Cooling

The front end electronics, based on the SALTRO16-chip provides a very versatile system in the sense that it offers the possibility to set various readout parameters (polarity, shaping time, gain, decay time) in the SALTRO pre-amplifier. It is optimized for low capacitance detectors, sensitive to femtocoulomb signals with digital correction of the base line, followed by advanced pulse recognition and zero suppression. In that sense the SALTRO-chip can be regarded as a highly sensitive 16 channel digital oscilloscope. The small units of the readout system are suitable for applications and detector R&D in a variety of other fields like medical diagnostics, material science at XFEL, and for investigations at ESS.

8.4 Calorimetry

8.4.1 Scintillator Strips

- photo-sensor named MPPC from Hamamatsu Photonics KK is employed for the T2K experiment, CMS upgrade (HC-CAL), Belle II detector (end-cap muon)
- PET and SPECT development

8.4.2 Silicon-Tungsten ECAL in ILD

- CMS phase-2 upgrade project of the endcap calorimetry (HGCAL).
- The compact Silicon-W design has been used in the PAMELA satellite (very similar to the CALICE SiW ECAL physics prototype) [188].
- Future circular $e^+ e^-$ high energy colliders (FCC in CERN, CEPC in China) may also use this technology.

8.4.3 Silicon Tungsten SiD ECAL

This work represents a significant step in the aggressive integration of silicon sensors with readout electronics, just short of integrating the electronics directly into the sensors. It has prompted consideration of this approach by CMS for calorimetry and by ATLAS for a muon system. It may have applications in sensors for light sources as well as other particle physics detectors.

8.4.4 DHCAL

The DHCAL technology was specifically developed for the hadron calorimeter of the ILC, with its low particle rate and radiation dose. To export the technology to other environments, the rate capability of the chambers and the radiation hardness of the readout need to be improved. The former is being addressed with low-resistivity plates (glass and Bakelite), while the latter will require a new front-end readout system based on an ASIC using a smaller feature size. Possible applications are the tail catcher of the forward calorimeters of CMS and the outer wheels of the ATLAS muon system. Both options are being pursued actively.

8.4.5 GEM

This technology is already being used in many areas of application: CMS forward chambers, planar chambers for TOTEM, and even in cylindrical geometries. Beyond HEP, GEM technology is used in many in many human and animal medical imaging systems, and in muon tomography for homeland security. Many applications can be found at the CERN RD51 web site and links to RD51 meetings therein [189].

8.4.6 THGEM-based sampling elements for DHCAL

So far, our studies of THGEM-based detectors, particularly the RPWELL, have yielded a cost-effective, single-stage completely stable device, with wide dynamic range. The RPWELL concept is suitable for a variety of applications that do not require very high spatial and energy resolutions. Current examples

are CsI-coated multipliers for UV-photon imaging in RICH detectors; cryogenic gaseous photomultipliers for recording scintillation-light in noble-liquid detectors, developed for future dark-matter and neutrino experiments, medical imaging and in combined neutron/gamma inspection systems; fast-neutron detectors with dedicated converter-foils and Muon tomography inspection systems for the detection of hazardous materials in cargo.

8.4.7 Dual Readout

High precision calorimetry is vital to many experiments, both collider and fixed target; dual-readout is considered for a space station experiment; and, a high-precision dual-readout calorimeter is being considered for an electron – ion collider.

8.4.8 FCAL

The expertise acquired within FCAL for radiation hard sensors and fast front-end electronics was used to build, commission and operate fast beam-conditions monitors at the CMS experiment at LHC. Radiation hard sensors developed within FCAL are used as beam-loss monitors with excellent time resolution at FLASH, XFEL and LHC. In addition, front-end ASICs are under development for the upgrade of the LHCb tracker.

8.5 Muon System

8.5.1 Scintillator/Silicon Photomultiplier

The development of the Digital SiPMs will have strong impact on the many application areas

One of the important application of practically full design and technology of the Muon /Tail Catcher System in the Homeland Security is the Muon Tomography for the security checking of the transport containers. The checking of the millions of the transport container in present time is one of the crucial and urgent problems, which don't have the efficient solution. The muon tomography, based on the HEP Muon System could be solution.

The development of the Digital SiPMs will have strong impact in Nuclear Medicine, in particular development of Positron Emission Tomography (PET). The new generation of the PET scanners will be developed on base of the All Digital SiPM Readout with more advanced performance.

8.6 AIDA-2020 for LC experiments

AIDA-2020 is a research initiative funded by the European Union to advance the development of infrastructures for research on detectors for accelerator experiments. It runs from 2015 to 2019 and unites 38 beneficiaries from 19 countries. The total budget amounts to 29 MEUR, including 10 MEUR of direct support from the EU. The program is aligned with the European strategy for particle physics; thus about 50% of the activities are motivated by the needs of LHC detector upgrades, but there is a significant fraction of about 25% targeted at linear collider experiments.

AIDA-2020 follows the successes of the previous initiatives EUDET and AIDA. The infrastructure theme, although interpreted in a wider sense, moves common interests of R&D groups into focus and helps structuring the activities. It builds on the achievements of EUDET and AIDA, e.g. test beam infrastructures like the TPC magnet, the pixel telescopes or software frameworks like DD4HEP, but it goes

beyond in many respects. There is a three times larger budget to directly support users of, e.g., test beams, and there are new topics, like novel silicon sensors and micro-channel cooling.

Efforts, with strong representation of LC groups, will enhance infrastructures to advance towards the construction phase of calorimeters and gaseous detectors. This includes test stands for the characterization of silicon sensors or optical read-out units for highly granular calorimeters, as well as installations for the production and characterization of large area gas detectors, RPCs, GEMs, and micromegas,. Test beam infrastructure is further improved, to keep pace with increased demands of precision detectors, e.g. by adding a silicon strip telescope to the TPC test stand at the DESY.

Development of micro-electronic ASICs directly supports the efforts in vertex detector, tracking and calorimeter R&D. Particular attention, and a special fund, is devoted to the cooperation with industry and the transfer of technologies, e.g. for the production of large areas of silicon devices. Work on advanced software is strongly driven by LC needs and includes work on tracking tools and particle flow algorithms (PandoraPFA). The LC community had assigned high priority, in the proposal preparation phase, to the creation of a common DAQ framework for test beam experiments of several linear collider sub-detector prototypes in a combined set-up, which is now being pursued in a dedicated work package.

While activities remain coordinated in the R&D collaborations, AIDA-2020 represents a unique forum for intensive exchange between LHC and LC communities united in common working groups. This matches well the move of focus towards precision on the LHC side as well as to realistic detector designs in the LC world.

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