Title: Si-strip detectors (General)

The aim of the microstrip detector R&D line is twofold:

(1) to develop a set of innovative technologies (new sensor concepts, ultralight and smart mechanics, low dissipation powering systems and low noise read out ASIC) to cope with the unprecedented tracking precision requirements of the future high-energy lepton linear collider

(2) to provide a complete and realistic silicon-based tracking solution.

Major R&D efforts and recent developments since the ILC DBD

At the present time, IMB-CNM is an internationally recognized provider of silicon radiation sensors based on 4-inch wafers with a long experience on all available planar technology [1]

Concerning the development of advanced tracking sensors, IMB-CNM, IFCA and ITA groups tackled several microstrips technologies of interest for the ILC tracking: semitransparent, thin, resistive-electrode and low gain avalanche microstrips [2-5]

[1] M. Ullan et al., Nucl. Instr. Meth. Phys. Res. A in Press (2013)
[2] M. Fernández et al., Nucl. Instr. and Meth. Phys. Res. A 624 (2010) 340-343
[3] D Bassignana et al., 2012 JINST 7 P02005
[4] P. Fernandez et al, Nucl. Instr. and Meth. Phys. Res. A 658 (2011) 98–102
[5] G. Pellegrini et al, RD50 funding project, 2011
[6] M. Fernández, 22nd RD50 Workshop (Albuquerque, USA)
[7] F.R. Palomo et al, International Journal of Numerical Modelling: Electronic Networks, Devices and Fields (2010), vol. 23, pp. 379-399

Engineering challenges

- Enable IMB-CNM as a qualified silicon sensor supplier for ILD for the Forward Tracker Disk of the ILD experiment.

- Uniformity (within wafer, WIW, and wafer-to-wafer, WTW) of the process parameters in the sensor fabrication

- Integration prototypes and characterization of the sensors. Thermal management in the mechanics R&D line.

- Use of time resolved techniques, proven useful in other devices (LGAD)

- Asses the reliability of a power pulsing system based on Super-capacitors or on DC-DC. Verify the level of radiation hardness of super-capacitors

- Design of FEE inmune to transients and noise in the power distribution network.

- To assure the noise and power constraints which require a good design of the analog front-end. To achieve full channel integration and evaluate floorplaning and crosstalk issues.

Detector R&D plans for the coming years

- AC coupled, 200 micron thick microstrip sensors fabricated on six inch wafers. Process optimization is required and will be performed via fabrication of standard p-on-n diodes.

- Production of standard “small” area micro-strip sensors. Each wafer will contain several microstrip sensors with standard design already used in four-inch technology

- Dummy sensors processed with the FTD layout and shapes in order to perform mechanical and thermal testing in dedicated mock-ups

- Characterization of sensors and manufacturing of a integrated microstrip system prototype. Complete the full characterization of the sensors, develop new techniques for the silicon sensors characterization (as time resolved characterizations by transient current technique(TCT) [6,7]), and the experimental evaluation of an integrated prototype including sensors, front-end electronics and powering system. Thermo-mechanical models will be designed and constructed.

- Design development and assessment of a power pulsing system. FEE will be synchronized with the small duty cycle of the beam (0.5%). The PS system should be able to deliver this power remotely and generate the required high currents locally to minimize transient effects.

- To carry out a set of circuit simulations (Pspcie,PSIM and MATLAB) to define the characteristics of transients and noise that will be present in the power network and how they will be propagate through the power network, complemented with a set of emissions and immunity test on prototypes (small and large scale) of ILC-FEE.

- To provide a multichannel read-out ASIC for reading silicon micro-strips with the ILC structure (timing sequence). First, design of an Analog Module design fulfilling the requirements of low noise, high dynamic range and low power consumption. After exhaustive testing integration in a hybrid system (modules in ASICs plus off-the-shelf elements) in a PCB connected to a customized DAQ.

- Development of a fully operative single and multi-channel readout line to test the whole processing chain, including the sensor, the powering system, the readout and a customized DAQ.

- Customized DAQ and test. Integration will be done to build a hybrid channel which will include the powering, trimming digital-to-analog converters, and an analog-to-digital converter operating at the necessary speed to allow operation with ILC structure. The basic scheme of the hybrid prototype will be a hybrid PCB holding the ASIC/s, a Zedboard from Xilinx, software and configware.

- Development of advanced tracking sensors: 2D position sensitive microstrips with resistive electrodes based on the resistive charge division concept; microstrips sensors with integrated proportional signal amplification

List of participating institutes:

CERN, IMB-CNM, IFCA, ITA, UB, US.

External institutes: HEPHY Viena

Perspectives of this R&D for applications beyond the LC

Other applications for the technology developed, such as the use in X-ray imaging of DEPFET detectors, medical imaging applications of APDs, etc., are possible.

Some of the developments presented may be transferred to industry or other areas such as aerospace.

Radiation detectors are critically important in high-energy physics, but also have a broad range of applications, from biomedicine, material science to national security

Title: Si-strip detectors (Readout)

Development of the part of the Readout which is on-board the detector, i.e., the Front-end Electronics (FE).The ASIC is a multi-channel System-on-Chip (SoC) for self-triggered detection and processing of low level charge signals.

Major R&D efforts and recent developments since the ILC DBD

Some designs have been already started oriented to the ILC characteristics and timing structure. Most of the previous work was already started in 2002 by LPNHE in IN2P3 under the R&D Collaboration SiLC (Silicon tracking for Linear Colliders), whis was based on generic R&D aiming to develop the next generation of large Silicon tracking systems for the Linear collider experiments. FE readout ASICs were produced in the 180 nm [1] and 130nm [2,3] CMOS technological nodes. A sophisticated degree of signal processing and a fully programmable operation mode was developed. Because of insufficient time and budget the collaboration dissappeared without achieving a finished chip.

[1] [M. Dhellot, J.F. Genat, H. Lebbolo, T.H. Pham, A. Savoy-Navarro, A 16-channel silicon strips readout chip in 180 nm CMOS technology, IEEE Nuclear Science Symposium Conference, 2005]

[2] [T.H. Pham, A. Charpy, C. Ciobanu, A. Comerma, J. David, M. Dhellot, A. Diéguez, D. Gascon, J.F. Genat, A. Savoy Navarro, R. Sefri,A 130 nm CMOS mixed mode front end readout chip for silicon strip tracking at the future linear collider, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 623, Issue 1, Pages 498-500, 2010

[3] A. Savoy-Navarro, J.F. Genat, Th.H. Pham, R. Sefri, A. Comerma, A. Dieguez, A new 130nm FE readout chip for microstrip detectors, Linear Collider Workshop, 2008]

[4] [H. Gunther-Moser, Silicon detector systems in high energy physics. Progress in Particle and Nuclear Physics, 63(1), pp.186-237, 2009].

[5] [J. Brau, M. , A. Dragone, G. Fields, R. Frey, D. Freytag, M. Freytag, C. Gallagher, G. Haller, R. Herbst, B. Holbrook, R. Lander, A. Moskaleva, C. Neher, T. Nelson, S. Schier, B. Schumm, D. Strom, M. Tripathi, M. Woods, KPiX - A 1,024 channel readout ASIC for the ILC, IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), pp. 1857-1860, 2012]

Engineering challenges and Detector

Readout chips for reading charge from micro-strips are not new in particle physics experiments [4] At the moment none of the existing chips can be incorporated to the tracking detector. ABCD3T is an analogue read-out chip for Si strip detector modules for LHC experiments. This chip is built in a DMILL 0.8um process, which is a special radiation hard BiCMOS process. It has 128 channels, has a power consumption of 3.1mW/channel and a shaping time of 25ns. APV25 is a deep submicron readout chip for CMS. The

APV25 ASIC is built in a CMOS 0.25um process. It consists of 128 channels, each with a power consumption of 1.8mW/channel and a shaping time of 50ns. It has two modes, peak detection and deconvolution mode. The Beetle chip was developed for the LHCb vertex detector. It was built in a CMOS 0.25um process, consisting in 128 channels and a power consumption of 5.2mW/channel and a shaping time of 25ns. The ABCD, APV25 and Beetle chips have only analog output and present a very short shaping time, according to the structure of LHC. None of them is of direct use in ILC.

On the other hand, SLAC started the design of the KPiX chip [5] which currently continues in the development phase. The KPiX is a multi-channel read-out chip that bump-bonds to the detector and communicates through a few digital signals, power, and detector bias. The KPiX front-end is a low-noise dual-range charge-amplifier with a dynamic range of 17 bit, achieved by autonomous switching of the feedback capacitor. The device takes advantage of the ILC duty cycle of 1 ms trains at 5 Hz rate by lowering the supply current after the data acquisition cycle. During the 1 ms train, up to four events exceeding a programmable threshold can be stored.

R&D plans for the coming years

So far, this work has been done in the framework of the European Project AIDA (Advanced European Infrastructures for Detectors and Accelerators), where the UB resumed the readout design of the SiLC collaboration. As a main difference with the KPiX chip, multiple samples and pedestal are stored for multiple events, which allow higher accuracy in the post-processing. Lower power consumption and better noise characteristics are also envisaged. A big jump to an ultra-deep submicron technology (65nm node) has been done based on power consumption, integration and resource sharing with other on-going developments (Belle II, DEPFET Collaboration). Being at different development stages by two groups at the moment (University of Barcelona, SLAC) there is still a lot of contribution to do in this critical part of the detector and hence the opportunity to provide the Readout still exists and is of strategic interest.

List of participating institutes:

UB

Perspectives of this R&D for applications beyond the LC

The use of a CMOS readout chip able to measure radiation in the high dynamic range of the proposed design by UB is also of interest for measurements in space and terrestrial applications.

Title: DEPFET active pixel sensors

DEPFET active pixel sensors are one of most mature candidates for the ILC vertex detector and the innermost disks of the forward tracker.

Major R&D efforts and recent developments since the ILC DBD

The concept of a DEPFET active pixel detector for vertex detection at collider experiments was initiated in the linear collider community (for TESLA).

The operation principle was extensively proven on small-scale prototypes. A recent reassessment of the DEPFET potential for a linear collider at the energy frontier is found in [1]

The collaboration is making rapid progress - fueled by the election of DEPFET for the Belle II detector - towards a full-blown detector system including solutions for services and supports.

A full-scale, 75 micron thin Belle II ladder was successfully submitted to a test in a beam of charged at DESY in January 2014.

[1] The DEPFET collaboration, "DEPFET active pixel detectors for a future linear e+e- collider", IEEE Trans. Nucl. Sc. 60, 2, 2 (2013).

Engineering challenges

Vertex detector ladders with a thickness of several tens of microns and a spatial resolution of well below 10 microns require very robust mechanical properties. The power generated by the sensor and ASICs must be removed with the smallest impact on the detector material.
Measurements on thin ladders under a realistic load, including pulsed powering according to the ILC beam structure, prove the excellent mechanical properties of the all-silicon ladder. A complete mock-up for the innermost disks is under construction.

Detector R&D plans for the coming years

Currently, the construction of the Belle II vertex detector (to be installed by 2016) implies a large effort of R&D, including:

- Develop the die-attach technology in a controlled atmosphere required for the mounting of passive components on the DEPFET active pixel detector ladders. The first milestone is a fully integrated electrical prototype based on the EMCM.

- First tests that will determine if all the ASICs on the ladder are fully functional

- The integration of read-out and steering ASICs on the pixel sensor to be performed using a flip-chip technique and so-called bump-bonding, using microscopic solder balls.

- The production of the Belle II vertex detector modules, a joint effort of the DEPFET collaboration

- The test of the last version of the DHP chips

In the near future we hope to characterize the performance of ILC-design prototypes with pixels of 20 x 20 micron^2:

- Perform an engineering design for a DEPFET all-silicon module with the required petal geometry

- A detailed characterization of the response of the device

- Design of the ancillary ASICs, taking full responsibility for future design cycles of the Front End read-out chip, the Drain Current Digitizer (DCD) that is relevant to the ILC and a Belle II upgrade. This chip converts the analog signal from the detector to digital and has a crucial impact on the detector performance.

List of participating institutes

Three Spanish institutes are members of the collaboration;
- IFCA - environmental monitoring using Bragg fibres
- IFIC - contact to (I)LC community, thermo-mechanical properties, assembly of ladders for Belle II
- UB - design of read-out electronics

Perspectives of this R&D for applications beyond the LC

The election of DEPFET technology for the Belle II detector therefore represents an important spin-off of linear collider detector R&D. DEPFET detectors are furthermore used for X-ray imaging at the XFEL. Future space missions envisage the use of DEPFET sensors. Their use in microscopy is being studied.

Title: DEPFET active pixel sensors Front End Electronics

Major R&D efforts and recent developments since the ILC DBD

The Front-end Electronics (FE), i.e., readout electronics, is currently organized by a set of several ASICs: The SWITCHER, DCD and DHP chips [1]

The SWITCHER control chips select segments of the sensor array for read-out. A separate driver supplies the clear pulse of up to 20 V to remove the collected signal from the internal gate after read-out. Several designs of the SWITCHER versions optimized for Belle II requirements have been produced and tested successfully in two different CMOS technologies (0.35um and 0.18um). The drain current signals from 256 columns of pixels are processed and digitized by the DCD chip (Drain Current Digitizer [2,3]

The analog input stage keeps the column line potential constant (necessary to achieve fast readout), compensates for variations in the DEPFET pedestal currents, and amplifies and shapes the signal. The last DCD version is implemented in UMC 0.18um CMOS technology using special radiation hard design techniques (e.g. enclosed NMOS gates) in the analog part. This DCD chip is optimized specifically for Belle II requirements. The derandomized raw data from the DCD are transmitted to the Data Handling Processors (DHP) [4] using fast parallel 8-bit digital outputs.

This third ASIC, located on the end of ladder area immediately behind the DCD, performs data processing (pedestal subtraction, common code correction), compression (zero suppression), buffering and fast serialization. It furthermore controls the other read-out ASICs.

The first full-scale DHP prototype was implemented in IBM 90 nm CMOS technology. With the discontinuity of this technology new designs started in the TSMC 65nm CMOS process being the DHPT v.1.0 the last full-scale chip.

[1] [H. Krüger, Front-end Electronics for DEPFET Pixel Detectors at SuperBelle (Belle II), Nucl. Instr. Meth. A 617, 337–341, 2010].

[2] [J. Knopf, P. Fischer, C. Kreidl, and I. Peric, “A 256 channel 8-Bit current digitizer ASIC for the Belle-II PXD,” JINST, vol. 6, p. C01085, 2011.],

[3] I. Peric, T. Armbruster, M. Koch, C. Kreidl, and P. Fischer, “DCD: The multi-channel current-mode ADC chip for the readout of DEPFET pixel detectors,” IEEE Trans.Nucl.Sci., vol. 57, pp. 743–753, 2010].

[4] [M. Lemarenko, M. Havranek, T. Hemperek, T. Kishishita, H. Kruger and N. Wermes, The data handling processor for the Belle II pixel vertex detector: Efficiency optimization, JINST , vol. 7, p. C01069, 2012.]

Engineering challenges

The UB responsibility is the slow control and biasing part of DHP. Versions DHP0.1 and DHP0.2 were designed in 90nm IBM CMOS process.

Several designs (DHPT0.1, DHPT0.2 and DHPT v.1.0) were submitted to fabrication with TSMC 65nm and were tested during the period 2011-2013. The first versions of these ASICs included sub-modules that where included in the final design. The design submitted by the UB comprises temperature independent current references, 11 bias 8-bit DACs with current output, an integrated temperature measuring system and JTAG control. This design has been successfully tested during early 2014.

Detector R&D plans for the coming years

In the longer term the DCD and DHP are envisaged to evolve into a single chip. Being large arrays of DEPFET pixels a promising technology for the vertex detector of the planned ILC, adaptation of the DCD and DHP chips must also be done.

List of participating institutes

UB and U. Bonn

Perspectives of this R&D for applications beyond the LC

Title: Geiger-mode avalanche photodiodes

We have studied the feasibility of the Geiger-mode avalanche photodiode (GAPD) technology for particle tracking at the future linear collider [1]. GAPD detectors offer outstanding qualities to meet the challenging requirements of the International Linear Collider (ILC) and the Compact Linear Collider (CLIC), such as an extraordinary high sensitivity, virtually infinite gain and ultra-fast response time, apart from compatibility with standard CMOS technologies. In particular, GAPDs enable the direct conversion of a single particle event onto a CMOS digital pulse in the sub-nanosecond time scale. As a result, GAPDs can be read out after each bunch crossing.

Major R&D efforts and recent developments since the ILC DBD

We have explored two different standard CMOS technology processes. In particular, we have designed and tested two Application Specific Integrated Circuits (ASICs) with GAPDs in the High-Voltage Austria Microsystems (HV-AMS) 0.35 µm technology process. This technology process has been explored as an option to minimize the high pattern noise of GAPDs and thus reduce their occupancy [2-4]. Moreover, we have also designed another ASIC in the Global Foundries 130 nm/Tezzaron 3D technology process as a solution to address the requirement on the 100% fill-factor [5].
Nevertheless, although the performance of the prototypes developed is encouraging, further studies concerning radiation effects and the sensor efficiency in the detection of high energy particles are needed. The features that we have studied with each one of the mentioned ASICs are detailed next.

- First ASIC in HV-AMS 0.35 µm (submitted in April 2010)

- Design:
- Several single pixels with different readout circuits and small arrays
- The sensors and the readout circuits are monolithically integrated on the same die
- The sensor size is 20 µm x 100 µm
- The pixels are operated in the time-gated mode and with low overbiases to reduce the sensor noise
- Both voltage-mode and current-mode readout circuits are included
- Pixels with digital output
- Experimental measurements:
- I(V) characteristic
- Dark count rate and afterpulsing
- Sensitivity to light and dynamic range

- Second ASIC in HV-AMS 0.35 µm (submitted in April 2011)

- Design:
- One large array with 10 x 43 GAPD pixels (sensitive area of 1 mm x 1 mm, fill-factor of 67%)
- Other single pixels and small arrays
- The sensors and the readout circuits are monolithically integrated on the same die

- The sensor size is 20 µm x 100 µm
- The pixels are operated in the time-gated mode and with low overbiases to reduce the sensor noise
- Pixels with digital output
- Experimental measurements:
- I(V) characteristic
- Dark count rate, afterpulsing and crosstalk
- Temperature effects
- Sensitivity to light and dynamic range
- Sensitivity to high energy particles (beam-tests at CERN and DESY)

A wide variety of measurements have been carried out to demonstrate the efficiency of the proposed techniques to decrease the sensor noise. Further improved results have been obtained with the reduction of the working temperature. Thus, the minimum measured Dark Count Probability (DCP) of the GAPD detector (see Fig. 1) is 10^{-6} noise counts/GAPD, with a gated-off period of 308 ns, gated-on period of 1 ns, overbias of 1 V and temperature of -20 ºC. The suitability of the proposed detector array for particle detection is shown with the results of a beam-test campaign conducted at CERN and DESY [6, 7]. The set-up used in the beam-tests, together with the results obtained, is shown in Fig. 2. The results obtained show a correlation between the GAPD detector and the telescope used for the calibration, which suggests that the GAPD technology can sense Minimum Ionizing Particles (MIPs).

[1] E. Vilella, “Feasibility of Geiger-mode avalanche photodiodes in CMOS standard technologies for tracker detectors”, PhD Thesis Dissertation, Department of Electronics, University of Barcelona, Barcelona, Spain, 2013.

[2] E. Vilella, A. Diéguez, “Readout schemes for low noise single-photon avalanche diodes fabricated in conventional HV-CMOS technologies”, Microelectron. J., vol. 44, pp. 941-947, 2013.

[3] E. Vilella, A. Diéguez, “A gated single-photon avalanche diode array fabricated in a conventional CMOS process for triggered applications”, Sens. Actuators A: Phys., vol. 186, pp. 163-168, 2012.

[4] E. Vilella, O. Alonso, A. Montiel, A. Vilà, A. Diéguez, “A low-noise time-gated single-photon detector in a HV-CMOS technology for triggered imaging”, Sens. Actuators A: Phys., vol. 201, pp. 342-351, 2013.

[5] E. Vilella, O. Alonso, A. Diéguez, “3D integration of Geiger-mode avalanche photodiodes aimed to very high fill-factor pixels for future linear colliders”, Nucl. Instr. Methods Phys. Res. Sect. A, vol. 731, pp. 103-108, 2013.

[6] E. Vilella, O. Alonso, J. Trenado, A. Vilà, R. Casanova, M. Vos, L. Garrido, A. Diéguez, “A test beam setup for the characterization of the Geiger-mode avalanche photodiode technology for particle tracking”, Nucl. Instr. Methods Phys. Res. Sect. A, vol. 694, pp. 199-204, 2012.

[7] E. Vilella, O. Alonso, A. Vilà, A. Diéguez, “SPADs for vertex tracker detectors in future colliders”, 22nd International Workshop on Vertex Detectors (Vertex 2013), Lake Starnberg (Germany), Proceedings of Science PoS 025, 2013.

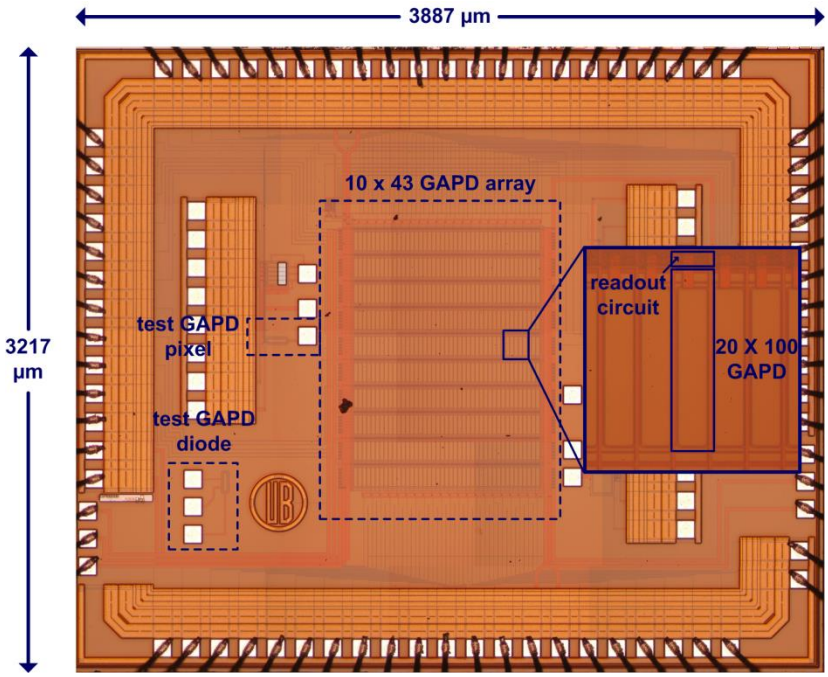

Figure 1 Micrograph of the fabricated ASIC with the 10 x 43 GAPD array.

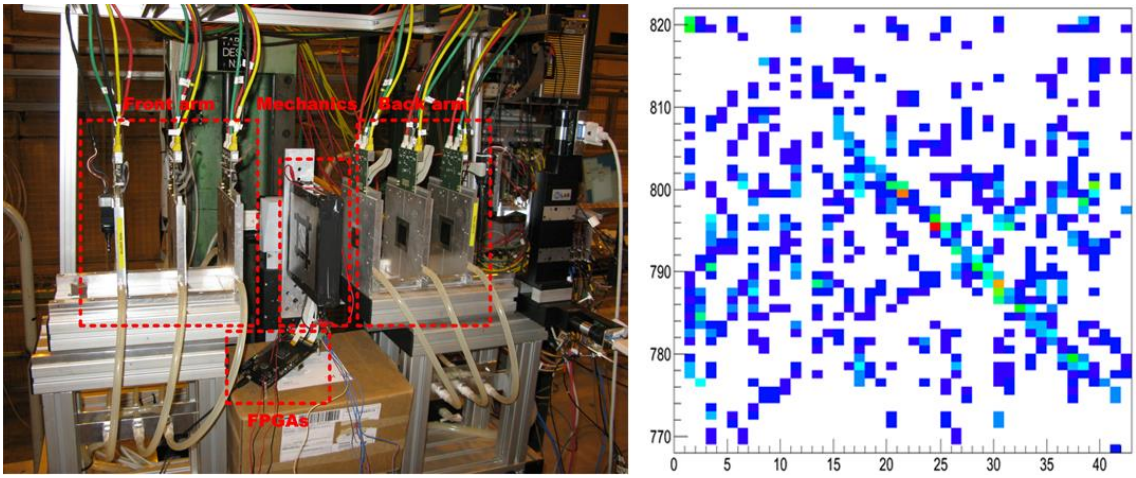

Figure 2 Set-up used at the CERN beam-test (left). Correlation between the GAPD detector array and the telescope used for the calibration (right). The axes indicate the position of the pixels.

Engineering challenges

In spite of all the advantages of GAPD detectors they suffer from two main problems. On the one side, there exist noise phenomena inherent to the sensor, which induce noise pulses that cannot be distinguished from real particle events and worsen the detector occupancy to unacceptable levels. On the other side, the fill-factor is too low and gives rise to a reduced detection efficiency. Solutions to these two problems and that are compliant with the severe specifications of the next generation of particle colliders have been thoroughly investigated as it is shown in the previous section.

Detector R&D plans for the coming years

- Third ASIC in Global Foundries 130 nm/Tezzaron 3D (not submitted)

- Design:
- One large array with two sub-detectors (with 48 x 24 GAPD pixels each)
- The sensor sizes are 18 µm x 18 µm for the first sub-detector, and 18 µm x 18 µm and 30 µm x 30 µm for the second sub-detector
- Each of these two sub-detectors has a fill-factor of 66% and 92%, respectively
- The pixels are operated in the time-gated mode and with low overbiases to reduce the sensor noise
- Pixels with digital output

Although the design of the GAPD detector in the 3D technology process is finished, it has not been submitted for fabrication due to the continuous delays in the Multi-Project Wafer (MPW) runs of the Global Foundries 130 nm/Tezzaron 3D technology. Nevertheless, the 3D GAPD detector demonstrates that the low fill-factor typical of GAPD technologies can be increased up to values close to 100%, as demanded by future linear colliders on detector systems.

List of participating institutes

UB

Perspectives of this R&D for applications beyond the LC

The Avalanche Photodiodes technology is highly interesting for medical devices, including for example PET (Positron-Electron tomography) or FLIM (Fluorescence Lifetime Imaging).

Title: Transparent microstrip detectors

A fast alignment system for microstrips, independent of tracks from particle collisions , has been pioneered by AMS and also implemented by the strip tracker of CMS [1]. Infrared laser beams perpendicular to the sensors to be aligned are used as pseudo- tracks of infinite momentum. The relative positions of the monitored sensors are calculated with respect to the laser beam.

[1] W. Wallraff, TAS status, AMS Tracker Meeting, CERN, 9 February 2005 http://ams.cern.ch/AMS/Tracker/Meetings/20050209/Wolfgang050113TASww1a.ppt

B. Wittmer et al., Nucl. Instr. and Meth. A, 581 (2007)

Major R&D efforts and recent developments since the ILC DBD

The groups of IFCA-Santander and CNM-Barcelona carried out an R&D project to study and produce enhanced IR transparent sensors. The sensor design was kept as close as possible to that of standard microstrips to avoid any degradation of their sensing performance.

- First, we simulate the passage of a coherent beam through the active volume of a detector model. Then the simulation was validated with test structures produced at CNM.
- In a second step, we fixed the geometrical parameters: (metal)strip-width/pitch ratio of the sensor, and simulated the same structure adjusting the thicknesses of the different material layers to improve the transmitance

Only the thickness of the outermost top and bottom nitride layers used as passivation (needed for electrical insulation and mechanical protection) was tuned to boost the transmittance. The rest of the parameters was left untouched. The reason is explained in the engineering section.

With this simple modification the final transmittance value reached 50% [2]. Up to 5 planes of silicon sensors can be aligned with such transmittance.

[2] Silicon microstrip detectors for future tracker alignment systems, Nucl. Instr. and Methods in Phys. Research A, Volume 628, 1 Feb 2011, Pages 276-281

Engineering challenges

For this system to perform, partial transparency of the sensors to the chosen wavelength is required. As a reference, commercial sensors from standard vendors exhibit a 20% transmittance in the IR.

Fabrication run need to be optimized and a challenge is the production method compatible with deposition tolerance of sensor manufacture. As tolerance and heterogeneity combined of the thickness of each layer in the different steps of oxidation, sputtering or deposition, will reduce the maximum transmittance value, a possible solution is to use the values measured for each material layer up to the passivation silicon dioxide and tuning the thickness of the last nitride layer, using the simulation, to yield the maximum transmittance

Detector R&D plans for the coming years

New simulations are being carried out to choose the thickness of the last Si3N4 layer which will boost the expected transmittance up to70%.

List of participating institutes

IFCA-Santander and CNM-Barcelona

Perspectives of this R&D for applications beyond the LC

The method is transferable to other alignment systems

Title: Resistive electrodes sensors

2D information in microstrip detectors is obtained by double sided processing of wafers. Another possibility is the use of 2 single sided detectors mounted back-to-back (stereo-angle configuration). In this case the thickness of the module is double the thickness of a 2-sided detector. An innovative solution for 2D spatial reconstruction on a single sided detector was proposed by IFCA and CNM. 1D microstrip sensors with resistive electrodes (non-metallic), read at both ends of each strip, allow measuring the coordinate along the strip in virtue of the different attenuation of the signal at each end. In the direction perpendicular to the strips the position is reconstructed as in any other 1D detector.

Major R&D efforts and recent developments since the ILC DBD

In an initial study [1], the feasibility of the charge division concept was demonstrated on fully fledged microstrip sensor with resistive electrodes where the ionization signals were induced by a near-infrared laser. An electrical simulation of the sensor's equivalent circuit, including the amplifying and filtering stages, was developed and benchmarked against the experimental data.

The simulation accounted for the major systematic effects degrading the response linearity; mainly, the nonconstant ballistic deficit due to the attenuation of the signal pulse during its propagation along the dispersive electrode.

The same microstrip detector with two different polysilicon electrode resistivities were tested [2] (Figure 1). Prototypes were studied using a laser beam and readout using a general purpose LHC-like electronics, not optimized for this specific sensor.

Yet, we achieved a spatial resolution along the strip of the order of 200 μm for a Signal to Noise ratio of 10 (20 is the standard for microstrip detectors, the difference coming from peaking time mismatch between sensor and electronics and resistivity of the electrodes).

The sensors were tested in a beamline using 120 GeV pions. Analysis of this data is on-going.

[1] D. Bassignana *et al.,* First Investigation of a novel 2D position-sensitive semiconductor detector concept
Journal of Instrumentation, 7 (2012), p. P02005

[2] 2D position sensitive microstrip sensors with charge division along the strips: studies on the position measurement error.
Nucl. Instrum. and Methods in Phys. Res. A (2013),
http://dx.doi.org/10.1016/j.nima.2013.06.018

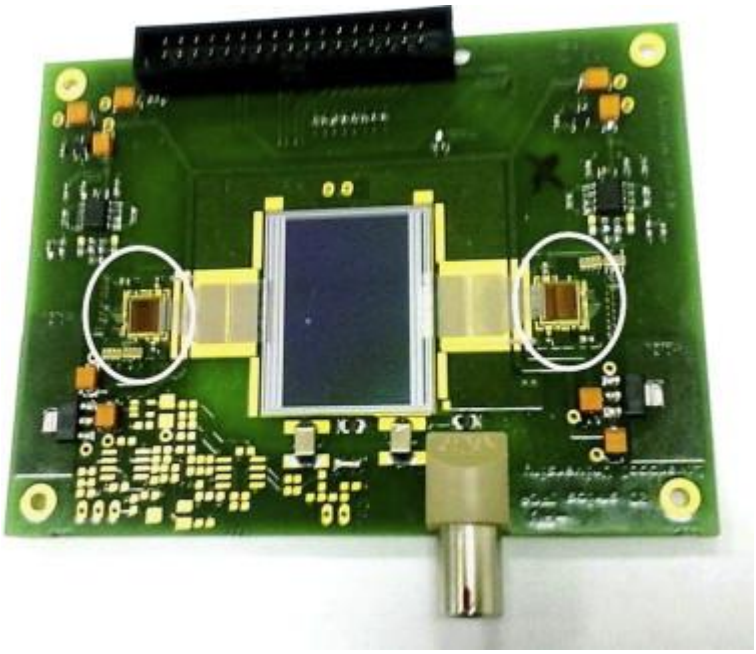

Fig.1

Engineering challenges

Optimize the electronics. To achieve the best signal/noise

Detector R&D plans for the coming years

List of participating institutes

IFCA and CNM

Perspectives of this R&D for applications beyond the LC

Title: Detectors with built-in low gain

Charge multiplication has been measured in detectors irradiated at fluences expected at the High Luminosity LHC (HL-LHC). The underlying mechanism of multiplication is the increase of the electric field near the electrodes, induced by an increase of the space charge at these regions. Under this increased field, electrons have enough energy to produce secondary electron-hole pairs by impact ionization. This process leads to charge collection efficiency above that of the unirradiated detector.

Detectors with a deliberate moderate gain could thus be a solution to the reduction of signal induced by radiation damage in Si and could compensate the signal loss due to thinning. The low gain value, besides, will allow using the same electronics for readout as for the thick counterparts.

Major R&D efforts and recent developments since the ILC DBD

Based on the design of Avalanche Photodiodes (APDs), n-on-p diodes with a deep p+ implant were produced at CNM [1]. The extra layer produces an electric field increase at the junction which is responsible for charge multiplication in this thin layer. The fact that the multiplication is limited only to electrons keeps the avalanche below the Geiger regime.

Prior to any more complex designs, simple diodes with built-in gain were studied with red laser from the backside. Gain values ranging from 3-10 were obtained.

Irradiation with neutrons up to fluences of HL-LHC show a decrease of the gain factor. This is being actively investigated at this moment.

[1] G. Pellegrini et al., Technology developments and first measurements of Low Gain Avalanche Detectors (LGAD) for High Energy Physics applications, Hiroshima Conference, HSTD9, Hiroshima, Japan. Nucl.Instrum.Meth A, in print.

Engineering challenges

Detector R&D plans for the coming years

The next step was the production of a run with microstrips with a multiplication layer. These detectors are now being distributed to collaborating institutes for a measurement campaign.

List of participating institutes

CNM, Institut Jozef Stefan, Ljubijana, USC(USA), IFCA

Perspectives of this R&D for applications beyond the LC

Title: Thin microstrip detectors

Thin bulk detectors are pursued to reduce the contribution of multiple scattering to the tracking performance of the system. The optimum thickness of a detector is a trade-off between scattering and signal level. In LHC systems, increased radiation hardness of thin sensors is another reason for thickness reduction. Lately, charge multiplication in highly irradiated detectors has been observed. This effect is even more important in thinner detectors, since the electric field is higher for the same bias voltage.

Major R&D efforts and recent developments since the ILC DBD

CNM and IFCA have designed, produced and measured 100 µm thick sensors produced on n-type bulk material. 4 microstrips per wafer were included, namely:

1 standard detector,

2 microstrips with integrated pitch adapters (1 with layout parallel to the strips,

1 with diagonal layout)

1 microstrip with polysilicon electrodes.

The wafer also included diodes and standard CMS test structures. The majority of sensors depleted at 20 V, and displayed leakage currents bellow 100 nA above full depletion. The yield after dicing was 70%.

Detector R&D plans for the coming years

The sensors need to be now characterized with transient current techniques before and after irradiation.

List of participating institutes

CNM, IFCA

Title: Powering new physics detectors

The future generation of Linear Collider experiments is trying to design systems with low energy consumption, in order to reduce the cooling system and minimize the material budget inside the detector volume. For that purpose, FEE operation will be synchronized with the small duty cycle of the beam. This design requirement leads to a synchronized power distribution that has to deal with an important amount of pulsed current.

Major R&D efforts and recent developments since the ILC DBD

Two different topologies are actually under study for the future linear colliders. One is based on switching mode power supplies and the other is based on supercapacitors.

The former is facing Electromagnetic Compatibility (EMC) issues associated with the noise emission from the power converters. The second represents the implementation of new technologies that perfectly fits with the operation mode of power pulsing FEE but it has not been validated to operate in the high energy physics environment.

During the last 7 years the Instituto Tecnológico de Aragon has been carried out several R&D studies focused on these two areas.

Regarding to switching technology, the focus was the EMC studies in the noise emission, the noise immunity and the noise propagation aspects presented in a power system based on switching converters. R&D working line has tried to identify the effects of the network impedance and the integration options (DC-DC converter location and granularity) defined by the noise emission of the switching converters. Additionally, immunity aspects such us noise coupling mechanism identification and grounding topology evaluations have been carried out. The main goal of those studies is to anticipate and minimize the total amount of noise present next to the detector and reduce the risks during the integration of the system. All these studies[1][2], based on real measurements and simulations, have been focused on the next generation of CMS Tracker sub-detector (Tracker Phase II) at CERN and in the PXD sub-detector for Belle II experiment.

Super-capacitors based power distribution system may be selected as an alternative option to power up the future linear colliders experiments. This technology plans to power the detector remotely by a current source that supplies low current to the periphery of each sub-detector. At that location, a set of super-capacitors store the charge and supply the high pulse current to the edge of each petal, where LV regulators stabilize the voltage at the input of each hybrid electronics. During the last years the R&D group has focused its research line trying to validate the used of this technology in the HEP environment. These activities have included the first radiation assessment of the super-capacitor for HEP[3] as well as the development of a prototype fully operational of a power group for ILC experiments based on supercapacitors .

[1] M.Iglesias, F.Arteche et Al. “Power Network impedance effects on noise emission of DC-DC converters” Journal of Instrumentation ,Vo7, 2012

[2] C.Esteban, F. Arteche et Al " Global noise studies for CMS Tracker upgrade" , Journal of Instrumentation Vol 5, 2010

[3] F. Arteche, C. Marinas, A.Pradas, M. Iglesias, I.Echeverria, FJ. Piedrafita, I.Vila "Super-capacitor characterization system for FTD-ILD sub-detector power distribution system" , ECFA - Linear Collider Workshop 2013 , Hamburg , Germany, May 2013

[4] F. Arteche, "Powering a low mass detector" ILD workshop Cracow, Poland, September 2013

[5] F. Arteche, I. Echeverria, A. Pradas , M. Ullan, I.Vila and A. Ruiz "Base line design for the ILC-FTD sub-detector power distribution system" LCWS 2012 International workshop for future Linear Colliders , Arlington , Texas, USA , October 2012

Engineering challenges

The preliminary results coming from these studies [4][5] encourage continuing with a more detailed analysis of the radiation hardness of capacitors. For one side, the super-capacitor has presented a small degradation after radiation tests and the super-capacitor based power supply system prototype has shown that this technology fits perfectly with the requirements of any power pulsing.

Detector R&D plans for the coming years

Future studies will be mainly focused on component optimization in order to minimize the mass and volume of the components used in these topologies. Additionally, radiation hardness studies will continue in order to obtain a full validation of these components for the HEP environment. Nowadays, most of the effort were focused on the tracking system but this technology may be extended to any power system presented in the experiments for future colliders based on power pulsing electronics.

List of participating institutes

ITA

Perspectives of this R&D for applications beyond the LC

The studies and developments carried out in these activities may be implemented not only in any HEP power system based on switching technology but also in any industrial or domestic environment. All these activities will be continuing in the next years focused on the immunity of the next generation of FEE.

Title: FBG Technology for LC

Fiber optic sensors are an established technology for temperature, deformation and displacement monitoring. In this case, between all FOS technologies we have selected FBG sensors in order to develop an structural an environmental monitoring system for particle physics trackers.

Major R&D efforts and recent developments since the ILC DBD and Engineering challenges

Since the DBD the main efforts related with FBG sensors have been oriented to develop a first self-monitoring support demonstrator. This demonstrator is a carbon fiber reinforced polymer sheet (CFRP) of 16 layers. The support has 4 sensors embedded between the first and the second layer and another 4 sensors between fifteenth and sixteenth layer. In Figure 1 it can be seen the sensors layout between CFRP layers.

We have in each layer 2 sensors to measure torsion and two sensors to measure flexion.

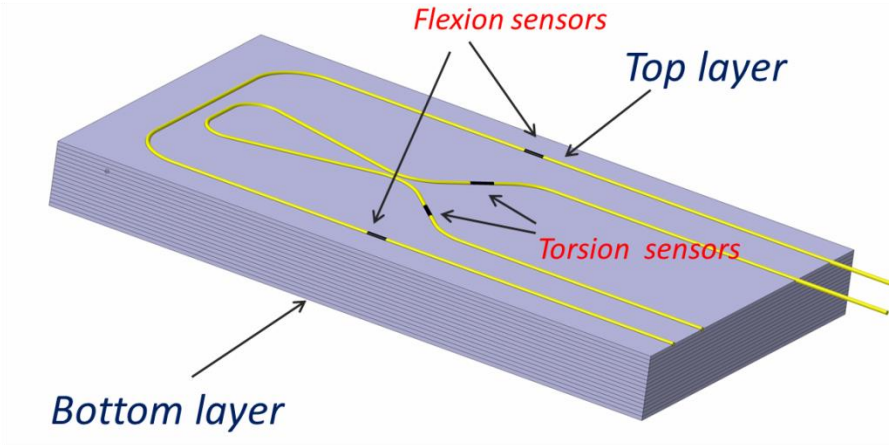

Figure 1

In figure 2 it can be seen the first manufactured demonstrator mounted in the calibration set-up. The main challenges for this self-monitoring structure were to design the ingress and egress of the fiber from the demonstrator. With this first mockup we found some production problems related with the cast used during the curing of the CFRP, obtaining a bad surface finishing. New cast have been bought and a new demonstrator is being manufactured. This two self-monitoring structures will be calibrated using an MMC.

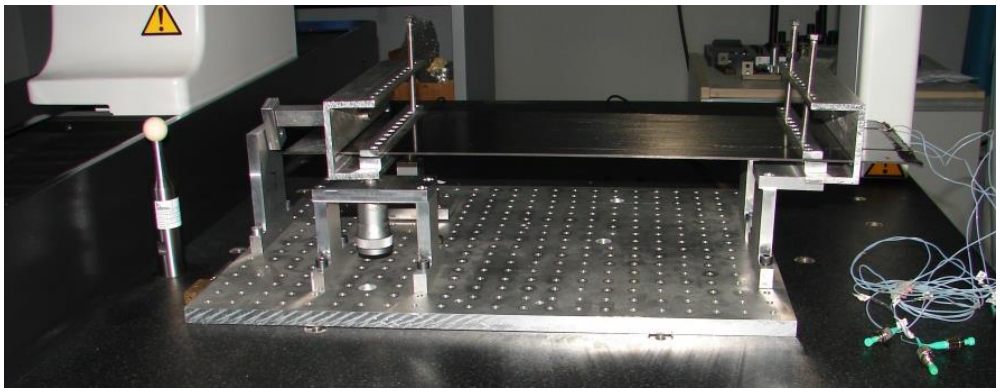

Figure 2

Another activity we have been working on has been the design of environmental monitoring systems for BELLE-II PXD –SVD common test beam on January 2014. During this test beam PXD and SVD sensors were inside an envelope in order to work with a dry atmosphere. We design a temperature-humidity monitor system in order to measure temperature and humidity change inside the envelope, and the temperature of the SVD cooling system inlet and outlet pipes. Is remarkable that our FBG sensors where the only sensors inside the envelope measuring temperature properly.

David Moya Martin: Fiber Bragg Grating Sensors for Smart-Trackers
ECFA Linear Collider Workshop 2013 , DESY 27-31 May

David Moya Martin: Status of Fibre Optical Sensors
3rd Belle II PXD/SVD Workshop and 12th International Workshop on DEPFET Detectors and Applications, Wetzlar 4-6 February

David Moya Martin: Update on FOS
4th Belle II PXD/SVD Workshop and 14th International Workshop on DEPFET Detectors and Applications., DESY 21-23 October

David Moya Martin: Bragg fibre sensor monitoring
CLIC Detector an Physics Collaboration Meeting, CERN, 1-2 October

Iván Vila Alvarez : R&D for silicon
ILD meeting 2013, Cracow, 4-6 September

Iván Vila Alvarez : Advanced Mechanics and polysilicon sensors
2nd Aida annual meeting, Cracow 10-12 April 2013

E. Currás, A. L. Virto, D. Moya, I. Vila, J. G. Carrión, M. Frövel, J. Garc´ıa-López, M. C. Jiménez,Y. Morilla, and F. R. Palomo : " Influence of the fiber coating type on the strain response of proton-irradiated fiber Bragg gratings."
IEEE TRANSACTIONS ON NUCLEAR SCIENCE , 59,4,937, August 2012

Detector R&D plans for the coming years

The plan for next years is to continue working in the development of self-monitoring structures. The first step is the calibration of these first technological demonstrators under torsion and flexion loads. For the middle of this year the plan is to manufacture a simplified FTD disks support with composite material, and some embedded FBG sensors. This disk will be used in a FTD pixels and strips disk common thermo mechanical setup to study the thermal behavior of the system and different cooling solutions. The FTD disk with FBG sensors embedded will allow us to measure temperature distribution in the support structure and the deformation and stress induced by the temperature. Finally we would like to manufacture a petal with the real geometry of the FTD petal and embed some sensors in order to be able to monitor deformations and temperature.

With respect to the environmental monitoring with FBG sensors, we are going to continue our activities in order to develop environmental monitors for detectors trackers. During the next year we are going to make some temperature measurements in the PXD – SVD common mock-up at Desy, and for the 2015 we have to design, install and commission an environmental and displacement monitoring system for the Belle II PXD detector.

The idea for the next years is to continue working in the implementation of these sensors for environmental and structural monitoring in next generation colliders' detectors trackers.

List of participating institutes

IFCA, IFIC, INTA

Perspectives of this R&D for applications beyond the LC

With respect to the possible applications outside the Particle physics area, we are already studying the possibility of using FBG sensors for nuclear industry in order to monitor environment temperature.

With respect to FBG related developments, some of them are of direct application for any kind of industry, and we have started to study the possibility of use this developments for another areas like for example cosmology.

Title: Development of Highly Granular calorimeters

The international CALICE (Calorimeter for the Linear Collider Experiment) collaboration is undertaking a major program of calorimetry R&D on finely segmented electromagnetic and hadronic calorimeters.

Major R&D efforts and recent developments since the ILC DBD

CIEMAT leads the mechanical activities of the Semi Digital Hadron Calorimeter (SDHCAL) based on gaseous resistive plate chambers (GRPC).

CIEMAT has been deeply involved in the construction of the first cubic-meter prototype that has been tested successfully in beams of particles at CERN. The design of the structure, the machining of the spacers, the final assembly and quality tests has been done at CIEMAT.

The planes of the 1m3 prototype were precisely machined, flatness <0.5mm (1mm required now). The plates were assembled together with the spacers using bolts.

Engineering challenges

The present SDHCAL goal is to build few larger GRPC chambers with the final dimensions of the biggest one (290x91cm2) foreseen for ILD, equip them with a new version of electronics and insert them in an absorber mechanical structure, built with the same procedures as the final one, capable to host up to 5 of them.

Detector R&D plans for the coming years

In the final module we plan welding the plates of the 1m3 prototype to reduce the lateral dimensions of the spacers to decrease the dead space.

Electron beam welding is probably the best but need vacuum conditions and could be not affordable for a big module, the Laser welding could be a better option. Standard, Electron beam and Laser welding will be tested at CIEMAT and external companies or CERN using also small plates already available.

Quality tests as the planarity or position precision will be performed by using a 3D articular precision arm already used for the 1m3 prototype tests.

Design, production and testing of a new DIF board to solve the problems found in the previous prototypes and to cope with the new front-end chip (HARDROC-3) and front end boards (ASUs) and also to fulfill the requirements of the new commands and synchronization system. It will include:

- DIF board production
- FPGA firmware and software design

The new prototype with large GRPCs (build at IN2P3-Lyon) must be tested (at CERN and DESY) with the new electronics in particle beams to demonstrate that the quality is not degraded, the noise does not increase and the new electronics fulfill the requirements for a real experiment. Tests of single chambers could be also considered.

List of participating institutes

CIEMAT, ITA

Perspectives of this R&D for applications beyond the LC