# 2 CMOS SENSOR BASED VERTEX DETECTOR

The ILC physics goals and running conditions require a vertex detector based on a pixel sensor technology and on thermo-mechanical performances differing significantly from those in use, in particular at LHC. The PICSEL group of IPHC [8] develops since many years CMOS Pixel Sensors (CPS) as well as ultra-light pixelated ladders and a specific vertex detector concept taking advantage of CPS to comply with the ILC requirements.

## 2.1 Physics objectives and detector requirements

The prominent reason to develop a specific pixel sensor technology and an ultra-light detector concept is the particularly high impact parameter resolution required at the ILC to comply with the ambitious flavour tagging capability. The ambitioned resolution is typically 2-3 (resp. 3-10) times better than the one achievable with an ATLAS-IBL layer in the plane transverse to (resp. containing) the beam lines. On the other hand, the required read-out speed and radiation tolerance are several orders of magnitude less demanding than at LHC.

The sensor spatial resolution should be better than 3 $\mu m$, the ladder material budget should not exceed 0.15% $X_0$ (or 0.3% $X_0$ in the double-sided geometry) and the inner detector radius should be below 2 cm. To be compatible with air flow cooling, the total power consumption should not exceed a few tens of W in average. The PICSEL group develops pixel sensors, detector ladders and a detector geometry matching these requirements.

## 2.2 Geometry and concept developed at IPHC

The vertex detector geometry constituting the framework of the studies is composed of three, nearly cylindrical, double-sided layers (see figure 4), equipped on both sides with 50 $\mu m$ thin CPS. This geometry is the baseline of the ILD concept [4]. A major difficulty consists in reconciling the required spatial resolution and read-out speed, since the former calls for small (and therefore numerous) pixels while the second calls for the smallest possible number of pixels to read out. The concept developed at IPHC resolves the conflict by sharing the two functionalities among the two (innermost) ladder sides (see figure 4).

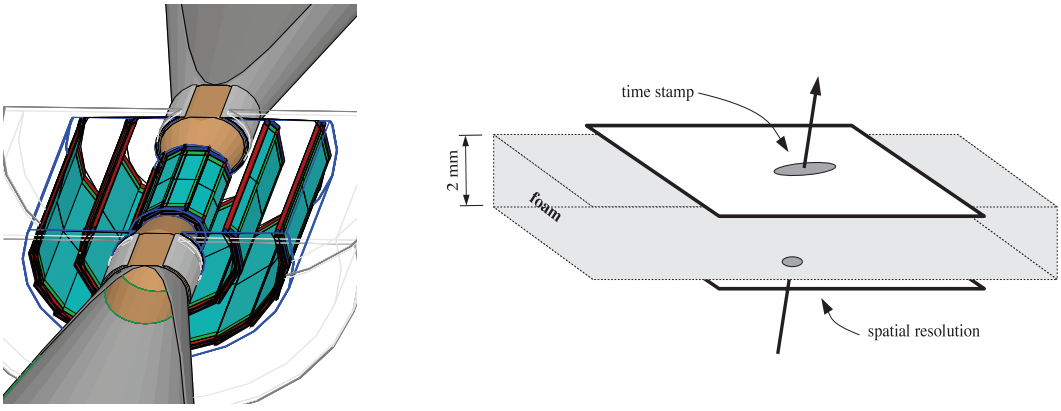


FIGURE 4 – Left : ILD vertex detector baseline geometry, relying on double-sided ladders. Right : Schematic view of the sharing concept between spatial resolution on one ladder side and timestamping on the other side.

Besides the requirements reflecting the physics goals, the detector has to face stringent requirements due to the running conditions close to the IP. The beam related background, dominated by beamstrahlung $e^{\pm}$ generated by the strong focusing and high density of the colliding bunches, induces a hit rate imposing a read-out frequency several orders of magnitude faster than required by the production rate of the signal final states alone (few Hz). The read-out time should therefore be kept in the order of a few tens of microseconds in the innermost layer, where the hit density is highest. This requirement, which tends to conflict with the demanded spatial resolution, may be alleviated for the outer layers, where a read-out time of $\sim 100\ \mu s$ is compatible with the strongly suppressed background hit rate (because of their low momentum, beamstrahlung $e^{\pm}$ are swept away by the experimental magnetic field).

Three different CPS variants are developed at IPHC. Two of them are intended to equip the two faces of the innermost layer, while the third sensor is devoted to the outer layers.

### 2.2.1 Pixel sensor R&D

CPS offer an attractive solution for an ILC vertex detector because of their low material budget due to their $\sim$ 20-30 $\mu m$ thin (high resistivity) sensitive volume, of the possibility to implement a high density sensing node lattice (leading to high spatial resolution) and of the possibility to integrate the full signal processing circuitry on the same substrate as the sensitive volume [9]. Detailed information on the different sensor designs and test results is provided in numerous publications which may be found on the PICSEL group home page [8]. This section concentrates on those aspects which are most essential for the validation of the CPS technology and for their application to an ILC vertex detector.

**The proof of principle of CPS for subatomic physics experiments** was achieved with the MIMOSA-26 sensor, developed for the beam telescope of the EU project EUDET [10]. The sensor architecture is based on a column parallel read-out with amplification and correlated double sampling inside each pixel. Each column is terminated with a high precision discriminator and is read out in a rolling shutter mode in 115 $\mu s$. Despite the binary charge encoding, the spatial resolution obtained with the 18.4 $\mu m$ pitch of MIMOSA-26 is close to 3 $\mu m$ (see figure 5).

This architecture was extended to a sensor (MIMOSA-28) [11] adapted to the PXL vertex detector of the STAR experiment at BNL, which is being equipped with 400 sensors exhibiting a 2x2 $cm^2$ sensitive area, thinned to 50 $\mu m$ and air cooled [12]. The m.i.p. detection efficiency observed at 30°C is displayed on figure 5 (right) as a function of the discriminator threshold and for a combined radiation load well above the ILC requirements [2]. Marginal performance variations are observed after irradiation, which validate the sensors for the radiation tolerance required at the ILC. The STAR-PXL is the pioneering detector for the CPS technology, based on ladders featuring a material budget of 0.37% $X_0$. An engineering prototype, composed of 3 complete sectors (out of 10) was operated successfully for the first time at RHIC within the STAR detector in May-June 2013 with pp and ArAr collisions. The complete detector will start its first physics data taking campaign in February 2014 ; It will act as a major milestone for establishing the CPS technology for the ILC.

**The design of CPS adapted to the ILC** is derived from the MIMOSA-26/-28 architecture, essentially in order to accommodate the read-out time and spatial resolution. Different CPS variants are foreseen in order to reach optimal performances in each layer.

**For the inner layer**, the sensors are optimised for single point resolution and read-out time, relaxing the power consumption constraint. The conflict between high granularity and fast read-out is resolved by equipping each ladder with two different types of sensors, one achieving the required spatial resolution and

2. $\lesssim$ 100 kRad and $10^{11}$ $n_{eq}/cm^2$ at 500 GeV.

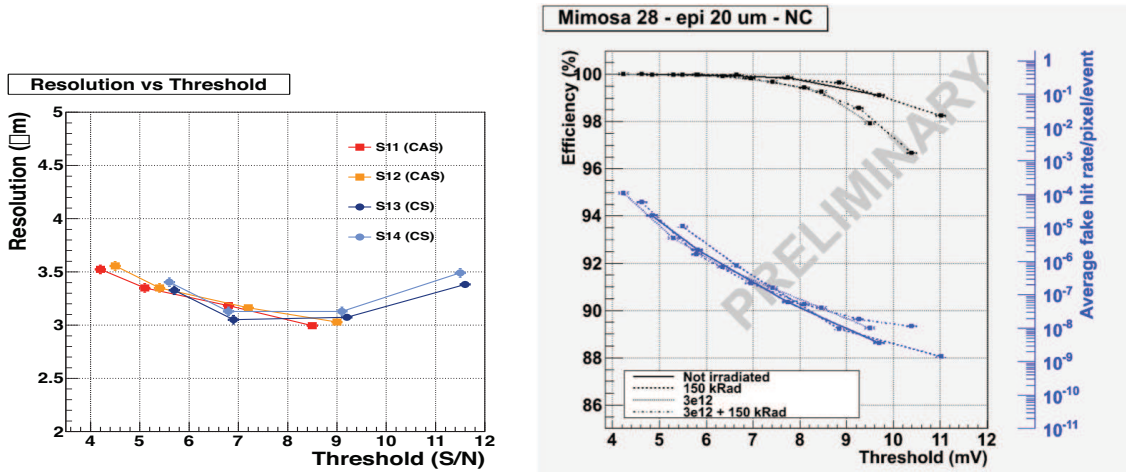


FIGURE 5 – Left : measured single point resolution for a 18.4 $\mu m$ pitch as a function of the discriminator threshold (the colours refer to in-pixel circuitry variants). Right : measured variation of the m.i.p. detection efficiency and fake hit rate (fraction of pixel noise fluctuations above threshold) of MIMOSA-28 as a function of the discriminator threshold, before an after irradiation (150 kRad, $3{\cdot}10^{12} n_{eq}/cm^2$), at a coolant temperature of 30°C.

one providing a fast time stamp. Both sensors are based on a 1-bit charge encoding achieved with on-chip high precision discriminators.

The highly granular sensors are mounted on one side of the ladders, and feature square pixels with $\sim 17$ $\mu m$ pitch providing a spatial resolution $< 3$ $\mu m$. Their frame read-out time is 50 $\mu s$. The fast sensors equip the other side of the ladder. They feature rectangular pixels (e.g. $17{\times}85$ $\mu m^2$), which result in 5 times less pixels per column, and therefore in a 10 $\mu s$ read-out time. The spatial resolution is $\lesssim 6$ $\mu m$ because of the pixel dimensions. Medium scale prototypes (MIMOSA-30a and -30b) were fabricated and tested in 2010/2011 in ordre to validate this approach.

It follows that correlating the $\sim 2$ mm apart impacts of traversing particles, the latter get assigned a spatial resolution of $< 3$ $\mu m$ and a time stamp of $\lesssim 10$ $\mu s$, which is expected to strongly suppress the perturbation of the track reconstruction due to beam related background, even in case of rates well in excess of the simulated values.

**For the outer layers**, the sensor design privileges power saving since these layers represent about 90% of the detector surface. This goal is achieved by enlarging the pixels in order to reduce the number of columns. The consecutive degradation of the spatial resolution is mitigated by ending each column with a 4-bit ADC. The $34{\times}34$ $\mu m^2$ large pixels foreseen deliver therefore a spatial resolution of $\sim 4$ $\mu m$, combined with a read-out time of $\sim 100$ $\mu s$. A small prototype of the sensor (MIMOSA-31) has been fabricated and tested in 2010/2012, demonstrating the validity of the approach at nominal frequency.

**Overall,** the detector would dissipate about 10 W in average, assuming power cycling with a 2 % duty cycle (i.e. 5 ms long periods of power dissipation centred on a 1 ms long train), a performance well compatible with air flow cooling.

The achievements above were obtained with a CMOS manufacturing technology based on a 0.35 $\mu m$ feature size which did not allow exploiting the real potential of CPS. In 2011 the PICSEL group moved to a 0.18 $\mu m$ CMOS technology offering more attractive fabrication parameters, motivated by the perspective of using CPS for the Inner Tracker System (ITS) upgrade of the ALICE experiment at the CERN-LHC. The prototyping performed in 2012 and 2013 has allowed reproducing all components of the MIMOSA-26 architecture in this technology to validate its modification for a twice faster read-out [13, 14].

### 2.2.2 Ladder developments

Double-sided ladders are being developed within a collaboration with Bristol University and DESY, based on a prototype called PLUME[3]. The main feature of the PLUME ladder concept is a double-sided layout, which consists of two sensor layers separated by a support structure [15]. A traversing particle produces two hits in the two ladder sensors. The hits, separated by approximately 2 mm, can be correlated and used to reconstruct a mini-vector with potential benefits of a better resolution, easier alignment and improved reconstruction of shallow angle tracks. The ladder concept is based on 2 sets of 6 MIMOSA-26 sensors (8 million pixels in total) thinned to 50 $\mu m$.

A first prototype was fabricated in 2011, composed of 2 sets of 6 MIMOSA-26 chips thinned to 50 $\mu m$ and mounted on thin flex cables assembled on both sides of a support structure made of SiC foam. It was successfully operated at nominal frequency. Its material budget, amounting to 0.61 % $X_0$, was not optimised. A new prototype is being fabricated, which features 0.35 % $X_0$, and is planned to be tested on beam in 2014.

## 2.3 Plans for the coming years

### 2.3.1 CPS development in 0.18 $\mu m$ technology

The outcome of the R&D on CPS performed up to now is a proof of principle for all 3 sensor variants envisaged for the different layers of an ILC vertex detector. The performances obtained are satisfactory and comply with the detector requirements up to 500 GeV, but can barely accommodate standalone tracking (nor running at 1 TeV). The 0.18 $\mu m$ technology used by the group for the ALICE-ITS [13, 14] allows for significantly faster read-out while simultaneously reducing the power consumption.

The main goal in the coming years is therefore to translate the 3 sensor variants described above from the 0.35 $\mu m$ CMOS process used for STAR to the 0.18 $\mu m$ process used for ALICE and to optimise their designs. A prominent objective is to achieve a time stamping resolution of $\lesssim 1$ $\mu s$, possibly 0.5 $\mu s$ to tag individual bunch crossings in the innermost layer. This will be complemented with the development of faster outer layer sensors, based on in-pixel ADCs. Both chips designs will be derived from the ASTRAL sensors developed for the ALICE-ITS.

An alternative detector read-out approach is also being considered, based on *fine pixels* ($\sim 5$ $\mu m$ pitch) integrating signals over a complete bunch train and read out during the 200 ms separating consecutive trains. A prototype was already fabricated and will be tested in 2014. The plan would be to next realise a low power 8-bit ADC complying simultaneously with a $< 200$ ms read-out time and an overall detector power consumption of a few tens of watts only.

### 2.3.2 Double-sided ladder developments and integration issues

There is still room to reduce the material budget of the PLUME double-sided ladder. Different approaches will be investigated, aiming at a target value $< 0.3\%$ $X_0$, possibly exploiting new materials for the support structure. A ladder associating 2 different types of sensors may also be developed, equipped with MIMOSA-26 chips on one side and with faster ($\lesssim 20$ $\mu s$) ASTRAL sensors (prototyped for the ALICE-ITS) on the other side, to test the concept of associating hits created by a traversing particle on both sides of a ladder equipped with complementary sensors..

Besides the ladder development itself, the ladders produced in 2014 will be used to address system issues. Micrometric alignment technics will be studied using sets of PLUME ladders assembled on 3 stations representing an azimuthal section of a vertex detector and installed on a beam line, possibly integrated in a work package of the successor of the AIDA project. Another important study concerns thermo-mechanical

3. standing for Pixellated Ladder with Ultra-light Material Embedding.

issues related to power cycling in a high magnetic field. Several other system integration aspects may also be studied, based on the forefront achievements coming out from the ALICE-ITS upgrade.

## 2.4 Resources associated to the activity

### 2.4.1 Personnel

The PICSEL group is composed of $\sim$ 20 staff personnel and 10 non-permanent members. The former are predominantly chip designers (11 engineers) and electronics engineers (5 engineers). The 4 physicists of the group are half from CNRS and half from Strasbourg University. The non-permanent members are predominantly PhD students (typically 4-6 chip designers and 1-2 physicists). There has been 1-2 post-docs in the group through the years concerned. Besides the PICSEL group, the micro-technics service of IPHC is involved in the PICSEL group projects at the level of 2 FTE in average. All together, the involvement of the personnel mentioned above adds up to typically 12 FTE·year staff involved in ILC activities and 5 FTE·year non-permanent staff.

Until 2016, the main activity of the group will address the ALICE-ITS upgrade, with a strong overlap with the ILC related CPS development. During 2016, activities directly addressing ILC may become the group main line, depending on the project evolution, and could result in a $\gtrsim$ 20 FTE·year involvement of IPHC.

### 2.4.2 Budget

The budget invested in ILC activities since 2008 is summarised in Appendix B, including resources allocated by IN2P3 and those obtained elsewhere (essentially CPER and EU).

The budget required to pursue the R&D for the ILC until 2016 will concentrate on integration aspects since the sensor R&D is essentially driven by the ALICE-ITS upgrade. Some dedicated ILC chip prototypes may however be fabricated (e.g. in-pixel ADC, elongated pixels for 1 $\mu s$ time stamping), demanding an annual contribution of $\sim$ 15-20 keuros. The system developments (mainly ladder production) require 10-15 keuros per annum. Test PCBs and equipment need yearly 10-15 keuros including test benches maintenance. Finally beam tests and meetings require a budget of 30-40 keuros per year. Overall, the annual budget required is about 70-80 keuros, out of which 20-30 keuros are likely to be found among collaborators. **The yearly budget required from IN2P3 for ILC activities on the vertex detector in the coming 2-3 years is therefore about 50 keuros**.