

Detector R&D Report

Editors
Jan Strube **Maxim Titov**
jan.strube@pnnl.gov maxim.titov@cea.fr

Contents

1	Vertex Detectors	3
1.1	Motivation and Constraints for Vertex Detectors at Linear Colliders	3
1.2	ChronoPixel	4
1.2.1	Introduction	4
1.2.2	Recent Milestones	5
1.2.3	Engineering Challenges	5
1.2.4	Future Plans	5
1.2.5	Applications Outside of Linear Colliders	6
1.3	CMOS	6
1.3.1	Introduction	6
1.3.2	Recent Milestones	7
1.3.3	Engineering Challenges	7
1.3.4	Future Plans	8
1.3.5	Applications Outside of Linear Colliders	8
1.4	DEPFET Pixel Sensors	9
1.4.1	The DEPFET Collaboration	9
1.4.2	Introduction	9
1.4.3	Recent Milestones	10
1.4.4	Engineering Challenges	10
1.4.5	Future Plans	11
1.4.6	Applications Outside of Linear Colliders	11
1.5	FPCCD	12
1.5.1	Collaborating Institutions	12
1.5.2	Introduction	12
1.5.3	Recent Milestones	12
1.5.4	Engineering Challenges	13
1.5.5	Future Plans	13
1.5.6	Applications Outside of Linear Colliders	13
1.6	SOI	13
1.6.1	Introduction	13
1.6.2	Recent Milestones	13
1.6.3	Engineering Challenges	15
1.6.4	Future Plans	15
1.7	3D Pixel Development	16

1.7.1	Introduction	16
1.7.2	Recent Milestones	16
1.7.3	Engineering Challenges	17
1.7.4	Future Plans	17
1.7.5	Applications outside of Linear Colliders	17
1.8	CLICpix	18
1.8.1	Introduction	18
1.8.2	Recent Milestones	18
1.8.3	Engineering Challenges	19
1.8.4	Future Plans	20
1.8.5	Applications Outside of Linear Colliders.	20
2	Silicon Trackers	22
2.1	Long-Ladder and Charge Division Tracking R&D	22
2.1.1	Introduction	22
2.1.2	Recent Milestones	22
2.1.3	Engineering Challenges	24
2.1.4	Future Plans	24
2.1.5	Applications outside Linear Colliders	24
2.2	Resistive charge-division on thinned micro-strips sensors with low signal amplification	24
2.2.1	Introduction and Motivation	24
2.2.2	Recent Developments and Milestones	25
2.2.3	Engineering Challenges	25
2.2.4	Future detector R&D	25
2.2.5	Applications outside LC	26
2.3	KPIX	26
2.3.1	Introduction	26
2.3.2	Recent Milestones	26
2.3.3	Engineering Challenges	26
2.3.4	Future Plans	27
2.3.5	Applications Outside of Linear Colliders	27
3	Gaseous Trackers	29
3.1	Time Projection Chamber – GridPix, Bonn	29
3.1.1	Introduction	29
3.1.2	Recent Milestones	29
3.1.3	Engineering Challenges	30
3.1.4	Future Plans	32
3.1.5	Applications Outside of Linear Colliders	32
3.2	Gaseous Tracking	32
3.2.1	Introduction	32

Chapter 1

Vertex Detectors

1.1 Motivation and Constraints for Vertex Detectors at Linear Colliders

The reconstruction of displaced decays has been an important part of particle physics programs since the days of bubble chambers and the discovery of “V” particles. This is still true in today’s high-energy collider experiments. If long-lived particles, such as B or D mesons, or tau leptons, decay to at least one charged track in the detector, they can in principle be resolved from the interactions of the primary collision. Similarly, the possibility to distinguish several primary interaction points significantly improves the reconstruction of events. To this end, modern vertex detectors use silicon sensors with small pixels, assembled in structures with as few radiation lengths as possible.

Highly performing vertex detectors are essential for the success of the physics program at the ILC. Discovery channels for a large class of new physics models involve third-generation fermions: b quarks that form long-lived mesons, top quarks that decay predominantly to a b quark and a W boson, and long-lived tau leptons. Furthermore, highly performing reconstruction of displaced vertices allows the distinction between the decays of B and D mesons and thus the reconstruction of the decay $H \rightarrow c\bar{c}$, which is not possible at the LHC experiments. The resolution of the perigee, or *impact parameter* of a helical track from the interaction point can be parameterized as

$$\sigma_{\text{ip}} = \left(\frac{\alpha}{p^{3/2} \sin \theta} \right) \quad (1.1)$$

The goal for the impact parameter resolution in an ILC experiment is $\approx 3 \mu\text{m}$. This could be achieved by a square pixel with a size of maximally $17 \times 17 \mu\text{m}^2$ without charge sharing between pixels. Taking advantage of charge sharing would allow designs with larger pixels to achieve the desired resolution.

Machine-induced background processes at the ILC and CLIC include electron–positron pairs produced in beam–beam interactions. These processes are nearly entirely responsible for the occupancy in the inner layers of the vertex detector at a linear collider.

FIXME: The dependence of the impact parameter resolution on the distance to the IP is ??? Must depend on the B field...

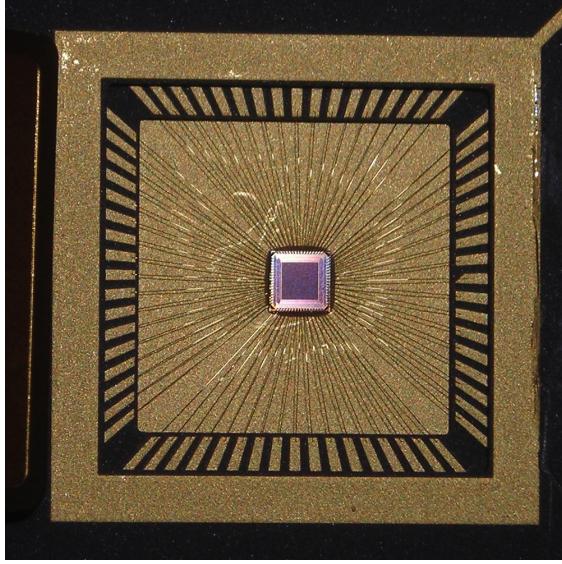


Figure 1.1: Photograph of the prototype 3 chip in its package. The chip has 48×48 pixels, each with a size of $25 \times 25 \mu\text{m}^2$.

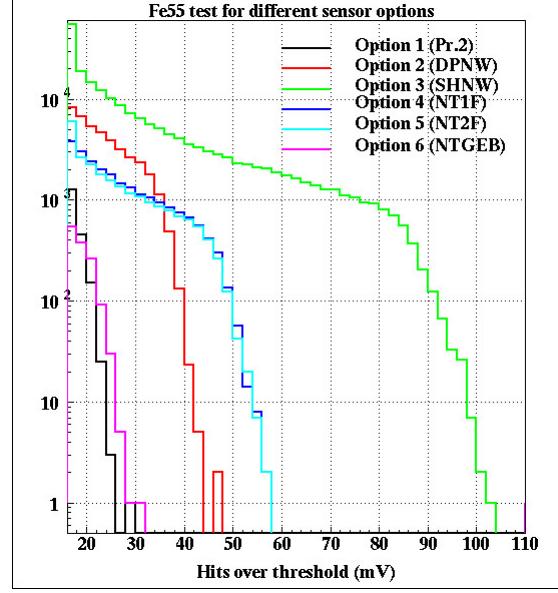


Figure 1.2: ^{55}Fe signal over threshold counts for 6 different sensor diode options, implemented in prototype 3. For comparison, option 1 is the same as in prototype 2.

1.2 ChronoPixel

1.2.1 Introduction

The ChronoPixel is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps of pixel hits by charged particles in a nominal ILC bunch train. This information is read out in the time interval between bunch trains. The ChronoPixel option for the ILC vertex detector was described in the ILC DBD [1]. By the time of the DBD, 2 prototypes had been built and tested, and the summary of test results was also presented in the DBD. The main points are:

- We have proven that we can record time stamps in every pixel with time resolution down to 150 ns.
- We have tested sparse readout, allowing to read only pixels with hits, thus reducing readout time to the level allowing readout of all pixels in the sensor in the intervals between bunch crossings.
- We have tested pulsed power for the analog part of the pixels and have proven [2] that turning power ON about 100 μs before bunch train and turning it off between bunch trains does not create any problems for threshold setting accuracy in the comparators.
- We have measured sensor noise level, including all pick-up and cross-talk. It was 24 e- r.m.s in prototype 1 and 26 e- r.m.s. in prototype 3, sensor option 3. Our specification was 25 e- noise.
- We have tested the idea of building all in-pixel electronics only from NMOS transistors, thus eliminating the need for a special process (deep p-well) to protect signal charge from parasitic collection

by in-pixel transistors. We have proven [3] that all NMOS electronics can be built in this way, and that this does not significantly increase the power consumption compared to CMOS electronics.

- We have tested the compensation of comparator offsets using analog calibration, when the value of the offset is stored as a voltage on the capacitor in each pixel. This has an advantage over digital calibration (where the offset value is stored as code in the special register) in that there are no discrete levels, and the accuracy of such a calibration scheme is not affected by the size of the register or the spread of the initial offsets.

1.2.2 Recent Milestones

- Test of prototype 2 revealed some problems. Possible solutions for these problems were discussed with Sarnoff engineers.
- A new contract with Sarnoff for the design of prototype 3 was signed in August 2013.
- Prototype 3 was manufactured in September 2014. Tests have shown that problems revealed in prototype 2 were solved.

The most recent report [4] on the status of ChronoPixel was presented by N. Sinev in June 2015 at Vertex2015 in Santa Fe, New Mexico.

1.2.3 Engineering Challenges

- The Vertex Detector for ILC faces many engineering challenges. The sensors need to be thinned to about $50\text{ }\mu\text{m}$ to reduce the amount of material in the detector. Support structures also need to be very light, but provide enough stability. Power dissipation of the entire detector should be small to be able to use only air cooling.
- If acceptable levels of the sensor diode capacitance can be achieved, the signal-to-noise ratio will improve. However, a lower value of the capacitance will make the pixels more sensitive to cross-talk through capacitive coupling. Reducing this coupling can be a challenge.
- Transition from small prototypes (few mm^2) to ILC detector size ($\approx 10\text{ cm}^2$) may meet additional problems. One of them will be the effect of Lorentz forces on the power supply buses, especially in the case of power pulsing. Power pulsing is the only way to achieve acceptable power dissipation in the vertex detector. However, it will generate varying Lorentz forces, acting on power supply lines. This may produce vibrations, which are unacceptable for the required spatial resolution of the detector.

1.2.4 Future Plans

- To achieve signal-to-noise ratio required for close to 100% signal registration efficiency. We have achieved very low sensor capacitance in prototype 3, and the signal-to-noise ratio with such a sensor capacitance for ^{55}Fe signal is about 60, however, for minimum ionizing particles the signal will be much smaller, depending on epitaxial layer thickness and charge collection efficiency. The signal-to-noise ratio for standard $7\text{ }\mu\text{m}$ epitaxial layer will be 20 if the charge collection efficiency is 100%, which is unlikely (we have not measured it yet). So we probably will need to increase the epitaxial layer thickness.

- To achieve the required pixel size (prototype 3 has $25\text{ }\mu\text{m}$ pixels, we would eventually like $15\text{ }\mu\text{m}$). It may require going to a technology with feature size less than 65 nm. There seems to be no problems in that, but both – good signal-to-noise ratio and pixel size requirements may be challenging.
- To achieve acceptable level of inter-pixel and digital-to-analog circuit cross talks and parasitic feedback.
- Depending on available funding, to build a complete sensor with a large enough area and full feature readout.

1.2.5 Applications Outside of Linear Colliders

With some modifications (for example, adding time-time converter) ChronoPixel architecture can be applied for any experiment requiring time stamping of individual hits – it may be HL-LHC, CLIC and so on.

1.3 CMOS

1.3.1 Introduction

CMOS Pixel Sensors (CPS) combine high granularity with low material budget and allow integrating the full signal processing circuitry on the sensor substrate. Being moreover cost effective because of the underlying industrial market, CPS are attractive for a wide range of applications. They are developed for the ILC since more than fifteen years and were shown to rather easily comply with the required spatial resolution and material budget of an ILC vertex detector and their radiation tolerance was observed to go well beyond the ILC requirements [5]. The state of the art of the technology is illustrated by the 400 ULTIMATE sensors operated in the STAR-PXL detector [6] at RHIC/BNL since 2014 and by the 10-100 times faster sensors developed for the upgrade of the ALICE Inner Tracker System (ITS) [7].

The achieved read-out speed of the CPS developed for an ILC vertex detector is already quite satisfactory [5], but is worth improving in order to facilitate track seeding at nominal ILC running conditions and to introduce a safety margin reflecting the uncertainties affecting the predicted beam related background rate.

The technology should in fact allow single bunch tagging, provided power consumption and, in turn, power cycling remain under control. The flexibility and detection performances of CPS are also indicating attractive perspectives for trackers, where relaxed constraints on the granularity may be exploited to find a well suited balance between speed, power saving and material budget. Ambitious goals for an ILC experiment may therefore be considered since their development may be carried out for numerous years until the design inputs of a vertex detector ought to be fixed.

The charged particle detection performances of CPS are currently essentially limited by manufacturing parametres. The latter evolve steadily since several years in a direction which makes them increasingly suited to the ILC vertexing and tracking. Besides achievements targetted with existing processes, the present R&D addresses also improvements expected from the evolution of the CMOS industry, mainly driven by the trend towards smaller feature sizes which would allow overcoming the conflict between the spatial resolution and the bunch tagging capability of CPS. This evolution is already well visible when comparing the performances achieved with the $0.35\text{ }\mu\text{m}$ process used for the STAR-PXL and the more recently addressed $0.18\text{ }\mu\text{m}$ process used for the ALICE experiment.

The R&D addresses presently four objectives :

- 2 or 3 CPS variants optimised for the different vertex detector layers :
 - inner layer : design privileging spatial resolution and read-out speed
 - outer layers : design privileging power saving, exploiting the less demanding spatial and time resolutions
- CPS adapted to tracking sub-systems, based on large pixels and privileging power saving
- ultra-light double sided ladders (called PLUME [8]) equipped with (identical or complementary) CPS on its two faces

1.3.2 Recent Milestones

Specific CPS are being developed since 2011 to equip the Inner Tracking System (ITS) of the ALICE experiment in the framework of its upcoming upgrade. The surface to cover exceeds 10 square meters, i.e. nearly two orders of magnitude more than the STAR-PXL or an ILC vertex detector.

Two CPS are being developed, differing by their read-out architectures. The most conservative of them, called MISTRAL-0, reproduces the ULTIMATE sensor equipping the STAR-PXL and is thus based on a synchronous, rolling-shutter, read-out. The concept underlying the other sensor, called ALPIDE, features an asynchronous read-out based on a token ring relying on a pre-amplifier/shaper/discriminator chain implemented in the pixel array. It allows for a few microsecond read-out time and for a power consumption below 50 mW/cm^2 . These performances were demonstrated in 2014 [9] on a real scale prototype.

MISTRAL-O relies on large pixels to achieve a $20\text{ }\mu\text{s}$ read-out time and a power consumption below 100 mW/cm^2 while providing $10\text{ }\mu\text{m}$ resolution with its integrated binary encoding. Its read-out architecture was validated in 2014 with a real scale prototype [10] featuring 160,000 small ($22 \times 33\text{ }\mu\text{m}^2$ large) pixels. More recently [11], prototypes composed of three times larger pixels were tested on beam and demonstrated satisfactory charged particle detection performances at 30°C and after radiation loads exceeding those expected at the ILC by several orders of magnitude.

In summary, the full chain of the ULTIMATE sensor has been reproduced in a $0.18\text{ }\mu\text{m}$ process with twice faster read-out frequency and improved sensitive volume (epitaxial layer) characteristics. The optimisation of this design for tracking systems, using relatively large pixels, is validated.

Moreover, a small prototype of a sensor optimised for the vertex detector outer layers was realised in the $0.18\text{ }\mu\text{m}$ process mentioned earlier. Low power is achieved using enlarged, $35\text{ }\mu\text{m}$ pitch, square pixels and the spatial resolution is kept below $4\text{ }\mu\text{m}$ by integrating a 3-bit ADC in each pixel. The approach was validated in the former $0.35\text{ }\mu\text{m}$ process with the MIMOSA-31 prototype, but the ADCs had to be kept at the sensor periphery because of process limitations, translating into larger power consumption and slower read-out. Laboratory tests of the new prototype were performed since last Summer, showing satisfactory noise performances at nominal read-out speed, thus validating the concept.

1.3.3 Engineering Challenges

Squeezing the material budget of the double-sided PLUME ladders below $0.3\% X_0$ will be the main engineering challenge, as the design has to account for the necessity to power pulse the ladders in the strong experimental magnetic field. Power pulsing seems mandatory in case of continuous read-out as the sensor design is unlikely to end up with a power density suppressed enough to avoid switching the sensors off in between consecutive trains. The possibility to introduce micro-channel cooling in the ladders will be studied in order to mitigate the power pulsing requirements.

1.3.4 Future Plans

Several development directions will be pursued in the coming years, to improve the performances of the CPS and to assess the added value of the ultra-light double-sided ladder concept.

The development of CPS will mainly aim at realising a prototype of a new sensor series, called IBISCUS¹, composed of pixels with less than 20 μm pitch providing a read-out time of about 1 μs (using a token ring read-out).

The R&D on the other CPS versions mentioned earlier (for the vertex detector outer layers and for tracking sub-systems) will be pursued with coarser priority. Besides these continuous read-out architectures, a sensor composed of 4 μm pitch square pixels with analog output, foreseen to be read out inbetween trains like FPCCDs, will also be studied.

Different versions of double-sided ladders will be realised and their performances evaluated in terms of spatial accuracy, including alignment issues, and in terms of stability against power pulsing, possibly in a high magnetic field.

The two main alternative design options are going to be compared to each other. One version is based on a high precision sensor ($< 3 \mu\text{m}$) on one side featuring $\lesssim 50 \mu\text{s}$ integration time, while a fast sensor ($\sim 2 - 3 \mu\text{s}$) equips the other side which provides $\sim 5 \mu\text{m}$ resolution. The other version is based on a single sensor equipping both ladder sides, which offers $\sim 4 \mu\text{m}$ spatial resolution and about 5 μs time resolution.

1.3.5 Applications Outside of Linear Colliders

CPS developed at IPHC in perspective of the ILC are used in several devices, as illustrated by the non-exhaustive list below:

- Several high precision transparent beam telescopes, adapted to ($< 1 \text{ GeV}$) electron beams, are equipped with the MIMOSA-26 or -28 (alias ULTIMATE) sensors
- The first generation of sensors with full on-chip signal processing developed at IPHC (in a 0.35 μm CMOS process) was applied to the STAR-PXL detector at RHIC, which completed successfully its first data campaign in 2014 and has started its 2015 run
- The upgraded ALICE ITS will be the next equipment based on CPS; it will provide insight of a token ring architecture pioneering the one considered for the IBISCUS chip mentioned above; it will also provide running experience with a tracker based on CPS
- The Micro-Vertex Detector of the CBM experiment at FAIR/GSI will also be based on the CPS presently developed for the ALICE-ITS upgrade
- The sensors were, or are, being applied outside of subatomic physics. They were for instance used in the FIRST experiment at GSI, for hadrontherapy monitoring; they are presently developed for soft X-Ray imaging and brain-imaging.

Sensors featuring pixels about 5 times larger than those equipping the STAR-PXL were fabricated in 2014, with different pixel design optimisations. Such large pixels are more exposed to the effects of signal charge recombination. The purpose of the paper is, among others, to show that the charge particle detection efficiency is not degraded, even after radiation loads representative of upcoming trackers, such the upgraded ALICE Inner Tracking System. The charged particle detection performances of these large pixel

¹standing for Ilc Bunch Identifying Sensor Compatible with Ultraprecise Spatial resolution

CPS prototypes with integrated signal processing and binary outputs were studied by exposing the sensors to a 450 MeV electron beam. The results obtained will be exposed and shown to validate the concept for its evolution towards large area tracking devices, with the perspective of integrating logical strips in the sensor.

1.4 DEPFET Pixel Sensors

1.4.1 The DEPFET Collaboration

The DEPFET collaboration consists of nearly 100 members from 13 institutes. It currently takes responsibility for the following work packages:

Mechanics The DEPFET ladder integrates the support structure with the sensor wafer using state-of-the-art silicon processing technology. Read-out electronics and signal routing are integrated on the silicon wafer. The resulting all-silicon ladder is fully self-supporting. The mechanical properties of thin ladders in a realistic environment are studied in detail using detailed models (mock-ups) for Belle II and the ILC .

Cooling The DEPFET cooling concept for Belle II relies on two-phase CO₂ cooling for the end-of-ladder. The sensor is cooled moreover with a forced flow of cold gas. The CO₂ cooling plant is developed by KEK, while the design for the cooling block/support structure is performed within the collaboration. The impact of the linear collider cooling strategy - based on reducing the power dissipated using a pulsed power supply to the detector and cooling through a forced air flow - is studied. A novel cooling strategy for future applications based on micro-channels in the sensors is being evaluated in the collaboration. Solutions for monitoring of environmental parameters are being developed.

Ancillary ASICs The operation of a DEPFET detector requires ancillary electronics in the form of a read-out ASIC (the Drain Current Digitizer), a steering ASIC (SWITCHER) and on-detector ASICs for digital data processing (DHP). These ASICs are developed within the collaboration.

Data Acquisition and Trigger The development of off-detector electronics to process the data from the Belle II vertex detector.

Characterization of prototypes, laboratory and beam tests This work package has contributions from nearly all institutes involved in the DEPFET collaboration.

Currently, the construction of the Belle II vertex detector [12] is the main focus of the collaboration. The requirements of the Belle II vertex detector are similar to those of the ILC, and more stringent in some aspects. The Belle II construction project therefore has considerable synergy with developments for a future linear collider. The LC-specific effort is focused on the development of small-pixel devices and the design of a forward vertex detector. We envisage that after the installation of the Belle II detector (2016) the balance between both projects is restored.

1.4.2 Introduction

The DEPFET technology implements amplification within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted high-resistivity silicon wafer. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate. The amplified signal is extracted from the pixel matrix by a numbers of

Table 1.1: Comparison of ILC and Belle II requirements of a vertex detector

	ILC	Belle II
occupancy	0.13 hits/ $\mu\text{m}^2/\text{s}$	0.4 hits/ $\mu\text{m}^2/\text{s}$
radiation	< 100 krad/yr	> 1 Mrad/yr
	$10^{11} \text{ MeVn}_{\text{eq}}/\text{yr}$	$2 \times 10^{12} \text{ MeVn}_{\text{eq}}/\text{yr}$
duty cycle	1/200	1
frame time	25 – 100 μs	20 μs
momentum range	100 keV – 500 GeV	$<\sim 1 \text{ GeV}$
angular acceptance	6°– 174°	17°– 150°
spatial resolution	excellent: 3 – 5 μm	moderate
pixel size	$20 \times 20 \mu\text{m}$	$50 \times 75 \mu\text{m}$
material budget	0.15% X_0/layer	0.21% X_0/layer

ASICs [13, 14] mounted directly on the sensor: The SWITCHER, Drain Current Digitizer (DCD) [15, 16] and Data Handling Processor (DHP) [17].

The DEPFET in-pixel amplification allows for a comfortable signal-to-noise ratio with a very thin active detector. The reduced sensor thickness of 75 μm for Belle II, 50 μm for the Linear Collider, is the key to remain within the material budget of 0.15% of a radiation length per layer. DEPFET prototypes with $20 \times 20 \mu\text{m}^2$, small enough to meet the stringent spatial resolution specifications of the ILC, have successfully been operated in beam tests [18, 19]. The DEPFET matrix is read out in rolling shutter mode at a rate of 100 ns/row. For the column depths relevant for the ILC and Belle II a frame rate of several tens of μs is achieved [20]. The expected performance of a DEPFET-based vertex detector meets the specifications drawn up by the ILD experiment. DEPFET is also considered as a back-up solution to the SiD concept, in case the single bunch crossing time stamping proves to be out of reach.

1.4.3 Recent Milestones

The concept of a DEPFET active pixel detector for vertex detection at collider experiments was initiated in the linear collider community (for TESLA). The operation principle was extensively proven [18, 19] on small-scale prototypes. A recent reassessment of the DEPFET potential for a linear collider at the energy frontier is found in [20] and in the report [21] for the ECFA detector R&D review in 2014. A large-scale, 75 μm thin Belle II ladder with the ancillary ASICs integrated on the sensor was successfully submitted to a test in an electron beam at DESY in January 2014[22].

The first full-scale DHP prototype was implemented in IBM 90 nm CMOS technology. As this technology was discontinued, more recent designs were submitted in the TSMC 65 nm CMOS process. DHPT v.1.0 comprises temperature independent current references, 11 bias 8-bit DACs with current output, an integrated temperature measuring system and JTAG control. This design has been successfully tested during early 2014[13].

1.4.4 Engineering Challenges

Vertex detector ladders with a thickness of several tens of microns and a spatial resolution of well below 10 μm require very robust mechanical properties. The power generated by the sensors and ASICs must be removed with the smallest impact on the detector material. Measurements on thin ladders under a realistic load, including pulsed powering according to the ILC beam structure, prove the excellent mechanical

properties of the all-silicon ladder [23].

1.4.5 Future Plans

Currently, the construction of the Belle II vertex detector (to be installed by 2016 for the first physics run in 2017) implies a large effort of R&D, including:

- Develop the die-attach technology in a controlled atmosphere required for the mounting of passive components on the DEPFET active pixel detector ladders. The first milestone is a fully integrated electrical prototype based on the EMCM.
- First tests that will determine if all the ASICs on the ladder are fully functional
- The integration of read-out and steering ASICs on the pixel sensor to be performed using a flip-chip technique and so-called bump-bonding, using microscopic solder balls.
- The production of the Belle II vertex detector modules, a joint effort of the DEPFET collaboration
- The test of the last version of the DHP chips

In the near future we hope to characterize the performance of a thin ILC-design prototypes with pixels of $20 \times 20 \mu\text{m}^2$

- Perform an engineering design for a DEPFET all-silicon module with the required petal geometry
- A detailed characterization of the response of the device
- Design of the ancillary ASICs, taking full responsibility for future design cycles of the Front End read-out chip, the Drain Current Digitizer (DCD) that is relevant to the ILC and a Belle II upgrade. This chip converts the analog signal from the detector to digital and has a crucial impact on the detector performance.

In the longer term the DCD and DHP are envisaged to evolve into a single chip. Being large arrays of DEPFET pixels a promising technology for the vertex detector of the planned ILC, adaptation of the DCD and DHP chips must also be done.

In the near future we hope to characterize the performance of ILC design prototypes with pixels of $20 \times 20 \mu\text{m}^2$. Important experience is furthermore gained with the thermal and mechanical properties of ultra-thin ladders. Measurements on thin ladders under a realistic load, including pulsed powering according to the ILC beam structure, prove the excellent mechanical properties of the all-silicon ladder. A complete mock-up for the innermost disks is under construction.

1.4.6 Applications Outside of Linear Colliders

The concept of a DEPFET active pixel detector for vertex detection at collider experiments was initiated in the linear collider community (for TESLA). The election of DEPFET technology for the Belle II detector therefore represents an important spin-off of linear collider detector R&D. DEPFET is also considered a strong candidate technology for the vertex detector at a future circular collider (<http://cepc.ihep.ac.cn/preCDR/volume.html>). DEPFET detectors are furthermore used for X-ray imaging at the XFEL [24]. Future space missions envisage the use of DEPFET sensors [25]. Their use in microscopy is being studied.

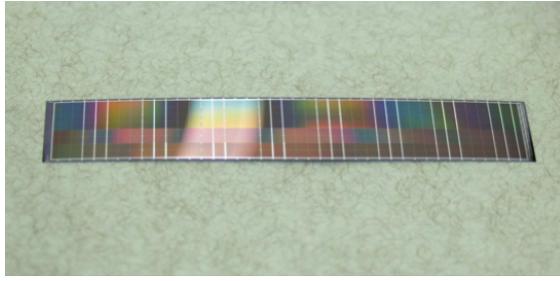


Figure 1.3: Real size FPCCD sensor thinned down to 50 μm

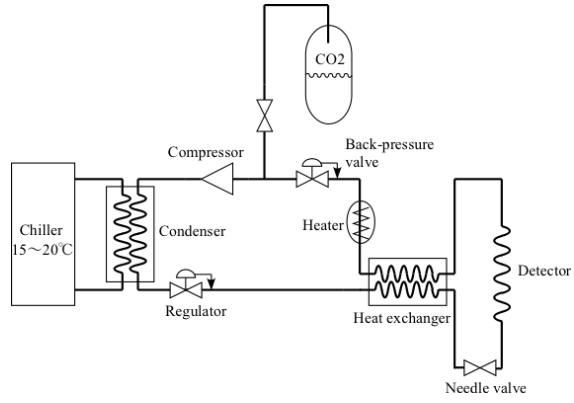


Figure 1.4: A simplified schematic diagram of the two-phase CO_2 cooling system

1.5 FPCCD

1.5.1 Collaborating Institutions

1.5.2 Introduction

Fine pixel CCD (FPCCD) is one of the candidate sensor options for the vertex detector of the ILD detector at the ILC [26, 27, 28]. In the present design, FPCCD sensors for the innermost layer of the vertex detector have a pixel size of 5 μm and a fully depleted epitaxial layer with a thickness of 15 μm . Because of the small size of the pixels, the occupancy is acceptably low even if the hits are accumulated for one nominal ILC bunch train ($\approx 1 \text{ ms}$). The efforts of the FPCCD collaboration are currently focused on pixel characterization and development, while we also pursue developments to the cooling system, electronics downstream of ASICs and the reconstruction software [29].

1.5.3 Recent Milestones

R&D activity for the FPCCD vertex detector at present is mainly focused on FPCCD sensors and a detector cooling system using 2-phase CO_2 . One of the achievements of FPCCD sensors after DBD is the fabrication of real size ($12.3 \times 62.4 \text{ mm}^2$) sensors with 50 μm total thickness. Figure 1.3 shows the real size prototype sensor. It has 8 readout nodes, and each channel has different pixel sizes of 12 μm , 8 μm , and 6 μm .

We have started a neutron damage test using small ($6 \text{ mm} \times 6 \text{ mm}$) FPCCD prototypes [30]. A prototype sensor was irradiated by a neutron beam of few tens of MeV at the CYRIC facility of Tohoku University. The detailed analysis on the irradiated sensor is still on-going. In order to increase the radiation immunity of FPCCD sensors, particularly to reduce the transfer inefficiency due to radiation damage, the sensors should be cooled down to -40 $^\circ\text{C}$. We have started R&D on a two-phase CO_2 cooling system for this purpose. There are several examples of utilizing two-phase CO_2 cooling systems for high energy physics experiments. For these cases, the CO_2 coolant is circulated using liquid pumps. This method is, however, not so efficient for very low temperature cooling of -40 $^\circ\text{C}$. Therefore, we adopted a CO_2 gas compressor for the circulation of CO_2 coolant. Figure 1.4 shows a simplified schematic diagram of the system. A prototype system has been constructed, and cooling between -40 $^\circ\text{C}$ and +15 $^\circ\text{C}$ has been successfully demonstrated using this system.

1.5.4 Engineering Challenges

In the present design of the ILD vertex detector, two sensor layers are mounted on both sides of a light-weight ladder of 2 mm thickness. Our goal of the material budget of this ladder is $0.3\% X_0/\text{ladder} = 0.15\% X_0/\text{layer}$. This goal would not be so easy to accomplish, and we need a lot of R&D effort. The ladders have to be cooled down to -40°C . We plan to achieve this cooling by heat conduction to the end-plate on which thin cooling tubes for 2-phase CO_2 are attached. The design of this structure is not trivial, and we need R&D including thermal simulation. There are challenges both with the mechanical structure and the electronics circuit for the ladder R&D. We have not started this effort yet.

1.5.5 Future Plans

We have been doing our R&D on the FPCCD vertex detector based on a Grant-in-aid for science research which expires at the end of FY2015. By that time, we plan to carry out the following R&D items:

- Characterization of FPCCD sensors including beam tests and radiation damage tests
- Development of FPCCD sensors with the pixel size of $5\ \mu\text{m}$, which is our ultimate goal
- Construction of prototype ladders for inner layers
- Development of readout electronics downstream of ASICs

If new funding is secured in future, the following R&D items have to be done:

- Development of larger FPCCD sensors and prototype ladders for outer layers
- Development of readout electronics which can fit in the small space of real experiment
- Construction of a real size engineering prototype and its cooling test

1.5.6 Applications Outside of Linear Colliders

Because of the relatively slow readout speed, the application of FPCCD sensors to other high energy physics experiments would be limited. However, high spatial resolution of small pixel size must be applicable to measurements of X-ray imaging. Two-phase CO_2 cooling system can be applied to any other detectors which require efficient cooling between -40°C and near room temperature. Our system, which uses a CO_2 gas compressor, has a great advantage for low temperature operation near -40°C compared with systems using liquid pumps for circulation.

1.6 SOI

1.6.1 Introduction

1.6.2 Recent Milestones

At present, major issues in the SOI pixel development are “back-gate effect”, “hole trap under the transistors by radiation,” and “sensor-circuit cross talks” as shown in Figure 1.5. For these, we have been developing a double SOI technology. The developed double SOI wafer has an additional middle-SOI(Si) layer under the transistors. The conduction layer of the middle-SOI can solve all the three issues. We could successfully process the double-SOI wafer (Figure 1.6). Threshold shift by radiations is successfully recovered by applying compensating voltage to the middle SOI layer (Figure 1.7).

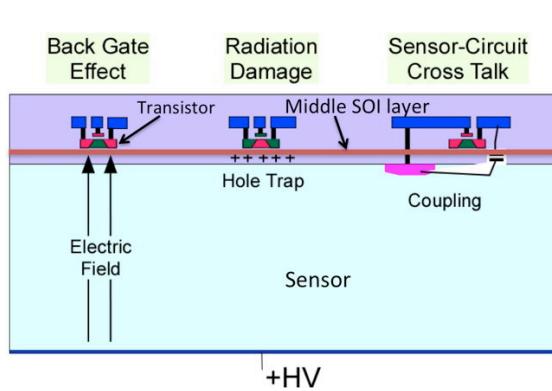


Figure 1.5: Major issues in the SOI pixel detector and introduction of a middle-SOI layer

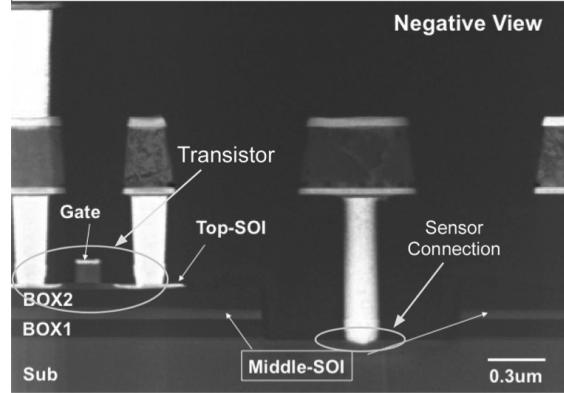


Figure 1.6: Cross section of the double SOI chip after processing

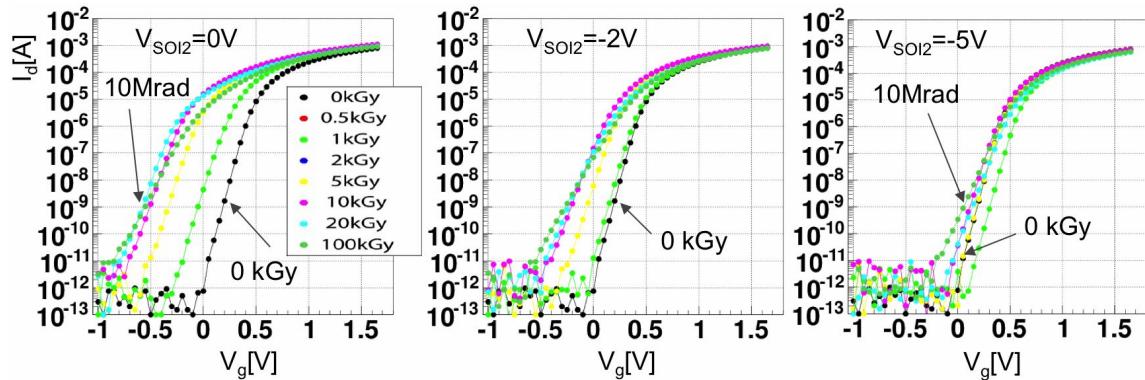


Figure 1.7: Threshold shift recovery by applying compensating voltage (V_{SOI2}) to the middle Si layer

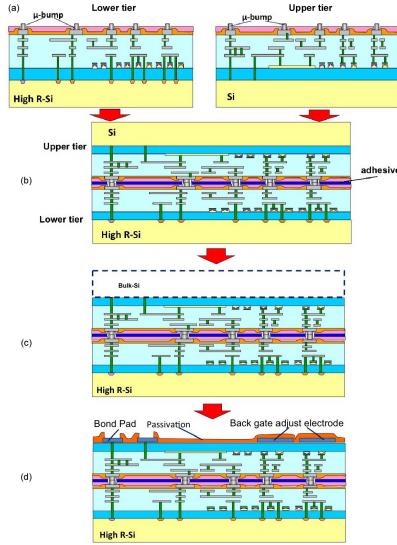


Figure 1.8: Micro-bump 3D integration process flow of the SOI pixel

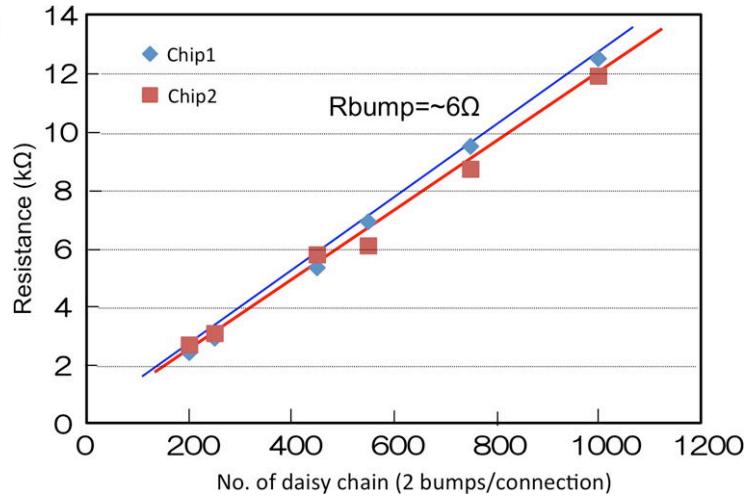


Figure 1.9: Resistance of micro-bump daisy chain between upper and lower tiers

1.6.3 Engineering Challenges

The impact parameter resolution for the ILC vertex detector is required to be a few μm . This means the pixel size must be less than about $20 \mu\text{m}^2$. On the other hand, each pixel must register arrival time of the hits during bunch train, which requires many transistors and capacitors to be located in each pixel. A solution to this is 3D vertical integration of the circuit layers. SOI technology is ideally suited for 3D integration, since the thinning is stopped at the buried oxide (BOX). We already tried 3D SOI pixel chip in collaboration with T-Micro Co. Ltd. The process flow of micro-bump 3D connection is shown in Figure 1.8. This process achieves a resistance of ($\sim 6 \Omega/\text{bump}$) between upper and lower tiers for 1,000 daisy chain (2,000 bumps) as shown in Figure 1.9. However, to achieve the density of digital circuitry necessary for ILC operations, 32 nm technology may be necessary for the upper tier in the ILC. This requires bonding of two different technology wafers. The 3D integration of different technology wafers (or chips) is still an engineering challenge.

1.6.4 Future Plans

Detector R&D plans for the coming years; We are planning following items for the coming year.

- Sep. 2014 : Complete architecture study for the ILC pixel detector.
- Mar. 2015 : Design and fabrication of first test chip for the ILC.
- Dec. 2015 : Beam test of the test chip.

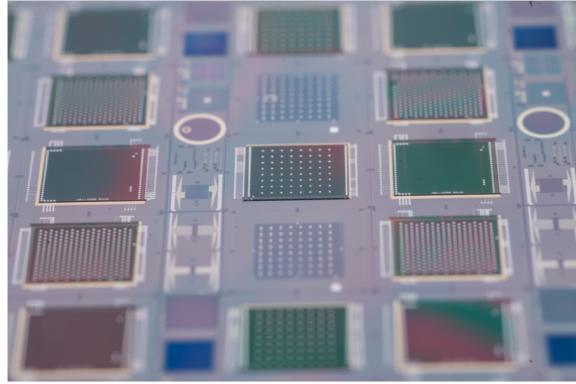


Figure 1.10: 3D chips placed on BNL sensor wafers. VIP is middle left and right

1.7 3D Pixel Development

1.7.1 Introduction

This R&D area covers sensors and electronics integrated utilizing 3-dimensional electronics technology. This technology is distinct from 3D sensors and builds on efforts in the electronics industry to stack multiple layers of electronics to form dense assemblies of complex devices. It is important for Particle Physics in that it allows very fine pitch ($4\text{ }\mu\text{m}$) integration of sensors with multiple layers of electronics, allows interconnection to both the top and bottom of devices, and provides techniques for low mass, thinned devices. The interconnection of top and bottom means that sensors can be bonded to complex electronics with no wasted area for interconnect and optimal delivery of power and ground.

1.7.2 Recent Milestones

We have completed our multi-year effort to demonstrate commercial 3D technology. This consists of two tiers of $0.13\text{ }\mu\text{m}$ CMOS interconnected with Direct Oxide Bonding (DBI) technology and access using Through-Silicon-Vias (TSV). The DBI bonds are at $4\text{ }\mu\text{m}$ pitch. Fermilab sponsored the first 3D multi-project run for Particle Physics. The wafers were delivered last summer. Fermilab had three chips on the run: VICTR – a CMS track trigger chip, VIPIC – an X-ray imaging chip, and VIP – an ILC vertex chip. Tests of the VIPIC and VICTR have shown working devices. Tests for the VIP chip were delayed due to lack of funding and personnel. We have recently restarted this work and initial tests are promising with the readout token successfully passed through the VIP.

In addition to the development of the 3D chips we have also explored the use of DBI to connect the 3D electronics with sensors. Brookhaven Laboratory fabricated a sensor wafer with regions that mate to the VIP, VIPIC and VICTR chips. The chips are ground to expose the top TSVs and contacts are deposited. The assembly is then attached to a handle wafer and the TSVs which project from the other side are exposed. Wafers are then process for DBI bonding and individual die from the 3D wafer are bonded to the sensor wafer. Finally the top “handle” silicon is ground and etched to reveal the previously formed contacts. The total thickness of the readout at the end of this process is about $25\text{ }\mu\text{m}$ (Figure 1.10). These wafers were received at the end of March 2014 and are being tested. Due to the fact that contacts to a 3D assembly can be made to the body of the die, rather than its edge, no space needs to be reserved for wire bond contacts

at the edge. This raises the possibility of fabricating large, complex pixel detector arrays of 4-side butted devices using sensors with active edges. We are in the process of demonstrating this technology utilizing active edge sensors fabricated at VTT and using wafer-to-wafer bonding to a 3D readout wafer. The active edge wafers are based on a silicon-on-insulator stack and thus can be fabricated with essentially arbitrarily thin sensors, in this case 200 μm . Sensor and dummy readout wafers have been fabricated and a test wafer is being etched at SLAC. We expect to have DBI bonded assemblies this summer.

1.7.3 Engineering Challenges

Major engineering challenges include:

- Development of widely commercially available 3D technologies. Based partly on our development the silicon brokers CMP, CMC, and MOSIS now include 3D multi-project runs as part of their standard offerings.
- Development of high yield 3D bonded chip-to-wafer devices. This is the subject of our active edge project.
- This development shares with other vertexing technologies the problems of low mass mechanical support, power delivery, and cooling. An SOI-based device can be made thin without special effort. Such thinned device will need low mass backing hybrid circuitry, presumably flex on carbon fiber or a similar technology

1.7.4 Future Plans

- Complete the 3D active edge project
- Apply our concepts to x-ray imaging devices
- ILC developments would await renewed funding in the US.

1.7.5 Applications outside of Linear Colliders

As stated above the technology is already being developed for CMS and x-ray imaging applications. The large area sensor concept is applicable for a variety of focal plane array concepts.

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1.8 CLICpix

1.8.1 Introduction

The precision physics needs at the CLIC TeV-scale linear electron-positron collider require a vertex-detector system with excellent flavour-tagging capabilities through a measurement of displaced vertices in an environment with high rates of beam-induced background events [37]. As a result, the CLIC vertex-detector system needs to have excellent spatial resolution ($3\text{ }\mu\text{m}$), full geometrical coverage extending to low polar angles, extremely low material budget ($0.2\% X_0$ per layer), low occupancy facilitated by time-tagging (10 ns precision), and sufficient heat removal from sensors and readout. A concept based on hybrid pixel-detector technology is under development for the CLIC vertex detector. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin planar sensors or active HV-CMOS sensors via low-mass interconnects. The power dissipation of the readout chips is reduced by means of power pulsing, allowing for a cooling system based on forced gas flow. Through-Silicon Via (TSV) vertical interconnects remove the need for wire bonding connections on the side of the readout ASICs and therefore allow for an efficient tiling to form larger modules with minimal inactive areas.

1.8.2 Recent Milestones

A broad hardware R&D program is in place, addressing the challenges for the CLIC vertex detector in an integrated approach [38]. Recent achievements in the sensor and readout domain include:

Hybrid pixel assemblies with ultra-thin planar sensors Planar pixel sensors with $55\text{ }\mu\text{m}$ pitch and different thicknesses ($50\text{--}300\text{ }\mu\text{m}$) were procured from different vendors and bump-bonded to Timepix [39] readout ASICs (100 and $700\text{ }\mu\text{m}$ thickness). Slim-edge sensor designs are compared to designs with active edges. Preliminary beam-test results show very good efficiencies in both cases, extending beyond the edge pixels [40]. For $50\text{ }\mu\text{m}$ sensor thickness and nominal readout parameters, the fraction of multi-pixel clusters is approximately 20%. Single-point resolutions of approximately $3\text{ }\mu\text{m}$ have been extracted for clusters of two pixels using charge interpolation and taking into account non-linear charge sharing.

CLICpix demonstrator ASIC A CLICpix demonstrator chip has been produced in 65 nm CMOS technology, including a 64×64 pixel matrix and power-pulsing capability [41]. The pixel size is $25\text{ }\mu\text{m}\times 25\text{ }\mu\text{m}$. Simultaneous 4-bit Time-Of-Arrival (ToA) and Time-Over-Threshold (ToT) measurements are implemented in each pixel, allowing for a front-end time slicing with approximately 10 ns and for measuring the charge to improve the position resolution through interpolation. The full chip can be read out in less than $800\text{ }\mu\text{s}$ (for 10% occupancy), using a 320 MHz readout clock and zero suppression. The power consumption of the chip is dominated by the analog frontend with a peak power corresponding to 2 W/cm^2 . The total average power consumption can be reduced to a value below the target of 50 mW/cm^2 by means of power gating for the analog part and clock gating for the digital part. Readout tests have confirmed that the CLICpix demonstrator chip is fully functional and the power consumption and performance are in agreement with simulations [42]. Hybrid modules of CLICpix ASICs with planar slim-edge sensor prototypes are currently in production.

Capacitively coupled active HV-CMOS sensors Hybrid assemblies of CLICpix prototype chips with CCPDv3 active sensors have been produced and tested. The sensors are implemented in a 180 nm high-voltage CMOS process [43]. A deep n-well above the low-resistivity (few Ωcm) p substrate surrounds low-voltage p-wells and acts as the signal collecting electrode. A nominal operation voltage

of -60 V at the n-well results in a depletion layer of approximately 10–20 μm in the p substrate. The fast drift signal collected in this depletion layer passes through a two-stage transimpedance amplifier in each pixel and the resulting voltage signal is capacitively coupled to the CLICpix ASIC through a layer of glue a few microns thick. Laboratory tests with radioactive sources show a good signal-to-noise performance for the active sensor output. Preliminary test-beam results with CLICpix-CCPDv3 assemblies suggest a detection efficiency of > 99% for minimum ionising particles and a high fraction of single-pixel clusters with a position resolution of approximately 7 μm , as expected for 25 μm pixel pitch.

Through Silicon Vias (TSV) A “via last” TSV process developed in collaboration with CEA-LETI has demonstrated the feasibility of TSVs on functional readout ASICs from the Medipix/Timepix chip family [44]. The project uses Medipix3 readout wafers produced in 130 nm CMOS technology. The wafers are thinned to 120 μm and the resulting vias have a diameter of 60 μm . An ongoing continuation of the TSV project aims at producing TSVs in Timepix3 ASIC wafers thinned to 50 μm .

1.8.3 Engineering Challenges

The detector performance requirements lead to challenging constraints for the mechanical and electrical integration of the vertex-detector components and its cooling system. An integrated approach is followed, addressing several of the critical R&D issues in these domains:

Power delivery and power pulsing A low-mass power-pulsing and power-delivery system optimised for the small duty cycle of the CLIC machine has been developed [45]. Controlled current sources deliver a low and almost constant current (< 300 mA per ladder) into the vertex region through low-mass cables. The energy needed by the readout ASICs during the time of the collisions and detector readout is stored locally in silicon capacitors. Low-dropout regulators provide the necessary stability of the output voltage for the analog ($\Delta V \approx 16\text{mV}$) and the digital part ($\Delta V \approx 70\text{mV}$) of the readout ASICs. Prototypes have been tested successfully with dummy loads emulating the power consumption of the 12 readout ASICs in a half ladder. The total contribution of the powering infrastructure to the material budget of each barrel layer is approximately 0.1% X_0 . It is expected to decrease to less than 0.05% X_0 with evolving silicon-capacitor technology.

Cooling Even with power pulsing a total power of approximately 500 W will be dissipated in the vertex detectors alone. To limit the amount of material in the vertex-detector region, a cooling system based on forced air flow is under development [46]. Finite-element Computational Fluid Dynamics (CFD) simulations show that air cooling is feasible. For a mass flow of 20 g/s, the temperature increase in the vertex detector is limited to approximately 40 °C. The proposed cooling scheme is being validated in thermal mockups. Preliminary results confirm the validity of the simulations.

Mechanical supports The low overall material budget leaves only about 0.05% X_0 per detection layer for mechanical supports. Prototypes based on Carbon-Fibre-Reinforced Polymers (CFRP) are under study [47]. Bending-stiffness calculations have been validated in finite-element simulations and with bending tests. Measurements within an air-cooling mockup show that the air-flow induced vibrations are at an acceptable level of approximately 1 – 2 μm RMS amplitude for the direction perpendicular to the detector plane and at nominal flow conditions.

Assembly and access scenarios Assembly and access scenarios for in-situ testing have been developed, taking into account the constraints from the surrounding detector elements [47]. Realistic cabling layouts are proposed and evaluated in terms of their impact on the global and local material budget.

1.8.4 Future Plans

The technical development programme for the CLIC vertex detector aims at building demonstration modules for the main components of the vertex detector system in time for the next update of the European Strategy for Particle Physics in 2018/19. To reach this medium-term goal, several technology prototypes are under development. Ultra-thin edgeless hybrid pixel assemblies with Timepix3 readout ASICs (including ASICs thinned to 50 µm and processed with TSVs) are currently in production. The next version of the CLICpix demonstrator ASIC (CLICpix2) is foreseen to be produced in the second half of 2015. It contains a larger pixel matrix (128×128) and higher dynamic range (8-bit ToA and 5-bit ToT). Slim-edge and edgeless sensors matching the 128×128 CLICpix2 footprint have already been produced and an improved version of the CCPD active HV-CMOS sensor will be submitted for production by the end of 2015.

1.8.5 Applications Outside of Linear Colliders.

The CLIC vertex-detector R&D shares its main challenges of simultaneously achieving small pixel pitch, low material budget and fast timing with other future pixel detector projects, such as the developments for the upgrades of the LHC detectors for high-luminosity operation or for future circular colliders. Synergies with these projects are exploited for example in the context of the RD53 collaboration for 65 nm hybrid readout ASICs [48] and via the AIDA2020 project for Advanced European Infrastructures for Detectors at Accelerators [49]. Moreover the CLICpix ASIC is derived from the Timepix/Medipix family of hybrid readout ASICs [50], which have a wide range of applications in medical imaging and material science.

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
ChronoPix	University of Oregon Yale University Sarnoff Corporation	ChronoPix is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps per pixel during the bunch train. Hits are read out in the time between bunches.	April 2014: Device tests of prototype 2 inform the design of prototype 3 to be submitted to foundry	Prototype 3 was manufactured in September 2014. Tests have shown that problems revealed in prototype 2 were solved.
CMOS MAPS	IPHC Strasbourg DESY, Hamburg University of Bristol University of Frankfurt	The CMOS pixel sensor uses as a sensitive volume the 10–20 μm thin high-resistivity epitaxial Si-layer deposited on low resistivity substrate of commercial CMOS processed chips. The generated charge is kept in a thin epi-layer atop the low resistivity silicon bulk by potential wells that develop at the boundary and reaches an n-well collection diode by thermal diffusion.	2016 : production of CPS for the ALICE-ITS upgrade 2018/19 : production of CPS for the micro-vertex detector of the CBM experiment at FAIR/GSI 2018/19 : validation of light double-sided ladder concept combining highly granular sensors on one side with timestamping sensors on the other side < 2020 : validation of power pulsing of double-sided ladders inside a high magnetic field 2022/23 : finalisation of the R&D on various CPS adapted to the different layers of a very high performance vertex detector at the ILC	Until 2018-2019: Development and production of CPS for the ALICE-ITS and CBM-MVD Development of various CPS optimised for the different layers of a vertex detector at the ILC, with emphasis on bunch tagging Development of low material double-sided ladders
DEPFET	University of Barcelona, Spain University of Bonn, Germany Heidelberg University, Germany Giessen University, Germany University of Göttingen KIT Karlsruhe, Germany IFJ PAN, Krakow, Poland MPI Munich MPG HLL, Munich, Germany Charles University, Prague, Czech Republic IFIC, CSIC-UVEG, Valencia, Spain DESY, Hamburg, Germany IFCA, CSIC-UC, Santander, Spain	The DEPFET technology implements a single active element within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted, detector-grade bulk silicon. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate.	2014: Full-scale 75 μm thin Belle II ladder in beam test at DESY	Development of die-attach technology Full-scale test of all ASICs on ladder Integration of read-out and steering ASICs on pixel sensor using flip-chip technique and microscopic solder ball bump-bonding Production of Belle II vertex detector modules Tests of the last version of the DHP chips Engineering design for all-silicon module with petal geometry required for ILC Detailed characterization of device response Design of ancillary ASICs, taking full responsibility for future design cycles of the FE read-out chip, called Drain Current Digitizer
FPCCD	KEK Shinshu University Tohoku University JAXA, Japan Aerospace Exploration Agency	Fine Pixel CCD sensors have pixel sizes of 5 μm and a fully depleted epitaxial layer with a thickness of 15 μm	Fabrication of real size (12.3 mm \times 62.4 mm) sensors with 50 μm total thickness Neutron irradiation of a small (6 mm \times 6 mm) FPCCD sensor Construction of a prototype cooling system and demonstration of cooling between -40°C and $+15^\circ\text{C}$	Characterization of FPCCD sensors including beam tests and radiation damage studies Development of FPCCD sensors with a pixel size of 5 μm Construction of prototype ladders for the inner layers of a vertex detector Development of readout electronics downstream of ASICs Development of larger FPCCD sensors and prototype ladders for outer layers Development of readout electronics with a small footprint Construction of a real size engineering prototype and cooling test
3D Pixels	Brown University Cornell University Fermilab Northern Illinois University SLAC University of Illinois Chicago	3D technology allows very fine pitch (4 μm) integration of sensors with multiple layers of electronics, allows interconnection to both the top and bottom of devices, and provides techniques for low mass, thinned devices.	Completed multi-year effort to demonstrate commercial 3D technology, consisting of 0.13 CMOS interconnected with Direct Oxide bonding technology and access using TSV. Received readout wafers with thickness of 25 μm , processed with TSV and DBI to connect to 3D electronics Currently working on active edge demonstrator devices	Complete the 3D active edge project Apply concepts to x-ray imaging devices Re-start ILC developments pending renewed funding
SOI	KEK University of Tsukuba Tohoku University Osaka University	In the Silicon-On-Insulator (SOI) technology the sensing and processing functionalities are separated in different layers; the sensing is provided by a high-resistive substrate connected through an insulating layer with the processing layer.		Sep 2014: Complete architecture study for the ILC pixel detector Mar 2015: Design and fabrication of first test chip for the ILC Dec 2015: Beam test of the chip
CLICpix	Cambridge University CERN University of Geneva Karlsruhe Institute of Technology (KIT) University of Liverpool SLAC Institute of Space Science Bucharest Spanish Network for Linear Colliders	Hybrid pixel-detector technology comprising fast, low-power and small-pitch readout. ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin planar or active HV-CMOS sensors via low-mass interconnects.	Beam tests of prototype assemblies with ultra-thin sensors (50–300 μm) CLICpix demonstrator ASIC in 65 nm technology Beam tests of assemblies with capacitive coupling between CCPDv3 HV-CMOS active sensors and CLICpix ASICs Power-pulsing demonstrator with dummy loads Prototypes of carbon-fibre ladder supports Full-scale thermal mockup of the CLIC vertex-detector region	Demonstration modules for all major components in time for the next update of the European Strategy for Particle Physics in 2018/19

Chapter 2

Silicon Trackers

2.1 Long-Ladder and Charge Division Tracking R&D

2.1.1 Introduction

The SiD collaboration has done microstrip R&D in two directions that might provide attractive alternatives to the SiD baseline: the exploration of the long-ladder limit for precision microstrip tracking, and the exploration of the use of ‘charge division’ – reading out resistive electrodes from both ends – to glean information about the longitudinal position of the track along the length of the sensor.

Two activities have been undertaken for the exploration of the long-ladder limit: the development of an optimized, time-over-threshold readout ASIC (the LSTFE chip) and a lab-bench study of the noise limitations associated with reading out long, thin electrodes. The possibility of using charge division to determine the longitudinal coordinate of deposited charge with sub-centimeter precision was explored using a mock electrode network read out with an optimized amplification and shaping chain. Milestones have been achieved in all three areas.

2.1.2 Recent Milestones

The properties of this Long Shaping-Time Front End (LSTFE) microstrip readout ASIC have been optimized for the readout of long ladders of silicon strip sensors that are motivated by the need for precise low-mass central tracking for a Linear Collider Detector. With a small and straightforward change to the shaping properties of the ASIC, it could be re-optimized for use for the short strips and high occupancy that would be expected for ILC forward-tracking applications. The LSTFE features optimized initial-amplification characteristics and shaping time to reduce voltage-referenced readout noise, as appropriate for narrow-strip, long-ladder applications. Unique to the LSTFE design, however, is the use of time-over-threshold readout to estimate the analog pulse-height generated by subatomic particles passing through. A pulse-development and readout simulation developed for the purpose of the designing the LSTFE suggests that the intrinsic statistical fluctuations of the charge-deposition process in 300 μm of silicon obviate the need for a precise measurement of deposited charge. A simulation of the centroid-finding (position-resolution) uncertainty provided by time-over-threshold readout showed little degradation relative to that provided by an exact measurement of deposited charge.

On the other hand, there are several advantages offered by the use of time-over-threshold readout. It is

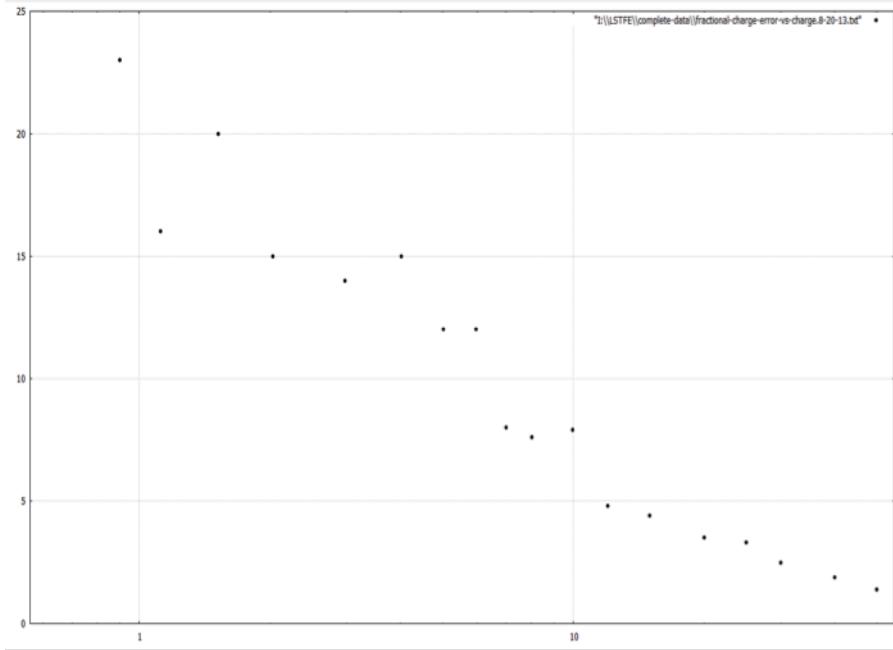


Figure 2.1: Fractional pulse-height uncertainty (percent) versus injected charge (fC) for the LSTFE front-end ASIC.

very simple to implement within a digital back-end to the LSTFE’s analog front end (the implementation would be on the same chip as the front-end readout), requiring only a measurement of the number of clock counts that the given channel is over threshold, and then the assembly and transmission of a single data word containing the time of the upward transition, the time over threshold after the transition, and the channel number. This happens in real time and is driven immediately off the chip into the DAQ, eliminating the need for buffering and ADC conversion. In particular, there is no limit to the rate at which particles can be detected other than the return-to-baseline of the analog signal, and so the data-accumulation rate capability of the device is very high. In addition, for forward tracking, for which short strips are envisioned, the shaping time can be shortened significantly. This will further improve the rate capability of the LSTFE readout, making it an excellent choice for the high-occupancy forward region. Figure 2.1 shows the fractional pulse-height uncertainty versus injected charge achieved with the LSTFE front-end ASIC.

The possibility of obtaining a longitudinal coordinate from silicon microstrip sensors has been explored [51], making use of the implant as a resistive electrode, with no overlain metallic electrode. A mock resistive microstrip-implant electrode network was constructed on a PC board out of discrete resistors and capacitors which was read out on both ends by an amplifying and shaping chain that was optimized to give the greatest precision in the longitudinal position of the charge deposition on the implant. For a 10 cm-long sensor, a longitudinal resolution of 6 mm was observed, achieving the resolution needed to aid in tracking reconstruction in dense jet environments. Finally, sources of readout noise were measured and modeled for sensors in the long, thin strip electrode limit [52]. The readout noise observed with the LSTFE ASIC was measured as a function of the length of a daisy-chained ladder of sensors, and the results

modeled with a SPICE simulation. It was found that network effects due to the distributed resistance and capacitance of the electrode provide significant mitigation of the readout noise relative to the assumption of single, lumped elements. It was also found that reading out the ladder at its center rather than from one end provided further noise suppression. Attaching this noise model to the pulse-development simulation developed for the LSTFE design suggested that ladders of as much as 75 cm long could be made operation with end readout. Ladders approaching 1 m in length could be operated with center readout.

2.1.3 Engineering Challenges

The primary remaining engineering challenges are the implementation of LSTFE power-cycling with a $\approx 1\%$ duty cycle, and the transfer of the digital back-end processing of the LSTFE information from an off-chip FPGA directly onto the ASIC.

2.1.4 Future Plans

Because of this work, the possibility of a tracker making use of long ladders of silicon microstrip sensors, or shorter strips with time-over-threshold readout in the forward region, remains an option for the SiD detector. However, at this time resources are being directed towards the modular KPXiX design.

2.1.5 Applications outside Linear Colliders

It should be noted that the exploration of noise limitations for long, thin electrodes apply independently of the sensor technology that generates the signals. Thus, this work may have relevance to detection issues across a wide array of fields.

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2.2 Resistive charge-division on thinned micro-strips sensors with low signal amplification

2.2.1 Introduction and Motivation

In the context of the ILC, the relatively low occupancy environment and the power pulsing operation of the front-end electronics provide an opportunity for the implementation of ultra-lightweight silicon-based tracking systems where the dominant contribution to the material budget in the fiducial volume comes from the sensors. Reducing the material budget has a major impact on the hit position resolution and hence the momentum resolution of the tracker system; therefore, we have pursued during the last three years an RD program for the development of very thin micro-strips sensors able to provide two dimensional information of the hit position.

The ultimate goal of this R&D is the development of a micro-strip sensor which combines signal amplification — allowing the thinning of the sensor’s substrate — and resistive electrodes — allowing the implementation of the charge-division method for the determination of the hit position along the strip direction. In a first phase, we are aiming to demonstrate the feasibility of each of the above mentioned features independently and, in a second phase, to integrate both technological solutions into the same micro-strip sensor; the thinning of the sensor will be done using the anisotropic wet etching (TMAH process) used for the DEPFET fabrication 1.4.

2.2.2 Recent Developments and Milestones

The use of the charge-division method in long micro-strip sensors, with a length of several tens of centimeters, was proposed as a possible tracking technology for the International Linear Collider detector concepts a few years ago [53]. More recently, we have demonstrated [54, 55, 56] the feasibility of the charge division concept on fully fledged micro-strip sensor with resistive electrodes made of poly-crystalline silicon achieving a spatial resolution along the strip direction of about 7% the strip length. One of the limitations of this technology is the attenuation of the signal along the resistive electrode; additionally, the position resolution along the strip is proportional to the signal-to-noise ratio. Therefore, to maintain or even increase the SNR without increasing the sensor substrate thickness we proposed the integration of signal amplification structures in the sensor itself. The Low Gain Avalanche Detector (LGAD) technology appears as a well suited technique for achieving the signal amplification. LGAD devices engineered as reach-trough avalanche detectors with a moderate gain where initially proposed and developed for timing application [Pellegrini 2014], the moderate signal amplification ensured that a relatively standard front-end readout electronics could be employed. As a spin-off of this original aim, we introduced the i-LGAD micro-strip concept for tracking, a LGAD device implemented in a p-type substrate where the ohmic electrode is strip-wise segmented; this design favors the uniform signal amplification over the sensors active volume overcoming the non-uniform gain in LGAD micro-strips sensors with a strip-wise segmented amplification layer that we recently characterized [57, 58]. The former R&D line is complemented with the development of a dedicated ASIC using a 180 nm AMS fabrication process which integrates a charge amplifier with long shaping time and time stamping functionalities; finally, we completed the study and testing of several pulsed power system topologies based on super-capacitors.

2.2.3 Engineering Challenges

Concerning the component aspects, the main challenges are to complete to proof-of-concept of the thinned micro-strips with charge amplification and resistive charge-division in a implementation suitable for the LC tracking needs, namely: proof the i-LGAD concept, integrating amplification and charge division, thinning of sensors substrate, large area sensors, manufacturing long ladder by daisy chaining of the sensors. Concerning the read out ASIC, the main challenge will be the design of the front-end with the required functionalities while keeping the power dissipation low enough. System wise, the main challenge is the design of an air-based cooling system and its integration on the CFRP supporting structure such that the material budget of the system remains acceptable from the point of view of it tracking performance.

2.2.4 Future detector R&D

During the next two years we will focus our activities on the testing of the i-LGAD devices and, if the results were positive, the integration of the low gain amplification and manufacturing of large area sensors

(100 cm^2). Concerning the front-end electronics, the main goal will be to complete a few channel demonstrator integrating the long shaping time amplifier and power pulsing. A real scale thermo-mechanical mockup is of the FTD sub-detector at ILD is currently under construction to assess different air forced cooling options.

2.2.5 Applications outside LC

The application of LGAD devices to the LC tracking is a spin-off of its original aim as timing devices for high radiation environments, this technology is being proposed as vertex locator technology for the LHC experiments: AFP2 and HGTD (ATLAS); and CT-PPS (CMS) [59].

2.3 KPiX

2.3.1 Introduction

KPiX is a 1024 channel “System on a Chip” intended for bump bonding to large area Si sensors, enabling low multiple scattering Si strip tracking and high density Particle Flow calorimetry for SiD at the International Linear Collider (ILC).

Each channel consists of a dynamically switchable gain charge amplifier; shaping; threshold discrimination; and 4 sample and hold capacitors and 4 timing registers. The chip permits 4 separate measurements of amplitude and time of threshold crossing during each train, and amplitude digitization and readout during the intertrain period. The dynamic range is from sub minimum ionizing particle (mip) (in $320\text{ }\mu\text{m}$ silicon) to more than 2000 mip. KPiX also has a calibration system for each channel, servos for leakage compensation, “DC” reset for asynchronous operation for testing with cosmic rays, and polarity inversion for use with GEMs and similar detectors. The noise floor is about 0.15 fC (≈ 1000 electrons), and the maximum signal is 10 pC (utilizing the dynamic range switching). The full dynamic range corresponds to 17 bits.

2.3.2 Recent Milestones

ILC related R&D in the US is largely unfunded and small efforts are being kept alive on the margins. The KPiX R&D is such an example of necessary work for SiD that is marginally alive.

2.3.3 Engineering Challenges

At this time, KPiX is seen as the baseline readout system for the tracker and electromagnetic calorimeter. A stack of 13 EMCal sensors with bump bonded KPiX was assembled for a beam test at SLAC in the summer of 2013. That test discovered that two kinds of crosstalk are significant:

- In-time crosstalk occurs due to parasitic coupling of traces on metal 2 of the sensor to other pixels. The level of crosstalk increases with the size of the signal, and decreases with increased speed of the front end charge amplifier (meaning increased current and power dissipation). A new sensor design is being developed that uses metal 1 to shield the traces of metal 2, and these ideas will be tested in the next sensor prototype.
- Out-of-time cross talk occurs when many pixels are hit and reset simultaneously. The resets collectively cause other pixels to trigger, and a cascade builds up. This uses up all the KPiX buffers. The

root cause of the problem appears to be some internal logic within KPiX that is not current limited, and will require design modification.

A more general issue is that both the EMCal and tracker sensors from Hamamatsu were ordered with Al pads, as it was believed that plating (by the zincate process) a stack of metals culminating with Au would be straightforward. This turns out to be wrong. Future sensors will be ordered with Au pads.

An additional issue is that the Tracker sensor was planned to be wire bonded to its (very thin) cable. The sensor oxide layer is not strong enough to allow wire bonding without damage, and so must be solder bumped. The pad pitch is small, and solder bumping the cable will be challenging. The trouble with the wire bonding to the sensor was unexpected. Another concern is that the current design of KPiX has deadtime after a pixel has accepted a trigger. Only the triggered pixel is affected; all the other pixels are available for signals. This deadtime is different from the usual notion of data acquisition deadtime where the entire detector is unavailable, but the correction to the luminosity integral is easy. Finally, the buffer requirement (4 in the current version of KPiX) is being re-evaluated in SiD simulations. A possible new architecture for KPiX is in early stages of evaluation. A small mechanical engineering effort has started to study the structure of the EMCal. The SiD EMCal has emphasized thin gaps between the tungsten layers to minimize the Moliere radius, and this implies that the structure is connected by columns at the vertices of the sensors. The DBD design shows hexagonal sensors, which indeed are the most efficient way of tiling large areas, but no consideration was given to the edges of these arrays. The design is being re-evaluated to optimize the cost-effectiveness over the whole area taking into account geometric efficiencies and total wafer cost. Tracker sensors are now at IZM for the pad plating and subsequent bonding of KPiX; they will then go to UCD for cable attachment and testing.

2.3.4 Future Plans

Assuming positive developments with Japan are announced soon, we expect the financial support to improve. It should be noted that an important effect of the withdrawal of support is that most of the US collaborators have been forced to move to other work.

- EMCal Sensors: A second round of prototypes will be designed and ordered with rectangular layout; shielded traces, and Au pads.
- Tracker Sensors: The current prototypes will be evaluated, and if appropriate tested in a beam.
- KPiX: A new architecture with little (or no) deadtime will be evaluated. A decision will be made to develop this new architecture or incrementally.
 - improve the existing design.
- The EMCal mechanical structure will be pushed towards a conceptual design.

2.3.5 Applications Outside of Linear Colliders

This work represents a significant step in the aggressive integration of silicon sensors with readout electronics, just short of integrating the electronics directly into the sensors. It has prompted consideration of this approach by CMS for calorimetry and by ATLAS for a muon system. It may have applications in sensors for light sources as well as other particle physics detectors.

R&D Techniques

text

Chapter 3

Gaseous Trackers

3.1 Time Projection Chamber – GridPix, Bonn

3.1.1 Introduction

The project studies the pixelized readout of a TPC for the ILD detector. The readout is based on the Timepix ASIC with a triple GEM or Micromegas based gas amplification.

3.1.2 Recent Milestones

The first studies were based on the triple GEM setup with a single Timepix chip. This readout was mounted in a small test detector in the Bonn laboratory. Here, the working principle was tested with a long drift distance. It could be demonstrated that the transverse spatial resolution of the reconstructed primary electrons was close to the expected diffusion limit of single electrons. The results are summarized in the following publications:

- C. Brezina et al. “Operation of a GEM-TPC With Pixel Readout”. In: *Nuclear Science, IEEE Transactions on* 59.6 (Dec. 2012), pp. 3221–3228. issn: 0018-9499
- J. Kaminski et al. “Time projection chamber with triple GEM and pixel readout”. In: *Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE*. Oct. 2008, pp. 2926–2929
- C Brezina et al. “A Time Projection Chamber with triple GEM and pixel readout”. In: *Journal of Instrumentation* 4.11 (2009), P11015
- Jochen Kaminski et al. “Time projection chamber with triple GEM and highly granulated pixel readout”. In: *Conf.Proc. C0908171* (2009), pp. 533–535
- Peter Schade and Jochen Kaminski. “A large {TPC} prototype for a linear collider detector”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 628.1 (2011). {VCI} 2010 Proceedings of the 12th International Vienna Conference on Instrumentation, pp. 128–132. issn: 0168-9002

The new focus are GridPix based detectors, where the gas amplification stage is a Micromegas produced in a postprocessing technique, which guarantees a high quality grid well aligned with the readout pixels.

This approach was pioneered by NIKHEF and the University of Bonn has modified the production process together with the Fraunhofer Institut IZM so that a wafer-based production of GridPix detectors is standard by now. The new GridPixels were tested on small prototype detectors and also assembled in an 8 GridPix module for the Large Prototype detector at DESY. A successful test beam campaign was performed last year.

- M Lupberger. "The Pixel-TPC: first results from an 8-InGrid module". In: *Journal of Instrumentation* 9.01 (2014), p. C01033
- W.J.C. Koppert et al. "GridPix detectors: Production and beam test results". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 732 (2013). Vienna Conference on Instrumentation 2013, pp. 245–249. ISSN: 0168-9002

The current work is focused on a new LP module with about 160 GridPixels. The central module is equipped with 96 GridPixels and the two outer modules have 32 GridPixels arranged to maximize the lever arm. This setup serves a demonstrator that larger areas (400 cm^2) can be produced and operated. It was tested in the Large Prototype of the LCTPC collaboration in March/April of 2015 and operated for more than one week permanently in the test beam. A total of about 200 runs with more than 1.5 million events were recorded. For this a number of challenges had to be overcome. In particular commercial readout systems are not easily scalable. This is why Bonn has developed a cheap and easily expandable system based on the Scalable Readout System (SRS) of the RD51 collaboration.

In addition Bonn is developing the software for reconstructing and analyzing the test beam and simulation data. For this the LCTPC software framework of MarlinTPC is used.

- Jason Abernathy et al. "MarlinTPC: A common software framework for TPC development". In: *Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE*. Oct. 2008, pp. 1704–1708

Finally, Bonn also takes part in designing new pixel chips. To test the new digitization and readout techniques two test chips were designed in collaboration with NIKHEF. Then Bonn also contributed to the design of the Timepix successor chip, Timepix3, which is being tested now:

- A Kruth et al. "GOSSIPO-3: measurements on the prototype of a read-out pixel chip for Micro-Pattern Gaseous Detectors". In: *Journal of Instrumentation* 5.12 (2010), p. C12005
- C. Brezina et al. "GOSSIPO-4: Evaluation of a Novel PLL-Based TDC-Technique for the Readout of GridPix-Detectors". In: *Nuclear Science, IEEE Transactions on* PP.99 (2014), pp. 1–1. ISSN: 0018-9499
- Y Fu et al. "The charge pump PLL clock generator designed for the 1.56 ns bin size time-to-digital converter pixel array of the Timepix3 readout ASIC". In: *Journal of Instrumentation* 9.01 (2014), p. C01052

3.1.3 Engineering Challenges

The production of a module with 160 GridPixels requires 4 main components:

1. The production of a large number of GridPixels with sufficiently good quality. This has been addressed by the new production method, which is based on complete wafers. The process was developed in collaboration with the Fraunhofer institute IZM in Berlin and yields up to 400 GridPixels per batch. Figure 3.1 shows a GridPix detector with a partially removed grid.
2. The challenge of the readout is being addressed by the new readout system as described above.

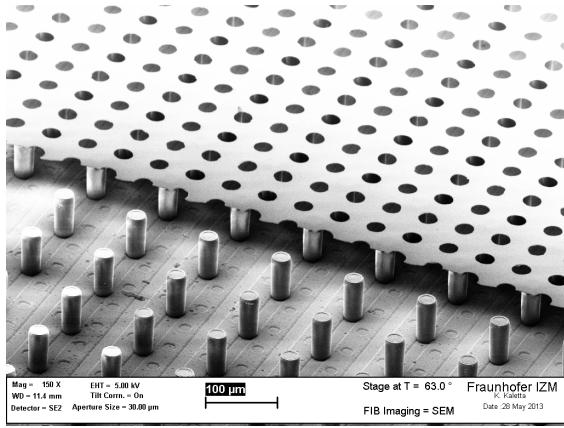


Figure 3.1: GridPix detector with a partially removed grid

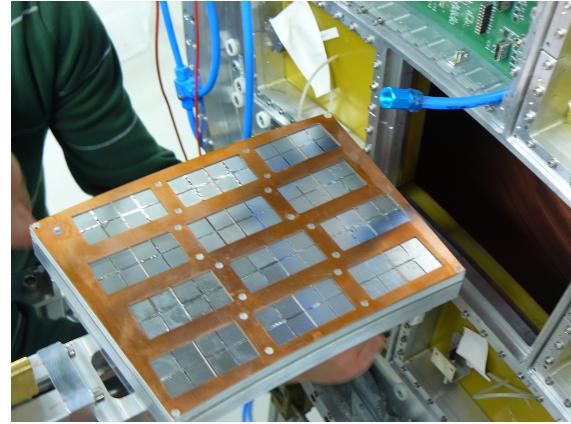


Figure 3.2: Fully equipped module as it is being mounted

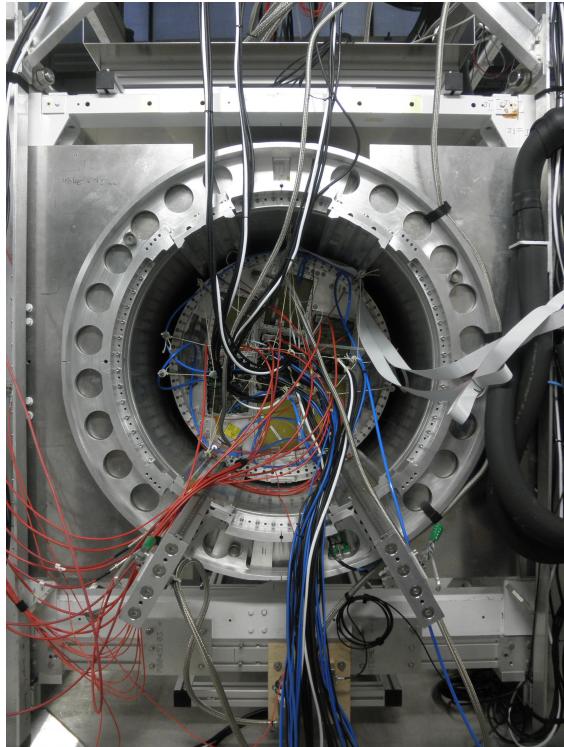


Figure 3.3: Fully cabled end plate

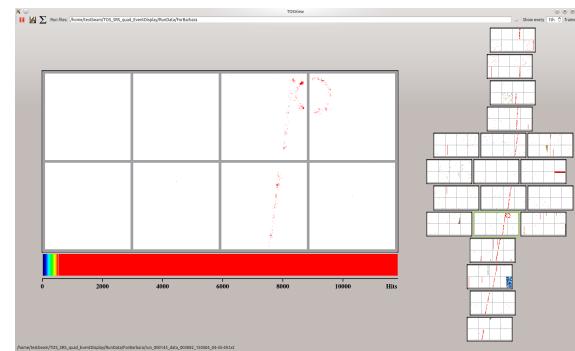


Figure 3.4: Online display of an example track

3. The distribution of the LV power to all ASICs which can reach peak values of 85 A at 2.2 V was studied in a Master thesis.
4. Cooling of the ASICs was done by cold water.

3.1.4 Future Plans

Currently, the main focus is on the analysis of the test beam data. The challenge of finding and fitting tracks with several thousand hits is quite different from the standard pad-based TPC analysis. On a longer term all participating institutes are working on software to simulate, reconstruct and analyze data of the ILD-TPC (i.e. about 10,000 hits per track) so that the difference in performance between a pad and a pixel-based TPC can be studied. On the hardware side we are interested in replacing the Timepix ASIC by the Timepix3 ASIC and produce GridPix detectors with this improved chip, which promises a much better performance, since it is multi-hit capable, can record both time and charge of each signal and has a much faster digitization frequency. There are also some ideas of how to improve the grid structure and make it more reliable.

3.1.5 Applications Outside of Linear Colliders

A single InGrid detector will be installed this year in the CAST experiment for axion search. For a TPC in a CLIC detector, a highly granular (i.e. pixelized) readout structure is mandatory to lower the occupancy.

3.2 Gaseous Tracking

Contact person: Jochen Kaminski (email : kaminski@physik.uni-bonn.de),
for the LCTPC collaboration

3.2.1 Introduction

Detectors for a high energy linear electron positron collider have been discussed since the early 1990's. For the main tracking a TPC was proposed early on. The advantages of a TPC are its ability to detect track elements in 3 dimensions while introducing very small amounts of dead material. A potential disadvantage could be the appearance of distortions due to $E \times B$ effects in the drift region, originating from possibly inhomogeneous magnetic or electric fields, which could be a consequence of the construction or from space-charge build-up as a result of ion back-flow.

In 1996, the first Linear Collider detector conceptual report [TESLA-CDR] considered the possibility to read out the end-cap chambers with MSGC, Micromegas and GEMs. Several advantages of the MPGDs were recognized immediately: the ion back-flow could be very limited by a suitable choice of the field configuration, and the $E \times B$ effects present close to the wires of a MWPC are very limited in the case of the microscopic structure of a MPGD. However it was also recognized that, to profit from the excellent resolution allowed by a limited diffusion and a very localized avalanche, either sufficiently small pads would be needed, to share the charge among several pads, or a mechanism for spreading the avalanche was needed. Without such a sharing, the only information obtained would have been which pad received the charge, and the hit position would have a flat probability over the pad width, limiting the resolution along a pad row to $p/\sqrt{12}$, p being the pitch over a pad row. It was also understood that for a multi-stage

GEM, the amount of natural spreading by diffusion in the gas amplification device itself, about $300\text{ }\mu\text{m}$ r.m.s., was sufficient to obtain enough charge spreading with $\sim 1\text{ mm}$ wide pads. For Micromegas, where the avalanche has typically a $15\mu\text{m}$ r.m.s., an additional charge-spreading mechanism was necessary, even for 1mm pads. Such a method was introduced by the Carleton group, using a superposition of an insulator and a resistive cover. This arrangement provides a continuous Resistor-Capacitance (RC) network over the surface which spreads the charge around the avalanche. The induced signal is measured, shaped and digitized by the electronics connected to each pad. Note that this technique is applicable also to GEMs and allows pad widths of 2, 3 or more mm.

At the beginning of the years 2000, several small prototypes were built in Aachen, Amsterdam, Saclay-Orsay with a Berkeley electronics, DESY, Munich, Karlsruhe, Carleton, Victoria, Saga, KEK, Tsinghua, to study various aspects of the GEM and Micromegas technology. Ion feed-back was studied, resolution was measured in various prototypes, and the possible gases were studied. The fundamental proof was made that a TPC with MPGD readout can be operated stably, and can reach intrinsically the anticipated resolutions.

Then, in 2004, part of the nascent collaboration gathered around a 5 GeV pion beam and cosmic-ray tests at KEK. The detector was immersed in a 1 T magnetic field from a permanent-current superconducting magnet. The 25 cm drift field cage was designed in Munich and electronics was recuperated from ALEPH. Several endplates were adapted to this cage with wires, Micromegas (without resistive foil) and GEM technologies. In 2006 the Carleton 16 cm drift length prototype with a Micromegas resistive foil took data simultaneously with the Munich prototype.

At the same time other developments took place in other institutes. Noteworthy was the use of 2 parallel laser beams in Victoria and later at DESY to study 2-track separation. This study showed that a separation of two tracks was possible down to 1 pad size distance between the laser beams.

Several groups carried out tests in a 5 T magnet at DESY in the years 2003-2007. The operation in such high fields could be established for both Micromegas and for GEMs, and the extrapolation of the resolutions previously measured at lower fields could be demonstrated.

The next step then was the construction and operation of a common large prototype. The European Union - funded project EUDET allowed a facility to be built at DESY, with a 1T SC magnet offered by KEK, a field cage designed at DESY, an endplate brought by Cornell, a cosmic trigger with SiPMs built by Saclay, a beam trigger from Nikhef, a gas system from DESY and Rostock, high density readout electronics by Saclay and Lund, etc..

The endplate has 7 openings to receive up to 7 identical modules. The 'keystone' shape of the modules is chosen to be as close as possible to the anticipated real configuration of a disc paved by concentric rows of modules. Data taking started in 2008 in the fixed magnet. At this time, to shoot the beam at a given z position along the drift axis was possible only by sliding the TPC in the magnet; this way, the large drift distances could only be obtained by taking the TPC in a very inhomogeneous field. This was solved the following years by the installation of a moving stage allowing horizontal and vertical translations, as well as rotations in the horizontal plane. Rotation of the TPC around the magnet axis could be performed by hand.

Since then beam tests took place nearly every year, alternating between GEMs from Japan, Micromegas, GEMs from DESY, and pixels.