

# **DEPFET active pixel detectors for a future linear $e^+e^-$ collider - Report for the ECFA Detector R&D review, DESY, June 2014**

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The DEPFET collaboration ([www.depfet.org](http://www.depfet.org))

*E-mail:* [marcel.vos@ific.uv.es](mailto:marcel.vos@ific.uv.es), [cmarinas@uni-bonn.de](mailto:cmarinas@uni-bonn.de),  
[chk@h11.mpg.de](mailto:chk@h11.mpg.de), [lca@h11.mpg.de](mailto:lca@h11.mpg.de)

**ABSTRACT:** The DEPFET collaboration develops highly granular, ultra-transparent active pixel detectors for high-performance vertex reconstruction at  $e^+e^-$  collider experiments, such as Belle II and a future  $e^+e^-$  collider at the energy frontier. In this report, we review measurements on prototypes that prove the potential of the DEPFET operation principle and provide a status report for the development of a complete detector concept, including solutions for mechanical support, cooling, and services. An overview is also given of LC-specific R&D. Based on this experience we revisit the expected performance of a DEPFET-based vertex detector and show that DEPFET can meet the stringent requirements of the detector concepts for a future linear  $e^+e^-$  collider.

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## 1 Introduction

A high-luminosity, high-energy, linear  $e^+e^-$  collider yields excellent opportunities for precision tests of the Standard Model of particle physics. The combination of precisely calculable electroweak production and strict control of the initial state with the relatively benign experimental environment and state-of-the-art detector systems allow for a characterization of Standard Model and new physics processes with a precision that goes well beyond what can be achieved at hadron colliders.

Two projects exist that pursue the creation of a linear electron-positron collider (referred to as Linear Colliders or LC in the remainder of this note):

- The proposal for an International Linear Collider (ILC [1, 2]) is based on existing super-conducting Radio-Frequency (RF) cavity technology. In the baseline design the ILC is envisaged to reach a center-of-mass energy of 500 GeV. Early stages of the physics programme are likely to involve running at a center-of-mass energy of 250–350 GeV to study the properties and couplings of the Higgs boson and to characterize the production threshold for  $t\bar{t}$  pair production. The possibility to upgrade the ILC to a maximum of  $\sqrt{s} = 1$  TeV is a crucial requirement to the design.
- To reach larger center-of-mass energies, the accelerating gradient obtained in the previous scheme is insufficient. The Compact Linear Collider (CLIC [3]) aims to open up the energy regime up to several TeV using a novel technology, where a drive beam is used to provide power to the room temperature RF cavities of the main Linac.

The physics case for a linear  $e^+e^-$  machine has been made in great detail in References [4–11]. The specific case of a multi-TeV  $e^+e^-$  collider is discussed in References [12–14]. The programme includes a precise determination of the properties of the Higgs boson discovered at the Large Hadron Collider (LHC). However, a linear collider that covers the energy regime from several hundreds of GeV to several TeV offers a much broader programme of Standard Model measurements and searches for new phenomena. The interplay of the broader LC programme with respect to the LHC is studied in Reference [5, 15].

A very active programme exists aimed at the development of detectors for a linear collider [16, 17]. Innovative approaches towards calorimetry, tracking and vertex detectors are pursued in detector R & D collaborations. Two detector concept groups have prepared complete detector designs [18, 19]. The same two detector concepts have been adapted to the CLIC environment [12].

Experiments at a future linear  $e^+e^-$  collider [20, 21] (LC) require extremely precise reconstruction of the reaction products to perform precision physics programs to study the electroweak symmetry breaking mechanism and physics beyond the Standard Model. Key figures of merit for the detector performance, such as the jet energy resolution, momentum resolution for charged tracks, and the vertexing capabilities of the experiment, must be improved significantly with respect to the state-of-the-art detectors realized in the LHC experiments or those under development for a future luminosity upgrade. A worldwide R & D effort is ongoing to develop detectors that satisfy these challenging requirements.

The Depleted Field Effect Transistor [22]) concept dates back to the eighties, when Lutz & Kemmer conceived a Field Effect Transistor (FET) integrated in the active material of a standard, fully depleted silicon detector. The small signal that is generated when charged particles traverse a thin layer of silicon is collected on an internal gate immediately underneath the FET. The accumulated charge modulates the drain current, in a similar fashion as a voltage gate applied to the regular gate terminal. An active detector is thus produced, that amplifies the tiny signal in the detector itself. Active sensors with DEPFET structures can achieve an excellent signal to noise ratio. The DEPFET concept therefore presents interesting possibilities for a number of applications:

- X-ray detection in the European XFEL [23]. A DEPFET-based detector with parallel

read-out is being developed for X-ray imaging in the European Free Electron Laser facility.

- Space-based X-ray Astronomy missions. The Athena+ [24] project is proposed as Europe’s next generation space-based X-ray observatory.
- Ultra-thin vertex detector for collider experiments. The internal amplification of the MIP signal allows for a strong reduction of the material budget of position-sensitive devices for charged particle detection at collider experiments. The proposal of a DEPFET vertex detector for a future linear  $e^+e^-$  collider [25, 26] dates back to 2002.

In the current report we focus on the latter application. Over the last decade an international collaboration has formed that has brought the DEPFET detector concept to maturity. The DEPFET collaboration has shown that finely segmented devices with large in-pixel gain can indeed be constructed and operated. Read-out and control ASICs have been designed and produced, and a novel ladder design with excellent thermo-mechanical properties has been developed. A fully engineered vertex detector design, including all supports and services, is being developed for the Belle II experiment [27].

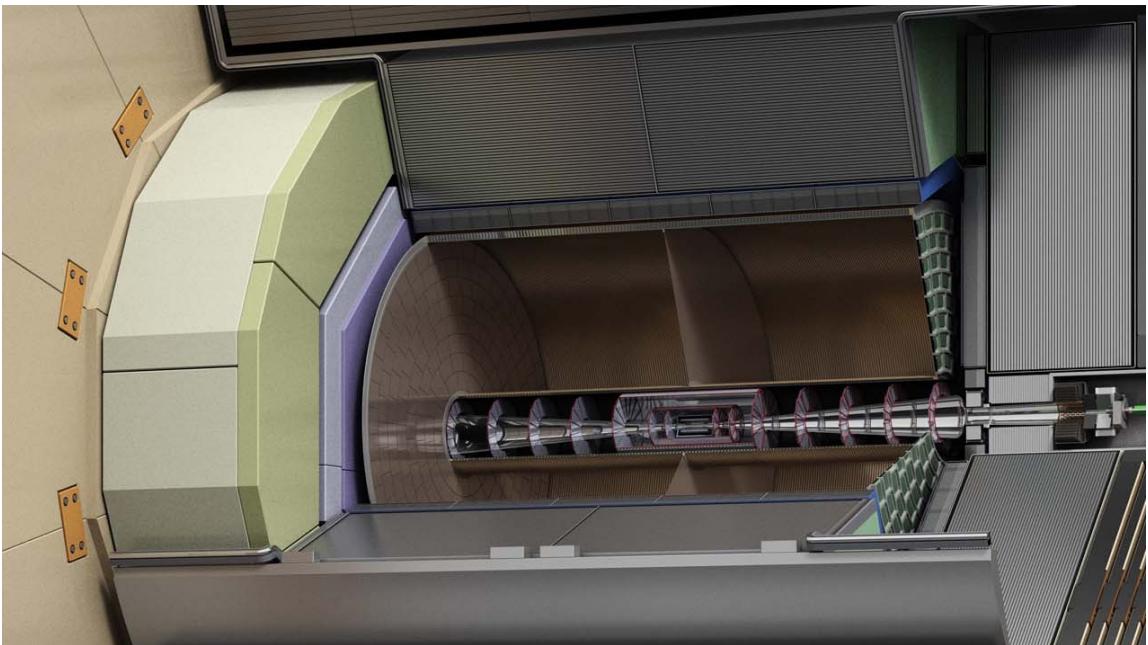
Recent descriptions of the DEPFET active pixel detector project are found in References [28] and [29]. The Belle II technical design report [27] provides a very complete description of the DEPFET-based vertex detector of that experiment (see also [30, 31]). The most recent documents reviewing DEPFET progress towards a vertex detector for a linear collider is a brief paper [32] that accompanied the publication of the ILD Technical Design Report. Older sources include the report [33] prepared for the ILC R & D panel in 2007.

In this report we present an up-to-date overview of major recent milestones towards the realization of a complete DEPFET vertex detector. With the more detailed understanding of the potential and limitations of the DEPFET concept gained in recent years, we revisit to what extent DEPFET can satisfy the stringent requirements of a linear  $e^+e^-$  collider at the energy frontier.

The requirements on an LC vertex detector are briefly summarized in Section 2 and compared to those of other projects in Section 3. The DEPFET concept is introduced in Section 4 and the thinning process that gives rise to the all-silicon ladder in Section 5. A ladder design for an LC vertex detector based on DEPFETs is schematically presented in Section 6. The following Sections highlight recent progress in the development of key components, the sensor in Section 7 and the read-out and steering ASICs in Section 8. In Section 9 and 10 recent results from the characterization of prototypes are presented. Section 11 and 12 present recent examples of detector R & D that aims specifically at the ILC, with recent results from the thermo-mechanical characterization of forward detector petals and ladders with an integrated micro-channel cooling circuit. Finally, Sections 13 through 15 revisit the expected performance of a DEPFET-based detector at the heart of the ILC experiments, with emphasis on material budget, read-out speed and spatial resolution. The most important findings are summarized in Section 16.

## 2 Requirements

Experiments at a future linear  $e^+e^-$  collider require extremely precise reconstruction of the reaction products to perform precision measurements of Higgs and top production and to search for signatures of new physics. Detector concept studies for future linear colliders have established a number of challenging performance goals based on the analysis of benchmark channels and an evaluation of the LC environment [18, 19, 21, 34, 35]. Key figures of merit for the detector performance, such as the jet energy resolution, momentum resolution for charged tracks, and the vertexing capabilities of the experiment, must be improved significantly with respect to the state-of-the-art detectors realized in the LHC experiments or those under development for a future luminosity upgrade.



**Figure 1.** The inner tracking system of the ILD detector concept for the ILC

A zoom image of the core of the ILD detector concept is shown in Figure 2. The inner tracking and vertexing system consist of two concentric “barrel” layers and two times five large disks, each equipped with micro-strip detectors. At the very core of the experiment six barrel layers and two further disks are found, that are to be instrumented with highly granular pixelated detectors. The first layer is situated at a radial distance from the interaction point of 16 mm.

The key goal of the innermost layers is the reconstruction of primary, secondary and tertiary vertices, that is crucial to *tag* the flavour of jets initiated by heavy quarks. The aim for the vertexing capabilities of the LC detectors is often summarized with the following

requirement on the impact parameter resolution:

$$\Delta d_0 = 5[\mu\text{m}] \oplus \frac{10[\mu\text{m}]}{p[\text{GeV}] \sin^{3/2} \theta} \text{ } ^1 \quad (2.1)$$

This goal represents a considerable improvement over vertex detectors built at collider experiments to date; the constant term is better by a factor of two to four than what was achieved at previous  $e^+e^-$  colliders and at the LHC. Achieving the requirement for the second (material) term is even more challenging; it has to decrease by a factor of six to ten with respect to most previous experiments. The best material term so far was achieved by the SLD vertex detector with  $\Delta d_0 = 9[\mu\text{m}] \oplus \frac{33[\mu\text{m}]}{p[\text{GeV}] \sin^{3/2} \theta}$ . This CCD based detector had 0.36% of a radiation length per layer. Indeed, the requirement in Formula 2.1 (together with the assumed inner radius of 15 mm) implies that the vertex detector must be built with a strict material budget of order 0.1% of a radiation length per layer, roughly equivalent to 100  $\mu\text{m}$  of silicon.

The first layer of the LC vertex detector must cope with large irreducible backgrounds due to incoherent  $e^+e^-$  pair production. Long bunch trains are envisaged in the ILC Technical Design Report, with 1312 bunches separated by 554 ns. These numbers have changed with respect to the ILC LOI [18, 19], that contemplated 2820 bunches with 337 ns spacing. However, these changes are accompanied by a factor of two increase in bunch current, such that the background hit density per unit area and unit time remains virtually unaltered. A background hit density of up to 10 hits/ $\text{cm}^2/\mu\text{s}$  in the innermost layers of the ILC vertex detector at 15 mm from the interaction point requires read out times of 50-100  $\mu\text{s}$  and a highly granular detector [18, 19].

The background hit rates scale approximately with the instantaneous luminosity, which is in turn expected to increase proportionally with the center-of-mass energy of the machine. The read-out speed requirements are therefore considerably more relaxed in the early low-energy stage (at 250 – 350 GeV) than in the nominal 500 GeV stage and in the envisaged 1 TeV upgrade.

Faster read-out offers a number of advantages, in particular in the pattern recognition of the innermost layers. The SiD detector concept aims for single-bunch time stamping at the ILC (i.e. 500 ns precision). In the CLIC environment, with short bunch trains of order 300 bunches with a 0.5 ns spacing, faster read-out may be mandatory even in the early, low-energy stages of the project. The CLIC detector concepts require 10 ns time-stamping capability. This is, in principle, feasible with a hybrid detector based on a DEPFET sensor. We do not pursue this possibility in the current document, that focuses on a solution that relies on the relatively slow, rolling-shutter read-out mode of the detector.

To comply with the strict material budget, the detector concepts aim to keep the (average) power consumption below 10 W for the entire vertex detector. With such a low power density (approximately 100 mW/cm<sup>2</sup>) no active cooling circuits are required. The key to achieve this goal is the bunch structure of the LC machines. The 0.7 ms long bunch trains at the ILC are separated by intervals of 200 ms. In a pulsed power scheme, where the

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<sup>1</sup>The value of the material term is increased from 10  $\mu\text{m}$  to 15  $\mu\text{m}$  in the CLIC requirement as a consequence of the increased inner radius.

detector power supply follows the machine duty cycle as closely as possible, a reduction of the average power consumption by a factor of (at maximum) 1/275 is possible. The CLIC bunch trains, with a length of just 156 ns, are separated by 20 ms.

The radiation levels in the innermost part of the tracker volume of an LC detector are modest. The non-ionizing dose is of the order of  $10^{10} - 10^{11} n_{eq}/cm^2/yr$ , while the ionizing radiation amounts to less than 1 kGy (100 krad) per year [18, 21]. The detectors must be operated in a strong magnetic field, ranging from 3.5 to 5 Tesla in the different detector concepts.

### 3 Comparison with other R & D efforts

It is useful to compare the requirements established in the previous Sections with the specifications of other projects.

Compared with the challenges faced by the large detector R & D effort for future operating phases of the LHC (and future collider experiments) there are a few important differences. At the ILC the emphasis shifts away from the ability to cope with a large density of particles and high levels of (non-ionizing) radiation, that strongly conditions detector R & D for hadron colliders. Where the LHC detectors are read out every 25 ns and the innermost layers must cope with a total dose equivalent to  $10^{16}$  1 MeV neutrons per  $cm^2$ , for future  $e^+e^-$  colliders a read-out speed of several tens of microseconds is sufficient<sup>2</sup> and radiation levels of  $10^{11} - 10^{12}$  1 MeV neutrons per  $cm^2$  per year are benign compared even to the outer radii of the LHC experiments. Detector concepts optimized for the benign environment of the ILC can significantly exceed the performance of previous experiments in terms of single-point spatial resolution and material budget.

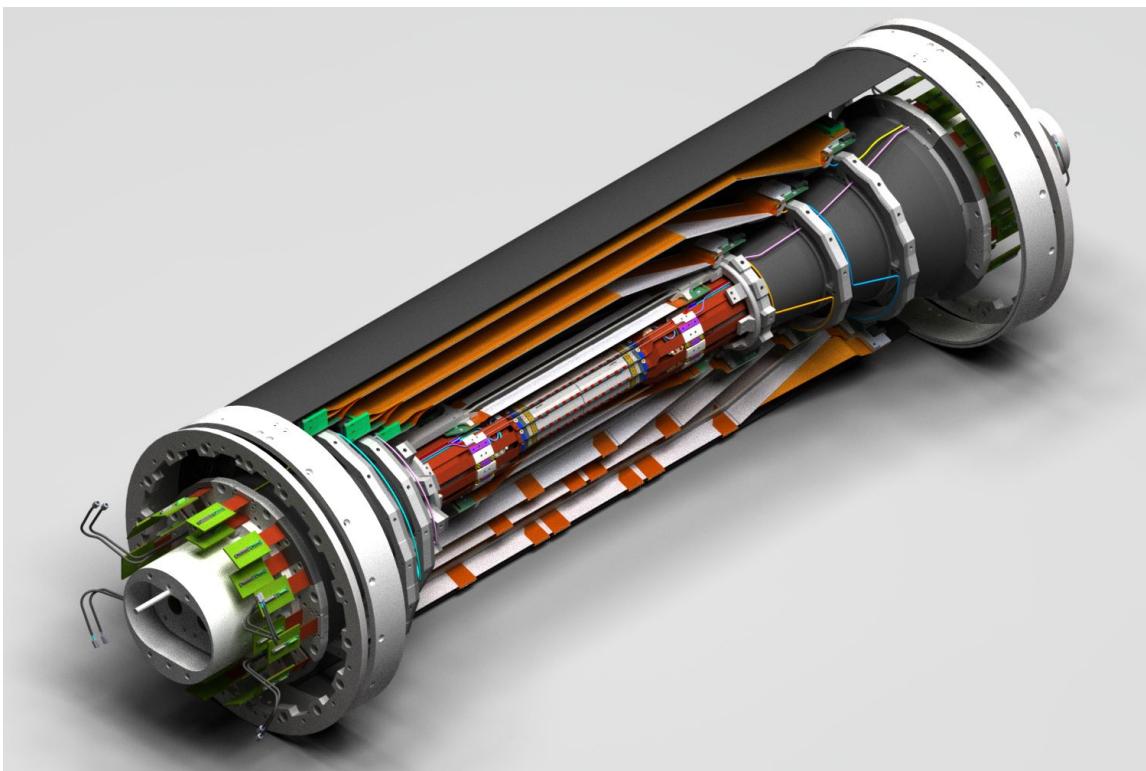
Of course, areas of interest common to hadron colliders and lepton colliders are easy to find: new silicon processing methods (through-silicon vias), novel powering schemes (serial powering and DC/DC) and new cooling schemes (micro-channel cooling) are developed in an effort that crosses the boundaries of the hadron and lepton collider communities.

The community involved in detector R & D for future lepton colliders is much smaller, but important synergies exist among the different experiments. The DEPFET collaboration, in particular, has accepted the challenge of building the Belle II vertex detector, that is to start operation in 2016. The Belle II vertex detector is shown in Figure 3, with its two layers of DEPFET-based pixel detectors surrounded by several layers of micro-strip detectors. The most important specifications for the experiments at Belle II and a future linear  $e^+e^-$  operating at  $\sqrt{s} = 500$  GeV are listed side-by-side in Table ??.

Clearly, two of the most challenging specifications - read-out speed and material budget - are very similar for Belle II and the ILC. The DEPFET-based solution for Belle II that is currently being developed by the collaboration therefore addresses several relevant challenges for ILC. In terms of radiation-hardness Belle II is a more challenging environment than the ILC.

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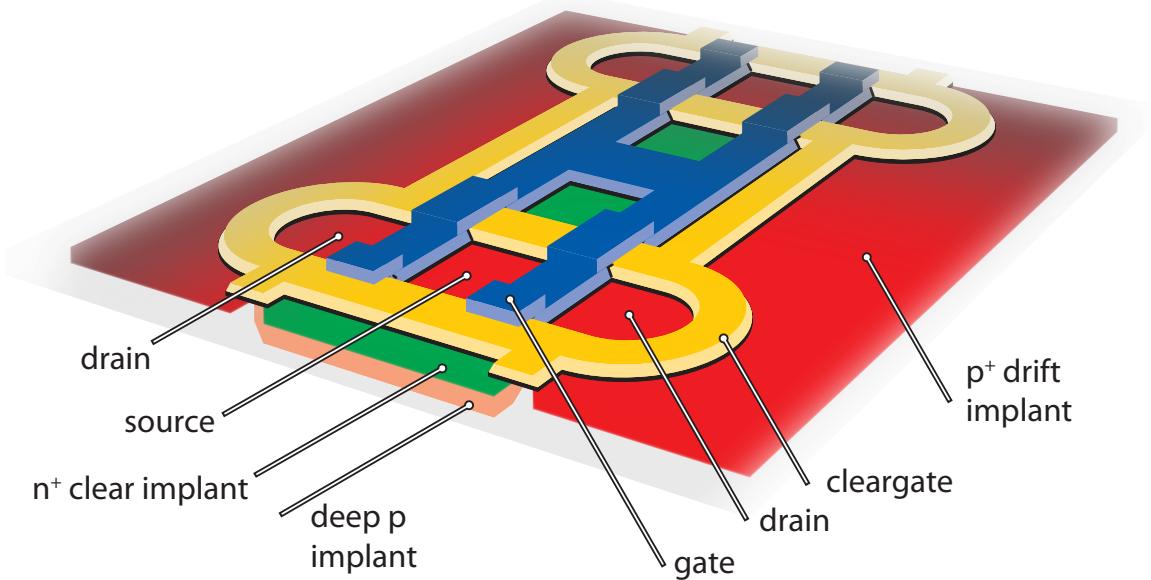
<sup>2</sup>The exception is the CLIC vertex detector that is required to time-stamp particles with approximately 10 ns precision.



**Figure 2.** The vertex detector of the Belle II experiment.

**Table 1.** Indicative specifications for the ILC500 and Belle II vertex detectors.

experiment	ILC ( $\sqrt{s} = 500$ GeV)	Belle II
particle rate		
occupancy	$\sim 0.13$ hits/ $\mu\text{m}^2/\text{s}$	0.4 hits/ $\mu\text{m}^2/\text{s}$
ionizing radiation	< 100 krad/year	2 Mrad/year
non-ionizing radiation	$10^{11} \text{ MeV} n_{eq}/\text{cm}^2/\text{year}$	$2 \times 10^{12} n_{eq}/\text{cm}^2/\text{year}$
read-out cycle		
duty cycle	1/275	1
read-out time	25-100 $\mu\text{s}$	20 $\mu\text{s}$
coverage		
particle momenta	100 MeV- 250 GeV	100 MeV - 5 GeV
angular coverage	6-174 $^\circ$	17-150 $^\circ$
precision		
spatial resolution	3-5 $\mu\text{m}$	8 $\mu\text{m}$
pixel size	$20 \times 20 \mu\text{m}^2$	$50 \times 75 \mu\text{m}^2$
material budget	$0.15\% / X_0/\text{layer}$	$0.21\% / X_0/\text{layer}$



**Figure 3.** Layout of the depleted Field Effect Transistor (DEPFET). The components of the FET - source, gate and drain - are indicated in the picture, as well as the clear contact and clear gate structure (the ring structure around the FET). The drift structure depicted here is only present in the large pixels for Belle II.

The most important difference between both experiments is maybe the angular coverage. Belle II covers a limited, and asymmetric, angular range. Supports and services for the Belle II vertex detector can be placed outside of the detector acceptance. The same is true for the  $CO_2$ -based cooling system, that is required in this machine with continuous operation. The ILC experiments, on the other hand, aim for high-performance instrumentation down to a polar angle of 6 degrees, the opening angle of the conical beam pipe envisaged for the experiments. Consequently, the ILC detector foresee pixelated disks to cover the very forward region. The material involved in supports and power and signal cables must be kept to a bare minimum. No liquid cooling is foreseen and detectors are expected to follow the 1/275 duty cycle of the machine (beam is delivered during brief  $\sim 0.7$  ms intervals every 200 ms) to reduce the *average* power consumption. To remove the heat dissipated in the detectors a forced flow of cold gas is expected to be sufficient. Petal-shaped ladder designs, pulsed powering and a cooling scheme that only relies on gas flow are among the ILC-specific challenges pursued in the collaboration.

#### 4 DEPFET active pixel detectors

A brief introduction of the Depleted Field Effect Transistor is presented in the following. For a complete discussion the reader is referred to more detailed descriptions elsewhere [27, 33].

A schematic view of the DEPFET concept is shown in Figure 3. A Field Effect Transistor (FET) is embedded in detector-grade silicon. An electric field is set up in the sensor to deplete it of free charge carriers and to ensure fast signal collection with limited diffusion.

The signal is collected on the *internal gate*, an  $n^+$  implant immediately below the FET, where it modulates the drain current. After read-out the collected signal is removed from the internal gate by applying a voltage pulse to the clear contact.

With this structure a first amplification of the signal is achieved that allows the reduction of the active detector thickness to several tens of microns while maintaining a comfortable S/N ratio for minimum ionizing particles (MIPs). The gain  $g_q = dI_{drain}/dq$  of this first stage (expressed in units of current per electron) is one of the crucial parameters of the DEPFET.

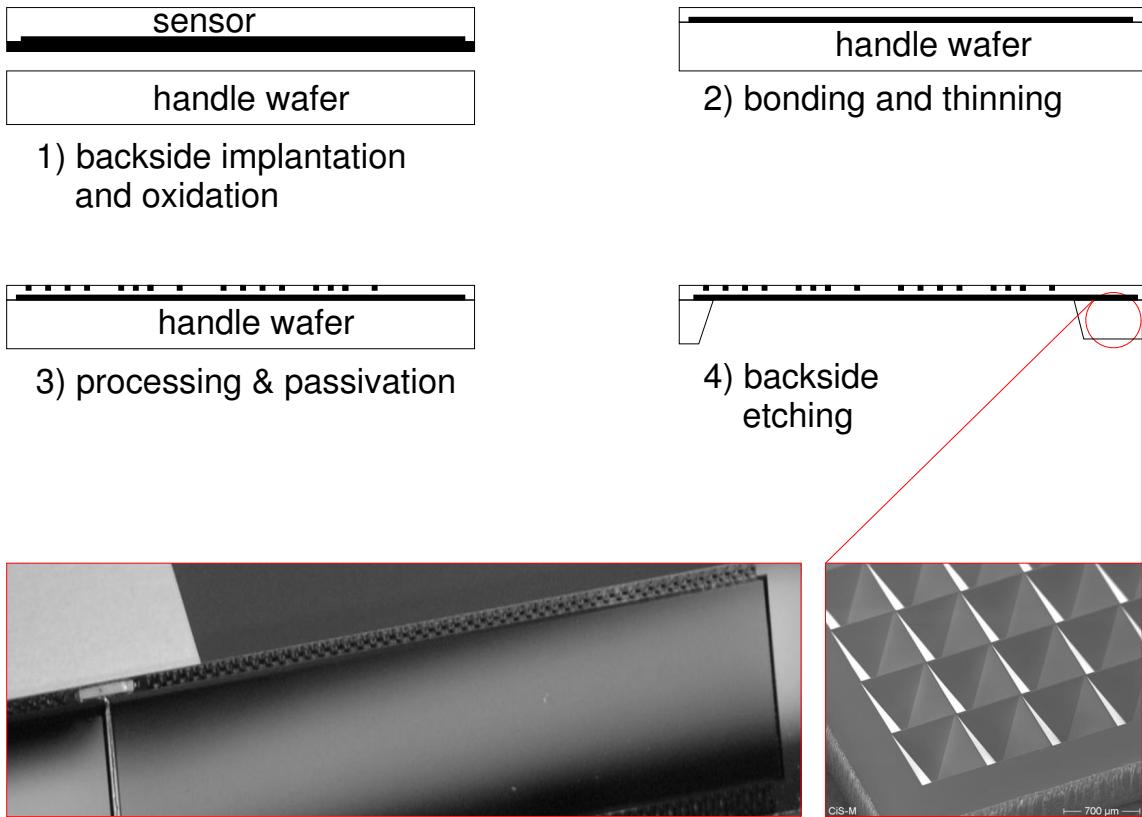
A finely segmented active pixel sensor is achieved by introducing a matrix of very small DEPFET structures on the surface of the sensor. Several read-out architectures could be envisaged. For applications such as the X-ray imagers in the XFEL all pixels are read out in parallel. In this report we focus on a read-out scheme in the rolling shutter architecture. An entire *column* of pixels is read out by a single channels on the read-out ASIC (the Drain Current Digitizer, or DCD). The design and status of the auxiliary ASICs required to operate and read out the DEPFET sensors are discussed in more detail in Section 8. Steering ASICs known as SWITCHERs are responsible for selecting subsequent *rows* of pixels. In this scheme the number of channels and interconnects is two to three orders of magnitude lower than in a fully parallel read-out architecture. The power consumption in sensor and read-out electronics is reduced proportionally.

## 5 The all-silicon ladder

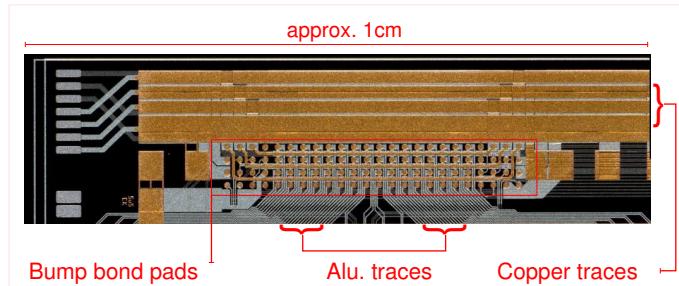
To comply with the very tight material budget the sensor must be thinned and the material in support and services must be reduced to the bare minimum. The all-silicon concept aims to achieve both by integrating active material, support structures, and the high-density interconnect in a self-supporting ladder [36, 37].

The most important process steps are illustrated in Figure 4. In the first step the backside implants are placed and the sensor wafer is oxidized. In the second step the sensor wafer is bonded to a thick handle wafer; the sensor is ground to a thickness of 50  $\mu\text{m}$  (75  $\mu\text{m}$  for Belle II). In the third step the DEPFET processing is performed on the front side. Through a final photolithographic step (deep anisotropic etching) windows are opened in the second (support) wafer below the sensitive part of the sensor. The thicker silicon around the edges of the sensor forms a support frame. A photo of the resulting ladder is shown in the same Figure. The material in the edges is further reduced in the same lithography step by introducing grooves. With the etching technique used complex structures can be produced. A good example is shown in Figure 4, which presents a scanning electron microscope image of an edge produced with this technique. The all-silicon ladders have excellent mechanical properties. The all-silicon mechanical concept is fully self-supporting and requires no external support structure over the length of the ladder. The use of a single material furthermore reduces the mechanical stress due to mismatching of thermal coefficients.

Auxiliary detector components such as the control and read-out ASICs are integrated onto the sensor using bump-bonding. Power and signal lines are routed on an additional



**Figure 4.** Illustration of the most important steps in the creation of a thin all-silicon ladder. A photograph of the ladder is also shown, as well as a scanning electron microscope image of a detail structure around the edge.

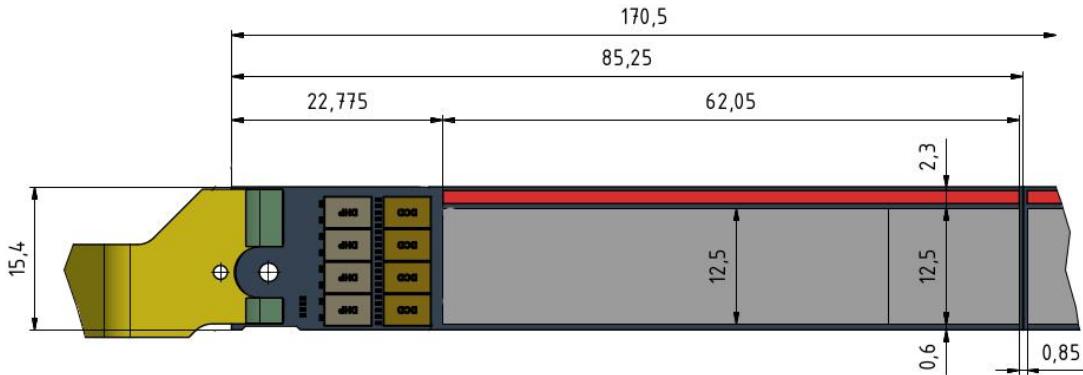


**Figure 5.** Photographs of part of the high-density interconnections in Copper and Aluminium layers on the balcony of a DEPFET ladder.

metal layer on the sensor, thus obviating the need for a separate high-density interconnect cable. A close-up image of part of the high-density interconnections on a Belle II ladder is shown in Figure 5.

## 6 A DEPFET vertex detector for the ILC

A schematic of a DEPFET ladder for the innermost layer of an LC vertex detector is depicted in Figure 6. The matrix of pixels is read out in a rolling shutter architecture, as discussed in Section 4. The SWITCHER control ASICs are located on a narrow *balcony* that stretches along the length of the ladder address subsequent *rows* of pixels. Each *column* composed of approximately 1000 DEPFET pixels is read out by two (or possibly four) channels of the DCD chip. The frame time needed to read out the complete matrix is given by the depth of the column multiplied by the time required to read out a single pixel and divided by two or four depending on the level of multiplexing.

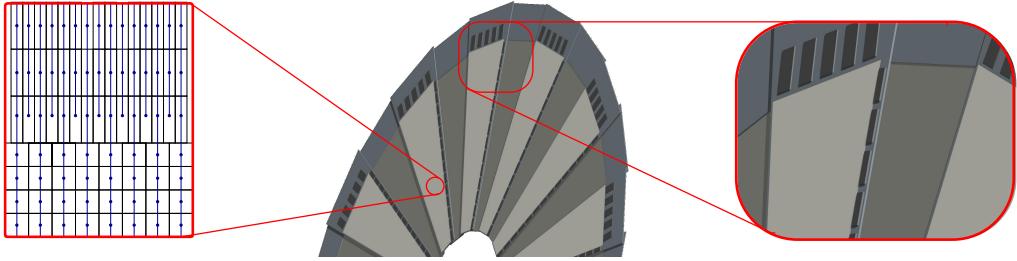


**Figure 6.** Schematic ladder layout for the innermost layer of an LC vertex detector. The end-of-ladder area that houses the read-out ASICs is visible on the leftmost side of the figure. The active area is indicated in light grey. The balcony that houses the control electronics is seen on top of the picture, running along the full length of the sensor. Dimensions are given in millimeters.

The 12.5 cm long inner layer of the ILC VXD is equipped with a single DEPFET ladder with read-out ASICs on both ends. Pixels in the center of the sensor are  $20 \times 25 \mu\text{m}^2$ . The pixel size is varied over the length of the sensor, ensuring that charge is shared over a small number of pixels independent of the z-position. The longitudinal pixel dimension is increased to  $50 \mu\text{m}$  at  $|z| = \pm 1 \text{ cm}$  and to  $100 \mu\text{m}$  at  $|z| = \pm 2 \text{ cm}$ .

In the ILD and SiD detector concepts the innermost measurements for charged particles emitted at very small polar angle are detected by pixelated disks. A conceptual design for a DEPFET-based solution for the innermost disk of the ILD Forward Tracker Disks (FTD) is presented in Figure 7. We have opted for radially oriented pixel columns, to minimize the material within the acceptance of the disks. The column pitch gradually increases towards larger radial distance from the beam line. To maintain good resolution over the area of the disk, even columns extend over the full length while odd columns only span approximately two thirds of the petal length (the blow-up of the sensor area shows this transition). The zoom image of the end-of-petal area shows the read-out chips located around the outer rim of the disk and the steering chips on a balcony along the length of the petal.

The expected performance of a DEPFET-based vertex detector for the ILC is discussed in Sections 13 through 15, after a brief presentation of the status of component production



**Figure 7.** Schematic disk layout for the vertex detector end-cap. The pixel columns are oriented radially, with a gradually reducing pitch. A blow-up of the sensor area shows the transition region where the column pitch is halved. The zoom image of the end-of-petal area shows the read-out chips located around the outer rim of the disk and the steering chips on a balcony along the length of the petal.

and their characterization.

## 7 Sensor production

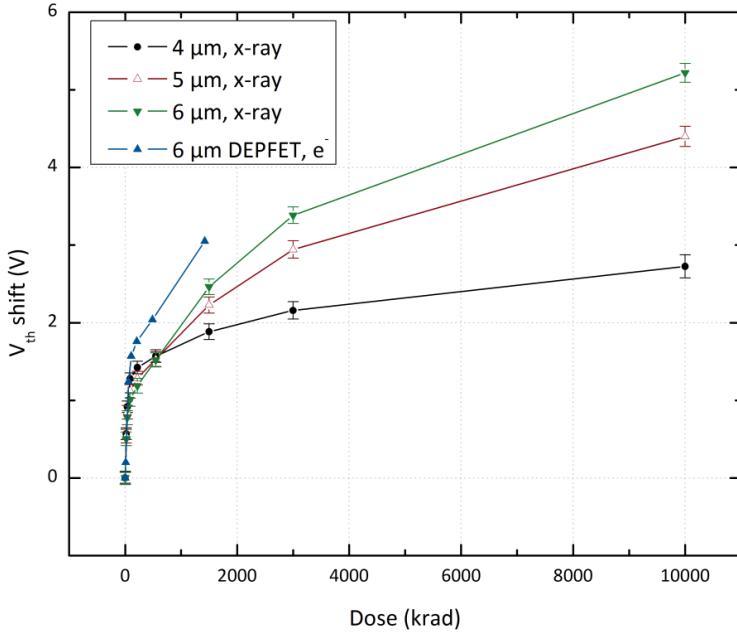
The DEPFET pixel technology contains 25 photolithographic mask steps and nine implantations. The process involves moreover very different technology aggregates like wafer bonding, Silicon-On-Insulator (SOI), double poly silicon, triple metal (including copper), back side thinning and double sided wafer processing. All processing steps except the SOI production are performed in-house.

Two early sensor production batches have proven the feasibility of small pixels down to  $20 \times 20 \mu\text{m}^2$ . The performance of the ILC prototypes constructed with these sensors is described in several previous publications [38, 39].

The more recent Belle II prototype production run (“PXD6”) was performed on an SOI wafer and all matrices were thinned to  $50 \mu\text{m}$ . Sensor designs with large pixels ( $50 \times 50 \mu\text{m}^2$  and  $50 \times 75 \mu\text{m}^2$ ) for Belle II were added to the mask, as well as further design variations of the pixel layout. The results of a characterization of these sensors are presented in Section 9.

In the Belle II experiment the vertex detector is expected to receive an ionizing dose of  $2 \text{ Mrad/yr}$  ( $20 \text{ kGy/yr}$ ) compared to less than  $100 \text{ krad/yr}$  ( $1 \text{ kGy/yr}$ ) for the inner layers of the ILC detectors [18]. With these significantly higher radiation levels radiation tolerance becomes an important factor in the design. In the production run for Belle II (“PXD9”) the gate and clear-gate dielectrics are reduced to  $100 \text{ nm}$ , approximately half the thickness used previously, to reduce the threshold shift induced by ionizing radiation. The evolution of the threshold versus ionizing dose is presented in Figure 8.

A side effect of the reduction of the dielectric is a reduction of the internal gain. According to a simple 2D model the gain of the in-pixel amplification stage has the following



**Figure 8.** The threshold shift in several test structures and a PXD6 DEPFET matrix after irradiation up to 10 Mrad. Further details are to be found in Reference [40].

relation with the layout parameters of the FET:

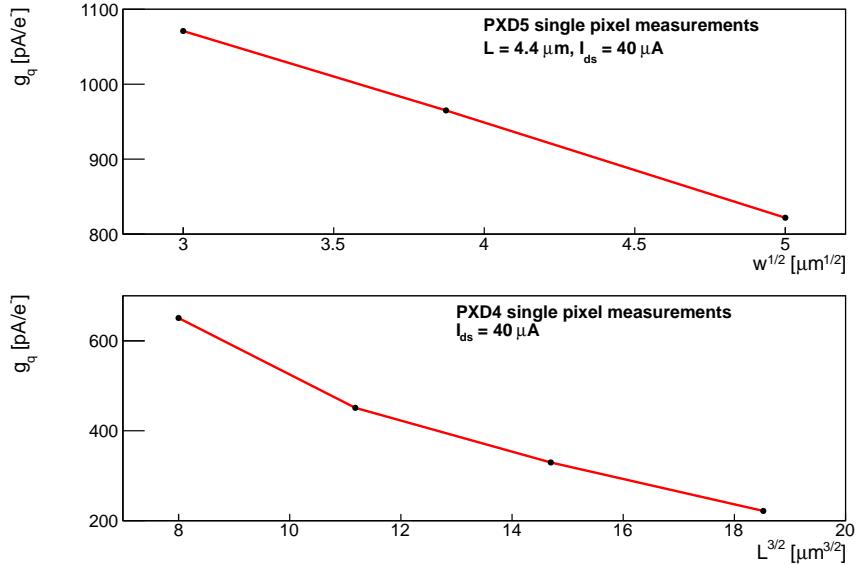
$$g_q \propto \frac{I_{ds}^{1/2} \times t_{ox}^{1/2}}{w^{1/2} \times L^{3/2}} \quad (7.1)$$

A particularly strong dependence is predicted for the length of the gate  $L$ , its width  $w$  and the oxide thickness  $t_{ox}$ . and on the drain-source current  $I_{ds}$ . This relation is found to hold approximately <sup>3</sup> in measurements of single-pixel gain measurements from References [41, 42], as shown in Figure 9. Measurements on large matrices confirm the findings here, albeit with lower statistics [32].

The internal gain of the sensor is partially recovered by modifying these other parameters of the FET layout. A more precise process for the production of the FETs can potentially yield a substantial increase of the gain of the in-pixel amplification stage (which leads to a proportional increase of the signal-to-noise ratio of the system and allows to further reduce the active sensor thickness).

The PXD9 production run for Belle II is currently ongoing. A preliminary yield estimate can be based on the tests performed on the wafers before the metallization steps. The results in Table 2 correspond to the point in the production process after 14 mask steps and 10 implantations, but before the deposition of the 3 metal (two Al, one Cu, 7 mask steps) and the backside thinning. Two types are distinguished: long ladders that are located at the center of the mask, and shorter ladders on the edge of the wafer. If ladders are affected that show either no defects, or a defect that affects a single pixel, the yield at this stage is

<sup>3</sup>For too large drain current the implicit assumption of constant carrier mobility is known to fail.



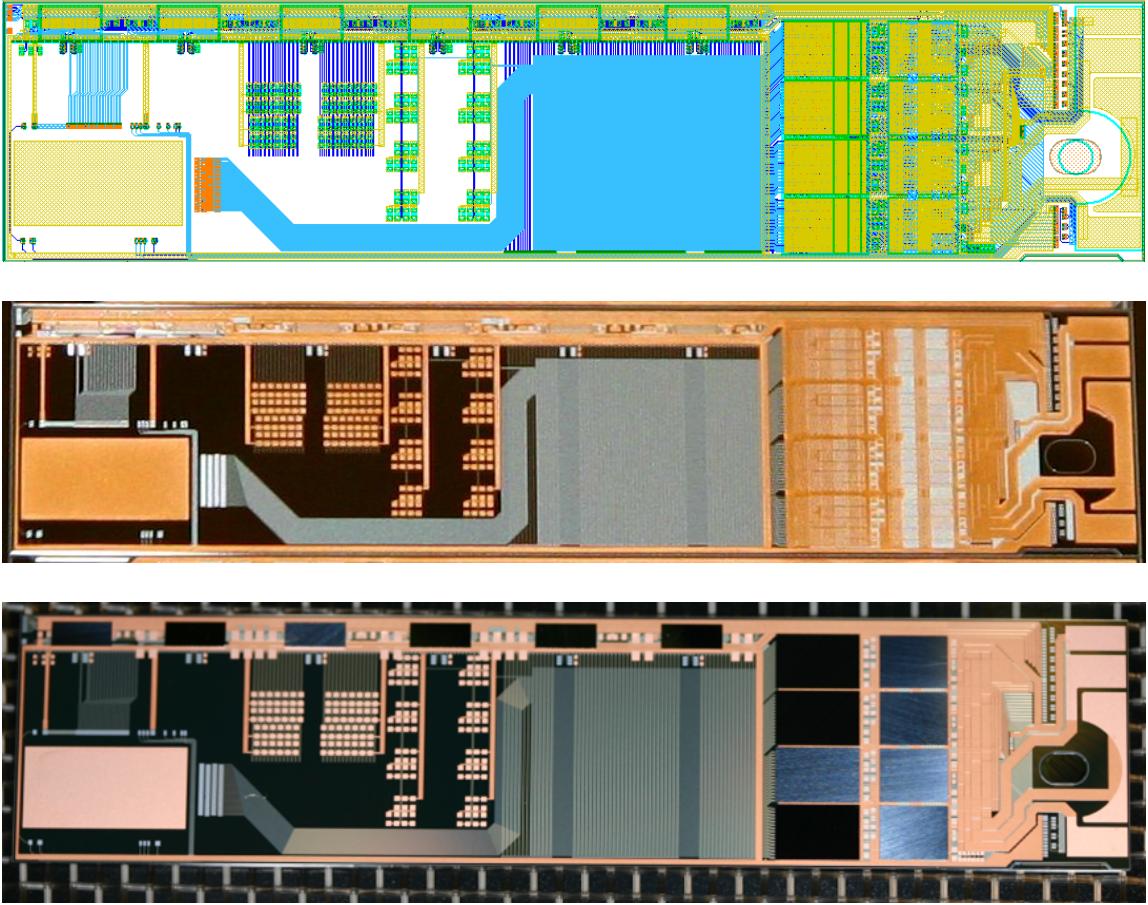
**Figure 9.** Gain measurements on single-pixel structures. The axes are chosen such that, according to Equation 7.1, the measurements should lie on a straight line.

**Table 2.** The yield in % of the most recent production run for the Belle II vertex detector. The six rows correspond to different sensor types and/or different locations on the wafer.

position	no defects	single	defective	likely	certain	unknown
position		pixel	row/column	module loss	module loss	impact
wafer edge	41	21	7	10	3.4	21
wafer center	47	15	11	6	2.6	20

slightly over 60%. Adding ladders with single defective rows or columns (leading to a loss of less than 1% of the ladder efficiency) the yield increase to over 70%. Possibly, a fraction of approximately 20% of ladders in the category “unknown” can be recovered once the impact of the defect is clarified.

Before proceeding with the final stages of the sensor production, the design of the metal layers is validated by producing electrical multi-chip modules (EMCMs). These contain all metal lines for the routing of signal and power lines and the bump bond pads for the connection to the read-out and steering ASICs. Solder pads for passive components (capacitors for decoupling and termination resistors for LVDS lines) are also implemented. No pixels are implanted, however, and the area reserved for the matrix of DEPFET pixels is filled with a number of test circuits. An image of the design and two photographs of recently produced EMCMs are presented in Figure 10. In the design the landing areas of the DCD and DHP are visible as yellow regions in the end-of-ladder area on the right-hand side of the image. The SWITCHERS are to be bump-bonded on the balcony that extends along the upper edge of the image. In the bare EMCM of the central panel the two metal layers are clearly visible, the Aluminum in light gray and the Copper layer in the characteristic



**Figure 10.** The electrical multi-chip module design (upper panel), a photograph of a bare EMCM (central panel), and the same module after flip-chip bump-bonding of the SWITCHER, DCD and DHP ASICs (lower panel).

reddish hue. The lowermost panel shows the EMCM after flip-chip bump-bonding of the SWITCHER, DCD and DHP ASICs.

The assembled EMCMS are connected to a test setup through a Kapton adapter cable and submitted to an exhaustive set of checks and measurements to verify the correct operation of the chips. The first, preliminary results indicate the chips integrated on the EMCM are fully functional, with a performance that is similar to that found when tested in isolation.

## 8 Control and read-out ASICs

Several auxiliary ASICs are required to operate the DEPFET sensor. The most important developments are briefly summarized in this Section.

The SWITCHER control chips select segments of the sensor (pairs of rows or 4-row segments) for read-out. A separate driver supplies the *clear* pulse to remove the collected signal from the internal gate after read-out.

The SWITCHERB18 design in 180 nm AMS/IBM HVCmos is smaller than its 350 nm predecessor and radiation hard to 36 Mrad. It can produce pulses with a maximum swing of 20 V in a voltage range of 50 V. Measurements show that the current SWITCHER chips can drive long lines, up to loads well beyond the requirements of the Belle II and LC vertex detectors.

The drain current signals from a column of pixels are processed and digitized by a channel of the DCD (Drain Current Digitizer [43–46]) chip. The analog input stage keeps the column line potential constant (necessary to achieve fast readout), compensates for variations in the DEPFET pedestal currents, and amplifies and shapes the signal. The current receivers in the most recent DCD versions are based on transimpedance amplifiers (replacing the regulated cascodes of earlier generations). The analog signal is digitized using (one or two) ADCs with a (combined) sampling frequency of 10 MSamples/s. The DCD can be operated in double correlated sampling mode or single sampling mode. The latter is preferred as it allows higher read-out speed.

The DCD is implemented in UMC 0.18  $\mu\text{m}$  CMOS technology using special radiation hard design techniques (e.g. enclosed NMOS gates) in the analog part. The 256-channel DCDB has an area of  $3.2 \times 5 \text{ mm}^2$ . The chips are found to resist an ionizing radiation dose of 20 Mrad, well in excess of the ILC requirement. The analog response of early DCD2 prototypes was characterized in detail [46, 47] on a test system where DCD and SWITCHER are connected to a full-size DEPFET sensor. The DCDB produced for Belle II has been shown to be fully functional at the nominal 320 MHz, that corresponds to a row read-out time of 100 ns, with a noise level of 35 nA. The change from the two cyclic ADCs of previous versions to a single ADC with a pipeline architecture in the most recent design allow for a reduction of the read-out speed. First tests at 500 MHz, corresponding to a row read-out time of 64 ns, show that chip remains functional at that speed.

The derandomized raw data from the DCD are transmitted to the Data Handling Processors (DHP [48]) using fast parallel  $8 \times 8$ -bit digital outputs. This third ASIC, located on the end-of-ladder area immediately behind the DCD, performs data processing (pedestal subtraction, common mode correction), compression (zero suppression), buffering and fast serialization. It furthermore controls the other read-out ASICs. The first full-scale DHP prototype were implemented in IBM 90 nm CMOS technology. Recently, the new DHPT1.0 was produced in the TSMC 65 nm process, tested and found fully functional. The DHP is radiation-hard to 100 Mrad.

Recent results on the performance of the DHP are presented in Reference [49]. In a test system with a SWITCHER and DCD chip several aspects of the DHP performance were verified:

- the DHP is capable of controlling the SWITCHER operation and sequence, thus forming a slow-control interface on the ladder
- the communication between DCD and DHP is demonstrated at full speed, with no data loss up to an occupancy of approximately 3%

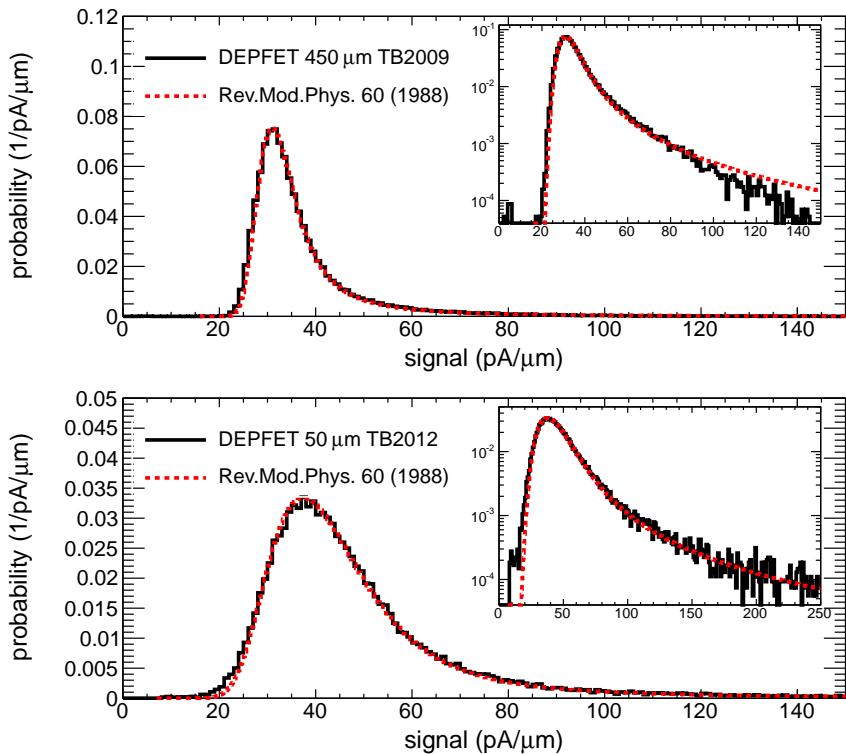
- the DHP can drive 15 m of infiniband cable to form the serial link to the off-detector electronics

In the longer term a single chip is to perform the analog functions of the DCD and the digital processing of the DHP.

The first full-size ladder equipped with SWITCHER, DCD and DHP chips was successfully tested in the combined beam test at DESY in January 2014. The results from this important milestone for the collaboration are reported in the next Section 10.

## 9 Characterization of prototypes

The response of DEPFET sensors from the PXD5 and PXD6 production has been characterized in beams of charged particles from accelerators at CERN and DESY [38, 39, 50, 51]. In these tests the DEPFET response is compared to the reference trajectory of particles reconstructed with a precise beam telescope <sup>4</sup>.



**Figure 11.** Signal distribution for a  $450\ \mu\text{m}$  thick DEPFET sensor (upper panel) and for a sensor thinned to  $50\ \mu\text{m}$  (lower panel). In both cases the measurement is expressed in pA per micron of active silicon. The measurements are compared to the prediction for the energy deposition in thin silicon layers of H. Bichsel [52]. The inset shows the same distributions on a logarithmic scale and with an extended axis range.

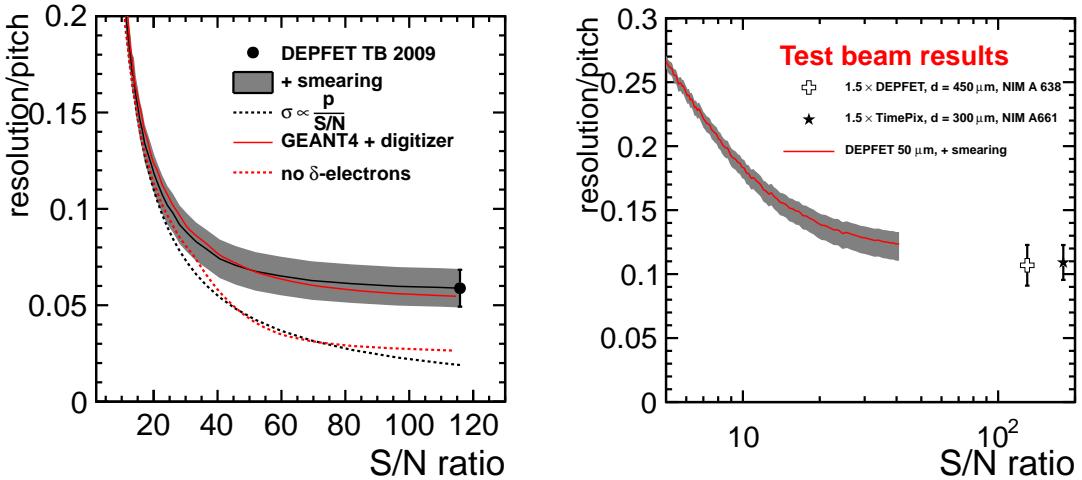
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<sup>4</sup>The EUDET and AIDA projects (grant agreements 26126 and H262025) have provided crucial infrastructure to perform these tests

The DEPFET drain current distributions due to perpendicularly incident 120 GeV pions from the CERN SPS are shown in Figure 11. The upper panel corresponds to a 450  $\mu\text{m}$  thick ILC-design “PXD5” sensor with a  $20 \times 20 \mu\text{m}^2$  pixel size. The lower panel presents the result for a Belle II design PXD6 sensor thinned to 50  $\mu\text{m}$  with  $50 \times 75 \mu\text{m}^2$  pixels. The signal in adjacent pixels is added using a simple clustering algorithm with a neighbor cut of  $2.6 \sigma$  [53]. The measured shape is in good agreement with the prediction for the energy deposition in thin silicon layers of H. Bichsel [52]. The quantum gain  $g_q$  of the sensors obtained (assuming an ionization potential of silicon of 3.62 eV and using the measured gain of the read-out chips) is found as 340  $\text{pA}/e^-$  for the 450  $\mu\text{m}$  thick sensor, in good agreement with the result of a calibration with a  $\gamma$  source, and 470  $\text{pA}/e^-$  for the thin sensor. Both results agree with the expectation from Equation 7.1.

The uniformity of the signal over the area of the sensor has been evaluated in beam tests of PXD5 devices with approximately 8000 pixels and 4 or 5  $\mu\text{m}$  gate length. A spread of  $5\% \pm 3\%$  is observed for the sensor with  $L = 4 \mu\text{m}$ , and of less than 3% for  $L = 5 \mu\text{m}$ , that has negligible impact on the detector performance.

As a key parameter, the spatial resolution of DEPFET devices has been studied exhaustively. Thick DEPFET sensors with an ILC pixel design (thickness  $\times$  pixel size of  $450 \times 20 \times 20 \mu\text{m}^3$ ) approach a 1  $\mu\text{m}$  resolution in the measurement of both coordinates [38, 39, 54]. At this level the resolution is limited by the physical processes responsible for the signal generation. The emission of  $\delta$  electrons limits progress beyond 1  $\mu\text{m}$  for perpendicular incidence [55], as shown in Figure 12.



**Figure 12.** The spatial resolution divided by pixel size for 120 GeV pions from the CERN SPS perpendicularly incident on a 450  $\mu\text{m}$  thick DEPFET device with a 24  $\mu\text{m}$  pixel size (leftmost panel) and for 3.75 GeV electrons traversing a 50  $\mu\text{m}$  thick DEPFET device with 50  $\mu\text{m}$  pitch under a 45° angle (rightmost panel). Data points are indicated by solid markers corresponds to the nominal measurement. The curves with the grey error bands are obtained by smearing the signal. The result is compared to the expected evolution for an idealized detector and to a GEANT4 simulation with and without  $\delta$ -electron emission.

The thin Belle II design sensors with  $50 \times 50 \times 75 \mu\text{m}^3$  pixels yield a spatial resolution of  $8 \mu\text{m}$  [53] for perpendicularly incident tracks, in good agreement with the expected performance. For inclined tracks the variations in the energy deposited in neighbouring pixels (Landau fluctuations) limit the performance even for such thin sensors <sup>5</sup>.

The response of DEPFET sensors has been modeled in detail in a *digitizer* model. It has been shown [27, 55] to reproduce the beam test results of a broad variety of devices, with sensor thicknesses ranging from 50 to  $450 \mu\text{m}$  and pixel dimensions from  $20 \times 20 \mu\text{m}^2$  to  $50 \times 75 \mu\text{m}$  to very good precision. We therefore trust that it can be used to predict the performance of devices with parameters that lie within these ranges.

## 10 First operation of a large-scale DEPFET ladder

In December 2013 and January 2014 the first large-scale DEPFET ladder was operated in a beam of particles at DESY. A schematic layout of the set-up is shown in Figure 13 on the next page. A photograph of the ladder is shown in the same Figure. It consists of a DEPFET sensor with  $480 \times 192$  pixels, with a  $50 \times 75 \mu\text{m}^2$  pixel pitch, resulting in an active area of  $36 \times 9.6 \text{ mm}^2$ .

The active area of the sensor (visible as the beige area in the center of the PCB) in the photograph, is thinned down to  $50 \mu\text{m}$ . The read-out ASICs are bump-bonded to the end-of-ladder in the leftmost part of the sensor. Closest to the active sensor area are the three DCDs. The three DHPs are mounted right behind them. Four SWITCHERs are bump-bonded on the balcony that forms the lower edge of the sensor.

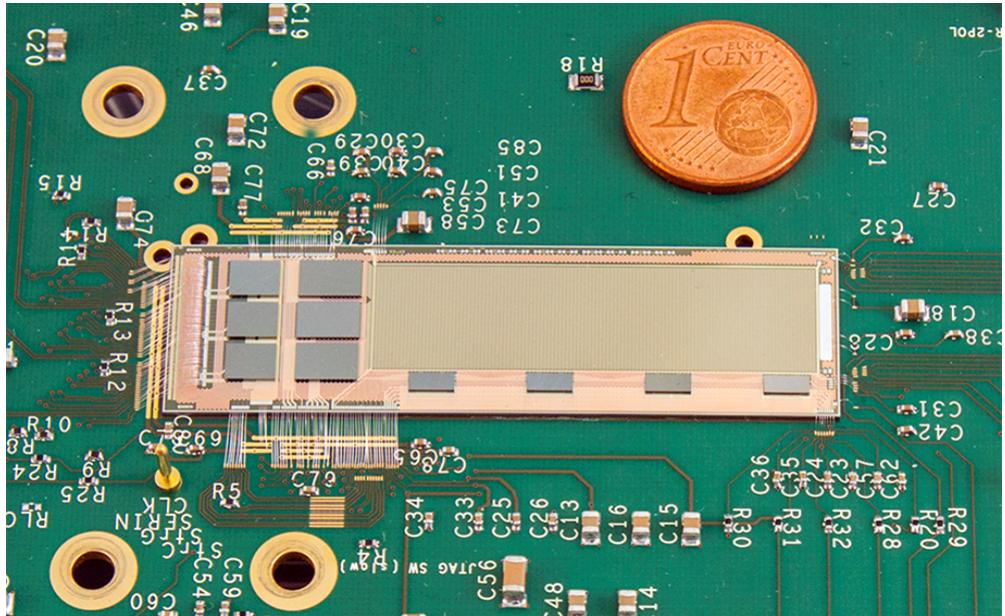
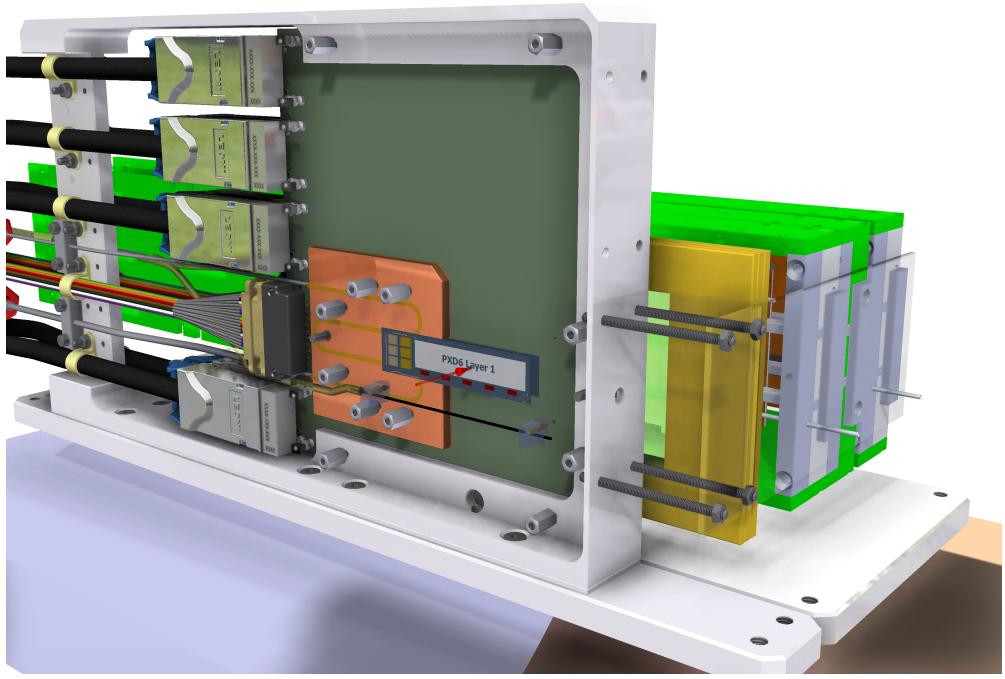
The goal of the test beam period was the combined operation of a small sector of final-design components of the Belle II vertex detector; namely, a thin close-to-final size DEPFET sensor and 4 SVD single module layers, arranged in a configuration that mimics the final Belle II vertex detector geometry (Figure 13).

The readout of such detector system was performed using a scaled version of the final full DAQ chain. The detectors were biased using the power supply prototypes with full length services (15 m for data and power)). The cooling consisted on bi-phase CO<sub>2</sub>, delivered into the detector chamber after 15 m long distribution lines from the cooling plant (a minimum of -18 °C was reached). In addition, a full set of environmental monitors (temperature and humidity) based on commercial sensors and calibrated optical fiber with Bragg structures were installed and integrated into the fully developed slow control system.

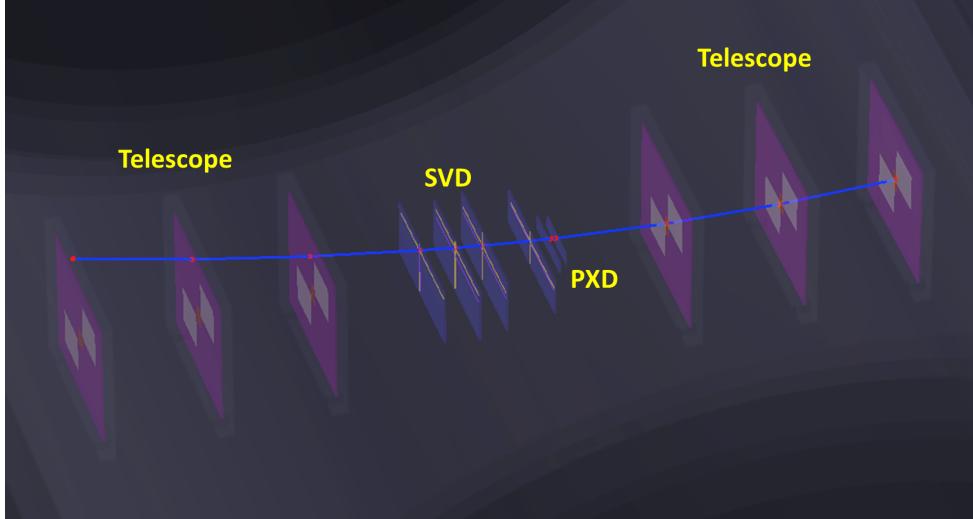
The beam test set-up was inserted in the PCMAG magnet that provides a 1 Tesla magnetic field. The event display of Figure 14 shows the reconstructed trajectory of a 5 GeV electron after entering the detector chamber through the magnet outer wall. The information contained in the micro-strip detector is used to reconstruct the track of the particle. The track is further extrapolated to the DEPFET sensor and a hit was found at the intersection between the track and the DEPFET active area. The electron also leaves a signal in the six telescope planes. Analysis of the data is ongoing at the time of writing and no quantitative results beyond basic distributions (hit maps, signal distributions) that

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<sup>5</sup>The plots in Figure 12 are reproduced from Reference [55], with permission from the authors.



**Figure 13.** The set-up of the December 2013–January 2014 beam test in a positron beam at DESY (uppermost panel). The DEPFET ladder is visible in the center of the image. The first large-scale DEPFET ladder (lowermost panel). The active area of the sensor is visible as the beige area in the center of the PCB. The balcony (lower edge of the sensor) is equipped with four SWITCHER ASICs, the end-of-ladder with three DCD and DHP ASICs (leftmost side of the ladder).



**Figure 14.** Event display with the reconstructed trajectory of a positron that leaves a signal in, from right to left, three telescope planes, the DEPFET ladder, four micro-strip detectors, and the three telescope planes of the second arm.

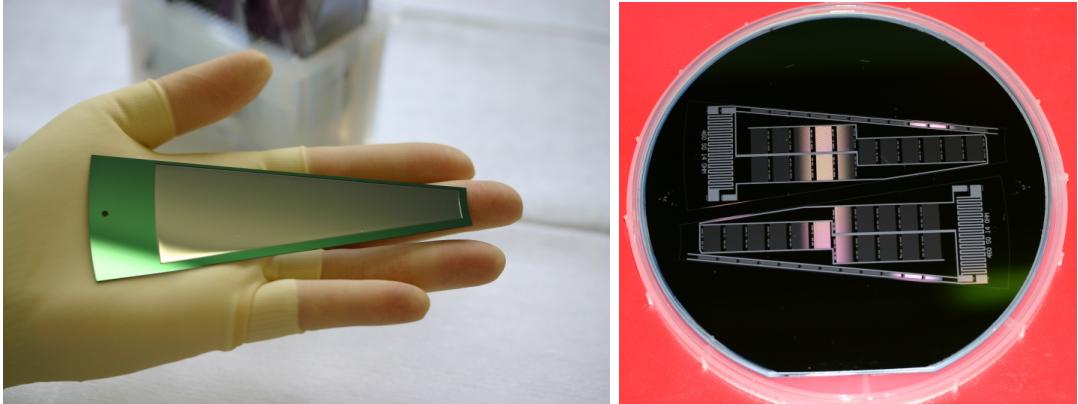
show that the DEPFET system indeed detected particles are available. This first full ladder corresponds to the Belle II design, but this achievement marks an important milestone also for the DEPFET-ILC project.

## 11 Thermal & mechanical tests of mechanical prototypes

Maintaining good thermo-mechanical performance within the tight material budget for the vertex detector of the ILC experiments represents a severe challenge. In recent years the collaboration has performed an exhaustive set of tests to characterize the mechanical performance (stiffness) of the all-silicon ladder. A complete thermo-mechanical mock-up has been built for the Belle II experiment, that allows to gain hands-on experience with cooling through a forced flow of cold gas in a realistic environment [56, 57].

In this Section we present a few recent results on the ILC petals of Figure 15. These are mechanically identical to all-silicon ladders, but lack all implantation steps. Resistor circuits are implemented in a single metal layer that mimic the power consumption of the sensor and on-ladder ASICs.

The mechanical rigidity of the sensor is measured using a precise coordinate measurement machine and a jig that ensures reproducible placement of the sensor on standard supports and of a set of weights in the center of the sensor. The deformation per unit force is registered for the mechanical samples ( $1.5 \text{ mm/N}$ ) and a reference silicon wafer of the same dimensions, but with a constant thickness of  $450 \mu\text{m}$  ( $0.55 \text{ mm/N}$ ). With over four times more material, the thick silicon wafer is only 3 times more rigid than the thin sample, in good agreement with the expectations from a Finite Element simulation. The thin sample is expected to be 23 times more rigid than a petal with a uniform thickness of  $115 \mu\text{m}$  (that amounts to the same average contribution to the material budget).



**Figure 15.** A mechanical sample for an FTD petal. The thinned section is visible as the grey area surrounded by thicker, green rims. The rightmost panel shows the *heater* circuits on two mechanical samples before wafer cutting.

The mechanical samples are exposed to the nominal power dissipation of the sensor and ASICs, with the ILC duty cycle of 1/200. The temperature of the center of the sensor is monitored with an IR camera with a frame rate of 100 Hz. Even faster variations are monitored with Bragg fibers sampled at 1 kHz<sup>6</sup>. We find that changes in the temperature of the ladder in response to a sudden increase or decrease in the thermal load have a typical time constant of 3 seconds. Without active cooling, the temperature of the sensor increases by less than 1 degree for the nominal 1/200 ns duty cycle,. The mechanical deformation of the sensor follows the temperature, with the same time constant of  $\sim 3$  s. No evidence is found for fast excursions of the temperature or deformations beyond those expected from the slow thermal expansion.

## 12 Micro-channel cooling: Proof of principle

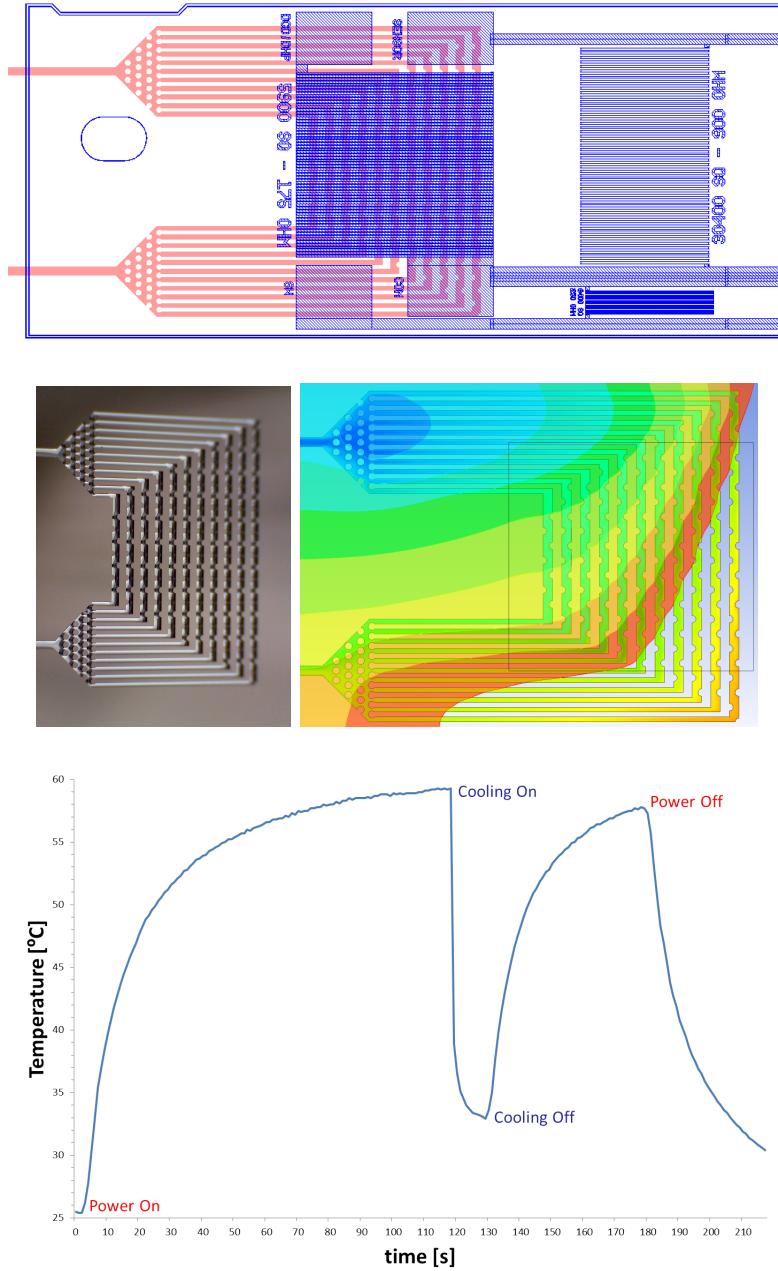
The baseline cooling concept of the ILD vertex detector concepts rely on forced convection with cold air as a coolant, chosen for its simplicity and low impact on the overall detector material. With the expected power consumption a forced gas flow is deemed adequate. The experience with the Belle II mock-up and simulation has strengthened confidence in the concept itself and the tools to design a working system. However, a rigorous proof-of-principle of the cooling concept based on forced gas flow only is still lacking, and no practical way of setting up the flow in the forward region has yet been presented.

Due to its higher heat transfer coefficient, the option to indirectly cool the front end electronics via micro-channels directly machined into the handle wafer is being investigated. It is relatively straightforward to extend the DEPFET process with a mask step that creates micro-channels in the thicker end-of-ladder areas, where most of the power is dissipated (Figure 16). The heat conduction volume can be increased by adding protrusions

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<sup>6</sup>Access to the Bragg fiber setup, and the construction of the pulsing power supply, were made possible by the AIDA project.

to the channels and additional staggered fins were introduced to homogenize the liquid flow through the channels as well as to serve as an additional compact heat exchangers.



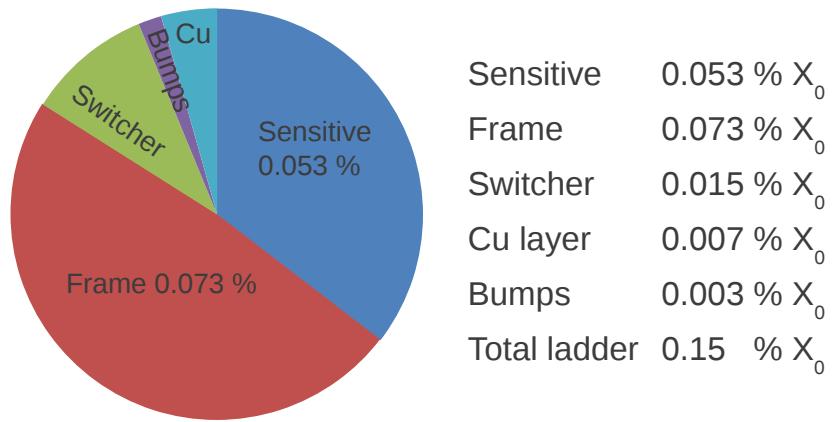
**Figure 16.** Uppermost panel: the micro-manifold design (in red) in the end-of-ladder of a mechanical DEPFET sample. Leftmost panel on the central row: photograph of the micro-cooling circuit in the handle wafer before bonding of the top (sensor) wafer. Rightmost panel of the central row: finite-element simulation of the CO<sub>2</sub> flow and resulting temperature for a nominal power load and a 1/25 duty cycle. Lowermost panel: time evolution of the end of the ladder temperature.

To prove the principle and validate the finite-element model, a mechanical sample was

exposed to a continuous load of  $2.5 \text{ W/cm}^2$  in the resistor circuit on the silicon surface. The evolution of the temperature with time is presented in Figure 16. Without active cooling an equilibrium temperature is reached of over 60 degrees C, that exceeds the limits for a safe detector operation. Once a modest mass flow of 0.1 l/h of water is circulated through the channels (corresponding to a pressure drop of less than 2.5 bar) the surface temperature decreases in a matter of seconds to less than 10 °C above the temperature of the water and surrounding air.

### 13 Expected performance: material budget

The ILC experiments require that the vertex detector should be as transparent as possible. The contribution of the ladder design presented in Section 6 is estimated in Figure 17. The total contribution is broken down among the components with the most important contributions. The ladder material (averaged over the ladder area) is equivalent to  $\sim 0.15\% X_0/\text{layer}$ .



**Figure 17.** Break-down among the detector components of the material expressed in units of radiation lengths over the acceptance of the all-silicon ladder design.

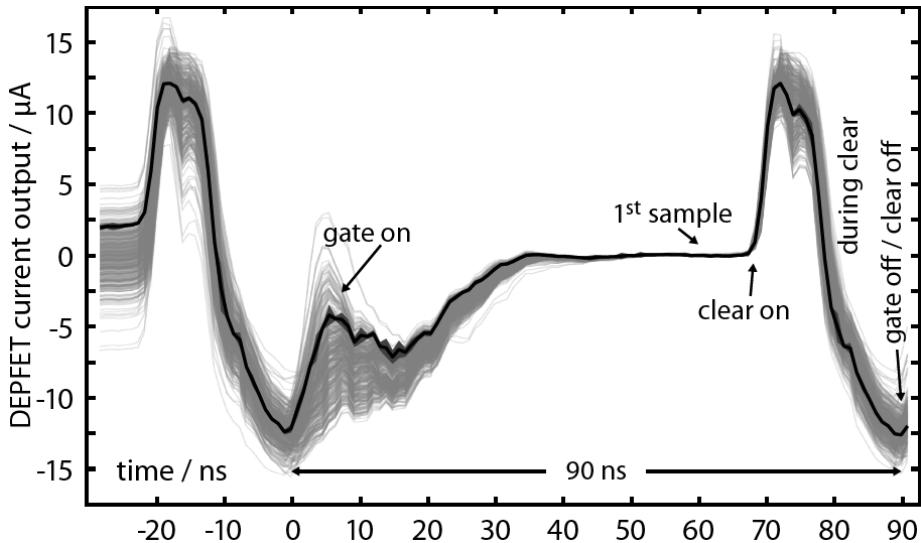
The fully engineered Belle II design [27] corresponds to  $0.21\% X_0/\text{layer}$  over the active area. The further reduction of the LC budget is achieved by a more aggressive thinning of the sensor. The thickness of the active material, one of the dominant contributions, is reduced from  $75 \mu\text{m}$  to  $50 \mu\text{m}$  (as already achieved in the Belle II prototype production run). The support frame is reduced from  $450 \mu\text{m}$  to  $400 \mu\text{m}$ .

The LHC experiments obtain maps of the detector material using a number of methods, based on conversions, nuclear interactions and multiple scattering angle. Members of the collaboration have extended the latter approach to beam tests for the first time. The results -  $0.16 \pm 0.03\% X_0$  for the material in the thin DEPFET sensor ( $50 \mu\text{m}$  of silicon + thin metal layers) and two Aluminium foils.

## 14 Expected performance: read-out speed

In the innermost layers of the vertex detector the occupancy due to pair background forces multiple read-outs during the bunch train. In the outermost barrel layers and the forward tracking disks the background level is two order of magnitude lower.

In a DEPFET-based vertex detector, the time to read out a complete *frame* (i.e. the time for the rolling shutter to complete a cycle through all rows of the DEPFET matrix) depends on the column depth and the time required to sample and clear a single row of pixels. A row rate of 1/80 ns was achieved with the first complete DCD chip reading out a full-length column. The drain current during a clear-read-out-clear cycle is presented in Figure 18. The long plateau before the first sample shows that there is ample margin to improve the row rate. We take 1/80 ns as a conservative estimate.



**Figure 18.** The DEPFET drain current (in  $\mu\text{A}$ ) versus time (in ns) during a 90 ns read-out cycle. In the time window that is shown the signal on the internal gate removed by applying a clear pulse, read out and cleared once more.

In the layout of the innermost layer presented in Section 6 the columns have a depth of 1025 pixels per half-ladder. With two rows sampled in parallel this implies a read-out time for a complete frame of 40  $\mu\text{s}$  for the innermost layer.

For Belle II, with twice larger pixel size, four-fold multiplexing is used to speed up the read-out. With an additional metal layer on the sensor to route the required extra signal lines one could envisage four-fold multiplexing also for the ILC. This results in a factor two in read-out, i.e. a frame read-out time of 20  $\mu\text{s}$  for the innermost layer.

## 15 Expected performance: spatial resolution

Using an extensive set of beam test results on both types of devices, a detailed model of the DEPFET response has been developed for use in simulations of the overall detector

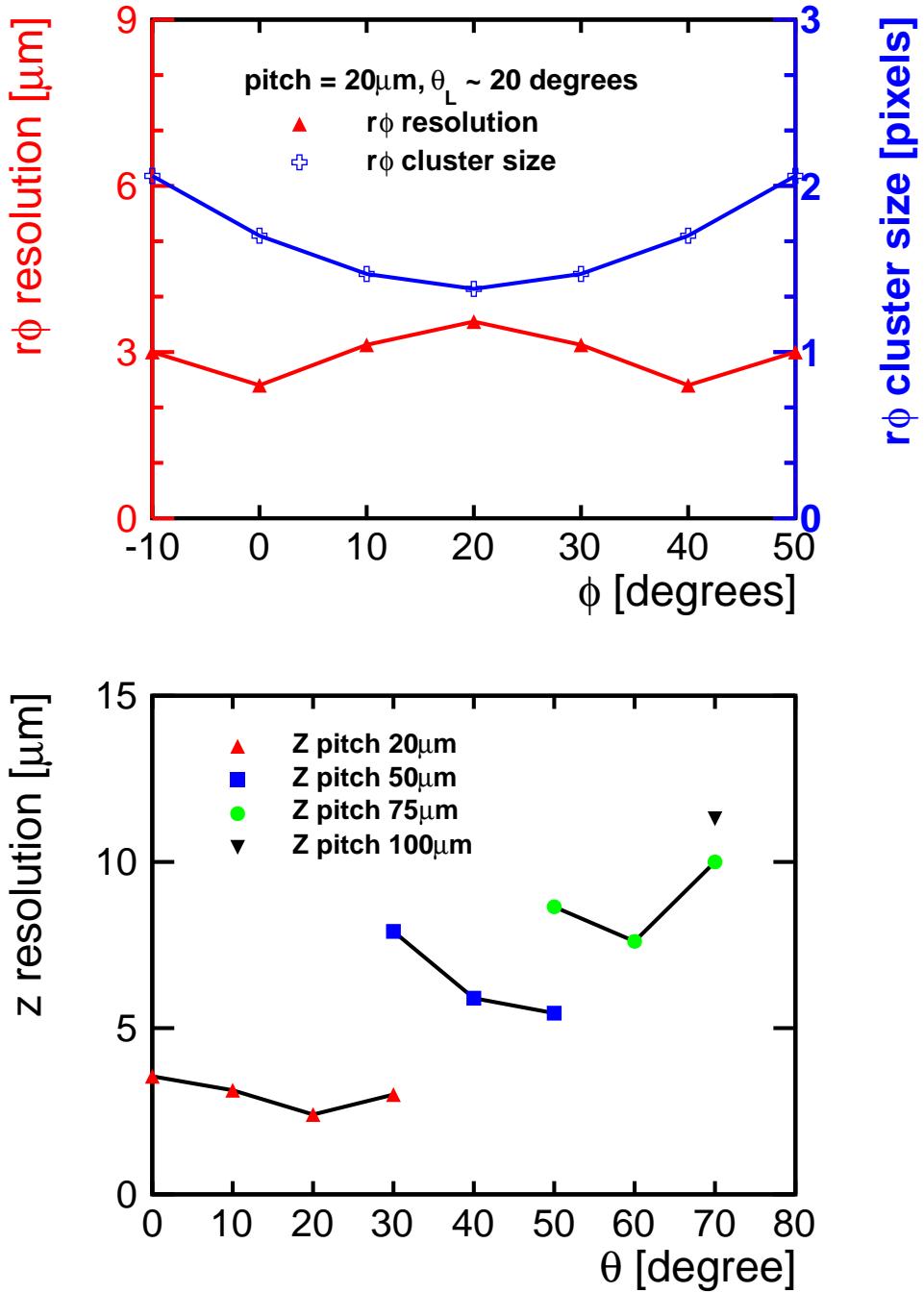
performance. The model is able to reproduce the signal sharing in neighbouring DEPFET pixels to good accuracy.

This *digitizer* model is used to predict the spatial resolution of an LC-design DEPFET sensor with a detector thickness of  $50\ \mu\text{m}$ . The estimates for the signal amplification and noise performance in the model are based on achieved results. The performance could improve significantly if further R&D finds a way to increase either parameter.

The model is used to predict the resolution of the  $r\phi$  coordinate (crucial for the transverse momentum and transverse impact parameter measurement) and that of the  $z$  measurement (the coordinate parallel to the beam line). The expected dependence of both on the incidence angle is shown in Figure 19. Under perpendicular incidence, and in the absence of a magnetic field, a DEPFET device with  $20 \times 20\ \mu\text{m}^2$  pixels on a  $50\ \mu\text{m}$  thick sensor is expected to achieve a spatial resolution of  $3.5\ \mu\text{m}$ . In a magnetic field of 3.5 to 5 Tesla, as envisaged by the ILC detector concepts, the carrier trajectory in the silicon is affected by the Hall effect. For a  $50\ \mu\text{m}$  thick sensor under a 25 V bias voltage, the expected Lorentz angle is approximately 20 degrees (prediction of the model in Reference [58] for a 3.5 Tesla field; the Lorentz angle is approximately proportional to the magnetic field). The average cluster dimension along the  $r\phi$  direction (i.e. counting only the number of columns that contribute to the cluster, independent of the number of rows) is shown in blue in the upper panel of Figure 19). The charge sharing reaches a minimum, with an average 1.3 columns containing the signal, when the track incidence angle exactly compensates for the Lorentz angle. For tracks at different angles the additional charge sharing between pixels helps to improve the resolution, reaching a resolution of  $2.3\ \mu\text{m}$  for an average cluster size along  $r\phi$  of 1.7.

The resolution of the  $z$ -coordinate measurement is presented in the lower panel of Figure 19. Very shallow tracks are expected towards the end-of-ladder of the barrel vertex detector. The spatial resolution in such cases is limited by *Landau fluctuations*, variations in the signal deposited in each pixel (see Reference [55] for a quantitative discussion). The results of several assumptions on the longitudinal dimension of the pixels are shown. Even if the solution with the variable pitch outlined in Section 6 is close to optimal, the spatial resolution is significantly degraded for very shallow tracks.

A DEPFET-based vertex detector with a design compatible with the ILD and SiD constraints can provide a spatial resolution of 2.3 to  $3.5\ \mu\text{m}$  in the  $r\phi$  coordinate. The  $z$ -resolution is expected to be well below  $5\ \mu\text{m}$  for the central tracks that dominate many benchmark physics processes.



**Figure 19.** Simulated resolution estimated as the width of the residual (= reconstructed – true position) distribution for an LC design based on a 50  $\mu$ m thick DEPFET sensor. In the upper figure the  $r_\phi$  resolution is presented, along with the cluster size. The lowermost panel presents the  $z$ -resolution versus track polar angle. Along the length of the ladder the longitudinal pixel dimension evolves as sketched in Section 6.

## 16 Conclusions and outlook

The DEPFET collaboration, an international consortium formed by over 100 scientists from 13 institutes, aims to develop an ultra-transparent high-precision solution for vertex detectors at Belle II and a future linear collider at the energy frontier.

The DEPFET sensor is a fully depleted, active silicon sensor with in-pixel amplification. The read-out is integrated onto the sensor, with signal and power routed through metal traces deposited on the silicon. A special thinning technique yields a self-supporting frame that requires no external support structure; in the all-silicon ladder concept the material in the active region stays within a tight budget of 0.15%  $X_0$ /layer.

Measurements on early prototypes have proven the feasibility of small pixels ( $20 \times 20 \mu\text{m}$ , thin sensor ( $50 \mu\text{m}$ ), fast read-out (1/80 ns row rate)). The first large production run of DEPFET sensors has shown adequate yield. All required ASICs have been produced and are found to perform within the specifications. In January 2014 the first full-scale half-ladder, fully integrated with final-design ASICs, was operated successfully in a beam of particles at DESY.

The DEPFET active pixel detector, as of today, meets the most challenging ILC requirements. A DEPFET all-silicon ladder is expected to contribute less than 0.15% of a radiation length to the material budget. The frame rate of the innermost vertex detector ladder can be as low as  $40 \mu\text{s}$ . The ladders provide a spatial resolution in the  $r\phi$  and  $z$  coordinate measurement down to  $2.3 \mu\text{m}$  for the optimal incidence angle and well below  $5 \mu\text{m}$  for angles below 40 degrees.

Ample room for further improvement in the key performance measures remains to be exploited in future R&D. A DEPFET concept for the forward tracking disks (or vertex detector end-cap) has been developed. Mechanical samples for ladders and petals have been produced and submitted to thermo-mechanical tests. The first tests on ladders with integrated micro-cooling circuits show that this novel cooling scheme holds great promise.

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