ECFA Detector R&D Panel
LCTPC
Review Report

LCTPC collaboration

November 3, 2013

Contents

Chapter 1

Introduction

This report is organised as follows. Chapter 1 presents the LCTPC collaboration and its connection to the ILD concept detector proposed for a future Linear Collider (ILC/CLIC). The following chapters describe in more detail the various R&D activities on the different gas multiplication technologies under study (chapter 2), the study of ion backflow (chapter 3), the overall mechanics of the ILD TPC (chapter 5), electronics (chapter 4) and software developments (chapter 6). The report concludes with an outlook for the coming 2-3 years (chapter 7).

1.1 LCTPC collaboration

A Time Projection Chamber (TPC) was already foreseen as a central tracker for a detector at the proposed TESLA linear collider [1] in 2001. In October 2001 an initial program of detector research was proposed by the LC TPC group [2] to be reviewed by the DESY PRC. Since then, roughly every second year a status report was prepared for review by the PRC, the last one in 2010 [3]. The PRC duties have since been transfered to the ECFA Detector Panel.

The LCTPC groups formed a collaboration by signing a Memorandum of Agreement (MOA) in 2007, and updates to the MOA appear at the end of each year as an Addendum. The MOA and the Addenda can be found on the LCTPC website [4]. A list of the participating institutes can be found in section 1.4 and is graphically represented in figure 1.1.

Part of the LCTPC organisation are
–The Collaboration Board (CB) (one member per institute) as the governing body. Every year the CB elects a member to chair its meetings.
–Three Regional Coordinators serve as an executive body. One of them is

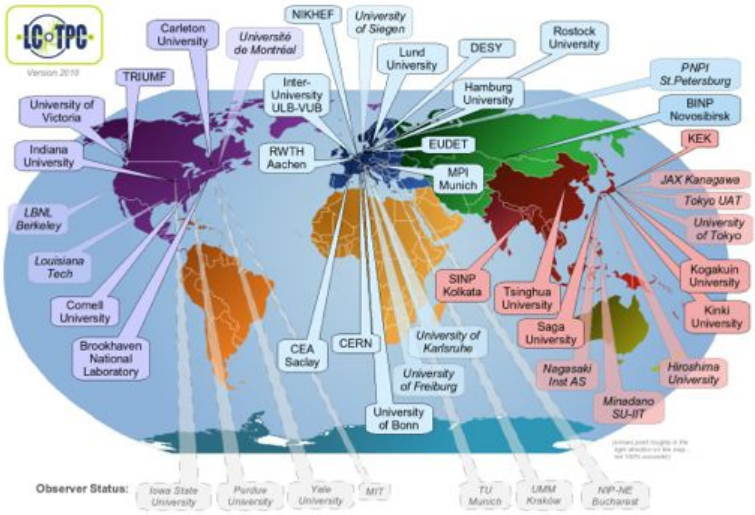

Figure 1.1: Map of the LCTPC collaboration member institutes

chosen as the Spokesperson, currently Jochen Kaminski (Bonn University). –A Speakers Bureau and an Editorial Board to monitor the Large Prototype TPC talks at major conferences and journal paper production.

Since the start of the official collaboration between the ILC (0.2 - 1.0 TeV with superconducting cavities) and CLIC (1.4 - 3.0 TeV with two-beam technology), the LCTPC collaboration has been preparing a TPC for the generic e^+e^- linear collider (LC). The LCTPC concept already allows for higher energies so that no change is needed in the organizational structure; the parameters of a TPC for ILC (see [5]) are somewhat different from those for CLIC (see [6]).

Recent efforts are underway to have the superconducting linear collider ILC built in Japan. It is envisaged to be realized in two or more stages: first stage, the 250 GeV machine (Higgs' precision measurements), followed by an extension to 500 GeV (top, Higgs' and other precision studies), and finally by an upgrade to ca. 1000 GeV. (Progress is regularly reported in the 'LC Newsline' http://newsline.linearcollider.org.)

In addition, a new leadership arrangement and collaboration, the oversight committee 'Linear Collider Board' and the international 'Linear Collider Collaboration' (LCB and LCC, see the LC Newsline), will replace the structure set up by the International Linear Collider Steering Committee several years ago and guide the construction of the ILC.

1.2 Motivation for the ILD TPC

The following is extracted from the ILD DBD report [5]. The first paragraph relates to the ILD detector at large, while the rest of the section is more TPC specific.

The particle flow paradigm translates into a detector design which stresses the topological reconstruction of events. A direct consequence of this is the need for a detector system which can separate efficiently charged and neutral particles, even inside jets. This emphazises the spatial resolution for all detector systems. A highly granular calorimeter system is combined with a central tracker which stresses redundancy and efficiency. The whole system is immersed in a strong magnetic field of 3.5 T. In addition, efficient reconstruction of secondary vertices and very good momentum resolution for charged particles are essential for an ILC detector. A view of a quarter of the ILD detector concept can be seen in figure 1.2.

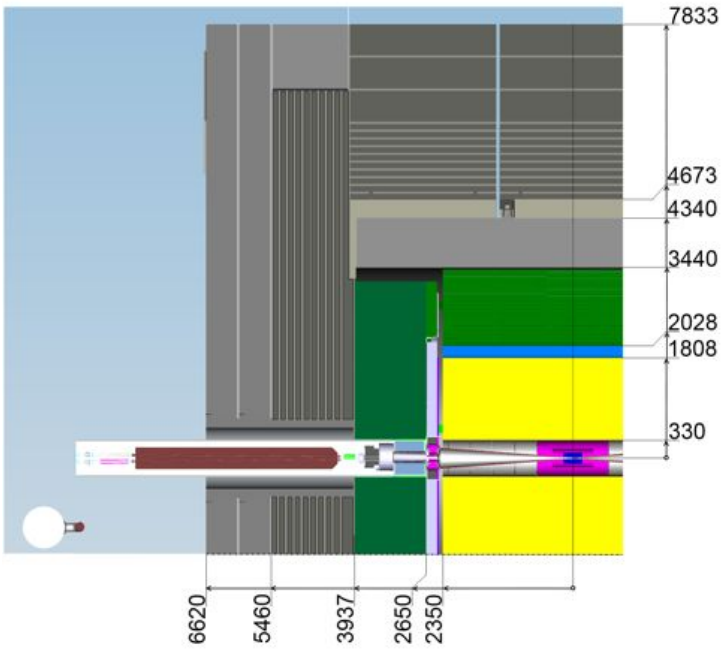

Figure 1.2: Quadrant view of the ILD detector concept. The interaction point is in the lower right corner of the picture. Dimensions are in mm. The part in yellow represents the TPC.

A TPC tracker in a linear collider experiment offers several advantages. Tracks can be measured with a large number of three-dimensional (r, ϕ, z) space points. The point resolution, σ_{point}, and double-hit resolution, which are moderate when compared to silicon detectors, are compensated by continuous tracking. The TPC presents a minimum amount of material as required for the best calorimeter and PFA performance. A low material budget also minimises the effects due to the $\simeq 10^3$ beamstrahlung photons per bunch-crossing which traverse the barrel region [7]. To obtain good momentum resolution and to suppress backgrounds, the detector will be situated in a strong magnetic field of 3.5 T. Under this condition a point resolution of better than 100 μm for the complete drift and a double hit resolution of < 2 mm are possible.

Continuous tracking facilitates the reconstruction of non-pointing tracks which are significant for the particle-flow measurement and for the reconstruction of physics signatures in many scenarios. The TPC yields particle identification via the specific energy loss dE/dx which is valuable for many physics analyses.

Over the past years systematic R&D work to develop the design of a high-resolution TPC for a linear collider detector has been pursued in the context of the LCTPC collaboration [4, 8, 9, 10].

The main parameters for the TPC are summarised in Table 1.1. The readout endplate being a concentric assembly of modules is shown in figure 1.3. The current design of the endplate foresees 240 modules of approximately 17×22 cm^2.

Parameter	
Geometrical parameters	r_{in} r_{out} z 329 mm 1808 mm $\pm$ 2350 mm
Solid angle coverage	Up to $\cos\theta \simeq 0.98$ (10 pad rows)
TPC material budget	$\simeq 0.05$ X_0 including outer fieldcage in r < 0.25 X_0 for readout endcaps in z
Number of pads/timebuckets	$\simeq$ 1-2 $\times 10^6$/1000 per endcap
Pad pitch/ no.padrows	$\simeq 1\times 6$ mm^2 for 220 padrows
σ_{point} in $r\phi$	$\simeq 60$ μm for zero drift, < 100 μm overall
σ_{point} in rz	$\simeq 0.4 - 1.4$ mm (for zero – full drift)
2-hit resolution in $r\phi$	$\simeq 2$ mm
2-hit resolution in rz	$\simeq 6$ mm
dE/dx resolution	$\simeq 5$ %
Momentum resolution at B=3.5 T	$\delta(1/p_t) \simeq 10^{-4}$/GeV/c (TPC only)

Table 1.1: Performance and design parameters for the TPC with standard electronics and pads. The momentum resolution of the full ILD tracking system is $\simeq 2 \times 10^{-5}$/GeV/c.

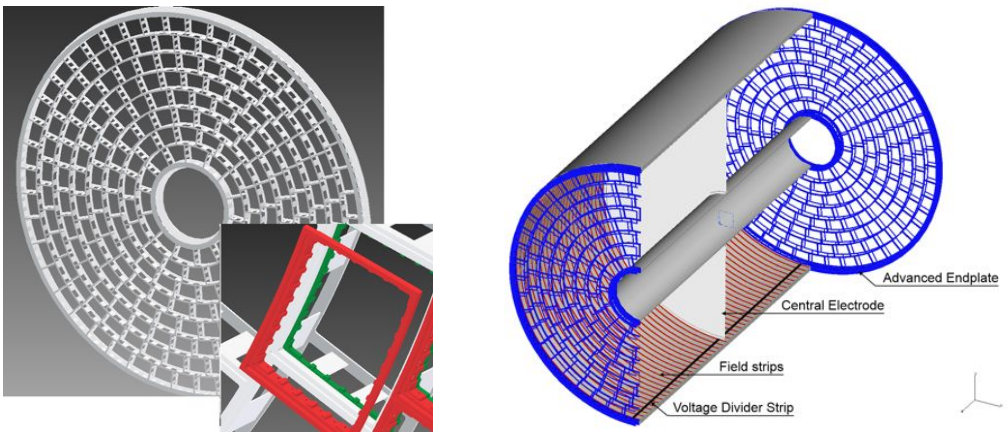

Figure 1.3: Left: Drawing of the proposed end-plate for the TPC. In the insert a backframe which is supporting the actual readout module, is shown. Right: Conceptual sketch of the TPC system showing the main parts of the TPC (not to scale).

1.3 LCTPC testbeam infrastructure

The setup in the DESY II testbeam area T24/1 consists of a large field cage with a modular endplate, allowing up to 7 detector modules to be mounted (Large Prototype TPC). The LP TPC can be inserted in the PCMAG superconducting magnet, which is mounted on a movable lifting stage (3 axes). High Voltage and gas supplies and corresponding slow control systems are available, as well as cosmic and beam scintillation counters trigger system. A laser calibration system has been used already in 2009 and is being recommissioned. A system of external silicon layers in the narrow space between the TPC and the magnet inner wall is still under consideration.

The fieldcage is made of light weight composite materials. Its diameter is 72 cm and the maximum drift distance is 57 cm. Figure 1.4 shows a picture of the magnet PCMAG inside the movable lifting stage (on the left) together with a view of the LP TPC with 7 Micromegas modules mounted (on the right).

Before 2012 the PCMAG magnet (on loan from KEK) had to be filled

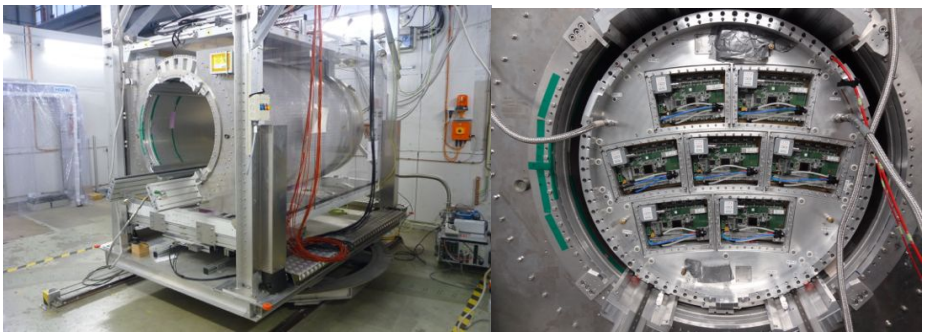

Figure 1.4: Left: PCMAG mounted on a movable lifting stage in the DESY testbeam area. Right: Seven micromegas modules mounted on the endplate of the LP, equipped with highly integrated electronics.

manually with liquid He from a dewar. Between July 2011 and April 2012 the magnet was shipped back to Japan and modified to run without liquid He using two cryo coolers and two He gas compressors. The upgraded system has been in operation since June 2012.

1.4 Institutes

Groups in the three global regions which have signaled interest in participating in the LCTPC R&D are listed here.

Americas

Carleton Univ & TRIUMF, Ottawa, ON K1S 5B6, Canada
Univ. de Montreal, Montreal, PQ H3C 3J7, Canada
Univ. of Victoria & TRIUMF, Victoria, BC V8W 3P6, Canada
Brookhaven National Laboratory, Upton, NY 11973-5000, USA
Cornell Univ., Ithaca, NY 14853-5002, USA
Indiana Univ., Bloomington, IN 47405, USA
Lawrence Berkeley National Lab., Berkeley, CA 94720-8153, USA

Asia

Tsinghua Univ., Beijing 100084, China
Saha Inst. of Nucl. Phys., Kolkata 700064, India
Hiroshima Univ., Higashi-Hiroshima, Hiroshima 739-8526, Japan
KEK, Tsukuba, Ibaraki 305-0801, Japan
Kinki Univ., Higashi-Osaka, Osaka 577-8502, Japan
Kogakuin Univ., 1-24-2, Nishi-Shinjuku, Shinjuku, Tokyo 163-8677, Japan
Faculty of Informatics, Nagasaki Inst. of Applied Science NiAS, Nagasaki 851-0193, Japan
Saga Univ., Faculty of Science and Engineering, Honjo, Saga 840-8502, Japan
Tokyo Univ. Agriculture and Technology, Koganei, Tokyo 184-8588, Japan
Univ. of Tokyo, ICEPP, Tokyo 113-0033, Japan

Europe

IIHE (Inter-university Institute for High Energies) ULB-VUB, B-1050 Bruxelles
CEA Saclay, Irfu, F-91191 Gif-sur-Yvette, France
RWTH Aachen, D-52056 Aachen, Germany
Univ. Bonn, D-53115 Bonn, Germany
DESY Hamburg, Notkestrasse 85, D-22607 Hamburg, Germany
Albert-Ludwigs Univ., D-79104 Freiburg, Germany
Taras Shevchenko National University of Kyiv, 01601 Kyiv, Ukraine
Univ. Hamburg, Inst. für Experimentalphysik, D-22761 Hamburg, Germany
Max-Plank-Inst. für Physik, D-80805 Munich, Germany
Univ. Rostock, D-18051 Rostock, Germany
Univ. Siegen, D-57068 Siegen, Germany
NIKHEF, NL-1009 DB Amsterdam, Netherlands
Budker Inst. of Nuclear Physics, RU-630090 Novosibirsk, Russia
Lund University, Dept. of Physics, Box 118, S-221 00 Lund, Sweden
CERN, CH-1211 Geneva 23, Switzerland

1.4.1 Observers

'Oberservers' are groups or persons that could not sign the MOA but want to be informed as to the progress, thus are included in the LCTPC mailing list:
Iowa State, MIT, Purdue, Yale, Louisiana Tech, JAX Kanagawa, Mindanao, LAL Orsay/IPN Orsay, TU Munich, Karlsruhe, UMM Krakow, Bucharest, St.Petersburg.

Chapter 2

Technologies and R&D

Various readout techniques are being studied to find the best option for the ILD TPC. These techniques were first tested in small prototypes at different institutes, but are now implemented in larger modules designed to fit into the Large Prototype at DESY [4].

2.1 Gas Amplification

Time Projection Chambers, which are in operation today or have been operated in the past were read out by multi-wire proportional chambers. However, the stringent requirements stated in chapter 1 can not be fulfilled with such a readout. The strong magnetic field of $B = 4$ T and the wide gap of 1-2 mm between wires leads to strong $E \times B$-effects. It was demonstrated in reference [11] that it is not possible to reach the required spatial resolution with a wire-based readout. The LCTPC collaboration has, therefore, investigated the use of Micropattern gaseous detectors to replace the MWPCs. The two most widely used MPGDs are Gas Electron Multipliers (GEMs) invented by F. Sauli [12] and Micromegas invented by Y. Giomataris and collaborators [13]. All MPGDs have the advantage of small pitches of order 10-100 µm between sensitive areas. This improves the spatial resolution and significantly reduces $E \times B$-effects. Additionally, the charge collection times are much shorter, since in GEMs only the electrons contribute to the signal and in Micromegas the slow ions have to drift only a short distance. Finally, a large fraction of the ions are guided to an electrode and are neutralized there. Thus, the number of ions potentially reaching the drift volume is greatly reduced.

2.1.1 Gas Electron Multiplier- GEMs

GEMs are foils made of a metal-insulator-metal sandwich. Standard CERN GEM use a 3 µm copper layer on both sides of a 50 µm kapton layer. A

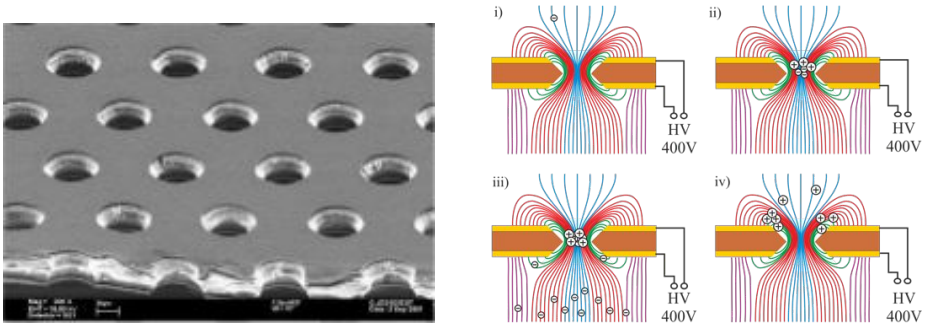

Figure 2.1: Left: SEM picture of a GEM foil, right: Schematic drawing of the working principle of a GEM [14].

hexagonal hole pattern is etched in the sandwich creating holes with a diameter of 60-70 µm at a pitch of 140 µm (SEM picture see figure 2.1 left). If an electrical potential is applied to the electrodes, strong electrical fields are created inside the holes and electrons entering a hole initiate a gas amplification avalanche (see figure 2.1 right). The electrons are released in the gas volume below and can either be collected on a pad or multiplied in a further gas amplification stage. Stacking several GEMs has many advantages. One is the reduction of the discharge probability: In the transfer gaps between the GEMs the charge is distributed over more holes reducing the charge density in the following amplification stage.

2.1.2 Micromegas

Micromegas consist of a mesh mounted at a short distance (50-200 µm) above the readout plane. The mesh is put on a lower electrical potential than the pads and the resulting electrical field is strong enough for gas amplification. If electrons enter the amplification gap from the conversion and drift volume, a very narrow signal is created, since the diffusion in the amplification gap adds only about 20 µm to the signal width. Therefore, the Micromegas are well adapted for detectors with fine readout pads. But in case of pitches in the order of several millimeters, the spatial resolution degrades rapidly, since only one pad is hit giving a resolution of pad pitch/$\sqrt{12}$. To improve the performance a new idea was pioneered in the LCTPC collaboration: The readout electrode is covered with a resistive layer grounded at the edges of the module [15] (see also section 2.2.3). Since the layer is disconnected from the pad by an insulating layer of glue, the signal can only be transmitted via capacitive coupling to the pads, while the charge propagates towards the module edge. In this way, the signal is spread over several pads and a more precise position determination is possible.

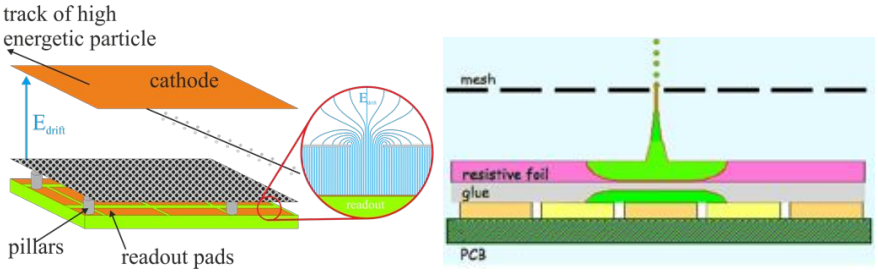

Figure 2.2: Left: Schematic drawing of the Micromegas detector working principle [14], right: Schematic drawing of a Micromegas detector with resistive anode [15].

2.1.3 Pixelized Readout

The fine pitch of the Micropattern Gaseous detectors allows for a better resolution of the primary charge than is possible with square-millimeter-size pads or long fine pitched strips. To adapt the feature size of the readout plane to the feature size of the gas-amplification stage, readout chips of a pixel detector are used as an active anode [17]. The bump bond pads usually used to connect the readout chip to the Si-sensor are used as charge collection pads and are placed directly below the gas amplification stage. The Timepix ASIC [18] is currently the preferred chip and is used by several groups.

To protect the ASIC from destructive discharges the active area is covered with an 8 µm thick resistive layer of silicon-richnitride (SiRN) [19]. In case of a discharge the charge does not enter directly into one or more pixel, but is collected on the resistive layer, stopping the discharge at an earlier stage by lowering the electric field between grid and layer. In addition, the charge is spread over a larger area and thus more pixels, reducing the probability of reaching destructive energies. The InGrid [20] itself is produced with photolithographic processes. The important feature is, that with modern post processing techniques the alignment can be done with excellent precision, so that each grid hole can be placed directly above a pixel of the ASIC. Therefore, the holes have a pitch of 55 µm and a diameter of about 30 µm.

Because of the small pixel size and the digitization close to the charge collection pad, the electronic noise is very low (ENC $\approx$ 90 e^-) and thresholds well below 1000 e^- can be applied. Since InGrids can easily reach gas gains of 5000 a very high detection efficiency of primary electrons is possible. If the primary charge is sufficiently spread due to the diffusion, then primary electrons are likely to enter in separate holes and every hit on a pixel corresponds to the detection of one primary electron.

The first InGrids were produced at the University of Twente. Because of limitations in the size of some machines, the process could not be applied

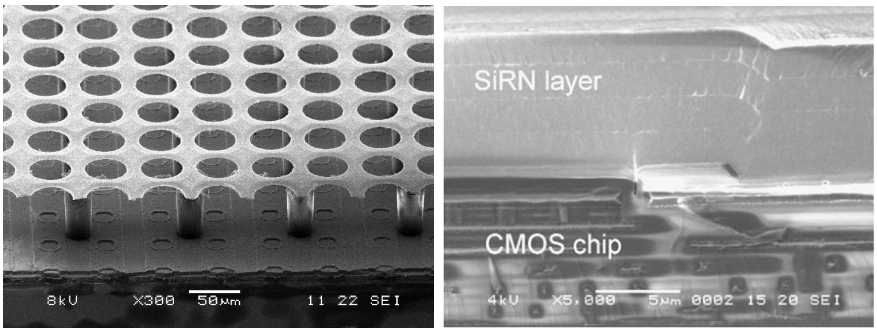

Figure 2.3: Left: SEM picture of an InGrid detector, right: Cross-section SEM picture of Timepix chip covered with 9 µm SiRN [19].

to full wafers, but only up to 9 chips at a time. To demonstrate that the coverage of a large area with InGrids can be done, the Universities of Bonn and Twente have established a new wafer-based process at the Fraunhofer Institute IZM at Berlin. Now, wafers with 107 InGrids each can be produced at the same time, providing a larger number of detectors for testing.

2.2 Module Layouts

The general module design is similar for all readout techniques. An aluminum backframe serves as a basis and will be used to mount the module on the endplate and ensure gas tightness with an O-ring. The backframes have a keystone like shape of the dimension 17×22 cm^2. They are made of aluminum and are two times cold shocked during the production to re-

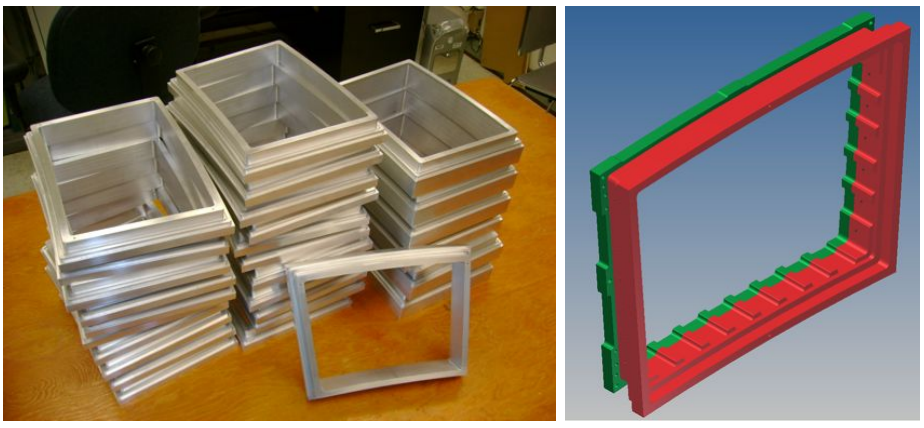

Figure 2.4: Left: First batch of backframes before delivery, right: 3D-model of a second version backframe. In red the backframe is shown and in green a mounting bracket necessary to fix the backframe to the endplate.

duce the mechanical stress and provide a precise basis stable in time for the modules. The modules are required to have an overall height of 45 mm. Therefore, the backframes were made with different heights varying from 27 to 41.8 mm to compensate for the different thicknesses of the gas amplification stages (see figure 2.4 left). A second version of the backframe was produced, where some material was reduced (see figure 2.4 right).

Multi-layer readout boards are glued on the backframes. To ensure a good knowledge of the board position, the alignment is done with two precision pins. In the case of a pad based readout, the signals are routed from the pads pointing to the inside of the detector to the connectors on the backside of the PCB, where the readout electronics will be situated. Finally, the gas amplification stage is mounted on the pad plane. Here different approaches have been tested to reduce insensitive area, to give sufficient support to the structure and to distribute the high voltage.

2.2.1 Asian Modules

The Asian modules use GEM stacks as a gas amplification stage and are optimized to reduce the insensitive area on the sides of the modules which point towards the detector center. Particles from the interaction point flying between the modules may not be detected if they are very stiff. Therefore, the Asian module foresees no frame along the sides and extends the sensitive area up to the edge of the backframe. To ensure a flat mounting of the GEMs, they are stretched on both arcs and are made of a stiffer material: GEMs with an insulator of 100 µm Liquid Crystal Polymer (LCP) covered with 5 µm copper on both sides were produced by SciEnergy. The holes were produced with CO_2 laser drilling and the GEMs were carefully cleaned by dry etching to remove potentially conductive residuals from the holes. The hole pattern is identical to standard CERN GEMs. Because of the thicker material also higher gas gains per GEM can be reached and a double GEM structure is sufficient. The two GEMs are mounted with an induction gap of 2 mm and a transfer gap 3 mm (see figure 2.5 left). The pads have a size of 1.2×5.4 mm^2 and there are 28 pad rows with a total of 5152 pads.

From the beginning the use of an ion gate (see chapter 3) was envisaged and, thus, the level of GEM1 was planned to be 1 cm below the nominal module height allowing for a later addition of the gate. To absorb the strength necessary to stretch the GEMs and the gate, strong metal poles were implemented at the top and bottom arch.

2.2.2 DESY Modules

The DESY modules are based on a stack of three standard CERN GEMs, which are divided into 4 quadrants to reduce the electrical energy stored in each sector to avoid destructive discharges. Also for these modules the in-

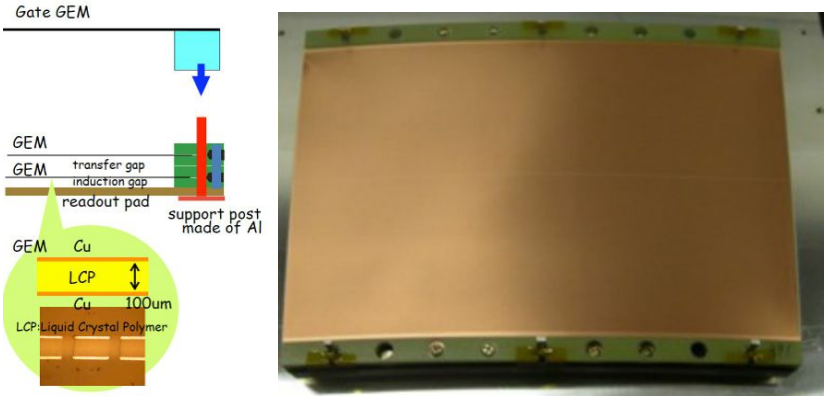

Figure 2.5: Left: Schematic drawing of the Asian module, right: Photograph of the Asian module.

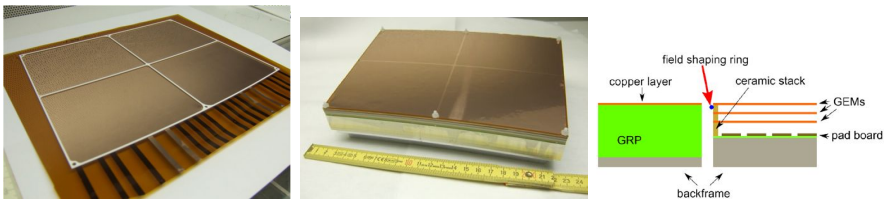

Figure 2.6: Left: DESY GEM during the mounting of a grid, middle: DESY module, right: cross section of the DESY module and neighboring dummy module used during tests.

sensitive area was minimized as much as possible, but without the emphasis on the side edges. Therefore, in contrast to the Asian approach no force is applied to stretch the GEMs in a frame, but the GEMs are glued to a 1 mm wide ceramic mounting grid, which supports the GEMs not only at the edges, but also with two central bars, where the separation of the GEM sectors already provide an insensitive area. The GEMs are mounted with transfer gaps of 2 mm and an induction gap of 3 mm on a the pad plane. The pads have a size of 1.26×5.85 mm^2 and there are 28 pad rows with a total of 4829 pads covering about 94 % of the module area.

2.2.3 Saclay Modules

Saclay has developed modules based on Micromegas with a resistive coverage of the pads. While both GEM modules used the ALTRO electronics as a readout, the Micromegas module used the AFTER chip in its readout chain. Since the packing of the AFTER chip was more challenging, and a limited number of channels was available - it was required to cover at least seven modules - larger pads of the size 3×7 mm^2 were chosen. These were placed in 24 rows with 72 pads each giving a total number of 1728 pads per module.

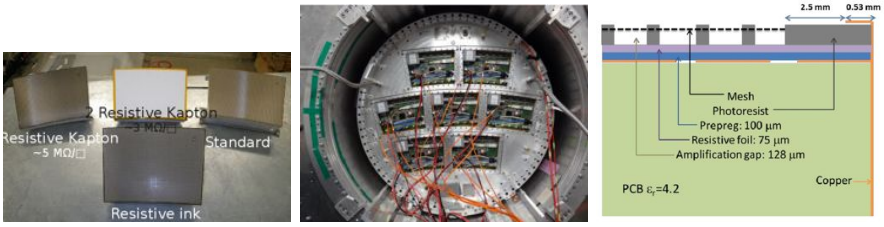

Figure 2.7: Left: 4 modules with different resistive layers, middle: 7 modules of the production series mounted in the Large Prototype, right: Schematic drawing of the border of the modules.[23]

In a first iteration two different resistive materials, resistive ink and carbon loaded kapton (CLK), and different resistivities, 3 MΩ/□ and 5 MΩ/□, were tested. The CLK proved more homogenous and was therefore preferred in later modules. For the given pad size, the resistivity of 3 MΩ/□ was best suited, but needs to be adapted, if different pad sizes are chosen. The resistive foil is pressed on the pad plane and the Micromegas is built on top of the resistive layer. Following the Bulk-Micromegas instruction [21] an amplification gap of 128 µm was used. A very good grid homogeneity was reached and a homogeneous gas gain throughout all modules could be demonstrated in dedicated calibration runs with an ^{55}Fe source, see reference [23].

The HV contact is realized on 2 dedicated pads in the sensitive area. In this way the sensitive area could be extended almost to the edge of the modules, limited only by a 3 mm wide frame made of photoresist, which holds the grid. The ground connection of the resisitive layer extends over the edge of the module and covers both the side of the module and also the frame of the module (see figure 2.7 right).

After establishing the technology a production series of 9 modules including a highly integrated electronics (see chapter 4) followed. Seven of the modules were used simultaneously in the Large Prototype. The experience of a quasi industrial production, where the pad plane and electronics PCBs were produced by ELTOS [22] and the resistive layer and Bulk-Micromegas were applied at the CERN workshop, was very positive and the quality of the modules was as high as on the prototype level. The complete module has an average radiation length of 21.38 $\frac{\mathrm{g}}{\mathrm{cm}^2}$.

2.2.4 Pixel Modules

Two different modules with InGrid readout have been constructed, but both modules feature only a small area covered with InGrids. They both have a single PCB, on which 8 InGrids can be mounted (see figure 2.8 left). The first module was built in 2010 by Saclay and NIKHEF (see figure 2.8 middle).

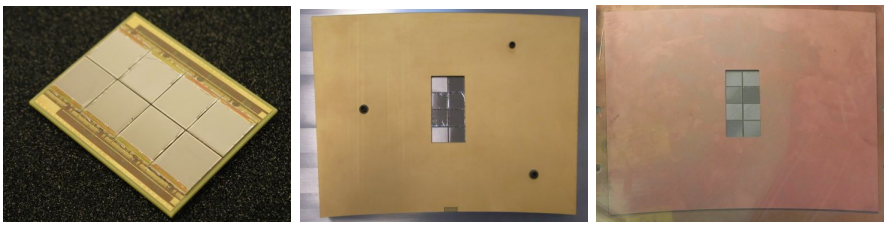

Figure 2.8: Left: PCB 'Octopuce' with 8 InGrids mounted, middle: First module with InGrids, right: Second module with InGrids.

The InGrids had been made at the University of Twente and the readout was a NIKHEF-built readout system MUROS2.0. The InGrids were mounted about 1 mm below the nominal height and a field termination plate was placed around the InGrids at the correct height. The small height difference was necessary to reduce the opening in the plate to the size of the active area of the InGrids and to cover the remaining area of the PCB, including the bond wires and HV supply lines. This arrangement reduces the local field distortions around the InGrids

To demonstrate that the coverage of a large area with InGrids is possible, the University of Bonn has initiated the above-mentioned wafer-based production of the InGrids. Also, a readout system is being developing which allows an easy scaling of the number of readout Timepix chips. The system is based on the Scalable Readout System (SRS) developed by the RD51 collaboration. To adapt the SRS, the FPGA code needs to be rewritten for the communication with the Timepix chip, and special adapter PCBs are necessary to combine and transfer the communication and data signals to and from the chip. The system can now be operated, but several features still await implementation and several further optimizations are planned.

To test these new developments on a smaller scale a second module with 8 InGrids was built in 2013 (see figure 2.8) and successfully operated in the Large Prototype.

2.3 Operation Experience and Performance

All modules have been tested in the Large Prototype at DESY. While each of the pad-based module was tested several times and optimized, both InGrid modules have been tested only during a short test beam campaign. The experience gained during all test beam periods as well as the best transverse spatial resolutions are shown in this section.

All groups have used the same gas mixture of Ar:C_4:iC_4H_{10} 95:3:2. The electric drift field was set in most cases to $E = 230$ V/cm, which is close to the maximum of the drift velocity, and alternatively to $E = 130$ V/cm, which is the minimum of the transverse diffusion.

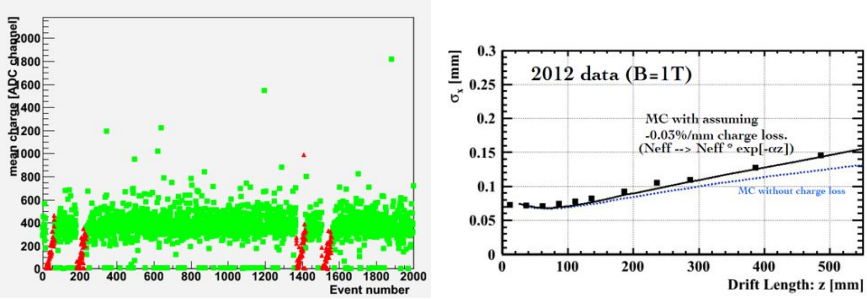

Figure 2.9: Left: Mean charge per hit in dependence on the event number. In red are events with reduced gain, which is likely because of a discharge, right: transverse spatial resolution of the best pad row in dependence on the drift distance. The dotted and solid lines are calculations with the analytic model with the charge loss switch on and off.

2.3.1 Asian Modules

The Asian group has built three modules from the beginning and has made several test beam periods at DESY (2009, 2010, 2012). The first campaigns were dominated by very strong field distortions because of the mounting pins and the bare frames. After introducing the field shaper, the distortions are comparable to the ones of other modules. One other important observation was a high number of discharges and HV glitches on the GEMs. Figure 2.9 shows the gain drops clearly visible in the histogram of mean charge per hit. To minimize the energy released in a discharge, the GEMs were segmented into four arches, each with an area of about 100 cm^2.

The transverse spatial resolution is shown in figure 2.9 right, where the spatial resolution of a single row in the middle of a module is shown. In this context an analytical formula was developed to predict the spatial resolution of a TPC. This formula includes not only the effect of diffusion, angle, noise and a finite pad-size, but also the influence of the electronics threshold, number of effective primary electrons, the Polya-parameter of the gas amplification, cross talk between pads and signal lines, charge loss because of attachment and the pad response function are taken into account. All these parameters can be varied and, if correctly chosen, describe well the measured data (see blue line in figure 2.9 right).

2.3.2 DESY Modules

First tests with the GridGEMs were in 2011, where a simplified readout board featuring about 900 nominal pads was used. These functionality tests disclosed several shortcomings in the HV distribution, leading also to the destruction of several GEMs. The shortcomings were identified and solved in the final design. Three modules were built and tested in 2012 and 2013.

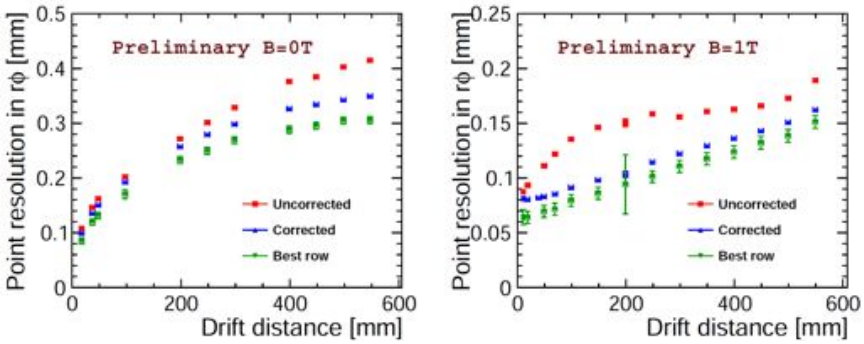

Figure 2.10: Left: transverse spatial resolution with $B = 0$ T, right: Transverse spatial resolution with $B = 1$ T. [16]

Since only a limited number of the readout channels was available each of the modules was equipped with about 2,400 channels, so that a continuous completely equipped area about 10 cm wide and 50 cm long was available for recording events.

During the data taking campaign in 2013 a large data set of more than 10^6 events was recorded. The transverse spatial resolution without (left) and with (right) a magnetic field is shown in figure 2.10. The figure shows in red uncorrected data, in blue data that was corrected for the field distortion described in section 2.4. For this a data driven approach correcting every hit by the mean offset recorded for the relevant pad row was used. Finally, the best pad row (row 16 in the middle of the central module) was used indicating the best possible performance in the case of almost no field distortions.

2.3.3 Saclay Modules

Saclay has organized seven test beam periods between 2008 and 2013 (see reference [23] for more details). After determining the best resistive cover of the pads in 2008-2010, the final design and the small series production was tested in 2012 and 2013. During the first test beam major problems with the connector between the pad plane and the readout electronics occurred and a large fraction of the pads became disconnected. This problem was solved during the second test beam campaign and a large data sample of more than 10^6 tracks was collected.

The transverse spatial resolution is shown in dependence on the drift distance in figure 2.11 left. The open symbols at the beginning were taken at a later time and show a worse resolution than expected. This might be because some environmental parameters like temperature or gas pressure changed in the meantime and the gas amplification was lowered. The closed symbols were included in the fit and give a good value for N_{eff} and the

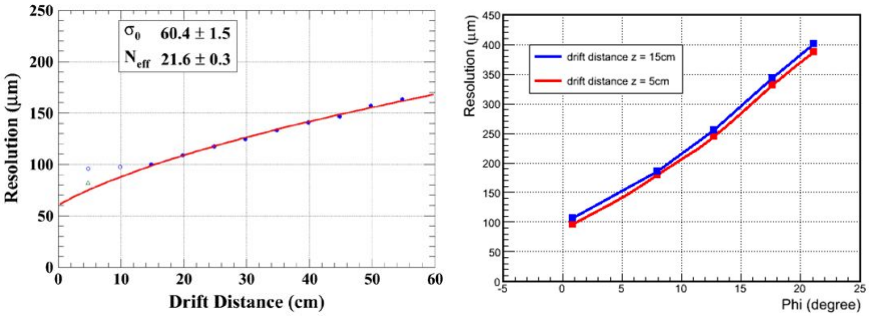

Figure 2.11: Results of the Micromegas module. Left: Transverse spatial resolution in dependence on the drift distance in $B = 1$ T. Right: Transverse spatial resolution in dependence on the track inclination ϕ. [23]

intrinsic detector resolution σ_0.

For better comparison between the GEM and Micromegas gas amplification stage, a pre-series module was equipped with the ALTRO electronics this year and a short test beam campaign was used to take data. A vital interest was the shorter shaping time of down to 30 ns, which is possible only with the ATLRO electronics, while the AFTER electronics has a minimum shaping time of 100 ns. The data, however, has not been analyzed yet.

2.3.4 Pixel Modules

The first InGrid module functioned well except that one of the InGrids was prone to discharges and only a low gas amplification could be reached. To keep the electric field distortions in an acceptable limit, the HV of the other InGrids had to be kept at the same potential. Therefore, the efficiency of the complete module was reduced. Nevertheless, tracks could be identified (see figure 2.12 left).

On the second module one Timepix ASIC showed a rather high noise level which could not be reduced. Because of this the threshold of this chip was set to a high level leaving this chip quasi insensitive, but not affecting the remaining chips. Besides, a large cross talk could be observed in many events. These events could be identified and removed from the analysis leaving sufficient good events such as depicted in figure 2.12 right. Even though the track length was only 5.6 cm, the analysis shows that a large number of electrons can be associated with each track (see figure 2.13 left) and the spatial resolution follows the single electron diffusion limit both with and without magnetic field (see figure 2.13 middle and right.) In this plot, the spatial resolution has been plotted for all electrons without correction. The large intrinsic detector resolution $\sigma_{xy,0}$ of 100-200 µm are caused by the field distortions around the InGrids as described in the next section.

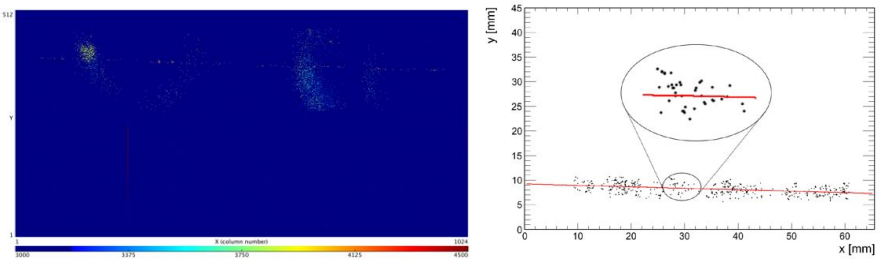

Figure 2.12: Left: Track of a 5 GeV electron in He:iC_4H_{10} recorded by the first InGrid module, right: Track of a 5 GeV electron in Ar:CF_4:iC_4H_{10} 95:3:2 recorded by the second InGrid module. The red line visualizes the reconstructed track.

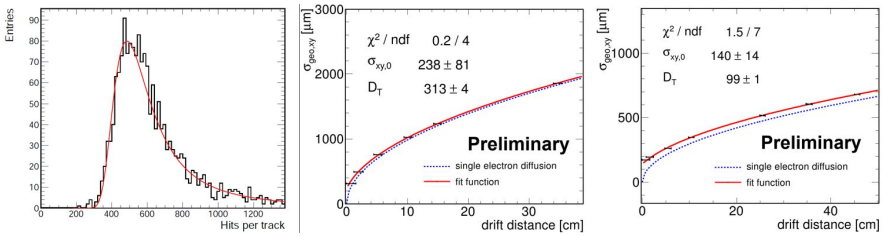

Figure 2.13: Left: Number of electrons associated with tracks of 5.6 cm with an InGrid module, middle: transverse spatial resolution dependence on the drift distance with $B = 0$ T (middle), and $B = 1$ T (right).

2.4 Field Distortions

All modules experience strong local field distortions at the module edges. A detailed simulation with CST and Garfield++ confirmed the suspicion, that underlaying lower potentials leak through the gaps between modules and cause the field distortions. Figure 2.14 left shows the electrical field at a transition between a dummy module and a DESY module. In the study 200 electrons were emitted at each of 50 equidistant points along a line perpendicular to the module edge. It was counted how many of these electrons are collected on a readout pad and how many are lost. The efficiency loss of the first 3 pad rows is clearly visible in figure 2.15 left and of the same magnitude as in the data collected in the experiment. To compensate the loss of charge, different forms of additional electrodes on the side of the module were studied. In figure 2.14 middle, the electric field can be seen when a thin wire (diameter of 150 µm) is attached to the side, and in figure 2.14 right the influence of a broader strip is shown. For the last test beam period, a wire was glued to the sides and put on the same potential as the topmost electrode of the GEM stack. As expected from simulations the efficiency drop observed at the first 2 rows of the module is

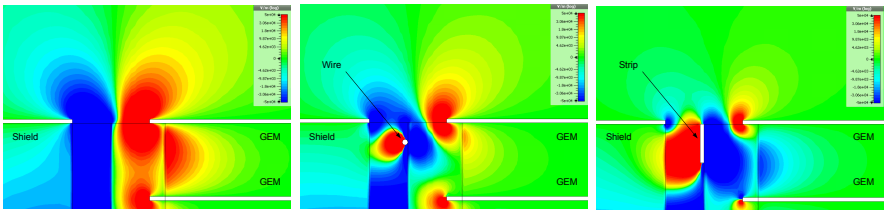

Figure 2.14: CST calculation of the field distortions around the DESY module. Left: without modification, middle: with a 150 µm thick wire around the module, right: with a 1 mm wide strip around the module.

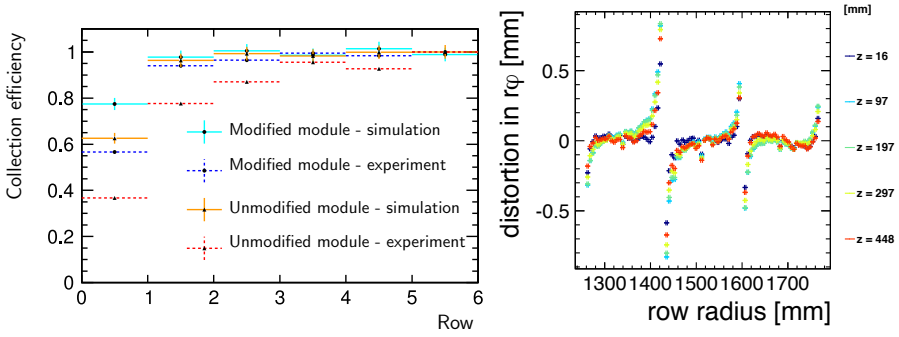

Figure 2.15: Left: charge collection efficiency in dependence on the row number in simulations and measurements with the DESY module. Right: Mean deviations of the charge from the track for different drift distances in dependence on the module row radius.

reduced by a factor of 2 (see figure 2.15 left). Despite this improvement the field distortions still have a major impact on the drift path of the primary electrons and the measured charge shows deviations from the reconstructed tracks. As an example in figure 2.15 right the mean deviation from the track is shown.

Similar observations were made with the Asian module (see figure 2.16 left), where small track distortions could be observed even between the GEM sectors and significant larger distortions at the module edges. In contrast to the DESY module, the segmentation of the Asian GEMs is on the side of the drift volume and therefore influences the drift of the primary electrons longer. In upcoming modules, the GEMs will be turned, so that the unsegmented side will point towards the drift volume. Figure 2.16 right and figure 2.17 left show very similar data, but with tracks inclined to either the right or left by 10°. The inclination increases the track distortions, because in this case the primary electrons are displaced from the original position not along the track, but at a given angle. Therefore, the charge broadening due to the electrical field distortions and $E \times B$ effect not only leads to a

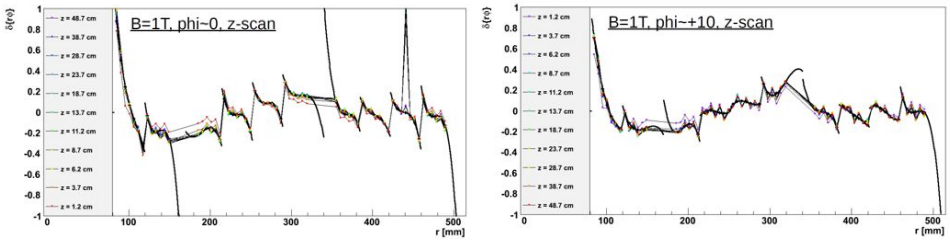

Figure 2.16: Mean deviations of the charge from the track in dependence on the row number for the Asian module. Left: 0°, right: +10°

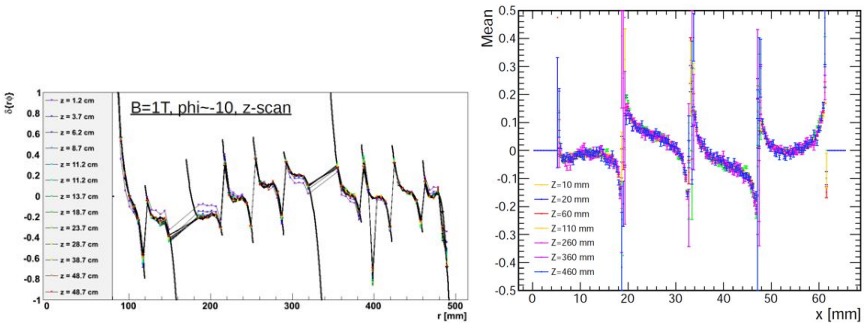

Figure 2.17: Left: Mean deviations of the charge from the track in dependence on the row number for the Asian module with inclinationd of -10°. Right: Mean deviations of the charge from the track in dependence on the position on the chip for the second InGrid module.

broader signal, but also to an additional displacement of the charge center. This effect is observed for all modules.

Also with the Micromegas module distortions due to field inhomogeneities were observed. In figure 2.18, the large impact of the magnetic field, which creates additional $E \times B$-effects is clearly visible. In case of the Micromegas, the track distortions without magnetic field is visible even for track inclinations of 0°. The origin of these distortions is still under investigation.

InGrid modules show the same deviations at each transition from InGrid to InGrid (see figure 2.17 right). Summarizing the observation of all different techniques is, that the field distortions were observed, if some lower potential (in particular ground) was not covered by a field termination plate, but a gap was left. In a first approximation the track distortions were found to be independent of the drift distance (> 1 cm) and thus originate only of local field inhomogeneities in the vicinity of the modules. As a first approach the displacement of the center was averaged over all drift distances. In a second iteration of the reconstruction the centers were corrected for the average displacement. This is however only possible for a specific set of tracks with identical inclination. For a long term use, the field distortions need to be

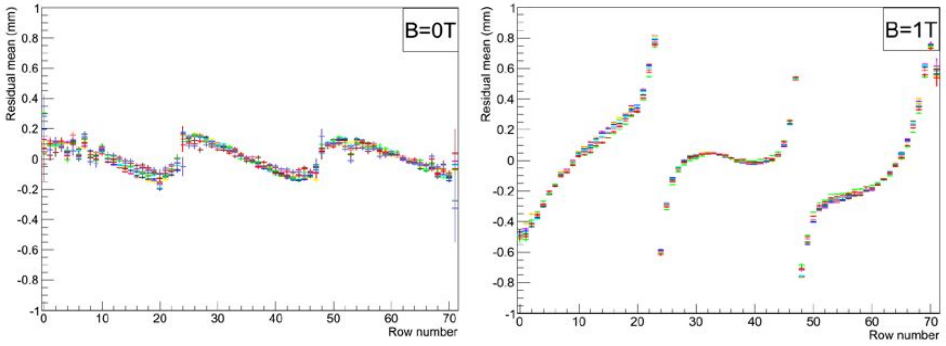

Figure 2.18: Mean deviations of the charge from the track in dependence on the row number for the Saclay modules. Left: $B = 0$ T, right: $B = 1$ T.

reduced and a complete model needs to be developed to correct for the remaining effects.

Chapter 3

Ion Back Flow

3.1 Simulation of Ion back flow in ILD TPC

Positive ions drifting back into the gas volume of the TPC is a well known issue for wire chambers. For MPGDs, the amount of ions drifting back is much lower, but can still be significant with a high track density.

Simulations have been done by D. Arai and T. Krautscheid, using the expected background in ILC, to evaluate the electrons displacement due to the electric field distortion induced by the ions. Due to the bunch-train structure of the beam of ILC (one 1 ms train every 200 ms), the ions from amplification will be concentrated in discs of about 1 cm thickness near the readout, and then drift back into the drift volume. There would be three such discs in the chamber in normal operation. Figure 3.1 shows the azimuthal displacement of electrons for different radial positions in the chamber.

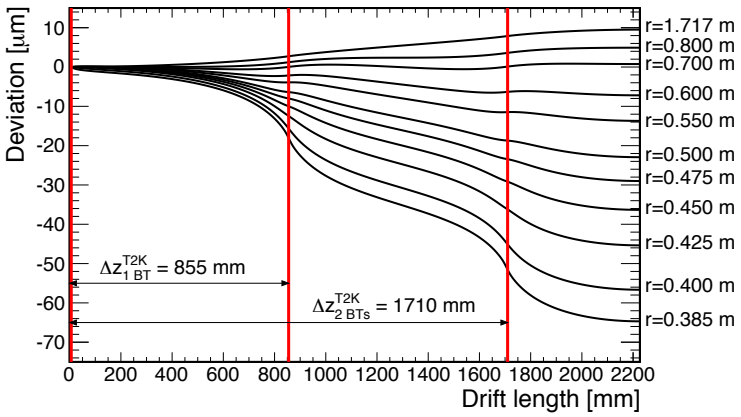

Figure 3.1: Displacement due to positive ions.

These simulations assume a back flow rate of unity, which means that

for every drift electron, only one positive ion drifts back. The amount of displacement should therefore be multiplied by the actual rate of the amplification system. It is obvious that a rate of one cannot possibly be achieved, so that distortions larger than 60 µm in parts of the TPC are unavoidable without a gate.

To cope with the resolution requirements of the ILD TPC, these distortions need to be either corrected or suppressed with an ion gating system. The fluctuations of the pair background in the TPC might be very large and render it impossible to make reliable corrections. Besides, the bunch-train configuration of ILC gives an ideal time structure for gating. The positive ions will drift about 1 cm during the 1 ms readout of a bunch train. There is then about 200 ms available to neutralise them. We therefore studied different possibilities to install a gating system in the TPC.

3.2 Wire grid

The first possible solution for a gate is the traditional wire technology. In order to minimise the angular dead spaces, and accomodate our module concept, the wires would have to be strung in the radial direction. Simple field calculations shown in reference [24] show that such a structure would have very little effect on the electron trajectories in the open configuration. There could be an angular effect due to the loss of electrons on the wires, but since the diffusion is typically larger than the wire width, this effect will be small.

There are two possible voltage schemes for the "closed" configuration of the wire gate:

Single potential By increasing the potential on all the wires, the drift field between the gate and the amplification is reversed. The positive ions will then drift back and be neutralised on the MPGD. This requires a fairly high voltage in the gate (several 100 V). The voltage will depend strongly on the distance of the gate from the MPGD, as shown in figure 3.2a-b).

Alternate potential By shifting the voltage alternately on every second wire, we can create an electric field (see figure 3.2c) that will make the ions drift towards the wires, where they will be neutralised. The voltages required are relatively small and strongly dependent on the wire spacing. This allows the gate to be slightly closer and switch faster, but it requires a more sophisticated structure to have two electrically isolated grids.

A wire gate is a well understood technology. A prototype gate fitting the Asian GEM module has been produced (figure 3.3). A set of 25 µm wire are spot welded on a stainless steel structure. This allows only a single

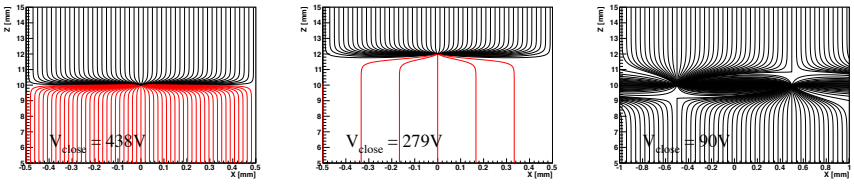

Figure 3.2: Electric field lines for closed gate configurations. (a) Single potential closed at the level of the gate. The red lines represent the different orientation of the electric field. (b) Single potential closed 2 mm below the gate. The field is much weaker below the gate. (c) Alternate potential. The field below the gate is the same as the drift field.

potential scheme, and the frame is too thick and would create large dead area. This prototype will be used to test the influence of the wire gate on the electron drift trajectories when the gate is open. Further studies are needed to realize a favorable mechanical structure with a thinner frame.

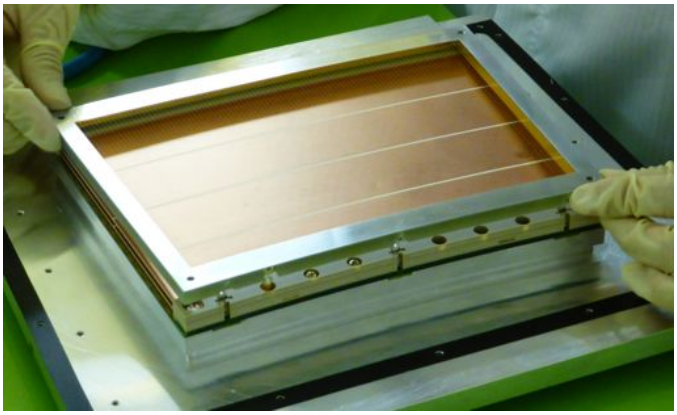

Figure 3.3: Prototype of wire gate installed on an Asian GEM module.

3.3 GEM gate

As an alternate gating solution, a GEM based system has been investigated. The use of a GEM makes it easier to integrate it into modules which are already designed for such technology. The two potential planes of the GEM makes it very easy to close the gate by changing the voltage of the lower electrode by a few volts and inverting the electric field in the holes of the GEMs. On the other hand, the open configuration will offer a reduced electron transparency, hence reducing the point resolution. A detailled study of the GEM gate through simulations can be found in reference [25].

A first gate prototype using 14 µm thick GEM, with 90 µm holes and

140 µm pitch was tested in 0 and 1 T magnetic fields. It showed a maximum transparency of 50 % in both cases. A consistent effect on the point resolution was observed. This transparency is too low for the performance requirements of the ILD TPC, and would probably be worse in a 3.5 T magnetic field.

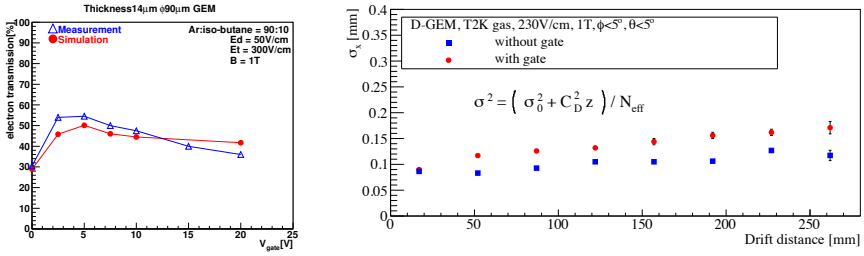

Figure 3.4: Left: transparency measurement for the GEM gate prototype, for different applied voltages. A maximum is observed around 5 V. Right: measured point resolution with and without gate. At long drift distances, the resolution is reduced by a factor consistent with the expected value of $\sqrt{2}$.

A simulation study was performed in [25], to determine what are the limits in transparency of a GEM structure. The simulations, using Garfield++, shows that in a 3.5 T magnetic field, the geometrical aperture of the GEM is the main factor that determines its transparency to electrons. As can be seen in figure 3.5, the maximum transparency is very close to the geometrical aperture, and obtained for low voltages. In that configuration, the electric field distortions are minimal and the electrons follow the magnetic field lines.

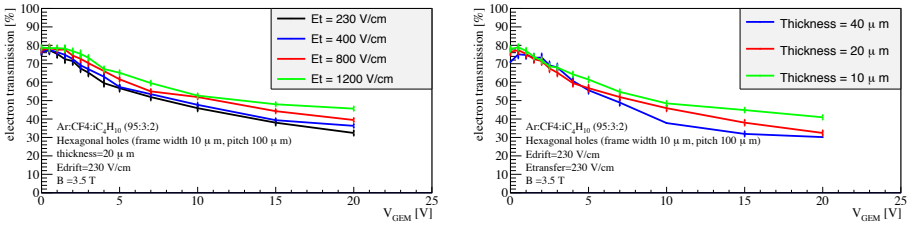

Figure 3.5: Simulated electron transmission of a honeycomb gate with 81 % geometrical aperture in a 3.5 T magnetic field. Different transfer fields and GEM thicknesses were checked. The transparency does not depend much on these parameters and the maximum transparency is obtained at very low voltage and is almost equal to the geometrical aperture.

There are now ongoing studies at the company Fujikura to manufacture GEMs with very large aperture. A structure with 300 µm diameter hole,

and 330 µm pitch (therefore offering about 70 % transparency) might be feasible, but could be expensive for large surfaces.

3.4 Conclusion

It has been shown that the ions from MPGD amplification in the ILD TPC can create sizable distortions of the drift field. The decision has been made to include a gating system to suppress this effect. A wire grid included in the readout module, with wires in the radial direction, should provide a good solution. Studies are still needed to build an appropriate mechanical structure, and to decide on the voltage configuration (single or alternate potential). Another solution using a dedicated GEM as a gate is still under consideration, but shows manufacturing difficulties and probably cannot offer transparency higher than 70 %.

Chapter 4

Electronics

4.1 Introduction

Several available electronics readout systems have been used prior to and during the EUDET-era, as for example STAR, AFTER from T2K and ALTRO from ALICE. They have been adapted/improved to be used for the readout of MPGDs. However, none of them fulfill the requirements of the final front-end electronics and therefore further development is required and is presently ongoing. The future aim is to produce electronics that is compatible with the pad size given by physics goals of the ILC. The requirements are described in the following section. The past and ongoing integration efforts are then reviewed (cooling and power pulsing). In the last section an attempt is made to give a roadmap toward the design and production of a suitable electronics in time for the startup.

4.2 Requirements

The electronics must be able to read full trains (2500 bunch crossings) at a 5 to 10 Hz frequency. It must realize a full wave sampling of each pad at a frequency which is consistent with the duration of the signal induced by a portion of a track on a padrow, that is 20 to 50 MHz. The ADC should be accurate enough to measure large fluctuations of the main pad and also the small signal of the neighboring pads to obtain the position accuracy. It was shown from test beam data [23] that down to 8-9 bit the space resolution is not significantly affected (see figure 4.1). The ILD TPC requires an unprecedented channel density. In the most demanding scheme, one channel must occupy an area of 4 mm^2 or more on the endplate, on average (taking into account space taken by the module frames, HV connections, etc.) and the total thickness of the front end electronics must be limited to 5 cm and 0.25 X_0.

In order to be able to run the gas amplification at low gain, which min-

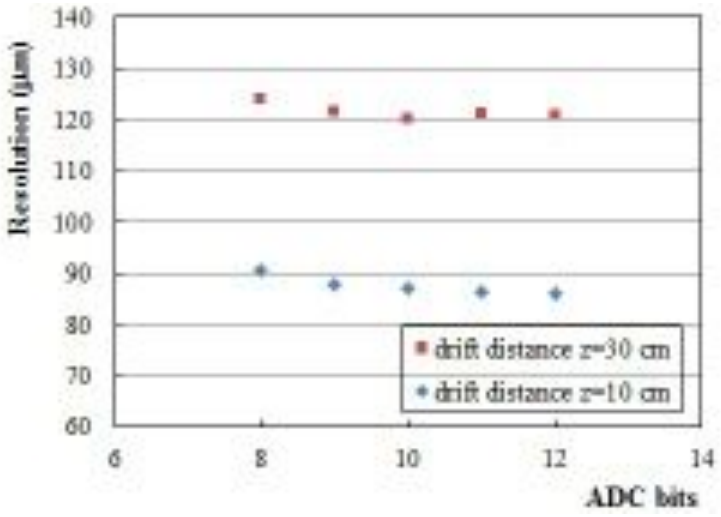

Figure 4.1: The resolution as measured from Micromegas test beam data, as a function of the number of ADC bits used (12 is the actual number of ADC bits and lower numbers are obtained by rounding up the amplitude to this accuracy).

imizes the problem with back-flowing ions, a low enough noise level for the front-end electronics has to be achieved. A goal of 600 electrons seems to be in reach, however with some trade-off with power consumption or shaping time. The shaping time should be kept as minimum for the z coordinate measurement and the 2-track separation, but values below 60-100 ns would not allow the full charge to be collected, because of longitudinal diffusion and other effects of comparable size. Thus, the aim is to operate the preamplifier with shaping times as short as 100 ns or 200 ns, irrespectivly of the gas amplification technology (GEM or Micromegas). A power consumption below 8 mW per channel seems to be realistic, but power pulsing would be needed to bring the total power consumption to an acceptable 100 W/m^2. Finally, in order to avoid dealing with useless information, an on-chip zero suppression with self-triggering and time stamping of the significant signals is necessary.

To first order, these requirements are comparable for both GEM and Micromegas, thus most of the electronics development can be done prior to the technology choice.

4.3 Test electronics

In going from small to large TPC prototypes, there was a need for test electronics to provide data which proved that the performance of the MPGDs could meet the physics goals of ILC. CERN and Lund developed an ALTRO-

based system which was used for the tests with GEMs. This electronics evolved, first by using a new amplifier-shaper PCA16. And later the analogue and digital signal processing were integrated in the same chip resulting in the SALTRO16 chip, which is now in the process of being mounted on cards. In parallel to this effort, the T2K electronics was successfully used for tests of Micromegas + resistive coating. Then it was adapted to fit on the back of a module.

4.3.1 The ongoing SALTRO16 development

The SALTRO16-chip, developed at CERN, includes a very-low-noise amplifier and an integrated 10 bit ADC. It contains power pulsing features and is very compact. The LCTPC collaboration has obtained 610 such chips (210 as a contribution from CERN and 400 bought by Japanese groups). In order to achieve a significant reduction in size of the front end electronics, most modern techniques for circuit assembly are used. In almost all aspects, it led to stretch the techniques beyond what is used in industrial manufacturing today.

The SALTRO16 readout system is schematically shown in figure 4.2 for one pad module. It is a highly advanced development project, which includes several subsystems like the Carrier Board, the MCMboard, the Low Voltage Board, the Detector Control Boards, the Serial Readout and the Monitoring. A complication is that these subsystems are not independent but have to be developed in parallel. In order to facilitate testing and debugging of the various subsystems, it has in some cases been necessary to construct prototype systems to avoid complications due to the requirements of compactness or due to other constraints. The Carrier Board and the MCM-board are especially challenging due to the tight space limitation and the high precision required. The project has to be performed in collaboration with industry, which has the necessary competence and experience. Due to limited number of chips existing, the unknown chip yield and their high cost extreme care has to be taken to minimize the number of prototype steps and in the choice of industry partner to minimize the loss due to unpredictable fabrication yield.

The SALTRO16 chip combines the analogue and digital signal processing of the incoming charge. The silicon die itself is 8.7×6.2 mm^2 and contains 16 readout channels which equals an area of 3.37 mm^2 per channel. The new chip can be turned off when no signals are expected, which drastically reduces the power consumption and the demands for cooling.

The alternative of using packaged chips is not a realistic choice since it requires too much space on the pad board in order to allow small enough pad sizes, although testing, mounting and service would be simpler. Due to the uncertainty in the yield it is unrealistic to assemble untested dies directly on a pad module with the requirement that all chips should work.

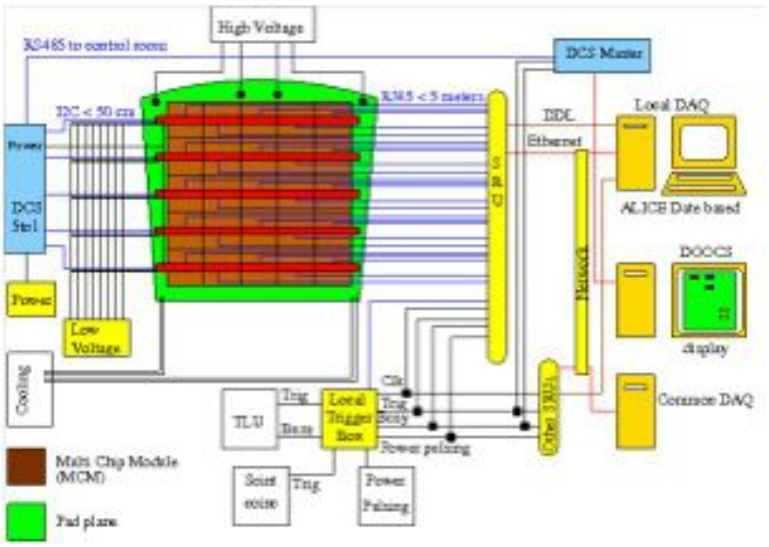

Figure 4.2: Schematic view showing the DAQ architecture of the SALTRO system.

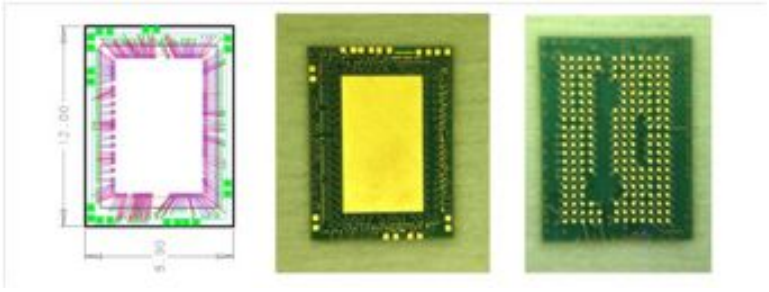

Figure 4.3: Layout of the carrier board with bonding wires and passive components (left) together with photos of the top (middle) and bottom (right) surface, respectively, of one circuit board.

Instead the chips will be mounted on Carrier Boards, only slightly bigger than the chips themselves.

This facilitates the handling and allows for tests of individual chips. The size of the Carrier Boards is 12.0×8.9 mm^2, which also includes space for bonding wires and some passive components. Eight of these Carrier Boards are soldered on one so called Multi Chip Module (MCM). The layout of the Carrier Board is shown in figure 4.2.

Recently 250 boards were delivered and figure 4.2 shows photos of the top and bottom surface, respectively, of one board. The yellow area on the top surface is where the SALTRO16 die will be glued.

The list of work in progress is kept up-to-date in reference [26] and

forthcoming versions.

The ongoing engineering phase aims at constructing a system that fulfills the various requirements of the final front-end electronics. The size of the electronics has been significantly reduced compared to the ALTRO-electronics used for the demonstration phase and corresponds to a pad size of 1×8.5 mm^2. Cooling will be provided by a system based on two-phase CO_2.

4.3.2 Micromegas Integration

In parallel to this effort, a similar integration work has been carried out using the AFTER chips designed for the T2K Micromegas TPC readout. At the same time, the acquisition was upgraded from single module capability to multi-module (up to 12). This required a complete revision of the architecture from the Front End to the backend. This work has been described in reference [29].

The front-end part uses 72-channel AFTER chips to perform detector charge signal amplification, shaping, and waveform sampling in a 511-timebin Switched Capacitor Array (SCA).

Following each detector signal sampling phase which is halted by an externally provided trigger signal, data stored in the SCAs are time-multiplexed and digitized at 20 MHz by multi-channel ADCs. Four AFTER chips are mounted on a Front-End Card (FECi) and six FECis are digitized and read out by a Front-End Mezzanine card (FEMi). Each FEMi communicates with a Data Concentrator Card (DCC) over a 2 Gbps duplex optical link. System settings, the global 100 MHz clock and trigger information are transported by the DCC to FEMi fiber while the acquired data and monitoring information travel over a second fiber stand.

By avoiding flat cables, the noise was reduced by 25 %, and the choice of a new ADC off the shelf allowed a 25 % saving in power consumption. Space was saved by wire-bonding directly the dies to FECis and by removing the protection diodes and resistances, the function of anti-spark protection being provided by the resistive-capacitive layer. Some of the passive components were transferred to the FEMi. Very flat 300 points connectors were used for the contact FECi-PCB, insuring dismountability. Single module data were taken in 2011, and 6 and 7 module data were taken in 2012 and 2013.

The plan is now to connect to the diphasic CO_2 cooling system to replace the present air cooling. The AFTER chip also has power pulsing capability on the analog part.

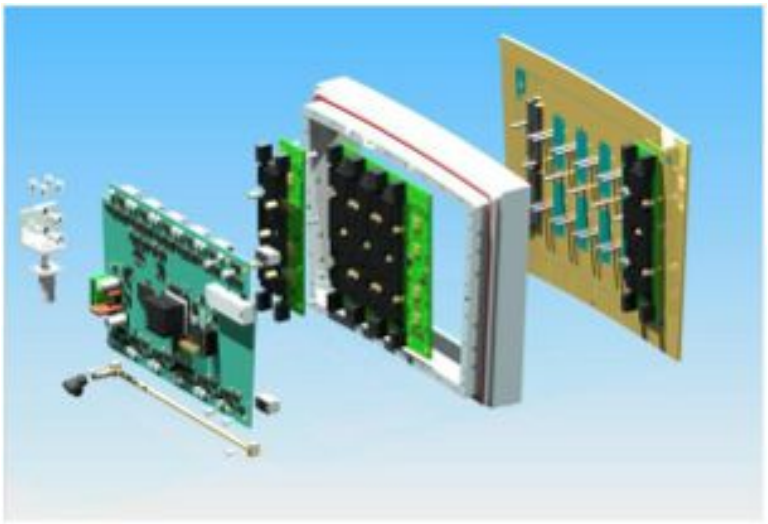

Figure 4.4: A fully integrated Micromegas panel, where one sees the Module Mezzanine card (FEMi), the air cooling pipe, the Front End Cards equipped of their radiators (in black), all this fixed to the detector PCB.

4.4 Tentative Roadmap towards the ILD TPC electronics

None of the test electronics realized so far is fully satisfactory for the ILD TPC. The AFTER electronics is based on analog memories of the SCA type, and these are not likely to reach a depth of nearly 20,000 buckets which would be necessary for a full train registering. On the other hand, the present SALTRO16 electronics requires further packing and its power consumption has to be optimized. This is the reason why the GdSP project offers a realistic alternative. The chosen deep submicron technology might have to be one supported by industry in the next decade. According to specialists, this will not be the case of 130 nm, but probably 65 nm minimum channel length is to be targeted. Already an overview study of this technology has begun within the European AIDA consortium. Going to such a fine technology will naturally save space on the die, and the power consumption will probably be reduced as such chips work at a reduced voltage. On the other hand, this might limit the total dynamic range, which is however not critical in our application. Present noise estimates with the 130 nm technology in standard conditions are of the order of 600 electrons. This will be thoroughly tested in the coming CFE (Common Front End) foundry of AIDA, end of November 2013. The GdSP would keep the digital filter integrated as for the SALTRO, but would feature several supplied voltage levels that could be switched independently during the course of the data taking, to optimize the power consumption. However, the future support

for this project is at the moment uncertain.

The ADC will have to be fully redesigned to minimize its consumption. The question arises whether or not this has to be done already in 130 nm technology. Some limited work could allow a suitable off-the-shelf design to be found.

If we aim at a startup around end of 2026, there is no real point starting the design already now. It would become obsolete at the time of production. So we should refine the requirements on the basis of detailed simulations in the next few years. If we want to make soon a new chip for testing purposes, in 130 nm, it will be difficult to fulfill all the requirements and it will probably obsolete at the time of chip production (around 2022). Whether and when new test electronics is needed is thus an open question and requires serious studies. A group has to be formed inside the LCTPC collaboration to consult specialists on chip design.

Chapter 5

Mechanics

The mechanical design challenges for the ILD TPC, i.e. the field cage, the endplate and the cathode, are to reach a high mechanical and electrical stability while keeping the material budget in front of the outer detectors minimal.

The mechanical stability and accuracy is needed to ensure a very homogeneous electric field inside the sensitive volume. To reach the resolution goal of 100 µm for the point resolution respectively $\delta(1/p_t) = 10^{-4}$ /GeV/c for the momentum resolution, the electric field has to be homogeneous to the level of $\Delta E/E \lesssim 10^{-4}$. The required electric stability results from the high fields used in the drift volume —$\mathcal{O}(100)$ kV, depending on the gas. Simulations showed that to keep energy loss in the TPC and conversions low to not signifcantly affect the calorimeter measurements and the particle flow reconstruction, the material budget has to be limited to 5% of a radiation lenght X_0 in the barrel region and 25% at the endcaps.

After tests with smaller prototypes with a diameter of about 300 mm, the Large Prototype with an outer diameter of 770 mm has been built to study and develop the design and manufacturing techniques for the ILD TPC. In the following sections the status of the development of the field cage (section 5.1) and the endplate (section 5.2) are presented.

5.1 Design of a new Fieldcage

One goal of the development of the Large Prototype was to study the momentum resolution and dE/dx measurement as a logical step after feasibility and point resolution studies performed with small prototypes. In addition, the technical challenges are studied, such as how to build a lightweight and mechanically precise field cage, anode endplate and cathode on a larger scale.

The field cage of the Large Prototype has been built in cooperation with industry. It is made of composite materials including additional layers for field shaping and insulation. This allows for a lightweight structure while

providing a high mechanical stability.

A schematic sketch of the field cage and the cathode is shown in figure 5.1. Its dimensions and a cut through the 25 mm thick wall is shown. Its length measures 610 mm —of which in operation about 570 mm are available as drift length— and an inner diameter of 720 mm. The material budget of the wall results in a radiation lenght of 1.21±0.1 % of X_0. The field shaping is done by a large, flexible printed circuit board with copper rings that divide the potential in small steps from cathode to anode. This board also has copper rings on the outer side to avoid distortions from the ground potential of the outer shielding layer. The current wall design has been tested for high voltage stability up to 30 kV. A more detailed description of the field cage and its construction can be found in [30].

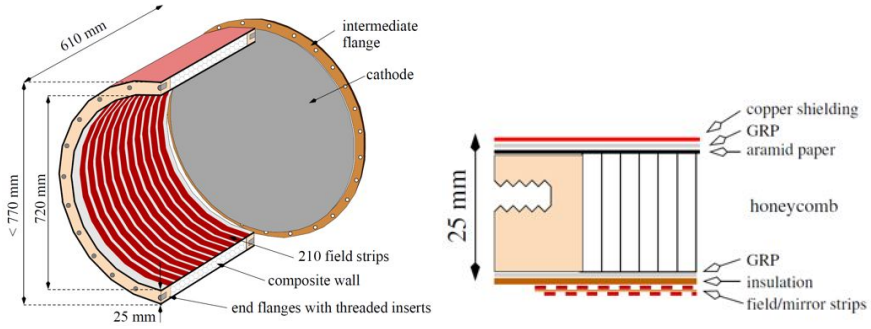

Figure 5.1: Schematics of the Large Prototype field cage (left) and cut though the field cage wall including the end flange at the anode side (right).

Due to a fabrication imperfection, the current field cage does not meet the accuracy specifications that are needed to ensure an electric field of the required homogeneity. The axis of the field cage barrel shows a shearing from the nominal axis of about 0.5 mm (figure 5.2), while 0.1 mm would have been acceptable for the needed field homogeneity. It was found that the reason for this shearing of the axis was an inaccurate mandrel on which the field cage was glued.

A second field cage is currently in development to correct the axis shearing. It is planned to build it in-house to gain experience with and have a better control of the production process. The mandrel has been worked over and measured so it fulfills now the precision requirements.

The new field cage will follow in most parts the design of the current one. However, some improvements besides the shearing correction are planned. The high voltage connection of the field shaping rings at the anode side will be re-designed based on experience gained during operation of the current field cage. This shall improve the high voltage stability and maintainability. Also, a further optimization of the material budget is planned. For this, it will be tested if some or all of the glass-fibre reinforced plastic (GRP)

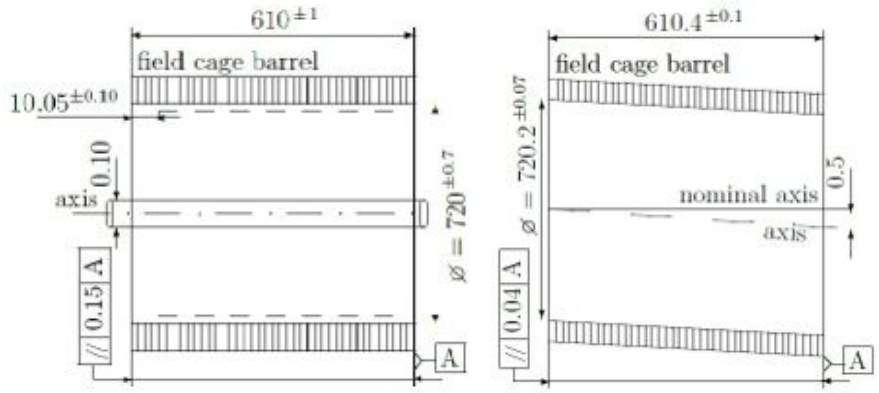

Figure 5.2: Dimension and precision specifications of the field cage (left) in comparison with the measured dimensions (right), showing the axis shearing.

layers could be replaced by Nomex paper without loosing mechanical stability. This replacement would also facilitate the gluing process during the production. In addition, it is considered to replace the metal inserts at the interface of the field cage to the cathode and anode endplates by inserts made of plastic. Which plastic types fulfill the mechanical requirements and could be used is currently under investigation.

The design and the implementation of the necessary machining tools has started as illustrated in figure 5.3, showing the design and the current status of the mandrel on which the field cage will be built.

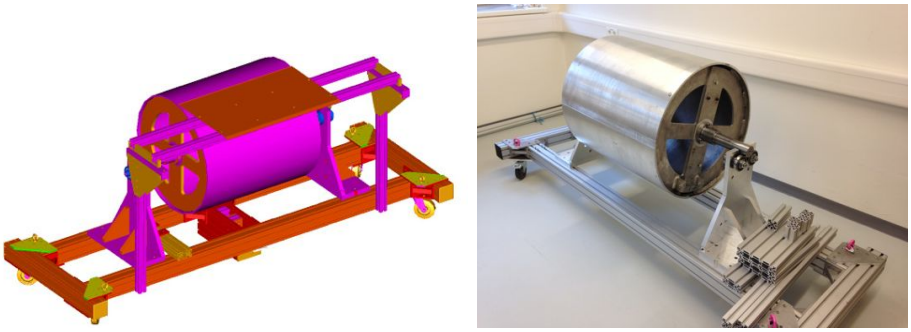

Figure 5.3: Design of the mandrel and the holding structure for fabricating the new fieldcage (left) and the current state of implementation (right).

The next step towards the second field cage will be to finish and align the mandrel holding structure. Then, some small test pieces will be produced first to test the mechanical and high voltage stability of a wall design without or with less GRP layers. Once a new wall structure is decided, one or more dummy field cage with a simplified wall design, i.e. without a field strip foil and an outer shielding layer, will be built to test the production

procedures. Once a production process is established, the final field cage will be built.
Further considerations for an improvement of this field cage or future iterations include the inclusion of a laser calibration system, that creates a "web" of ionizing beams inside the sensitive volume using a system of glass fibers and mirrors. Also, a simpler design for the field strip board is considered as described in reference [31].

Also, improvements of the cathode design are being investigated. The current cathode is built from a massive aluminum plate with copper plating. Two design alternatives are currently being studied. The first option is a more lightweight plate made from composite material with a copper layer. The production of sample pieces is planned once the production procedures for composite materials are established. The second option is to use a stretched, copper plated foil. First stretching tests with different foil types have been performed, but further studies are needed to determine the feasibility of this option.

In addition to the on-going development of the Large Prototype, studies are being performed how its design will scale to the dimensions of the ILD TPC. Due to the complexity of mechanical calculations and simulations including composite materials, contact has been established to specialized companies. First, very preliminary studies show promising results for the mechanical stability and precision of an ILD TPC using a scaled-up version of the current design. But to reach a reliable conclusion, further more detailed studies are needed and planned.

5.2 Development of a Low-Material TPC Endplate for ILD

As part of the development of a low-material TPC endplate for the ILD, a computer model of a space-frame endplate for the full ILD endplate has been generated and studied at Cornell. In addition, a fully functional space-frame endplate for the Large Prototype has been designed, modeled and constructed at Cornell. (In this document, the original Large Prototype, with the original endplate is referred to as LP1. The evolution of the Large Prototype, with a low-material endplate and other upgrades, is referred to as LP2.) Physical properties of the LP2 endplate have been measured and compared to model predictions to validate the model predictions for the ILD endplate. The LP2 endplate has been delivered to DESY for system evaluation.

Earlier work on the design and construction of the ILD and LP2 endplate have been previously reported in reference [32]. This document will mostly cover measurements made since that report.

5.2.1 Motivation

The central tracker for the International Large Detector (ILD) is a Time Projection Chamber (TPC) with outer radius 1.808 m, inner radius 0.329 m, total area 9.93 m^2, and half-length 2.350 m, shown in figure 5.4. The active area of each half of the TPC has outer radius 1.739 m, inner radius 0.395 m, total area 9.01 m^2, and drift length 2.2475 m.

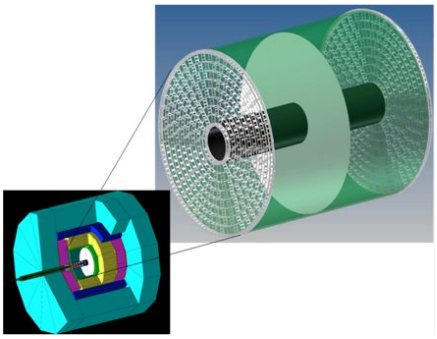

Figure 5.4: A TPC central tracker is shown in the exploded view.

While TPCs have been successfully employed at recent experiments, notably Aleph, STAR, and Alice, the tracking precision goals at the ILD lead to demanding design requirements.

Modular design: MPGD based gas amplification necessitates a modular design of the endplate which requires a certain amount of material to support the modules but keeps the structure rigid.

Rigidity: The requirements on the magnetic field calibration are at, or better than, that previously achieved with probe measurements. It is expected that track-based calibrations will be required to reach the required precision for both the mechanical and magnetic distortions. To partially decouple the mechanical and magnetic calibrations, the mechanical precision and stability of the modules must be limited to 50 µm. This mechanical requirement is at the limit of machining and fabrication practices; reaching this goal will require specialized construction techniques.

Low material: ILD end-cap calorimetry and Particle Flow Analysis (PFA) set a limit on the material that can be in the TPC endplate and readout. Current simulations set this limit at 25 % X_0, of which 8 % is allocated to the mechanical structure including module frames and supporting frame.

Minimal longitudinal space: ILD PFA also demands that the longitudinal space between the TPC active volume and the calorimeter be limited to 100 mm.

Simultaneously meeting all of these requirements is a challenge. The requirements for minimal space and material compete with the requirements

rigidity and a modular construction.

5.2.2 Measurements of the LP2 endplate

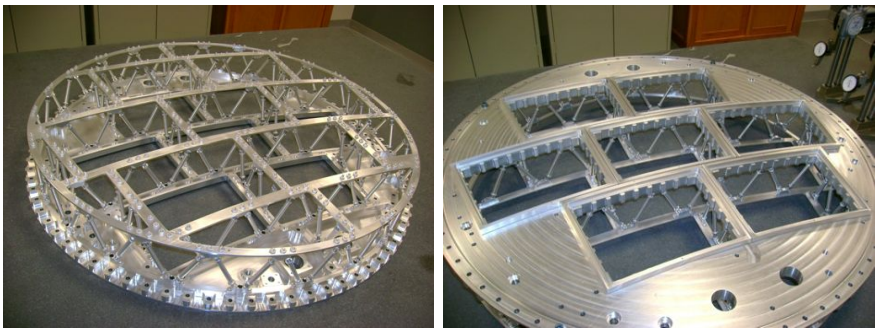

Figure 5.5: (left) The LCTPC LP2 endplate is shown from outside the chamber. This endplate is interchangeable with the LP1 endplate on the LP1 field cage. It is constructed in a strut space-frame design. (right) The same endplate is shown from inside the chamber.

The LP2 endplate, shown in figures 5.5 and 5.6 left, was completed 25-March-2012. Deflection of the LP2 endplate under load was measured and compared to the FEA. Load was applied uniformly over the mounting surface for the center module, as shown in figure 5.6 right. LP2 measurements were repeated since the 2012 note with the new measurement reported here. The

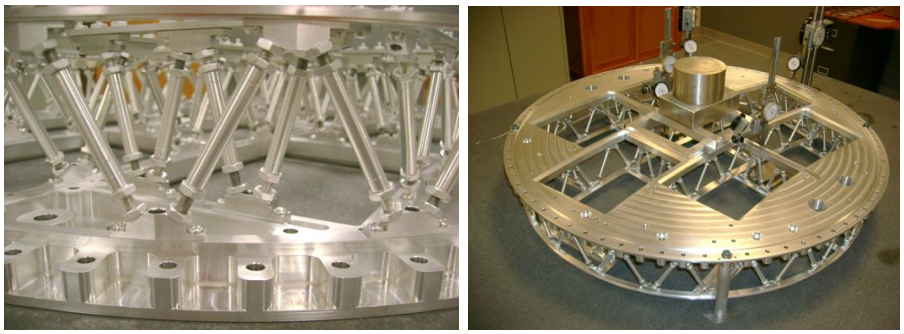

Figure 5.6: Left: A detail of the LCTPC LP2 endplate shows the strut space-frame construction. Right: The space-frame endplate is loaded at the location of the center module and instrumented for deflection measurements.

deflection is linear, as seen in figure 5.7. Comparisons of measured deflection with FEA calculations for the LP1 and LP2 endplates are summarized in table 5.1. The LP2 endplate measured deflection is 17 % higher than calculated. Table 5.1 also includes a lightened version of the LP1 endplate in which extra material is removed from the outer ring and uninstrumented

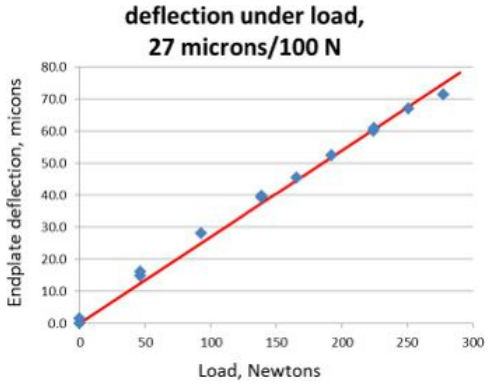

Figure 5.7: Observed deflection of the LP2 endplate as a function of applied load at the center of the endplate.

design	mass kg	material average % X_0	stress maximum % of yield	FEA deflection mm/100 N	Measured deflection mm/100 N
LP1	18.87	16.9	0.006	0.029	0.033
LP1, lightened	8.93	8.0	0.013	0.068	
LP2, strut space-frame	8.38	7.5	0.017	0.023	0.027

Table 5.1: Comparison of deflection measurements with FEA calculations for LP1 size endplates.

areas. This version retains the stiffening rib as used in the LP1 endplate. A material reduction similar to that of the space-frame design is achieved but with greater predicted deflection.

A goal was set for the surface flatness of the endplate to have a total run-out (difference between maximum deviation and minimum deviation) of 200 µm. After allowing the endplate to relax for six months after assembly, measurements of the surface flatness were taken by measuring the height of the surface above a flat table as shown in figure 5.8. The measured points are indicated in the figure, with a color-bar to indicate the deviation from the median level. The observed total run-out was 277 µm. After one iteration of realignment of the space-frame struts, as shown in figure 5.9, the endplate flatness was reduced to be within the specification. The final total run-out was then 178 µm as shown in figure 5.9 right.

5.2.3 Measurements using the ILD endplate model

Deflection of the ILD endplate due to a gas overpressure of 2.1 millibar, 2190 N total force on the endplate, was calculated with Finite Element Analysis

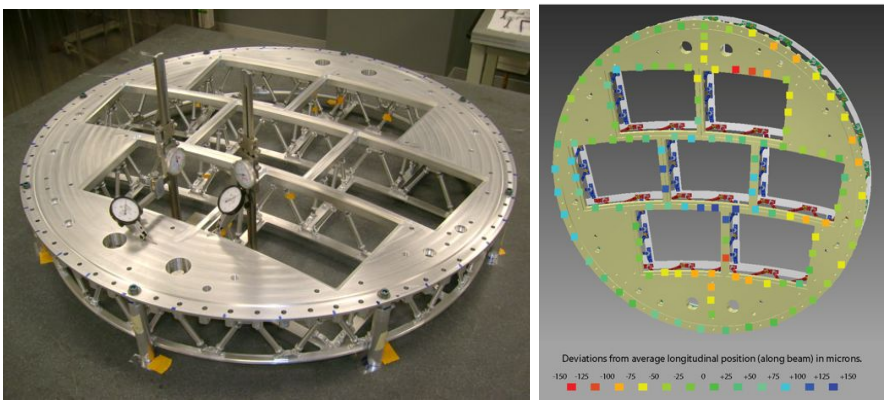

Figure 5.8: Left: Surface flatness is measured relative to a granite table. Right: Measurements are taken at multiple closely spaced points. The color-bar indicates the deviation from the median height.

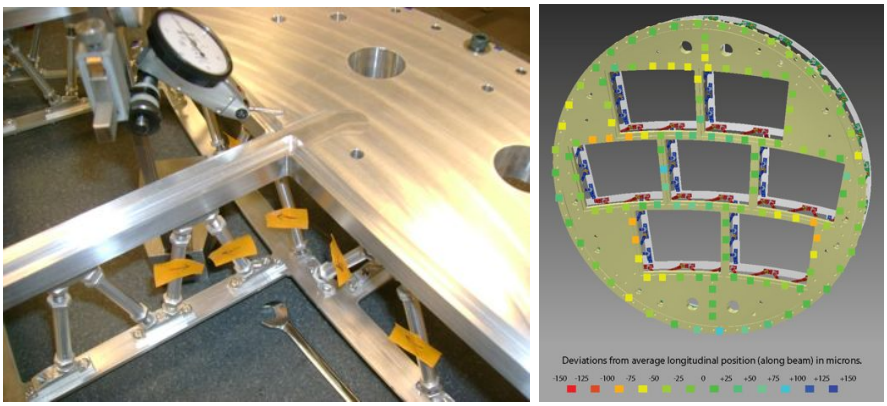

Figure 5.9: Left: Surface flatness is corrected by changing the lengths of the struts, which are precision turnbuckles with a pitch of 264 µm/turn. Right: Surface flatness measurements after realignment.

(FEA) to be 0.19 mm. Validation of this calculation was performed with measurements of deflection for small sections and the LP1 size endplates, which indicate that the FEA is accurate to within 17 %. Further FEA of the ILD endplate model was performed to predict more detailed performance of the endplate.

In the first test, the effect of installing an out-of-tolerance module was studied. As it is more straightforward to apply a stress, rather than a strain, to the model, the out-of-tolerance module was simulated as a stress that results in a 0.02 mm strain across a diagonal as shown in figure 5.10 left. The calculated strain, shown in figure 5.10 right, indicates that the local strain propagates across the endplate such that the strain is still 50 % of the

applied strain at a distance of 5 modules. The inner ring was seen to rotate by 10 % of the applied strain. The lesson is that a tolerance of about 0.030 mm is required for the locating the holes in the endplate and the modules to avoid propagating misalignment into the endplate. However, the existence of other modules may help to constrain the long-distance effects of out-of-tolerance modules. The effect may also be mitigated by installing modules with alignment holes only on one edge, eliminating the strain transferred to the endplate. Whether the locating tolerance can be achieved with fewer locating holes should be studied.

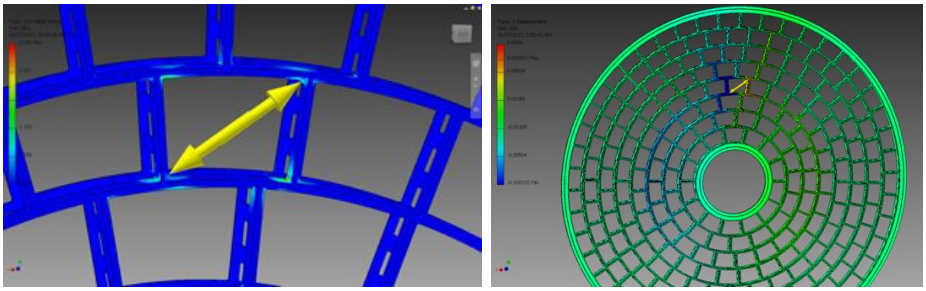

Figure 5.10: Left: A diagonal stress is applied across the location of a read-out module to simulate the effect of installing an out-of-tolerance module. Right: Calculated vertical motion resulting from an applied diagonal stress.

In a second test, the effect of supporting the vertical load of the TPC on finite point was studied. Forces and supports were applied as indicated in figure 5.11 left to simulate a 4-point support at the outer radius and a uniform vertical load at the center. (The center ring is rigid enough to distribute the discrete loads.) Scaling the calculated strain, shown in figure 5.11 right, to a total load of 104 N, the maximum vertical motion is 0.43 mm at the center of the endplate. While the motion is rather smooth, the differential motion over the distance a module is about 50 µm, which is at the threshold of loading the modules.

In a third test, the effect of a smaller number of module rows was studied. A variation of the endplate model was made with 4 module rows. In the standard model with 8 rows, each module covers 37700 mm^2. With pad dimension of 1×4 mm, there are approximately 10,000 pads per module. In the model with 4 rows, there are approximately 36,000 pads per module. Figure 5.12 shows the 8-row and 4-row variations of the model with an applied longitudinal force simulating the gas pressure. The longitudinal displacement on the 8-row model, when scaled to a force of 2190 N, is 0.19 mm as described above. The longitudinal displacement of the 4-row model is increased by a factor of 1.4. In the 4-row design, there is increased buckling as seen in the local variation in the horizontal displacement shown in figure 5.13. The amount of the buckling is 44 µm with the applied load of the

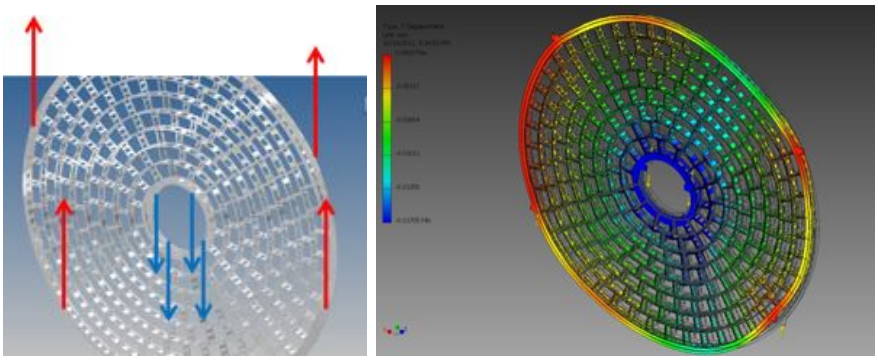

Figure 5.11: Left: Loads and supports used for calculating the endplate deflection due to supports at finite points. Loads (downward) are shown in blue and applied at 4 points. Supports (upward) are shown in red. Constraints are applied to stabilize the FEA. The upper right point is fixed for both rotations and motion in the longitudinal direction; the upper left point is fixed for rotation. The lower supports are simple forces. Right: Vertical displacement of the endplate under load. The color-bar indicates displacement for a 400 Newton total load. The maximum is zero at the support points; the minimum is -0.17 mm at the endplate center.

gas pressure. The buckling is in the back disk, not in the main plate that locates the module. However, the buckling should be studied for other load conditions if a 4-row design is pursued.

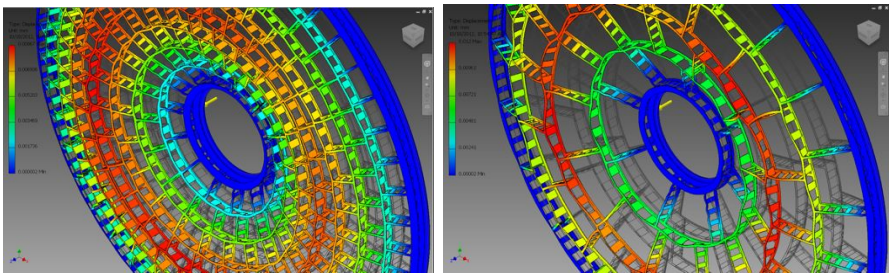

Figure 5.12: Left: Longitudinal strain for an 8-row model, right: Longitudinal strain for a 4-row model. In each case, force was uniformly applied to simulate the gas pressure. (The total force in the simulation is 100 N while the actual force on the endplate will be 2190 N.)

5.2.4 Issues related to the plate design space-frame

An equivalent plate design for the space-frame was considered and contracted at the scale of a small beam. (See reference [32]) The plates, by definition, are constructed to have strength that is equivalent to the struts.

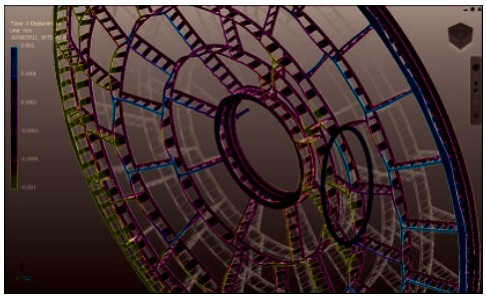

Figure 5.13: Horizontal strain in the 4-row model. The circle indicates a region of excessive local variation in the displacement.

This design may have advantages over the strut design constructed for the LP2 endplate. While the struts can be adjusted with precision, the plates can be made manufactured with precision height. But the plates must be glued in place and a procedure must be developed for gluing the plates in a controlled way in a structure of the size of the ILD endplate. In addition, the struts require attachment with aluminum screws which are tightened to about 40 % of the yield strength; creep may be a problem.

5.2.5 Possible issues related to scaling the LP2 design to the ILD endplate

A space-frame LP2 endplate has been successfully constructed. As this endplate has an outer diameter of 0.8 m, materials and facilities to machine the endplate are readily available. For the ILD endplate, producing the raw materials will require a custom set-up. Machining in one piece will require a milling machine with 3.6 m travel. These exist. Local tolerance can be as low as 25 µm, but global tolerance may be as high as 125 µm.

The assembly will require the installation of 3000 struts. Scaling the time to assembly the LP2 endplate, this will require 250 hours, but much of the work can be done by multiple people in parallel.

The alignment of the endplate, which requires adjustment of the struts, is not a 3000 degree-of-freedom exercise. Usually, 5 to 8 struts must be changed at any one time to effect a local alignment correction. An alignment iteration of the LP2 endplate required two hours. It can be expected that this time will scale linearly with the size of the endplate, so one alignment iteration can be performed on the ILD endplate in 40 hours.

Handling the ILD endplate may require special fixtures.

None of the above scaling issues present an unsolvable obstacle to building a precision space-frame ILD endplate.

Chapter 6

Software and Simulation

6.1 The Software Framework

The core software is provided by ILCSoft [33]. The basis is a common persistent data model called LCIO [34] which is used for simulation as well as for real data. The relevant geometry information for reconstruction and analysis is accessed through the GEAR [35] interface. The processing of data is handled through the Marlin [36] framework. Every reconstruction or analysis task is called a processor and runs on an event by event basis on LCIO files. These core tools provide a necessary basis to exchange data and reconstruction code. For the TPC specific software and especially for the data taken with the Large Prototype we have developed MarlinTPC [37] within the LCTPC collaboration. MarlinTPC contains reconstruction chains for all the different technologies and makes it possible to share the same code wherever possible. In addition dedicated simulation chains are available simulating the processes in the TPC in different levels of detail. Over a hundred processors are available to reconstruct and analyze data. MarlinTPC is distributed and developed using svn [38] allowing multiple developers to contribute to the software. Significant improvements were implemented within the last 2 years including the implementation of the GEAR interface for the TPC requirements and a basic reconstruction chain for all technologies.

6.2 Simulation

Different approaches to simulation are being followed within the LCTPC collaboration depending on the focus of the study:

- A detailed simulation chain of charge creation, drift, amplification and pad signal creation within MarlinTPC.
- Simulation of electrostatic and magnetic fields with CST™ [39].

- Simulating the drift of electrons in electric and magnetic fields can be done to a certain extent in MarlinTPC. In addition Garfield++ [40] is used to track electrons through field maps created for example by CST™.

- Simulation of field distortion due to ions is possible in MarlinTPC. Analytical methods are also applied to calculate the effects of ion disks on the field configuration.

- A simple simulation of the test beam setup consisting of the magnet and the Large Prototype is realized in Geant4 [41] to study for example the energy loss and multiple scattering effects of the geometrical setup.

The goal of the simulation is to describe the processes in the TPC from the charge creation to the measured data in various levels of detail. The transition from simulation into digitization is fluent. There are three main approaches as indicated in figure 6.1

1. Simple Digitization
   The energy loss is calculated with Geant4. A simple smearing of the position of the charge according to a parametrization obtained from prototype studies is applied.

2. Electron Cloud Simulation
   The ionization process creates charge clouds that can then be drifted including effects from magnetic field lines. The amplification is modeled based on knowledge from measurements

3. Primary Electron Simulation
   Each primary electron is created in the simulation, then drifted considering the electric field lines. The same is carried out for the created primary ions. Electrons are amplified including a feed back loop to account for the ions created during amplification.

Common to all simulation chains is the modeling of the electronics to create pulses stored in the raw data format to match the real data measured with prototypes.

6.3 Data Reconstruction

Depending on the readout granularity we have to distinguish between two concepts: pad based and pixel based readout. The row based reconstruction approach applied to the pad based readout is not suitable for the pixelized readout as the concept of a row is no longer valid, thus different reconstruction strategies are followed as explained in the following two subsections.

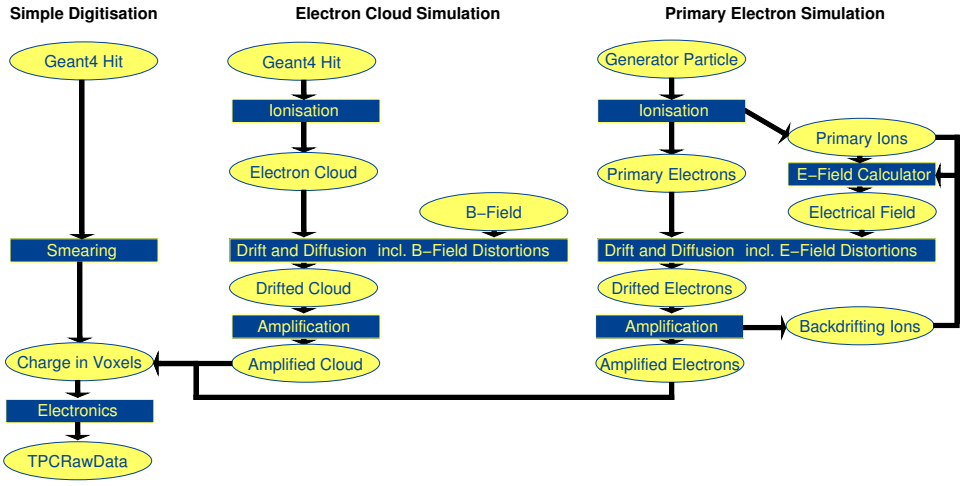

Figure 6.1: Overview over the three different simulation approaches with different levels of detail.

6.3.1 Pad Based

During the reconstruction of the raw data taken with a TPC, different data objects listed in table 6.1 are created and filled with information successively.

Data object	Description in the context of LP data
TrackerRawData	The ADC spectrum as it comes from the electronics.
TrackerData	The ADC spectrum after e.g. calibration.
TrackerPulse	A pulse is a charge bucket in time on channel basis.
TrackerHit	A hit combines pulses belonging to a cluster along a row and in time into a 3D position.
Track	List of all TrackerHits forming one Track and the computed track parameters.

Table 6.1: LCIO data objects used for the TPC reconstruction.

The main reconstruction steps for GEM and MicroMegas amplification technologies are:

1. Find pulses on each channel.
2. Combine pulses close to each other along a row into a hit.
3. Find and fit a track.

Figure 6.2 shows one example of an iterative reconstruction flow currently used in the analysis of recent test beam data with GEM modules. In a

first iteration a reconstruction is carried out assuming knowledge of some parameters like the drift velocity. A second iteration than applies and uses the information gained from the first iteration. In a last step corrections are applied that have been determined in the second pass.

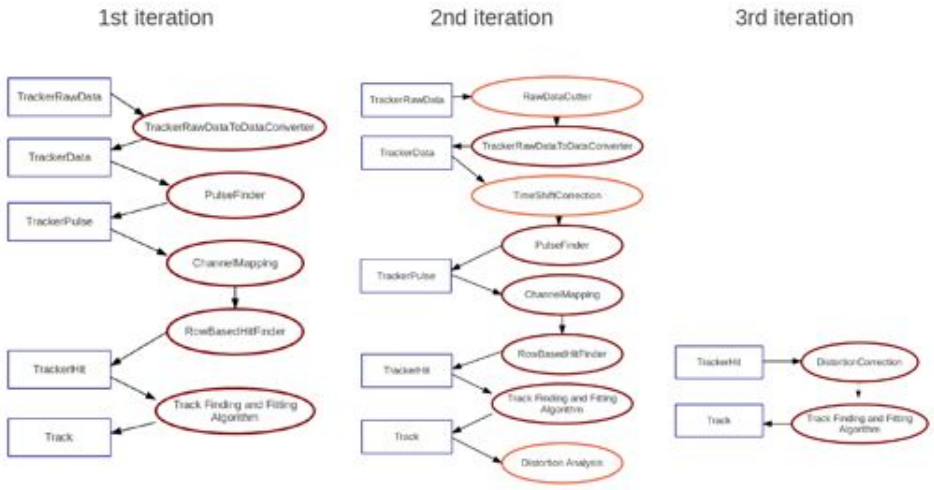

Figure 6.2: An example of an iterative reconstruction flow currently used in the analysis of recent test beam data for a GEM readout.

The reconstruction for GEMs and MicroMegas up to the hit level follows slightly different approaches due to differences originating from the technology choice itself and the different readout electronics used. The pulse reconstruction differs due to the pulse shape which is dominated by the readout electronics. The other differences in the reconstruction stem from the fact that the MicroMegas use a resistive foil to spread the charge across the pads. This changes the timing of pulses within a hit and the way the charge is obtained. Those are the main reasons why the reconstruction of GEMs and MicroMegas each have their own pulse and hit reconstruction processors. For a better understanding of the differences due to the readout electronics a test beam campaign was carried out, by reading out a MicroMegas module with the ALTRO electronics usually used for GEM modules. The data analysis is still ongoing.

6.3.2 Pixel Based

Each pixel records either the charge collected or the time at which the pixel is hit. Starting from the counter values of the pixels that have collected some charge, the data objects provided by LCIO are subsequently filled as listed in table 6.2

The definition of a hit is different depending on the amplification struc-

Data Object	Description in context of LP data
TrackerRawData	Counter values as read in from the original ASCII files
TrackerData	As above after interpolation of defective pixels and application of zero supression, calibration and time walk correction.
TrackerHit	Positions of the primary charges derived from the centers of the hit pixels and the measured drift times.
Track	List of all TrackerHits forming one Track and the computed track parameters

Table 6.2: LCIO data objects used during reconstruction of pixel-TPC data.

ture used. In case of the InGrid based readout, it is assumed that each primary electron traverses one hole in the grid and, consequently, triggers only one pixel. The original position is then calculated from the pixel center and the measured arrival time of the incident charge.

In case of the GEM based readout, each primary electron creates a charge cloud triggering many pixels. A hit is reconstructed as the center of gravity of the measured electron cloud underneath the GEM stack.

6.3.3 Tracking

Finding a collection of hits belonging to a track and then fitting those, is a common reconstruction issue for all technologies and readouts. However in the case of a pixelized readout the number of hits can be very large. This poses a challenge to the software in terms of CPU time and at a certain point also to the memory management. Within the last year several new packages have been developed to find and fit tracks. Very recently the tracking package used in ILCSoft for the full detector simulation and reconstruction has been adapted to work as well on the LP data. Finding algorithms range from a Hough Transformation over topological pattern recognition to the application of Kalman Filter techniques. The same is true for fitting algorithms where the variety is even greater. The next step is a systematic study of the performance of the main packages. Based on these results we will be able to choose a default track finder and track fitter for our data reconstruction.

An important point to keep in mind is that the tracking tools need to be able to cope with alignment. This means that the geometry used inside the tracking has to be flexible enough to allow for rotations and translations of the modules and therefore the measurement layers. Another important aspect is that information about the alignment can be obtained during the track fitting stage. This for example is used in the General Broken Line (GBL) algorithm which calculates the necessary input for Millepede, an

alignment program.

In the future the tracking also needs to be able to handle inhomogeneous electric and magnetic fields.

6.4 Data Analysis

The goal is to provide all necessary tools to ensure a procedure that allows to compare all technologies proposed on equal ground. This requires common and exchangeable code, but also a set of rules and conventions. Efforts have started to define common procedures and plots. We are now well on the way to provide common analysis processors in MarlinTPC which create the same plots under the same conditions. This will then allow us to understand and compare the performance of the different module designs, electronics and technology performance. Recently we have defined a list of plots that will enable us to carry out such a comparison. The plots are divided into categories. The first contains the performance plots shown at conferences and most likely used to compare the technologies. The second category are plots to ensure the data quality and show the results in a more detailed way. The following performance plots were defined:

- Resolution in $r\phi$ and z for B=0,1T at $\theta = 0$ and for two ϕ angles Two curves should be shown in the resolution curve. The first showing the resolution of the best row only indicating what the module could do. The second should combine all rows but separate the effects caused by distortion. One simnple way to achieve that is to evaluate the resolution of each row separately and then the mean is taken. This curve then shows the overall performance of the module if distortions can be corrected.

- Distortions for each row in ($r\phi$,z) for B=0,1T at $\theta = 0$ and for two ϕ angles

- Diffusion: The width of the Pad Response Function width dependence on the drift distance

- Hit Efficiency for one row as a function of the drift distance

- Hit Efficiency with dependence on the row

- Momentum Resolution

For the pixel based readout the same plots can be made. Resolution and distortions are evaluated in xy instead of $r\phi$ and hit efficiency will be defined differently.

6.5 Conditions Database and Grid Usage

During reconstruction certain information is needed e.g. the channel mapping, electronics information like the noise level of a channel and many other details about the conditions at the time the data was taken. For this purpose a data base can be used to store this information. The Linear Collider Conditions Data toolkit (LCDD) [42] facilitates the communication with the data base and allows a Marlin processor to monitor at run time whether the conditions have changed on an event by event basis.

Test beam data is stored on the grid making it available to all groups. The raw data as well as the converted LCIO files and corresponding information like the gear file and the channel mapping are stored. All data sets from test beam campaigns in the recent years have been uploaded.

6.6 Outlook and Tasks

Good progress has been made in the last couple of years towards full reconstruction chains for all readout modules developed within the LCTPC collaboration. Different track finding and fitting tools have become available and need to evaluated. We have started to look into the alignment of the modules and test especially the tracking packages for their capability to handle misaligned modules.

The correction of distortions are at the moment data driven. A better way would be to develop a better understanding of the contributions to the distortions and use a model prediction to apply such a correction.

Recently the focus turned towards common tools and methods especially for the analysis. We expect significant progress towards a common analysis tool base by the end of the year.

Some issues have been identified, mostly related to improvements in the reconstruction of pulses and corrections due to pulses in over-range or dead channels in a hit. Systematic effects like a time walk were observed in the time reconstruction and need further studies to develop a strategy for corrections.

The data analysis has been focused so far on the single point resolution. The next important step would be to look at the momentum resolution. Without an external reference at the low energy electron test beam at DESY, this is extremely different. We have some ideas on how to create a reference from the data itself which have to be tested.

Another topic is the dE/dx measurement. Tools for such an analysis can be prepared, but a multiple particle beam would be needed for a proper evaluation of the separation power. A key item in order to study dE/dx is a proper gain calibration. This includes a channel by channel electronics calibration as well as the non-uniformity within the amplification structures. At

present no software exist due to the lack of information from measurements. A place for such information is however foreseen in the data base.

Chapter 7

Outlook

7.1 Performance of the ILD TPC

The physics at the linear collider requires significant advances in detector performance. For the tracking system the main requirements are twofold:

◦ The charged-track momentum resolution is driven by the Higgs-strahlung process, where the recoiling Higgs is reconstructed from the associated Z boson decaying into a lepton pair. The resolution goal for the tracking is $\delta 1/p = 2 \times 10^{-5}$ / (GeV/c).

◦ Particle Flow Algorithm (PFA) needs excellent performance of the calorimeter and the tracking. Much (about 65%) of the energy deposited in the calorimeter is generated by charged tracks which must be well measured and followed into the calorimeter. The success of our PFA, with envisaged precision of 3 to 4 % for 100 GeV jets, means that we need a highly efficient tracking down to low momentum in the multi-jet events.

As central tracker for the ILD detector, the LCTPC collaboration has been developing a TPC based on the MPGD technology with $r\phi$ spatial resolution of 100 microns or better for all drift distances. The push since 2008 has been work using the Large Prototype at DESY. R&D efforts have been described in the previous sections of this report.

An overview of the goals as presented in the DBD is given in Table 1.1 of chapter 1.

A summary of what has been learned up to now is:
◦ the MWPC option has been ruled out,
◦ the Micromegas option without resistive anode has been ruled out,
◦ gas properties have been well measured,
◦ many years of MPGD experience has been gathered,
◦ the best possible point resolution is understood,
◦ the resistive-anode charge-dispersion technique has been demonstrated,
◦ reliable assemblies of GEM-modules and Micromegas-modules have been developed,

◦ CMOS pixel RO technology has been demonstrated.

7.1.1 Remaining R&D Issues for the next few years.

Although we have shown that the ILD TPC satisfies the basic requirements, we have several R&D issues which must be worked on:

◦ Design/test gating device
◦ Issues for the MPGD technologies
◦ Local distortions
◦ Demonstration of power pulsing for the readout electronics
◦ Cooling of the electronics and temperature control
◦ Demonstration of performance at 3.5 T
◦ Measurement of double track/hit resolution.

7.1.2 The Ion Gate

One of the most important and urgent issue is the ion gate. A ion gate in front of the MPGD module prevents feedback of secondary ions that are produced the gas amplification region from entering into the drift region.

Preferred by many is a GEM gate option with a high electron transmission ($\geq$ 70-80 %) which would avoid a large deterioration of the momentum resolution. A GEM gate can be stretched on the current MPGD modules with minimum modification of the structures. The only existing GEM gate fabricated for the Asian GEM module has an electron transmission of only about 50 % at 1 T.

The challenges for the GEM gate R&D are:
◦ how to fabricate a GEM gate with large optical aperture and very thin rims, and
◦ to find a product that is strong and stable enough to be stretched onto the MPGD modules.
The recent R&D for the GEM gate in Japan is promising, but there has been no realistic hardware prototype to test yet.

If the GEM gate turns out to be problematic, it will be necessary to use a traditional gate with fine wires stretched directly on the MPGD module and the gating function given by switching between alternating wire-to-wire voltages. Another possibility is a simple grid or wire mesh for which the voltage is the same for all wires and is swung to reverse the drift field and absorb the ions; for this type of gate, measurements must be made to find out which ion suppression can be achieved for which voltages. In either case it would be necessary to redesign the module, and this modification might result in an increase of dead area and of material budget around the module boundary.

According to the overall ILC schedule presently discussed, we should decide which type of the ion gate to be used at ILC in one or two years. This early decision is necessary in order to finalize the designs of the MPGD modules, and to test them. These tests could eventually result in prioritization of the MPGD technologies for the final module design for the ILD TPC.

7.1.3 Issues for the MPGD technologies

For the multilayer-GEM technology the readout pads see the real charges of the gas-amplified electrons, and the data analysis for the GEM modules is simpler.

In the case of the resistive anode readout, the readout pads see only the induced charges of the currents in the resistive anode which flow to ground along the resistive anode. At the linear collider there will be many hits from the physics events as well as from backgrounds. Although the Micromegas detectors readout by the resistive anode has been measured to be as fast as 10 or 20 kHz per 10 cm^2, the hits from events and backgrounds will be much higher. Therefore one should make sure either by simulation or measurement that there will no signal pile up problem in the resistive anode at the ILC which might deteriorate the spatial resolution.

There are also issues with GEM technology. The module structure of the multilayer GEM module is more complicated with several layers of GEMs and multiple high voltage connections. Here we have to design for reliable operation of many GEM modules for long periods of time at the ILC. At the moment, Asian GEMs have micro-discharges which have to be eliminated during the next iteration. The DESY GEM modules no longer have this problem which was recently solved

The current digital TPC option with the InGrid Timepix using bonding wires for contact with the chips is still has far to go for a final module design. To replace these bonding wires, which are the sources of local distortions and dead regions, with silicon through-holes, it will be helpful to have an early transition to the Timepix-3 chip.

The digital TPC team plans to build an Large Prototype module fully covered by the current InGrid Timepix chips, and the GEM and Micromegas groups are also preparing further tests in the Large Prototype at DESY

7.1.4 Local distortions

In the module design we try to minimize the dead regions in rϕ between the MPGD modules to avoid losing significant parts of tracks in those regions.

We have found in the Large Prototype beam-test results rather large local distortions for all modules as discussed in the chapter 2. The local distortions arise from the $E \times B$ effects due to local non-uniformities of the

electric field. These are either due to
◦ the gaps between the MPGD modules, and/or
◦ design of the MPGD module boundaries.
It looks like that these can be reduced in the near future.

More serious is the distortion at the gap between the modules. This gap is needed for installing the modules. The current gaps are roughly 1 mm. Our simulation programs to calculate the electric field can reproduce the distortions, so that it will be possible to propose measures to reduce the distortions, in this case by adding electrodes on the modules. This was demonstrated for the DESY GEM modules.

Since we aim at a much better spatial resolution than the size of the distortions, we still have sufficient work ahead to correct them.

7.1.5 Demonstration of power pulsing for the readout electronics

As discussed in the chapter 4 above, we need a power pulsing of the frontend electronics, which will be determined by the ILC beam bunch structure, in order to further reduce the power consumption and therefore the heat dissipation. During the interval of 199 ms between the 1 ms bunch trains at ILC, the readout electronics is kept in its standby mode.

The test of the power pulsing of the SALTRO chip has been made, and the power reduction factor of around 30 was demonstrated. The power consumption of the SALTRO16 chips is about 750 mW (with present ADCs which have rather high power consumption), and in the standby mode about 30 mW. We plan to demonstrate the power pulsing of the SALTRO16 electronics at the board level in beam tests, hopefully in 2014-2015.

7.1.6 Cooling of the electronics and temperature control

We plan to use two phase CO2 (2PCO2) cooling for the readout electronics on the back of the MPGD modules. This cooling method uses high pressure 2PCO2 has a large cooling capacity (300 Watt/g) at constant temperature. The 2PCO2 flows with low viscosity and at high pressure so that thin cooling channels embedded in the MPGD modules may be used with a minimum of material budget. The ILD TPC project is now preparing two small cooling units of the 2PCO2 for cooling tests, one of them is at KEK (together with the Vertex group, for -40° C operation), and another unit at NIKHEF optimized for the room temperature cooling which is foreseen for the TPC operation. The NIKHEF system will be set up at the DESY beam test area in 2014.

7.1.7 Demonstration of performance at 3.5 T

Most of our beam tests have been carried out in the 1 T magnetic field of the Large Prototype at DESY. Extrapolation of the results to the 3.5 T magnetic field of ILD have been done using our analytic formula for the MPGD TPC spatial resolution. Although this analytic formula is reliable, being based on a few principles of a gaseous detector, the parameters of the TPC gas at 3.5 T are taken from simulations.

Thus it would be advisable
◦ to confirm these parameters and the MPGD performance at high magnetic field, and
◦ to address some mechanical issues at 3.5 T (for example, possible vibrations due to the power pulsing).

We used the 5 T solenoid KOMAG at DESY for some time measuring the spatial resolution of a small prototype. Unfortunately this magnet has been disconnected from the new liquid He line at DESY and not usable any more. For the tests, it would be desirable to use a magnet organized by one of the institutes of the LCTPC collaboration.

7.2 Engineering design issues for the ILD TPC

After completion of the ILD DBD this year we are approaching the engineering design phase of the ILD TPC. The Technical Design Report (TDR) for the ILD TPC and tracker system is due in 4-5 years time.

7.2.1 Readout electronics

In chapter 4, many aspects for the electronics were described: T2K electronics, ALTRO electronics with PCA16 preamplifier chips, and the SALTRO16 electronics currently developed. Planned was that the GdSP development, successor to the SALTRO project, be the start of the final effort.

The problem now is that the project has lost some clients and support. Also, the LCTPC collaboration is missing its own group of electronic experts and its own budget for the development of the read out.

Considering the current situation of the our collaboration and the ILC schedule, we are trying to develop a plan to build up our own group of electronics experts including chip designers. The aim will be to activate its final design study in 2017-2019. Meanwhile we will focus on the development of the SALTRO16 system to test power pulsing, to minimize the number of the power boards, and to read out new modules with gate in the Large Prototype.

7.2.2 Fieldcage and endplates

The status of the mechanics is covered in chapter 5.

We have done so far the following; construction of a light and thin fieldcage for the Large Prototype, the construction of the two types of Al endplates for the Large Prototype, simulation work for the fieldcage and for thinner endplates, and a study of the TPC support inside the ILD detector. In addition, we are preparing a thin central cathode, a tool for the installing the modules, and a laser-beam calibration system.

However many of the details are still to be studied. They include:
◦ Detailed overall mechanical design of the TPC
◦ Procedures for the TPC assembly and installation
◦ Detailed plan of for construction and task sharing
◦ Structures related to the field cages
◦ A device for the TPC gas circulation
◦ A thermal design of ILD TPC
◦ A monitor system to align and position control, and other passive monitor systems.

To carry out of all the above in time for the TDR, we have to enlarge our LCTPC mechanical group as soon as possible.

7.2.3 Software

A summary of software and simulation efforts is the subject of chapter 6.

So far we have developed the software packages for the Large Prototype beam test and also for our TPC R&D. MarlinTPC is the commonly used software package for reconstruction of TPC tracks and analysis. The reconstruction code is used also in the physics simulations for the ILD detector showing that the TPC continuous tracking is very robust against backgrounds. We have now a tracking code for a non-uniform magnetic field. The study of the local distortions of the MPGD modules has to be continued using simulation programs for the design of new modules with an ion gate. The correction software for remaining distortions is also urgent.

In coming few years before the TDR, further software efforts are listed next:
◦ more simulations of the local distortion and its correction
◦ simulation studies for the TPC optimization
◦ continuous update of the background expected in the TPC (including neutrons)
◦ demonstration of the bunch tagging in the ILC multi-bunch events
◦ finished completion of the tracking code for the digital TPC.

Here again we have the problem of resources, in particular human resources.

7.3 A possible timeline for the ILD TPC R&D

This timeline has been developed by physicists (like us). The final time schedule will depend on political realities, i.e., when the world politicians agree on how and when the ILC can be financed and built.

2014 R&D on GEM/wire gates
2015 Decision on the ion gate
2015-17 Beam tests of new Large Prototype modules with the gate
2017 ILC accelerator & ILD detector proposals
2017 Prioritization of the MPGD technology and modules
2017-19 Design of the readout electronics for ILD TPC and its verification
2018-19 Design of ILD TPC and TDR (for the ILD tracking system)
2019-23 Prototyping and production: Electronics
2020-23 Prototyping and production: Modules
2020-23 Production: Field cage, endplate and related things
2024-25 TPC integration and test
2026 TPC Installation into the ILD detector
2027 ILC commissioning

7.4 Conclusions

The TPC Large Prototype beam tests at DESY have shown that the basic performance goals for of the ILD TPC, in particular, the pad readout options, are satisfied. It was demonstrated how to build some important components such as a thin field cage and lightened Al endplates.

The important R&D issues discussed above will addressed in coming few years before the detector proposal. The timeline for the ILD detector looks rather tight, while the available resources of the LCTPC collaboration are very limited.

We expect the manpower situation to improve as soon at the ILC in Japan is approved officially.

Nevertheless we would like to ask for more support for our activities now.

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