ILC R&D activities involving SOI pixel detectors (addendum)

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http://rd.kek.jp/project/soi/

\* Major R&D efforts and recent developments since ILC DBD (with publications/references to major results);

At present, major issues in the SOI pixel development are 'back-gate effect', 'hole trap under the transistors by radiation', and 'sensor-circuit cross talks' as shown in Fig. 1. For these, we have been developing a double SOI technology. The developed double SOI wafer has an additional middle-SOI(Si) layer under the transistors. The conduction layer of the middle-SOI can solve all the three issues. We could successfully process the double-SOI wafer (Fig. 2). Threshold shift by radiations is successfully recovered by applying compensating voltage to the middle SOI layer (Fig. 3).

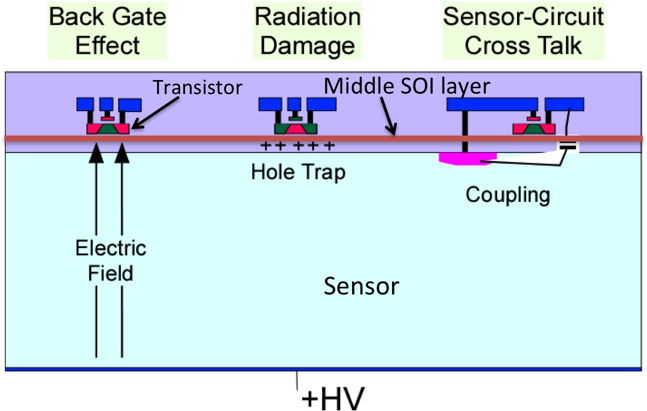


Fig. 1 Major issues in the SOI pixel detector and introduction of a middle-SOI layer.

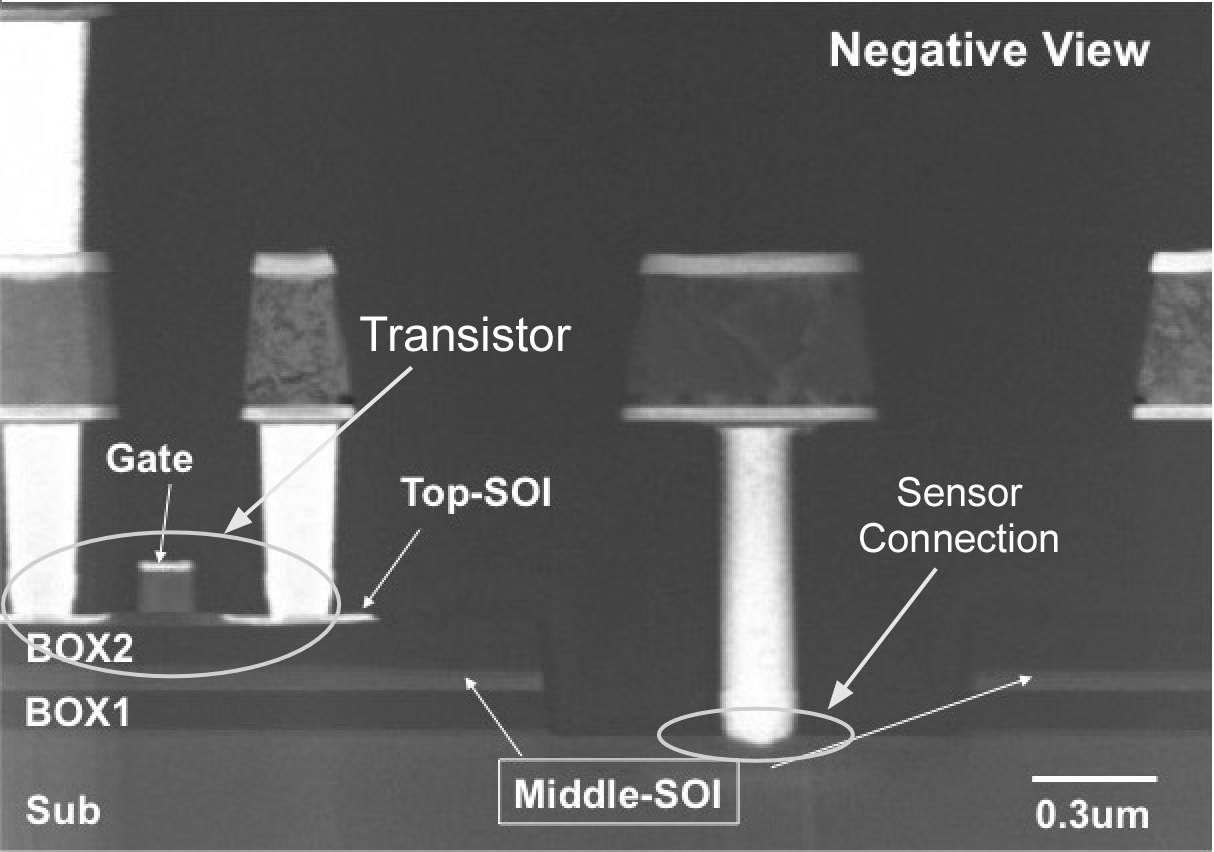


Fig. 2 Cross section of the double SOI chip after processing.

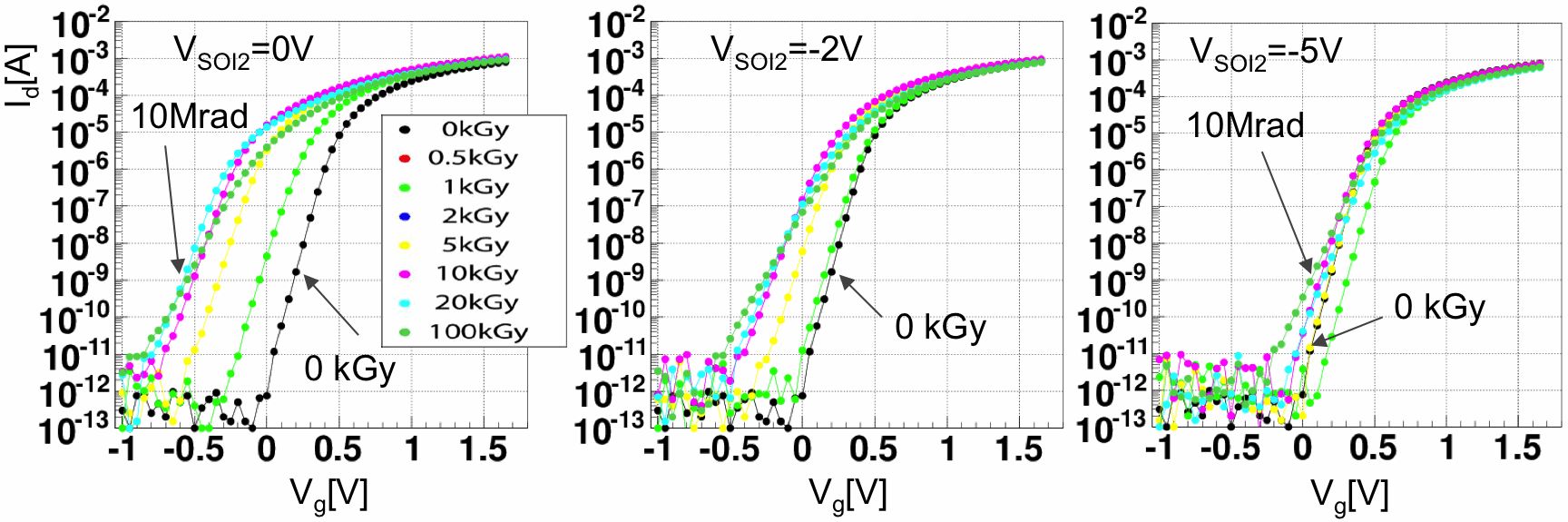


Fig. 3 Threshold shift recovery by applying compensating voltage (Vsoi2) to the middle Si layer.

\* Engineering challenges;

The resolution for the ILC vertex detector is required as better as a few um. This means pixel size must be less than 20 um square or so. On the other hand, each pixel must register arrival time of the hits during bunch train etc., so this requires many transistors and capacitors must be located in each pixel area.

Natural solution to this is 3D vertical integration of circuit layer. SOI technology is very fit to the 3D integration since the thinning is stopped at the buried oxide (BOX). We already tried 3D SOI pixel chip in collaboration with T-Micro Co. Ltd. Process flow of micro-bump 3D connection is shown in Fig. 4. We have confirmed low resistance (~6 Ohm/bump) between upper and lower tiers for 1,000 daisy chain (2,000 bumps) as show in Fig. 5.

However, we think much higher density digital circuit such as 32nm technology may be necessary for the upper tier in the ILC. This requires bonding of two different technology wafers. The 3D integration of different technology wafers (or chips) is still engineering challenge.

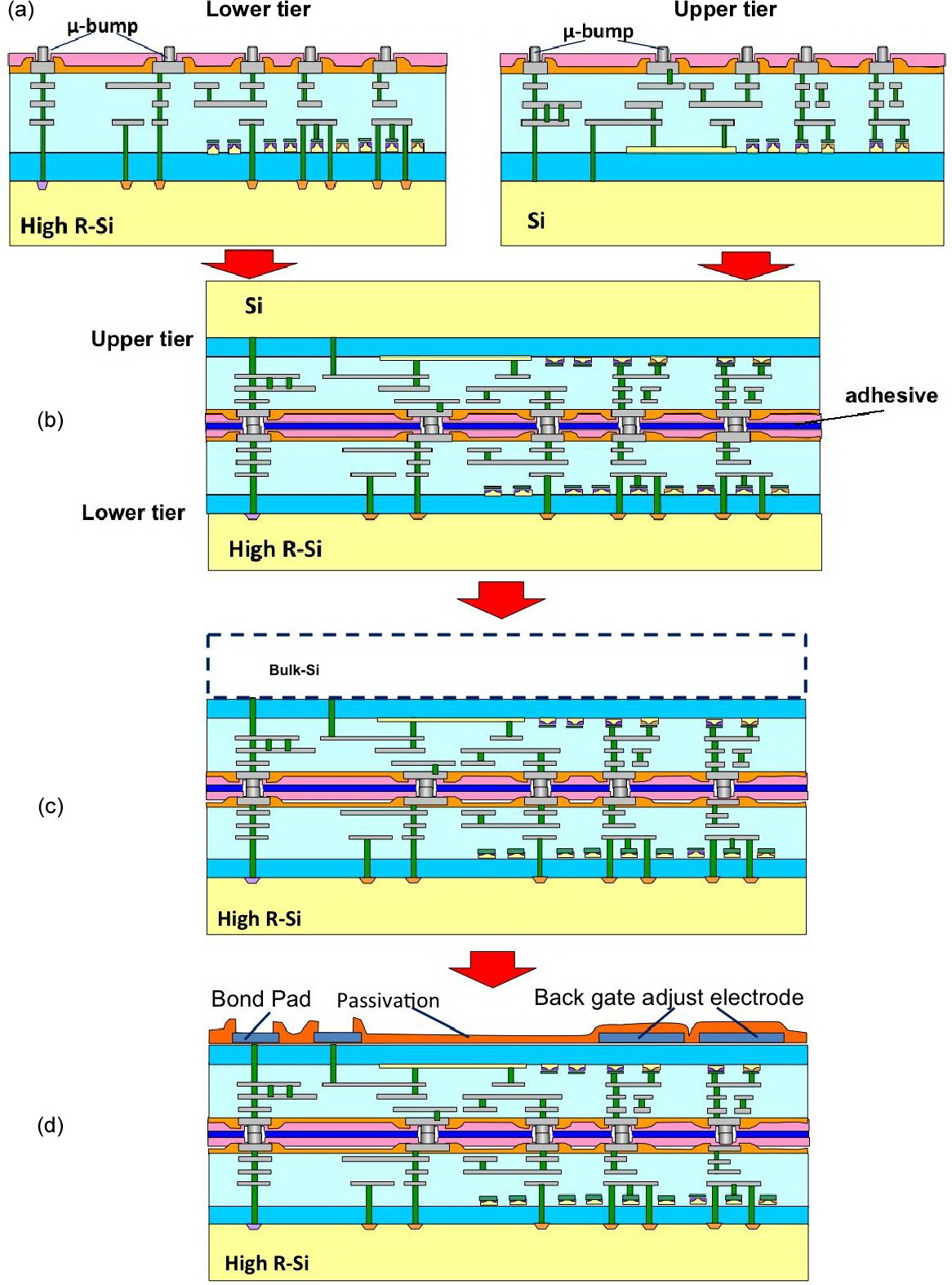


Fig. 4 Micro-bump 3D integration process flow of the SOI pixel.

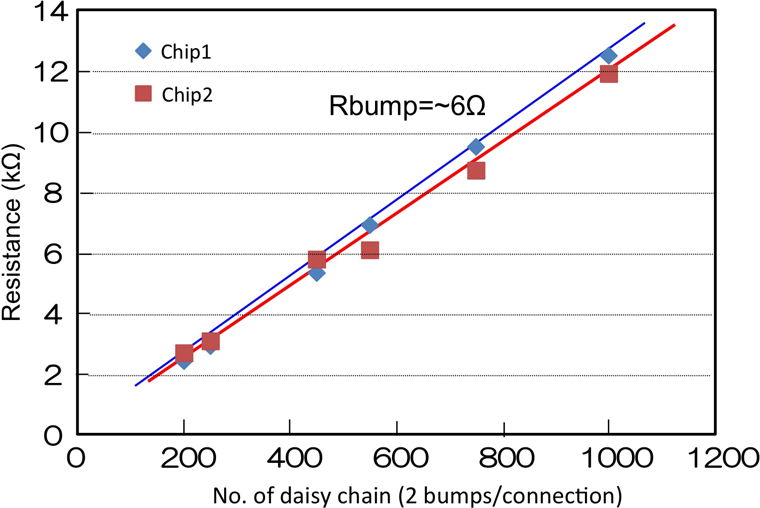


Fig. 5 Resistance of micro-bump daisy chain between upper and lower tiers.

\* Detector R&D plans for the coming years;

We are planning following items for the coming year.

* ~Sep. 2014 : Complete architecture study for the ILC pixel detector.
* ~Mar. 2015 : Design and fabrication of first test chip for the ILC.
* ~Dec. 2015 : Beam test of the test chip.