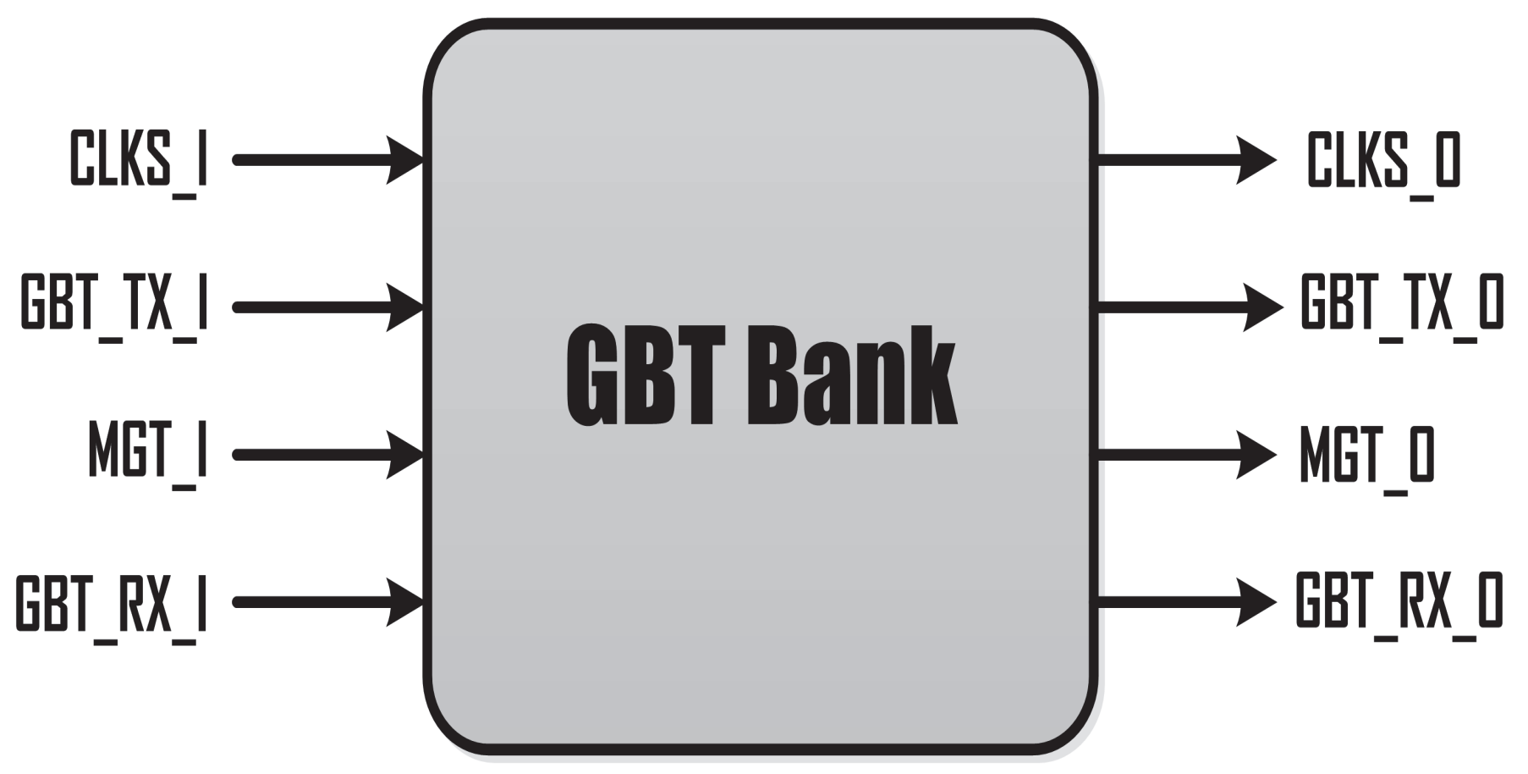
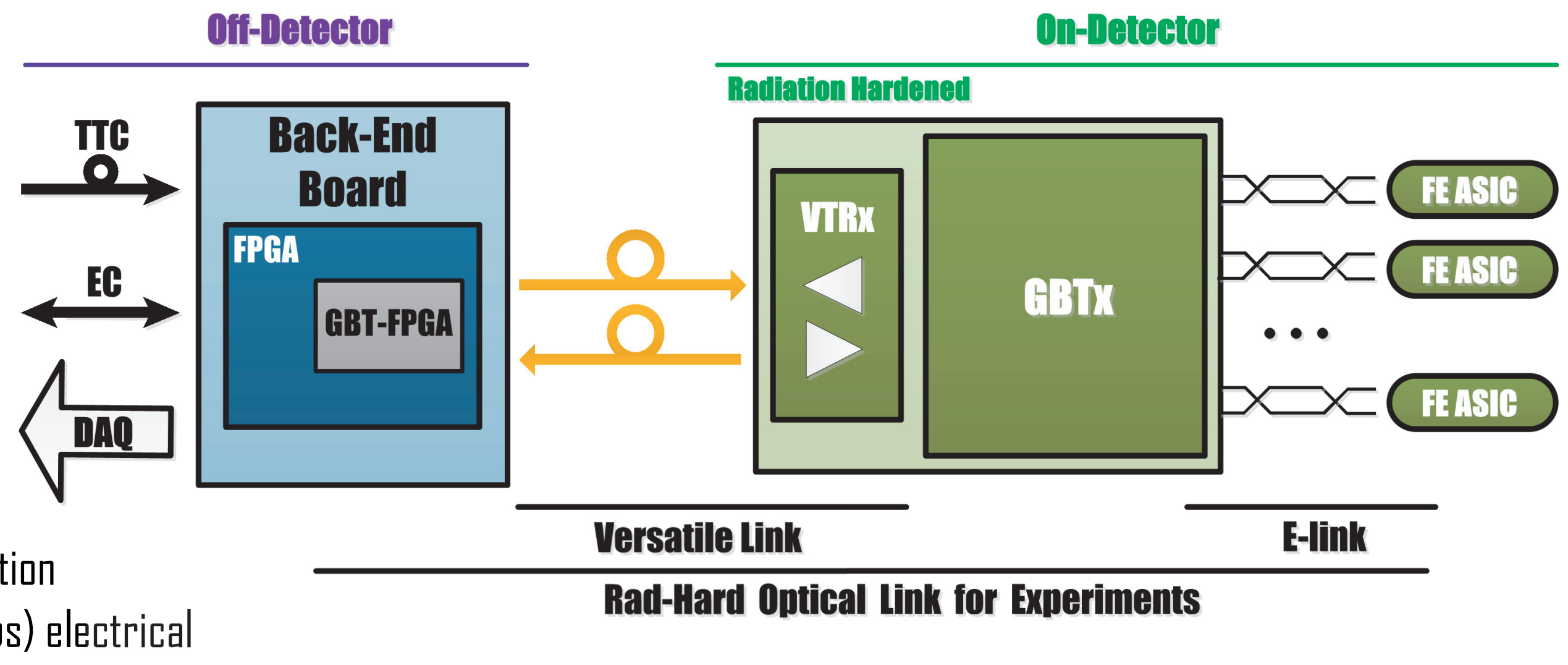
The GBT-FPGA project *(One unified core for multiple users)*



Following a study made in 2009 to implement the GBT SERDES in Stratix II and Virtex 5 FPGAs, a GBT-FPGA project was launched to provide GBTx users with a "GBT Starter kit" (a VHDL-based IP core) either to allow communication with the GBTx high-speed link from the counting room or to emulate part of the GBTx chip in an FPGA for test purpose. It will provide two types of implementation for the transmitter and the receiver ("Standard" and "Latency-Optimized") as well as the three available encoding schemes proposed by the GBTx serializer/desrializer ASIC ("GBT-Frame" (Reed-Solomon), "Wide-Bus" and "8b10b"). In addition, some example designs will be provided for the most common FPGA development kits.

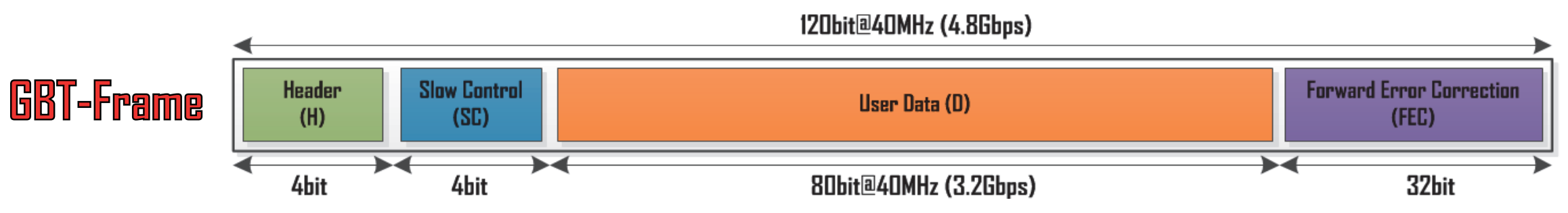
The Rad-Hard Optical Link for Experiments



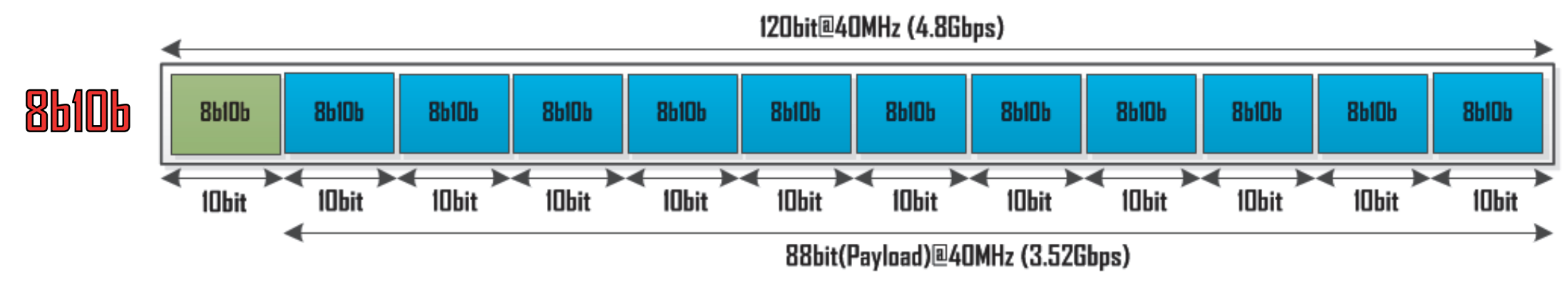
The diagram shown in this section of the poster, depicts a typical system featuring the "Rad-Hard Optical Link for Experiments", highlighting its major components. On the off-detector side, a Back-End (BE) FPGA-based board loading the GBT-FPGA firmware acts as the single-connection point with the detector, transmitting Timing, Triger and Control (TTC) and Experiment Control (EC) data to the Front-End (FE) as well as receiving and forwarding detector data to the central data acquisition (DAQ). On the on-detector side, the GBTx serializer/deserializer (SERDES) ASIC forwards the TTC information to FE ASICs and reads them out through low-speed (80, 160 or 320 Mbps) electrical links named E-links. The physical link between the BE and the GBTx ASIC is known as the "Versatile Link" (VL), a high-speed (4.8 Gbps) optical link which its major component is a custom plug-in module performing optical-to-electrical conversion (and vice versa) named the Versatile Link transceiver (VTRx). It is important to mention that only custom parts are used on-detector since they have to cope with extremely high radiation levels.

Data frame & Encodings

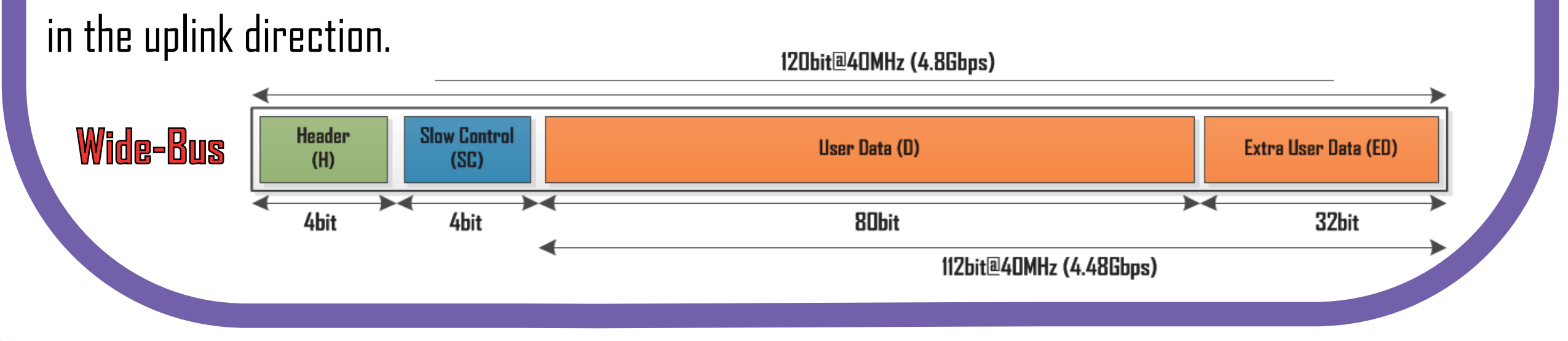
The GBT-FPGA supports the three available encoding schemes proposed by the GBTx:
The "GBT-Frame" adopts the Reed-Solomon that can correct bursts of bit errors caused by Single Event Upsets (SEU). This encoding scheme can be used for Data Acquisition (DAQ), Timing Trigger & Control (TTC) and Experiment Control (EC).



The "8b10b" provides 4bit more than the GBT-Frame to be used by the user at the cost of no error correction and limited error detection capability. This encoding scheme can only be used for DAQ and EC in the uplink direction (Front-End to Back-End).

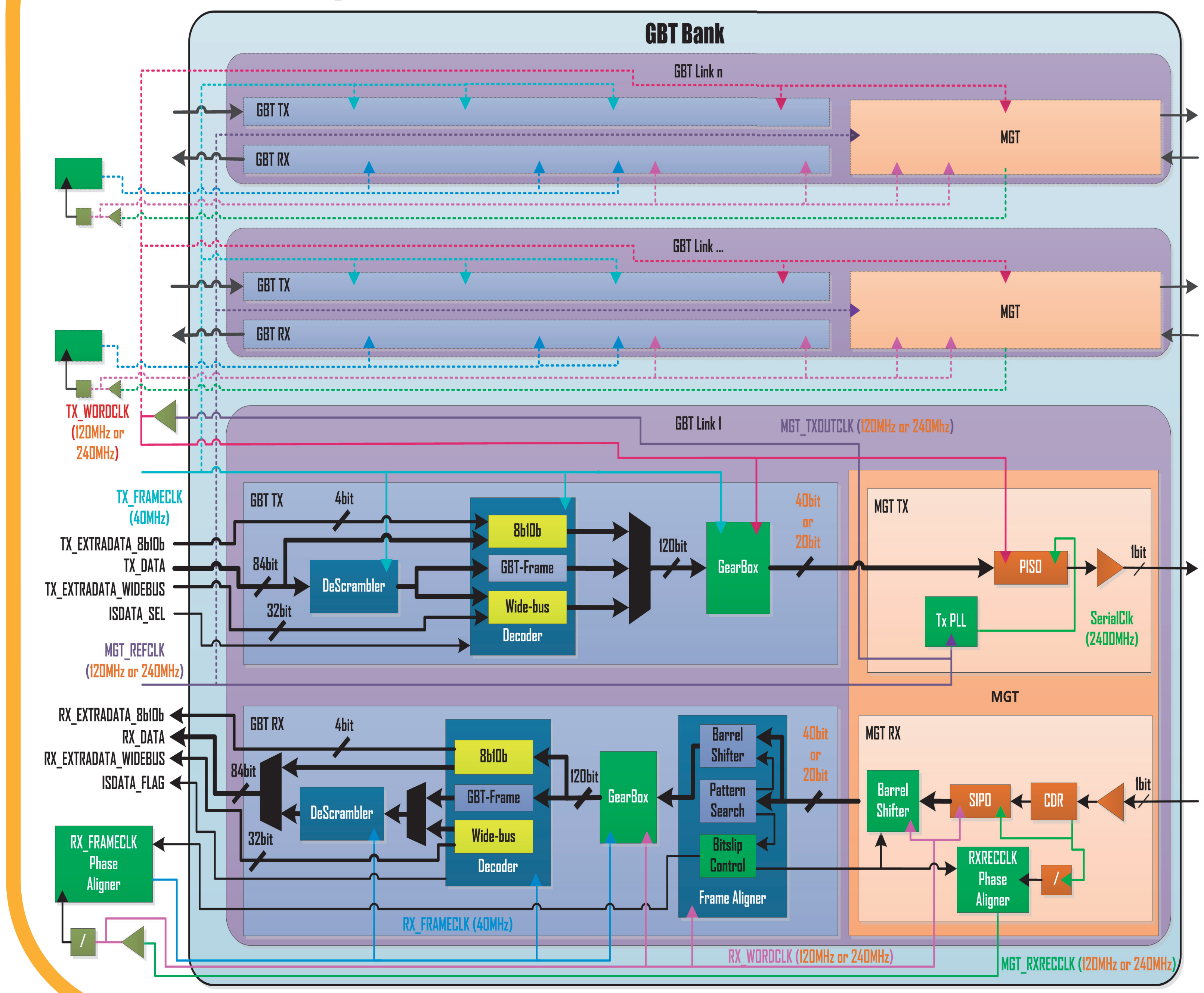


For the "Wide-Bus", the FEC field is fully replaced by user data at the cost of no error detection nor correction capability. This encoding scheme can only be used for DAQ and EC in the uplink direction.



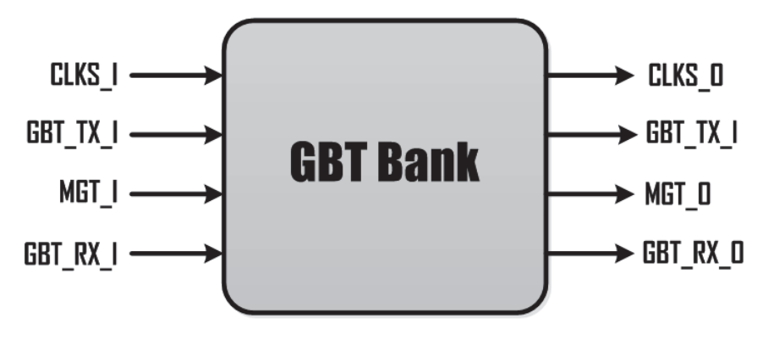
The GBT Bank

GBT Bank Diagram

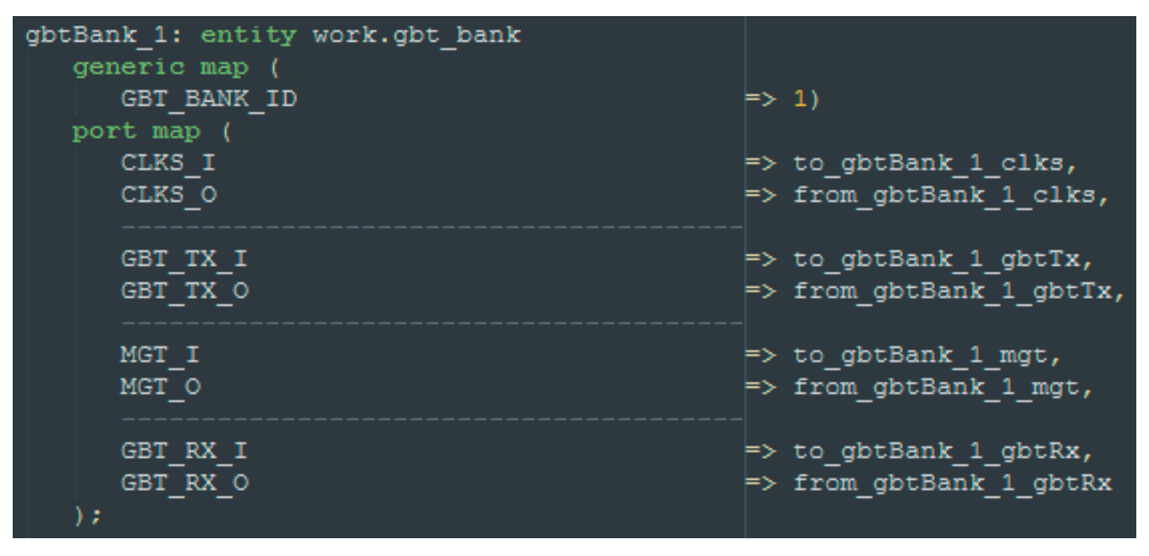


In order to facilitate the in-system implementation and the user support of the GBT-FPGA, the different components of the core are integrated in a single module called "GBT Bank". Most of these components are common for the different platforms. The GBT Bank may include up to four "GBT Links" (this number is vendor dependent). Each GBT Link is composed by a GBT TX, a GBT RX and a MultiGigabit Transceiver (MGT). The clocking resources are external to the GBT Bank so the user can connect the different clocks as desired. The number of GBT Links of the GBT Bank as well as the three encoding schemes proposed by the GBTx ASIC ("GBT-Frame" (Reed-Solomon), "Wide-Bus" and "8b10b") and the two types of optimization ("Standard" and "Latency-Optimized"), may be selected at implementation time through a single file (GBT User Configuration File).

GBT Bank Module



GBT Bank Instantiation (VHDL)



```
gbtBank_1: entity work.gbt_bank
   generic map (
      GBT_BANK_ID                               => 1)
   port map (
      CLKS_I                                    => to_gbtBank_1_clks,
      CLKS_O                                    => from_gbtBank_1_clks,
      ---------------------------------------
      GBT_TX_I                                  => to_gbtBank_1_gbtTx,
      GBT_TX_O                                  => from_gbtBank_1_gbtTx,
      ---------------------------------------
      MGT_I                                     => to_gbtBank_1_mgt,
      MGT_O                                     => from_gbtBank_1_mgt,
      ---------------------------------------
      GBT_RX_I                                  => to_gbtBank_1_gbtRx,
      GBT_RX_O                                  => from_gbtBank_1_gbtRx
   );
```

The Context

- **Multiple Roles:**
  - Back-End connection point with GBTx
  - GBTx emulation
  - Versatile Link fanout
  - Etc.
- **Multiple Categories of Users:**
  - Experiments
  - Accelerators

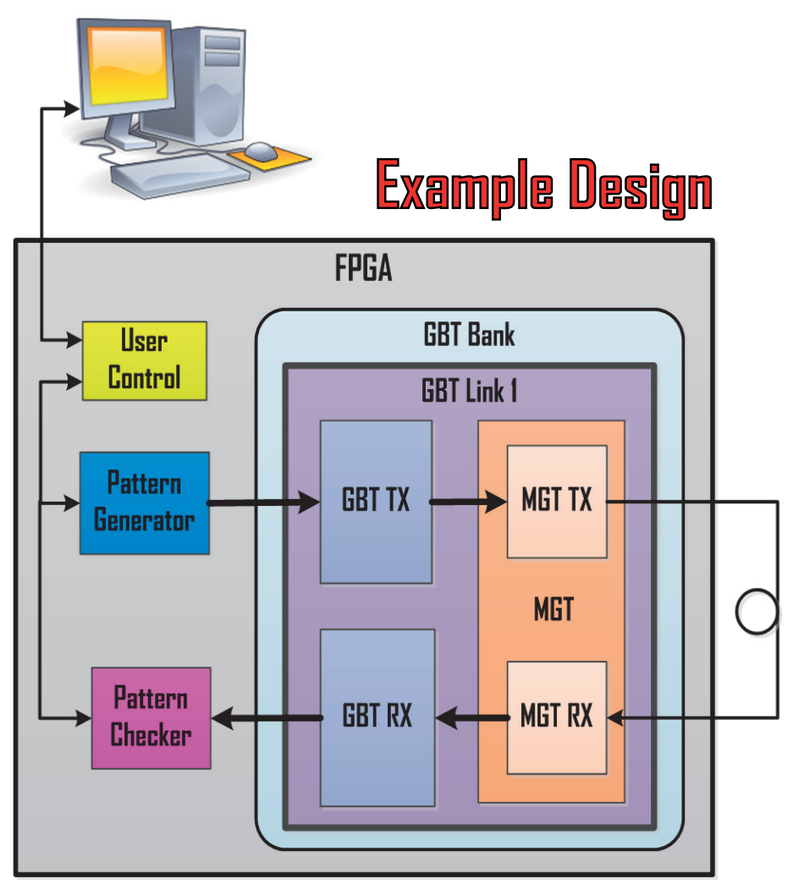
LHC (Beams Instrumentation)

- **Multiple Platforms:**
  - Xilinx
    Virtex 5, Virtex 6, Kintex 7, Virtex 7
  - Altera
    Stratix V, Cyclone V

Example Design

Besides the firmware of the GBT Bank, the GBT-FPGA project delivers example designs for some FPGA-based cards and the most common FPGA devkits. These example designs consist of a GBT Bank implementing one GBT Link. The TX is connected to a pattern generator whilst the RX is connected to a pattern checker. The GBT Link may be connected in loopbak but also to any other GBT compatible device. The control of the example design is done through a PC using HDL cores and software provided by the FPGA vendors (Xilinx's ChipScope and Altera's In-System Sources and Probes/SignalTap II).

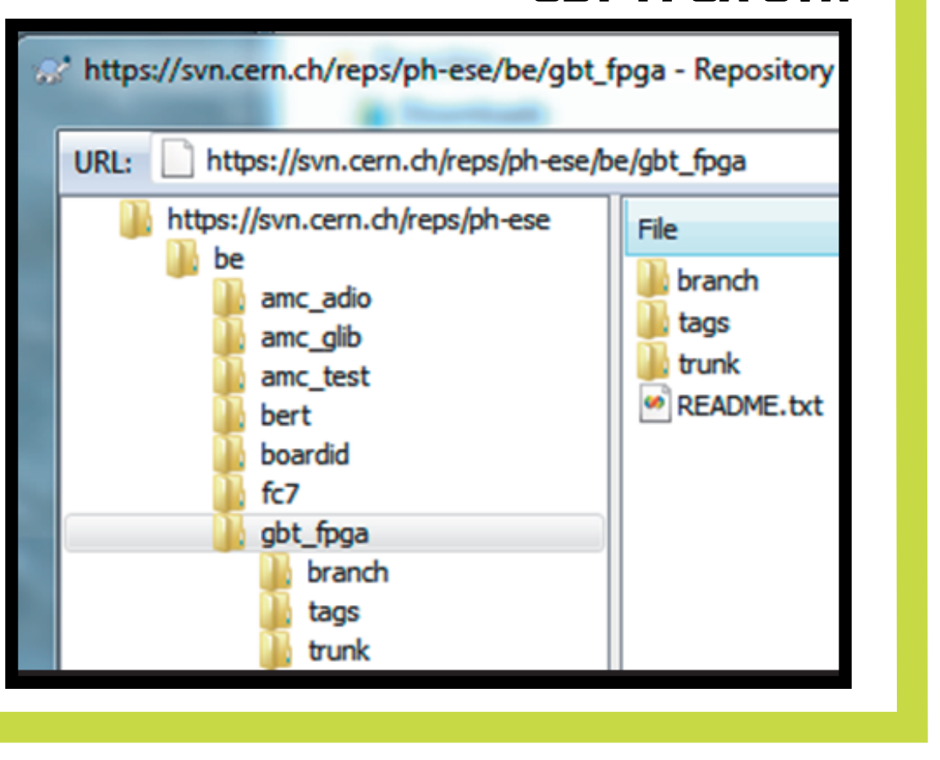
Example Design



SVN repository

The source files, documentation and TCL scripts of the GBT-FPGA project are available on a CERN subversion (SVN) repository and supported by the members of the GBT-FPGA team. To access the SVN repository, the user may use any of the numerous open source SVN clients (e.g. TortoiseSVN).

GBT-FPGA SVN


https://svn.cern.ch/reps/ph-ese/be/gbt_fpga - Repository
URL: https://svn.cern.ch/reps/ph-ese/be/gbt_fpga
https://svn.cern.ch/reps/ph-ese
be
amc_adio
amc_glib
amc_test
bert
boardid
fc7
gbt_fpga
branch
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trunk
File
branch
tags
trunk
README.txt

Standard vs Latency-Optimized

Trigger related electronic systems in High Energy Physics (HEP) experiments, such as Timing Trigger and Control (TTC), require a fixed, low and deterministic latency in the transmission of the clock and data to ensure correct event building. On the other hand, other electronic systems that are not time critical, such as Data Acquisition (DAQ), do not need to comply with this requirement. The GBT-FPGA project provides two types of implementation for the transmitter and the receiver: the "Standard" version, targeted for non-time critical applications and the "Latency-Optimized" version, ensuring a fixed, low and deterministic latency of the clock and data (at the cost of a more complex implementation). With the purpose of providing a graphical comparison of both architectures, the different components that are optimized on the Latency-Optimized version, in order to achieve a fixed, low and deterministic latency are highlighted in green colour in the figure labelled "GBT Bank Diagram".

	Standard	Latency-Optimized
Latency	Non Fixed, Higher & Non Deterministic	Fixed, Low & Deterministic
Logic Resources Utilization	Low	Low
Clocking Resources Utilization	Low	High
Clock Domain Crossing	Don't Care	Critical
Implementation	Simpler	Complex

Status

- **GBT-FPGA Development kit Includes:**
  - HDL Sources
  - Example Designs
  - Documentation
  - TCL Scrips

First Release: 11/04/2014

- **Available for:**
  - Xilinx Virtex 6 (GLIB, ML605)
  - Xilinx Kintex 7 (FC7, KC705)
  - Xilinx Virtex 7 (VC707)
  - Altera Cyclone V (SAT, Cyclone V GT Devkit)
  - Altera Stratix V (AMC40)
- **Encodings & Optimizations:**
  - Encodings: GBT-Frame, Wide-Bus
  - Optimizations: Standard, Latency-Optimized
- **To do:**
  - Finalize 8b10b encoding scheme
  - Implement New Versions (Artix 7?, Microsemi?, etc.)
  - Different studies (Latency measurements, etc.)

The GBT-FPGA team: S. Baron (Sophie.Baron@cern.ch) and M. Barros Marin (manoel.barros.marin@cern.ch)

Web site: https://espace.cern.ch/GBT-Project/GBT-FPGA/default.aspx
SVN repository: https://svn.cern.ch/reps/ph-ese/be/gbt_fpga

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