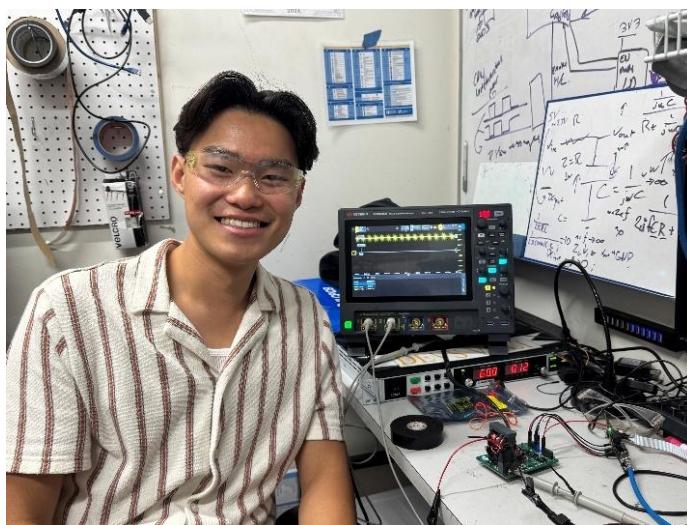
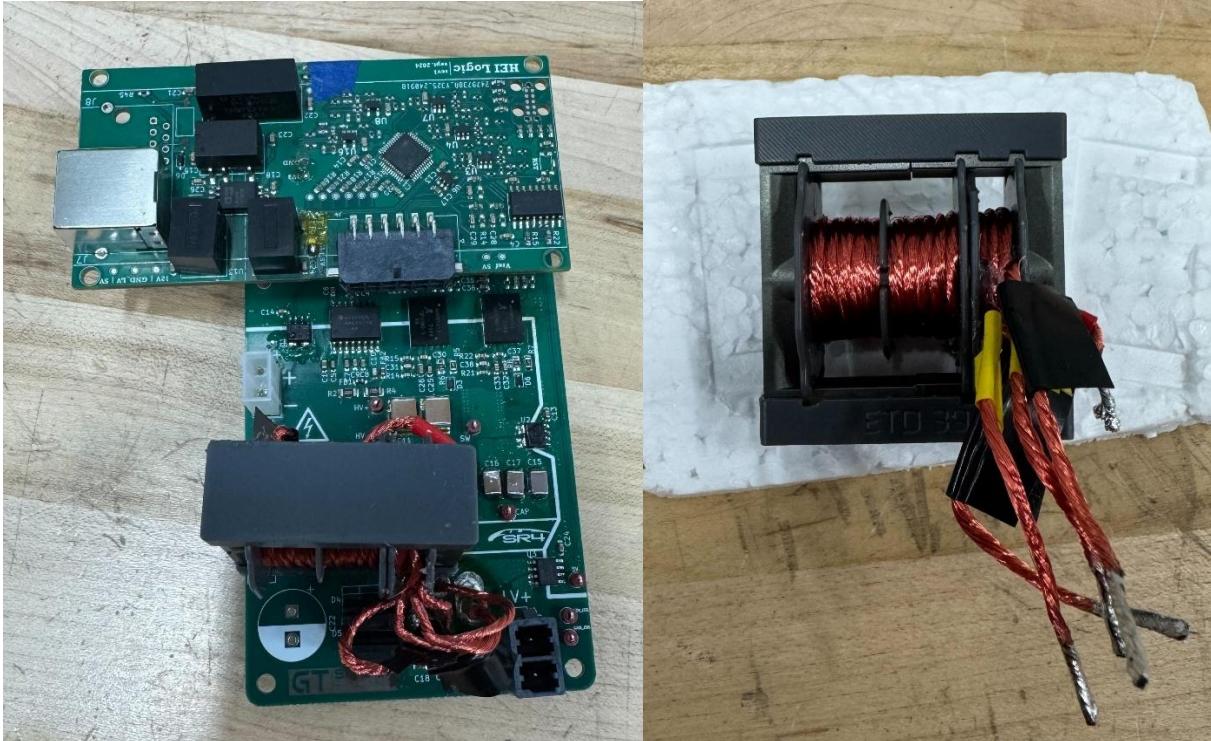


DC/DC LLC Resonant Converter

Documentation for Georgia Tech Solar Racing



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1 Introduction

Georgia Tech Solar Racing (GTSR) is a student-run organization that designs, builds, and races solar-powered vehicles. The team participates in the Formula Sun Grand Prix and American Solar Challenge. Within this organization, the Electrical Team is responsible for the design of the Auxiliary, Battery, Drivetrain, Solar, and Telemetry systems of the Solar Car, among other things. A DC/DC converter is required to supply the low-voltage components in the electrical system from a high-voltage battery source. This documentation is dedicated to a in-house DC/DC converter utilizing a LLC Resonant Converter topology.

Although there is no requirement from event rules to utilize a custom-made converter, the author believes that the skills obtained from the design process have immense value towards the development of an engineer and their power electronics expertise. In addition, the experience gained from this project assisted in the development of other in-house power electronic products in the team (namely the Motor Controller and MPPT).

2 Version History

2.1 Revision 0 (2024 – 2025)

The research for a new custom-made DC/DC converter was started in late 2024. One of the most important requirements is for the converter to have isolation. Multiple topologies were explored, such as a flyback, push-pull, and forward converter, but an LLC Resonant topology was finally developed.

This topology offers various advantages:

1. It requires few components. Additionally, the leakage inductance of the transformer can be used as the resonant inductance, removing the need for a separate inductor.
2. The input voltage has a wide range as parameters can be changed to realize a larger/smaller gain produced by the resonant tank.
3. High efficiency is achieved due to Zero Voltage Switching (ZVS) on the primary FETs and Zero Current Switching (ZCS) on the secondary rectification.

Revision 0 is mostly a “proof-of-concept” project, intended to demonstrate the feasibility of a custom-made DC/DC converter. The target power of 100W and ~94% peak efficiency was achieved. In addition, GaN FETs were used over traditional MOSFETs to achieve switching frequencies over 500 kHz. However, this goal was not met due to other design parameters.

2.2 Revision 1 (2025 - Present)

The next revision of the board is intended to be extensively tested, reliable, and ready to be utilized in our Solar Car. The author plans to implement numerous improvements:

1. Active rectification on the secondary side (Revision 0 utilizes Schottky diodes for passive rectification). The NCP4305 is a likely candidate to drive the synchronous rectification FETs.
2. Utilize a split capacitor topology instead of a single resonant capacitor to reduce voltage ripple on the DC link.
3. Addition of EMI filters to the input and output; pi filters at the input and output.
4. Precharge input and output capacitors using soft start controls.
5. Obtain switching frequencies greater than 500 kHz.
6. Design a more compact PCB layout to reduce parasitic inductances and capacitance.

3 Overview

3.1 Soft Switching

In conventional flyback or push-pull converter, the FETs are commutating with hard switching behavior. This means that the FETs turn on while their C_{DS} are still charged to the blocking voltage and turn off while the entire load current is still flowing through them. In hard switching, the FETs are exposed to high switching stresses and incur larger switching losses. Figure 1 shows the switching events of a switch as it turns off and on. For example, let us analyze the turn off switching event. Initially, a current I_o flows through the switch. When a turn off signal is applied, the voltage across the switch rises to V_d while current decreases to 0. As shown, the two waveforms overlap each other, resulting in a triangle that represents the power lost in that switching event.

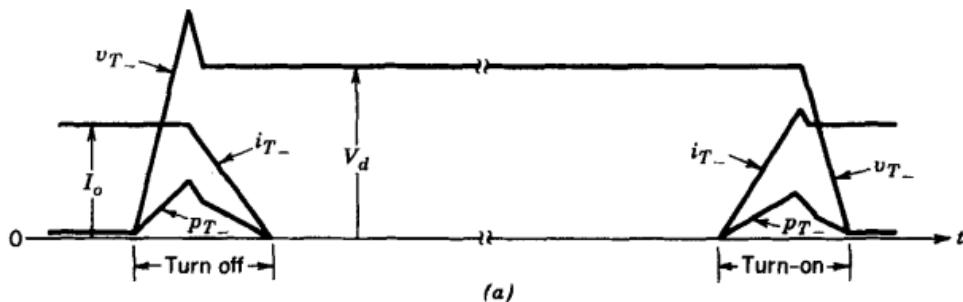


Fig. 1: Voltage and Current Waveforms for a Switch During Turn On and Turn Off Events.

Mohan, N., Undeland, T. M., & Robbins, W. P. (2012). Power Electronics: Converters, Applications, and Design. John Wiley & Sons. Page 250, Figure 9-2(a).

In the last decade, progress in power electronics has pushed converters to be more powerful and smaller. Now, engineers are designing for ever higher switching frequencies to meet these requirements. This amplifies the shortcomings of hard switching as switching loss increases linearly with switching frequency (due to more switching events per second). Therefore, to minimize switching loss at higher frequencies, the switch in a converter should turn on or off while the voltage across it or the current through it is zero.

3.2 LLC Resonant Topology

Resonant converters are popular topologies used to achieve ZVS and ZCS. At the core of the LLC converter is the resonant tank, consisting of a resonant capacitor (C_r), resonant inductor (L_r), and magnetizing inductor (L_m). Before the resonant tank, a switching bridge (half or full bridge) generates a square wave to excite the resonant tank. As the resonant tank is alternatively switched between the supply voltage and ground (or the negative of supply voltage), the resonant capacitor is charged and discharged. The alternating current produced is used to transfer energy from the primary to the secondary side with the help of the transformer. Finally, a rectification stage and output capacitors are used to rectify the sinusoid to a DC voltage on the output of the transformer.

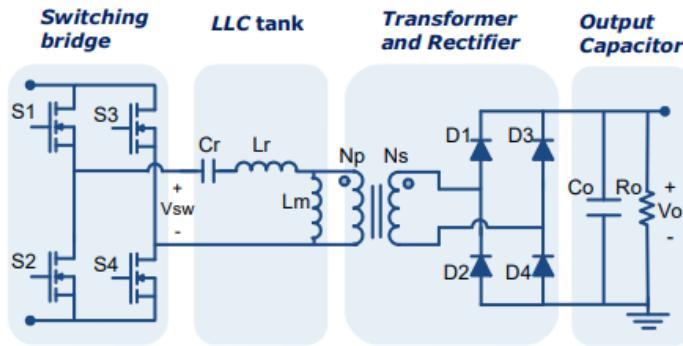


Fig. 2: Full-Bridge LLC Converter with Full-Bridge Rectifier. [Infineon Design Note](#), Page 4,

3.2.1 Voltage Gain

By utilizing the resonant tank, a specific gain can be produced to either boost or buck the voltage. Additionally, the transformer winding ratio can apply another gain to the voltage level. Figure 3 shows a graph between gain and normalized switching frequency. As the switching frequency is increased, the gain decreases, and vice versa. At the resonant frequency (labeled F_x), the gain of the tank is 1. The switching bridge also has a gain, where it is 1 for a full-bridge and 0.5 for a half-bridge. The overall converter gain is:

$$(1) \quad V_{OUT} = V_{IN} * G_{BRIDGE} * G_{TANK} * \frac{N_{SEC}}{N_{PRIM}}$$

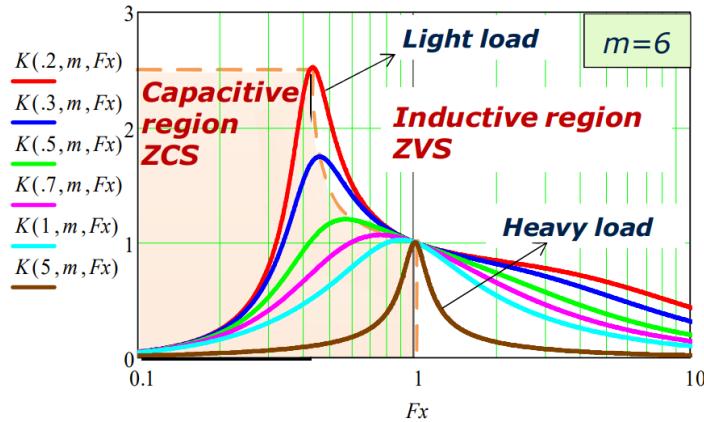


Fig. 3: Gain vs Normalized Switching Frequency, [Infineon Design Note](#), Page 6

3.2.2 Operation

In LLC converters, the half-bridge is usually operated at a frequency that maintains inductive operation. Figure 3 shows that the gain curves have peaks which bound the capacitive and inductive regions. This means that the currents across the power switches (FETs) lag the voltage. Therefore, the switches start their conduction period with a negative current and end with a positive current. It is desired to operate in the inductive region across the input voltage and load ranges to achieve ZVS in the input half bridge, reducing switching losses.

Another factor that must be considered is the dead time needed. The dead time is the time between when one switch is turned off and the next is turned on in the half-bridge, which ensures both cannot conduct simultaneously. While dead time is conventionally used to prevent shoot-through, it is also utilized here to ensure that there is enough time for the output capacitance of the switches to be discharged and achieve ZVS. Hence, the dead time must be sufficient to cover turn-off of the switches and resonant transition time. Figure 4 explains the simplified current paths during a switching cycle and dead time regions.

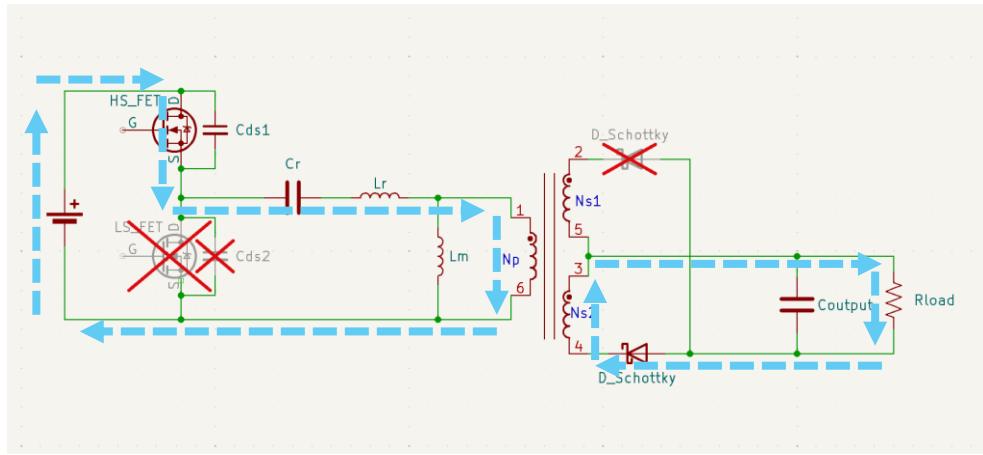


Fig. 4(a): Positive Voltage Power Delivery

First, the resonant tank is excited with a positive by turning on the high side switch and turning off the low side switch, so the current resonates in the positive direction. Then, the high side switch turns off while its current is still positive. Assuming the switch can be turned off quickly enough, the output capacitance holds the voltage across the high side switch low during turn off, providing ZVS turn off.

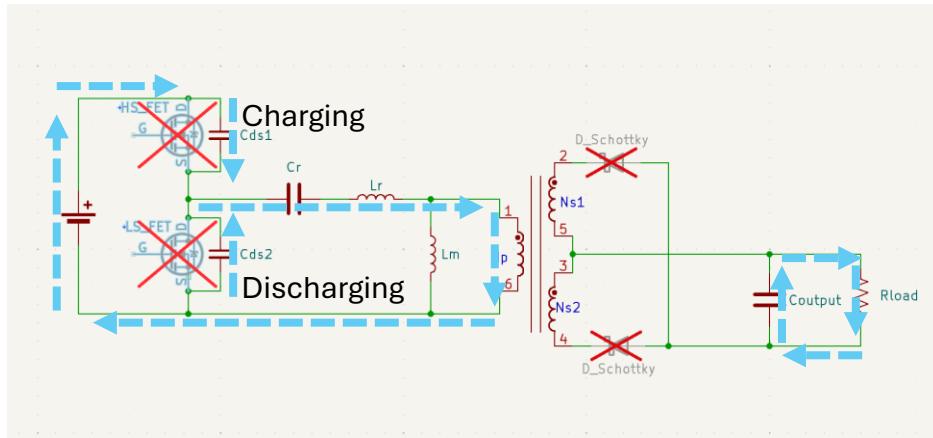


Fig. 4(b): Dead Time after Positive Voltage Power Delivery

Next, both switches are turned off, which happens during the dead time. Because the resonant current is still positive, it charges the output capacitance of the high side switch while discharging the output capacitance of the low side switch. Once the voltage across the low side switch decays to zero, its body diode starts conducting and clamps the voltage of its output capacitance. The low side switch can now be turned on with ZVS.

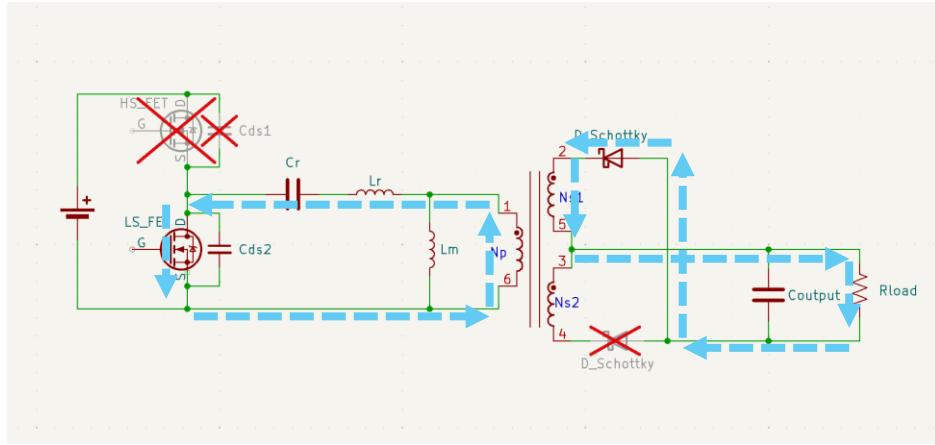


Fig. 4(c): Negative Voltage Power Delivery

The resonant tank is excited with negative (or zero) voltage in this switching phase. The resonant current is negative and flows through the low side switch. The switch continues to conduct the negative resonant current as it turns off. Similar to the positive power phase, the switch can achieve turn off ZVS if its turn off time is small enough.

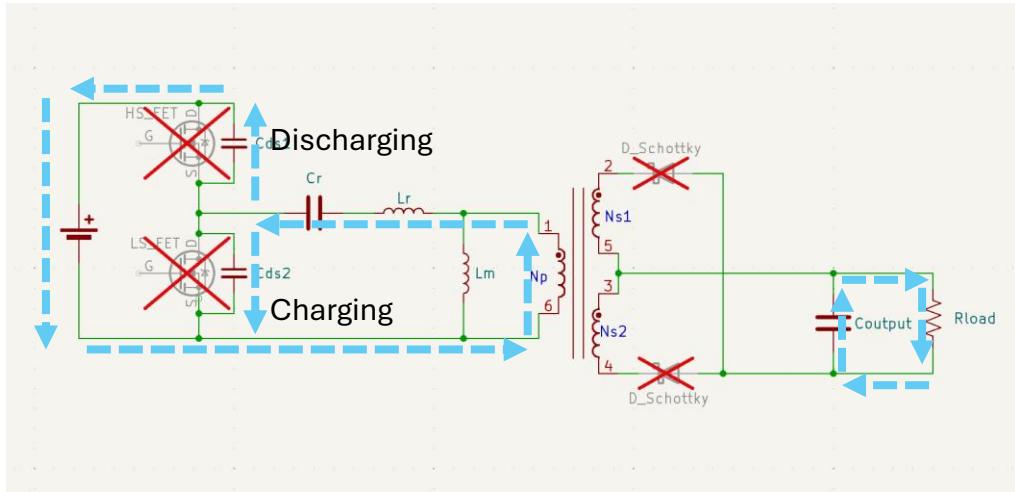


Fig. 4(d): Dead Time after Negative Voltage Power Delivery

As the resonant current is negative, the output capacitance across the high side switch is discharged while the low side output capacitance is charged. This happens until the high side body diode turns on, allowing the high side switch to be turned on with ZVS. Finally, the positive voltage power delivery phase can start again.

4 Converter Design

4.1 Requirements

Output Voltage	12V
Input Voltage	45V – 75.6V
Nominal Input Voltage	~120V
Output Power	100W
Resonant Frequency	100 kHz

4.2 Resonant Tank

Online resources such a [calculator excel spreadsheet](#) from Onsemi for the NCP4390 LLC controller was used to design the resonant and transformer parameters of this Converter.

The resonant tank gain can be found using equation 2.

$$(2) K(Q, m, F_x) = \frac{F_x^2(m - 1)}{\sqrt{(m * F_x^2 - 1)^2 + F_x^2 * (F_x^2 - 1)^2 * (m - 1)^2 * Q^2}}$$

Where,

$$(3) Q = \frac{\sqrt{L_r}}{R_{ac}} \quad \text{Quality Factor}$$

$$(4) R_{ac} = \frac{8 * R_o * N_p^2}{\pi^2 * N_s^2} \quad \text{Reflected Load Resistance}$$

$$(5) F_x = \frac{f_s}{f_r} \quad \text{Normalized Switching Frequency}$$

$$(6) f_r = \frac{1}{2 * \pi * \sqrt{L_r * C_r}} \quad \text{Resonant Frequency}$$

$$(7) m = \frac{L_r + L_m}{L_r} \quad \text{Ratio of Primary Inductance to Resonant Inductance}$$

Equations 2 – 7 are taken from this [Infineon Design Note](#), Page 6.

The Quality Factor depends on the load of converter. Outputting a larger power output corresponds to high Q values, while lighter power output has lower Q values. Figure 5 shows the effect of the Q value on the gain curve. A lower Q value allows the tank to reach a larger gain while a high Q value limits the possible gain.

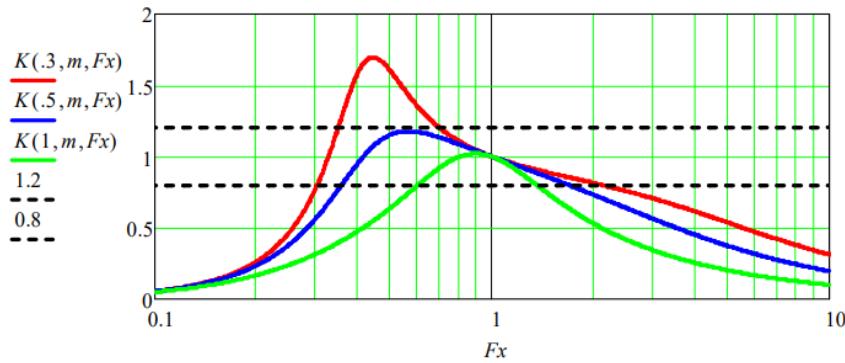


Fig. 5: Gain vs Normalized Switching Frequency, [Infineon Design Note](#), Page 9

The m value is a parameter that solely depends on the design of the transformer. A separate inductor can be added to increase the value of the resonant inductance, however only the leakage inductance of the transformer was used to supply the resonant inductance in this design. Similar to the Q value, the m value affects the possible gain met by the resonant tank. A lower m value increases the possible gain, and a larger m value decreases the possible gain. A lower m value is very beneficial if the converter covers a large input voltage range. In addition, the value of the magnetizing inductance L_m controls the magnetizing current. A smaller magnetizing inductance value results in larger magnetizing current, causing increased circulating energy and power loss. Figure 6 illustrates this behavior.

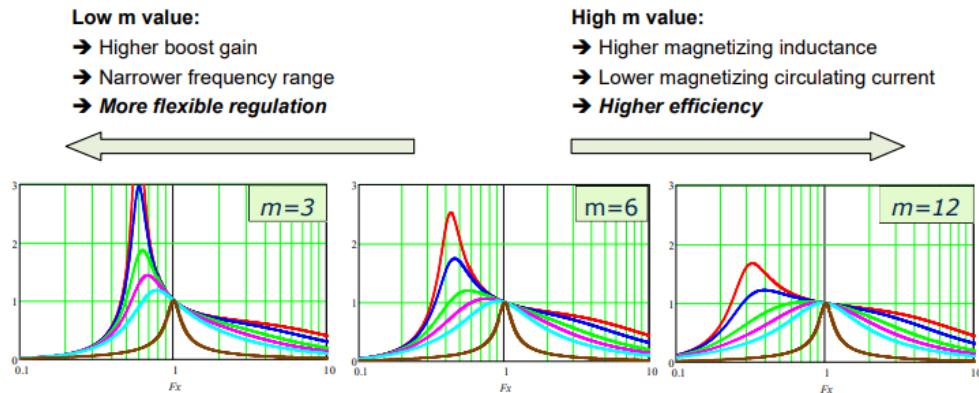


Fig. 6: Gain vs Normalized Switching Frequency, [Infineon Design Note](#), Page 9

Lastly, the magnetizing and leakage inductance values depend greatly on the transformer design. Often times, it is beneficial to add an “air gap” in the transformer core to prevent saturation. Introducing an air gap, however, will decrease the magnetizing inductance. The design and number of the transformer windings will also affect the leakage inductance. These parameters will be discussed in the Transformer Design section.

Using Equation 1, the target minimum and maximum gain of the resonant tank can be calculated. Here, a half bridge is utilized (gain of 0.5) and the transformer has 10 primary windings and 4 secondary windings.

$$V_{OUT} = 75.6 * 0.5 * G_{TANK_min} * \frac{4}{10} = 12V$$

$$G_{TANK_min} = 0.794$$

$$V_{OUT} = 45 * 0.5 * G_{TANK_max} * \frac{4}{10} = 12V$$

$$G_{TANK_max} = 1.33$$

4.3 Input Switching Bridge

The first stage of the converter is a bridge circuit that excites the resonant tank with a square waveform. This can be accomplished by either using a full bridge or half bridge. A half bridge would have twice the rms current of a full bridge, but half the number of switches. In total, the total conduction losses in a half bridge are double the losses in a full bridge. In addition, a half bridge has a voltage gain of 0.5 while a full bridge has a unity gain. For Revision 0 of this converter, a half bridge was selected to simplify the firmware needed to control the converter. A full bridge will most likely be used for the next revision.

Parameters of Half Bridge Compared to Full Bridge				
I _{RMS}	I _{RMS} ²	Number of Switches	Total Conduction Loss	Gain
× 2	× 4	÷ 2	× 2	÷ 2

One of the main goals of this project is to realize a compact and power dense converter. GaN FETs were then chosen to achieve the high switching frequencies needed. However, difficulties in the transformer design (discussed in the transformer section), limited the resonant switching frequency to 100 kHz. The next revision of the converter aims to increase that number to 500 kHz.

Although the benefits of high switching frequency from the GaN FETs were not fully realized, the lower R_{DS(on)} and output capacitance (C_{oss}) values are still advantageous to the design. The LLC operates close to the resonant tank frequency at nominal conditions, which causes the conduction losses to dominate the switching losses (due to ZVS). On the other hand, a smaller C_{oss} means that less dead time is needed to fully discharge the capacitance to achieve ZVS. The EPC2304 was chosen due to these parameters:

R_{DS(on)} = 3.5 mΩ

[Datasheet link](#)

C_{oss} = 704 pF

4.4 Gate Driver

The [AHV85111](#) is an isolated gate driver specially designed to drive GaN FETs with a source/sink current of 2A/4A. The driver has an integrated positive/negative output bias supply, allowing it to drive a floating switch. The main feature of this gate driver is its rated ability to switch up to 1 MHz. There is no adjustable dead time on the gate driver, so that is taken care of by the Microcontroller and firmware.

4.5 Secondary Rectification

A rectification scheme is needed in the secondary side to rectify the sinusoid output of the transformer. LLC converters can be implemented with either a full bridge or full wave (using a center tapped transformer) rectifier. A full wave rectifier only has 2 diodes (compared to 4 in a full bridge), but they require twice the voltage rating. Since the average current flowing through each diode is equivalent in both configurations, the full wave rectifier has half the total conduction losses. However, the number of secondary windings is doubled in a full wave rectifier.

In most low voltage applications (12V output in this case), a full wave rectifier is preferred because the higher voltage rating is not a difficult issue to design around.

Parameters of Full Wave Compared to Full Bridge				
Voltage Rating	Number of diodes	Diode Conduction Loss	No. of Secondary Windings	Transformer Conduction Loss
× 2	÷ 2	÷ 2	× 2	× 2

In Revision 0, Schottky diodes ([STPS1545FP](#)) were used to build the rectification stage. This was done to simplify the firmware required to control the converter. For the next revision, active rectification will be used instead to decrease conduction losses. For example:

$$P_{\text{diode_loss}} = I * V_{\text{fw}} = 2A * 0.5V = 1W$$

$$P_{\text{sw_loss}} = I^2 * R_{\text{DS(on)}} = (2A)^2 * 10 \text{ m}\Omega = 40 \text{ mW}$$

The current plan is to utilize the [NCP4305](#) chip to drive the rectification MOSFETs. The chip measures the drain to source voltage of the FETs and switches them on when the voltage falls below a threshold (-75 mV). Effectively, this allows the FETs to function like diodes.

4.6 Resonant Capacitor

The resonant capacitor is chosen with careful consideration to the high frequencies it is exposed to. For example, a film capacitor's voltage and current ratings significantly decrease as the switching frequency increases. This means that if we are to achieve

switching frequencies in the hundreds of kHz range, the capacitors must be specified for a much greater value than at lower switching frequencies.

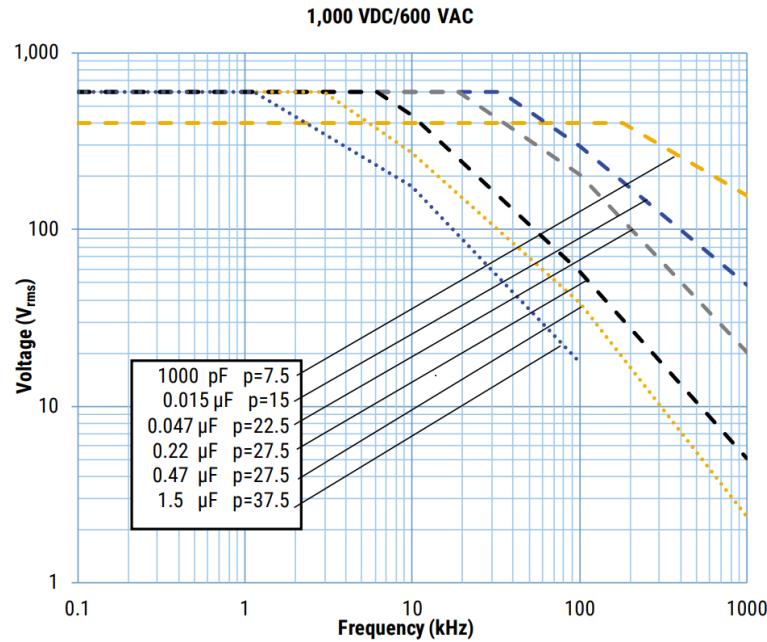


Fig. 7: Voltage Derating Curves of a Film Capacitor, [KEMET](#)

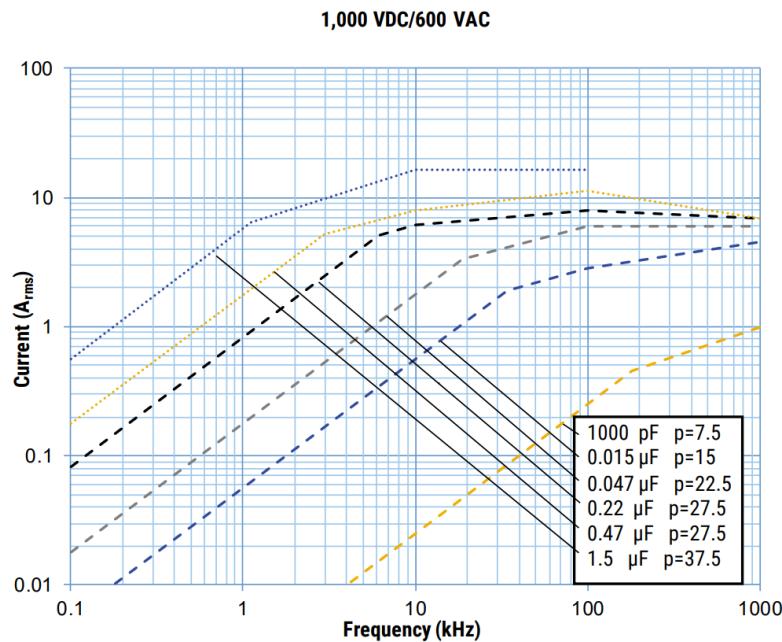


Fig. 8: Current Derating Curves of a Film Capacitor, [KEMET](#)

Next, ceramic capacitors were considered due to their compact packaging. However, the conventional X5R and X7R Multilayer Ceramic Capacitor also suffered from capacitance derating. Their capacitance decreases significantly as frequency increases.

Ceramic capacitors with a C0G or PN0 dielectric were finally chosen as they have the most stable properties. The downside of these capacitors is that they usually come in larger packaging compared to the X5R/X7R capacitors. In Revision 0, 300 nF of resonant capacitance is needed to reach a suitable quality factor and resonant frequency. The smallest packaging the author could find for 100 nF capacitors was 1812. Hence, 3 of these capacitors are connected in parallel. The larger 1812 footprint is not ideal because it increases the equivalent series inductance (ESL) and equivalent series resistance (ESR).

For the next revision, a smaller resonant capacitance is designed for by decreasing the resonant inductance (leakage inductance of the transformer).

4.7 High Frequency Transformer Design

A simple transformer consists of coils (windings) and a material between the coils. The number of coils can vary (2 windings in this converter) and many options are also available for the core material, even air can be used as a medium (inductive charging in cell phones).

4.7.1 Core Material

Each material has a characteristic magnetic conductivity (permeability). The relative permeability (μ_r) of air is around 1 while the μ_r of a ferrite core can be in the thousands range depending on the material. In addition, different materials have different magnetic field saturation values (B_s). When a magnetic material reaches saturation, further increases in external magnetic field no longer increase its magnetization. In other words, increasing the magnetic field intensity H no longer increases the flux density B , as shown in Figure 9.

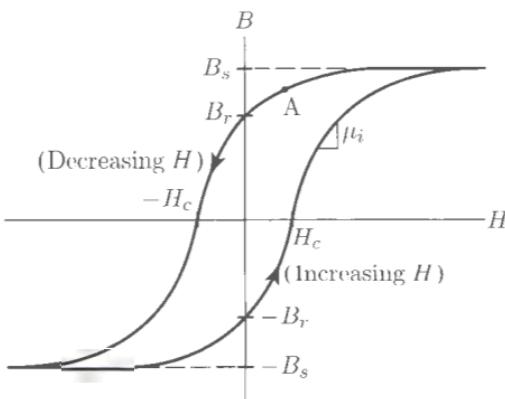


Fig. 9: Typical B-H Curve for Magnetic Material. Kassakian, J. G., Perreault, D. J., Verghese, G. C., & Schlecht, M. F. (2024). Principles of Power Electronics. Cambridge University Press.

Generally, it is desirable to stay below the B_s value. A B_s of 0.2 – 0.3 Tesla can be expected in ferrite cores while transformer sheets have a value around 1.2 – 1.8 Tesla. However, the magnetic poles in transformer sheets can only be magnetized slowly, causing it to generate heat and power loss at high frequencies. Ferrites, on the other, can be used up to the MHz range. Ferrites will also incur core losses at higher frequencies (shown in figure 10), but at lower values.

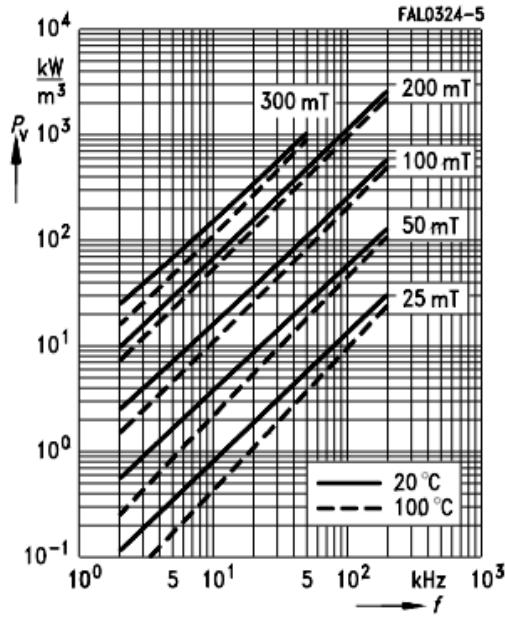


Fig. 10: Relative core losses against frequency, [N27 material datasheet from TDK page 5](#)

Three ferrite core materials from TDK were explored: N27, N87. And N97. The N27 material is recommended for applications between 25 – 150 kHz, so this material was chosen.

Optimum frequency range	f_{\min} f_{\max}	kHz kHz	25 150
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Fig. 11: [Datasheet](#) for TDK N27 material

4.7.2 Core Shape

The core shape was chosen to prioritize a small footprint size and ease of winding. The ETD and PQ form factors from TDK were explored, but the ETD was finally chosen. The ETD has a middle leg that provides much space for the user to easily wind the coil by hand. The one downside of the current winding design is that the primary and secondary windings have a large distance between them, increasing the leakage inductance of the transformer.

The ETD39 N27 from TDK (mfr. no. [B66363G0000X127](#)) was finally chosen.



Fig. 12 Two Halves of the ETD39 Transformer

4.7.3 Primary Inductance L_{prim} and Air Gap

The primary inductance L_{prim} is obtained by measuring the inductance of the primary winding using an LCR meter while the secondary windings are left open. This test effectively measures the leakage inductance $L_{\text{leak}} + \text{magnetizing inductance } L_m$.

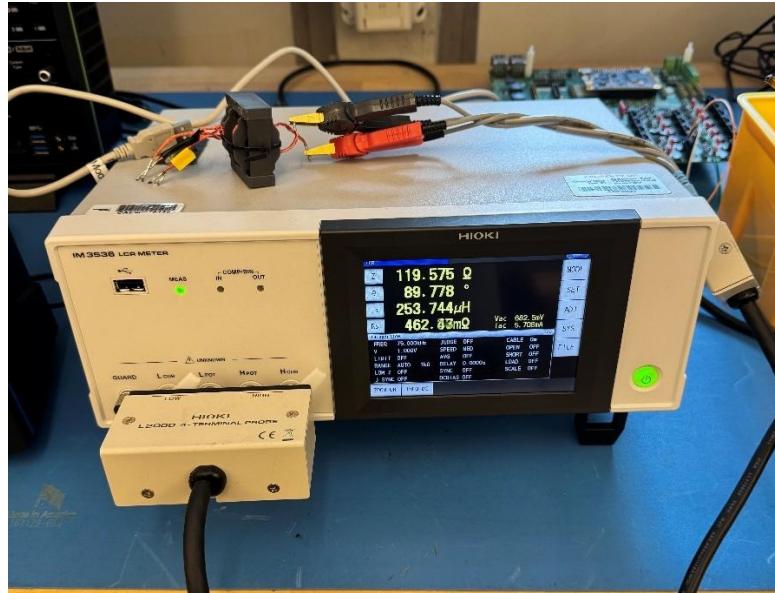


Fig. 13: Measuring Primary Inductance, Without Air Gap

The primary inductance value can also be estimated using

$$(8) L = A_L * N^2$$

A_L [nH] is an inductance constant provided by the core material datasheet.

Material	A_L value nH	μ_e	B_s mT	P_V W/set	Ordering code
N27	2550 +30/-20%	1500	320 ¹⁾	< 2.22 (200 mT, 25 kHz, 100 °C)	B66363G0000X127
N87	2700 +30/-20%	1600	320 ¹⁾	< 6.00 (200 mT, 100 kHz, 100 °C)	B66363G0000X187
N97	2800 +30/-20%	1650	320 ¹⁾	< 5.10 (200 mT, 100 kHz, 100 °C)	B66363G0000X197

1) $H = 250 \text{ A/m}$; $f = 10 \text{ kHz}$; $T = 100 \text{ }^{\circ}\text{C}$

Fig. 14: A_L Values for Different Materials, [TDK Datasheet](#), Page 2

With 10 primary windings, the theoretical primary inductance for N27 is:

$A_L * N^2 = 2550 * 10^2 = 255 \mu\text{H}$. The measured value from figure 11 is 253.74 μH , very much within tolerance.

Figure 14 also shows that maximum flux density B_s of N27 is 320 mT. The transformer should always operate below saturation to minimize core losses. An LTSpice simulation was used to complete the maximum flux density produced by the converter.

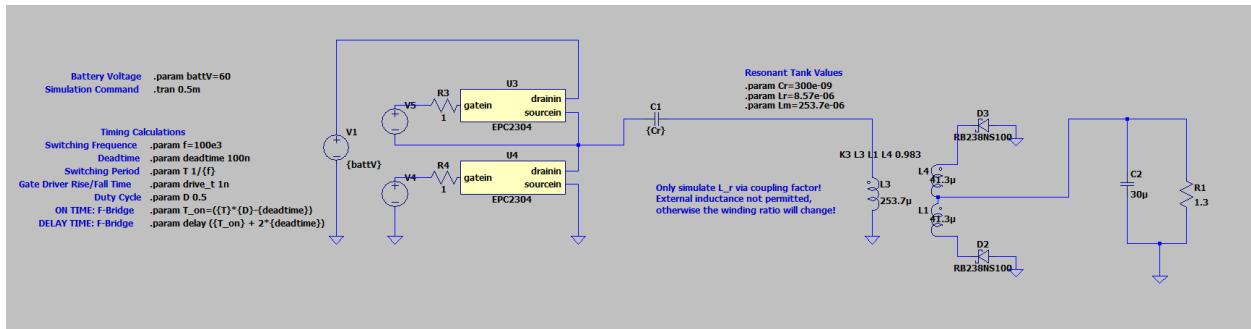


Fig. 15: LTSpice Simulation for LLC Converter

There are several ways to calculate flux density, one way is by derivation through the inductance of a coil.

$$L = \frac{N * \Phi}{I}$$

$$L = \frac{N * B * A}{I * \sqrt{2}}$$

$$(9) B = \frac{I * L * \sqrt{2}}{N * A}$$

From the simulation at high load (100W):

$$I = 3.73 A$$

$$L = 253.7 \mu H$$

$$N = 10 \text{ turns}$$

$$A = 125 \text{ mm}^2 \text{ (from ETD datasheet)}$$

Finally, $B = 1.07 \text{ Tesla}$

This value is above the maximum flux density of 0.32 Tesla. Another method for calculating the flux density through the core is to use the equation for magnetic field strength H .

$$(10) H = \frac{I * N}{\sqrt{l^2 + D^2}}$$

$$(11) B = H * \mu_r * \mu_0$$

To reduce the flux density from 1.07 Tesla to <0.32 Tesla, an air gap is often added to the transformer core. Air only has a conductance (μ_r) of 1 while N27 has a conductance of 1500. This means that the B field produced by the same H value is significantly less when the material is air instead of N27. In other words, an air gap increases the magnetic resistance of the transformer and allows greater field strengths before the core saturates. Graphically, the B-H graph is horizontally elongated to allow a larger H value before reaching B_s .

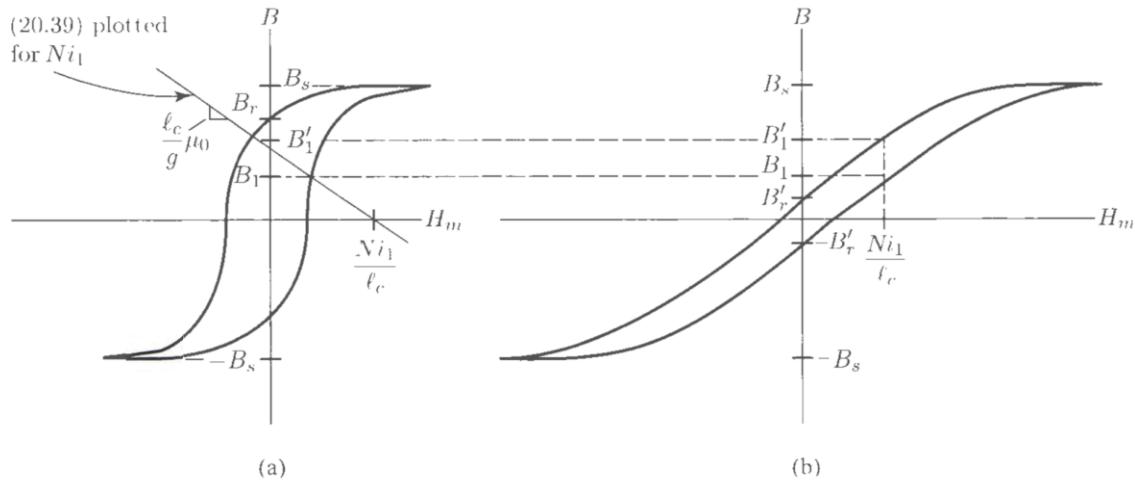


Fig. 16: B-H Graph for Ungapped and Gapped Core. Kassakian, J. G., Perreault, D. J., Verghese, G. C., & Schlecht, M. F. (2024). Principles of Power Electronics. Cambridge University Press.

By using equation (9), the value of inductance L can be calculated when B = 0.32 Tesla. The primary inductance should be less than 75.83 uH. To calculate the air gap needed, equation (12) is given from the [E cores: General Information](#) datasheet by TDK.

$$(12) s = \left(\frac{A_L}{K1}\right)^{\frac{1}{K2}}$$

$$A_L = nH \text{ and } s = \text{mm}$$

Where K1 and K2 are given in the TDK ETD core [datasheet](#).

Material	Relationship between air gap – A_L value		Calculation of saturation current			
	K1 (25 °C)	K2 (25 °C)	K3 (25 °C)	K4 (25 °C)	K3 (100 °C)	K4 (100 °C)
N27	196	-0.734	308	-0.847	287	-0.865
N87	196	-0.734	300	-0.796	280	-0.873

Validity range:
 K1, K2: 0.10 mm < s < 3.00 mm
 K3, K4: 90 nH < A_L < 850 nH

Fig. 17: K1 and K2 values from TDK Datasheet

$$A_L = \frac{L_p}{N^2} = \frac{75830 \text{ nH}}{100}$$

Substituting A_L into s,

$$s = 0.158 \text{ mm}$$

The initial idea was to carefully grind the middle leg of the ETD core until this air gap is achieved. After the author spent a few hours grinding, it became apparent that the tools available could not precisely shave off 0.158mm of ferrite material. Moreover, grinding did not produce replicable values between each transformer core. After consulting with a friend who is a PhD student at the author's research lab, they advised to use Kapton tape at the transformer legs instead. Through trial and error, it was found that 20 mils of Kapton tape at the bottom, middle, and top legs of the transformer core resulted in 79.27 uH of primary inductance. The author concluded that this value is satisfactory.

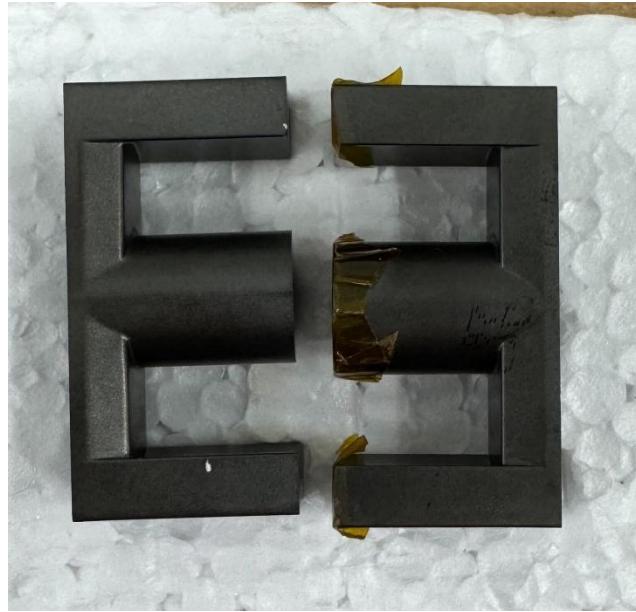


Fig. 18: Transformer Halves with Kapton as Air Gap



Fig. 19: Measuring Primary Inductance, With Air Gap

4.7.4 Leakage Inductance L_{leak} and Coil Windings

In real life conditions, not all the magnetic flux created by the primary winding flows through the magnetic circuit and links the other winding. This creates a leakage inductance, which describes the proportion of the magnetic field lines that does not flow to the secondary winding. This value is independent of the core material or air gap, instead, it depends on the position of the coils in relation with each other and the number of turns, thickness, and length of the coils. In Revision 0, the coils were wounded next to each other. With 10 primary turns and 4 secondary turns, a leakage inductance of 8.57 uH was

achieved. The leakage inductance is utilized as the resonant inductor in this LLC converter design. The next revision aims to reduce this leakage inductance so that higher switching frequencies can be achieved.

Different winding techniques can be applied to reduce leakage. Sectional winding was used to produce these coils, “bank winding” could help reduce leakage, but is very difficult to do by hand. In addition, winding the secondary on top of the primary coils can drastically reduce the value as well. The other techniques have not been tested with the current revision but will be tried on Revision 1 so that the switching frequency can be increased.

$$(13) k = \sqrt{1 - \frac{L_{leak}}{L_{prim}}}$$

The term hard/rigid coupling is used when the coupling factor is very high (ideally 1). The opposite is soft or loose coupling. This value will be used in the LTSpice simulations. The primary leakage inductance can be estimated by measuring the inductance of the primary coil while the secondary coil is shorted.

Coil formers coils were printed using resin, due to their heat resistance and isolation properties.



Fig. 20: Resin Printed Coil Formers

High frequency litz wire was chosen for the coil windings to reduce the losses caused by skin depth effect. It is difficult to obtain litz wire from official vendors and no datasheet for the litz wire products were found online. Ultimately, [litz wire from Remmington Industries](#) was purchased. They were chosen for the appropriate gauge size and ideal operating switching frequency of 100 kHz.



Fig. 21: Litz Wire

Both primary and secondary were wounded clockwise, with 10 turns on the primary and 4 turns on the secondary. The secondary has two 4-turn coils because the transformer is utilized in a center tapped configuration.

4.7.5 Magnetizing Inductance L_m

The magnetizing inductance can be seen as the inductance of a transformer's core. This inductance is responsible for magnetically coupling the B-field produced by one winding to the other windings of a transformer core. In an ideal transformer model, the magnetizing inductance is in shunt with the transformer windings, as shown below.

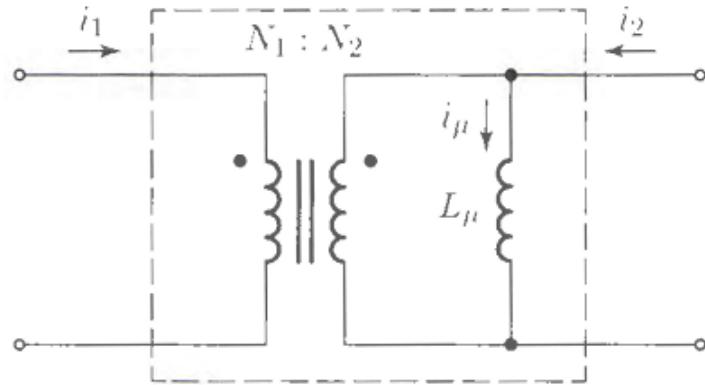


Fig. 22: Ideal Transformer Model with Magnetizing Inductance. Kassakian, J. G., Perreault, D. J., Verghese, G. C., & Schlecht, M. F. (2024). Principles of Power Electronics. Cambridge University Press.

The magnetizing inductance can be placed on either side of the transformer (primary or secondary), as long as it is multiplied by the turns ratio squared.

$$(14) \frac{N_{prim}^2}{N_{sec}^2} = \frac{L_{m,prim}}{L_{m,sec}}$$

If the magnetizing is much larger than the leakage inductance, equation 15 can be approximated.

$$(15) \frac{N_{prim}^2}{N_{sec}^2} = \frac{L_{prim}}{L_{sec}}$$

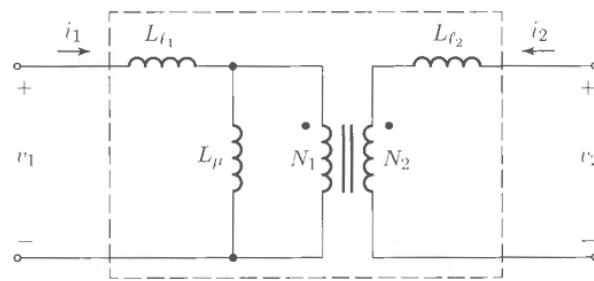


Fig. 23: Transformer Model with Magnetizing and Leakage Inductance. Kassakian, J. G., Perreault, D. J., Verghese, G. C., & Schlecht, M. F. (2024). Principles of Power Electronics. Cambridge University Press.

The magnetizing inductance can be approximated by subtracting the leakage inductance measurement form the primary inductance. Below is the list of parameters of the final transformer. W1, W2, and W3 represent the primary and 2 secondary windings.

Parameter	Test Procedure	Measurment
Primary Inductance L_{prim}	W1 measured, W2 and W3 open	79.27 uH
Secondary Inductance L_{sec}	W2 or W3 measured, W1 open	14.51 uH
Leakage Inductance L_{leak}	W1 measure, W2 or W3 shorted	8.43 uH
Magnetizing Inductance L_m	$L_{prim} - L_{leak}$	70.84 uH



Fig. 24: Completed Transformer

4.9 Simulation

The final parameters obtained are as follows:

Parameter	Value
Resonant Capacitance	300 nF
Resonant Inductance	8.43 uH
Magnetizing Inductance	70.84 uH
Switching Bridge	Half Bridge
Rectification	Full Wave with Center Tapped Transformer
Primary Turns	10
Secondary Turns	4

LTS spice is used to simulate the behavior of the LLC Converter. The EPC 2304 model files must be obtained from their website. The simulation was a great help in understanding what voltage and current behavior is expected at different switching frequencies.

The leakage inductance of the transformer is modeled using the coupling factor k (equation 13) of the transformer. The symbol L3 models the primary inductance while L4 and L1 models the two secondary inductances. Lastly, the directive “K3 L3 L1 L4 0.876” explains that the three inductances are magnetically linked with a coupling factor of 0.876.

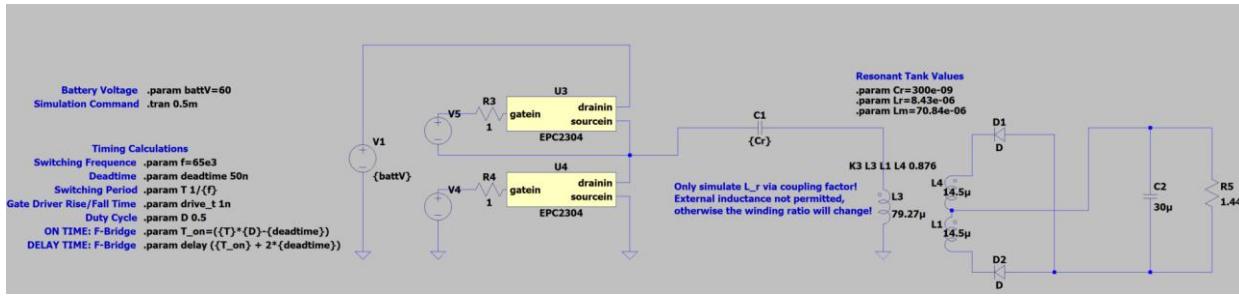


Fig. 25: LTSpice Model

5 Schematic

The open source KiCad software is used to design the LLC converter. The Power Stage board contains:

1. Gate Driver IC (AHV85111KNHTR)
2. GaN FET half bridge (EPC2304)
3. 300 nF Resonant Capacitance ()
4. Custom Transformer
5. Schottky Rectification Diodes (STPS1545)
6. 5 MHz Bandwidth Current Sensing IC (ACS37032)
7. 275 kHz Bandwidth Voltage Sensing IC (AMC3311QDWERQ1)
8. Input and output capacitance
9. Female headers to interface with the Logic Board
10. High Voltage (HV) input and Low Voltage (LV) output connectors

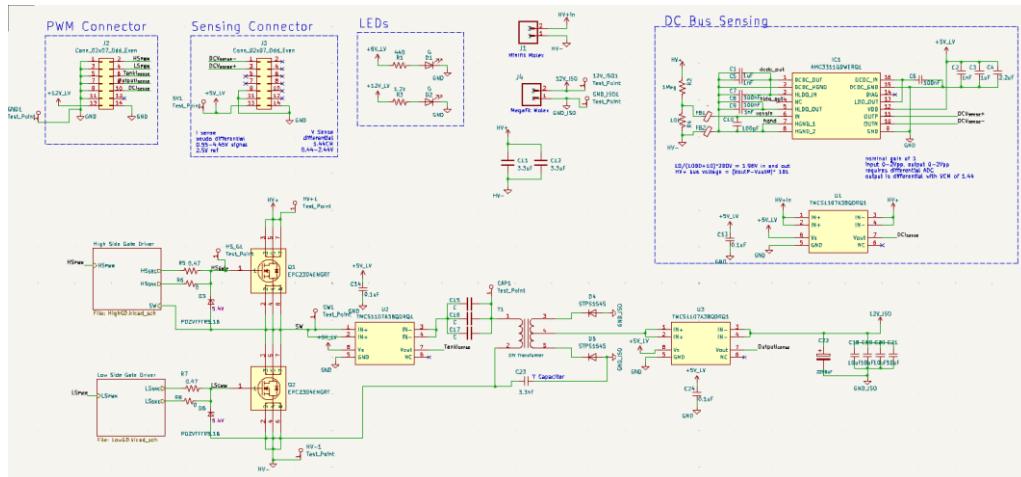


Fig. 26: KiCad Schematic

The Logic Board houses an STM32F334C8T6 microcontroller and differential sensing amplifiers. The STM32 generates the gate PWM signals using its high-resolution timers. In the current firmware, both switching frequency and dead time are adjustable, while closed-loop feedback control and a soft-start scheme are still under development.

6 Layout

The impact of parasitic inductance on performance is greatly magnified when these GaN FETs are switching at high frequencies. The PCB design of this converter aims to minimize these parasitic by implementing techniques provided by the manufacturer EPC. In a half bridge configuration, there are two main power loops to consider:

1. High-frequency power loop. Formed by the two power switching devices and the high-frequency DC bus capacitor.
2. Gate-drive loop. Formed by the gate driver, the power device, and the high-frequency gate-drive capacitor.

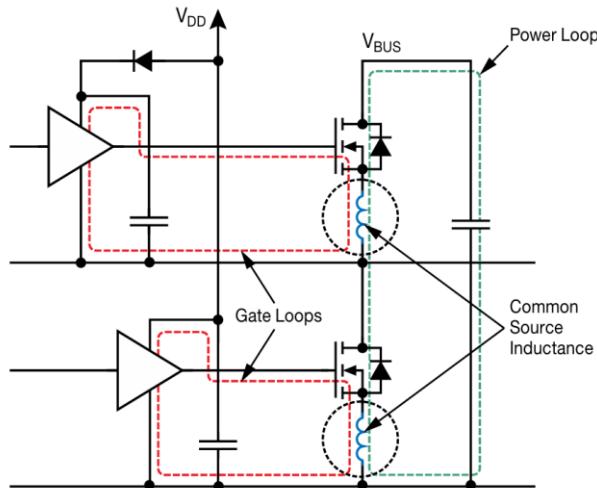


Fig. 27: Main Power Loops. Lidow, A., De Rooij, M., Strydom, J., Reusch, D., & Glaser, J. (2020). GAN transistors for Efficient Power Conversion. Wiley.

These GaN FETs come in tiny QFN packages with a land grid array formation to reduce package inductance. Although the EPC2304 does not provide a dedicated gate return source pin, the source pad closest to the gate driver is allocated as the “star” connection point for the gate loop and power loop, reducing common source inductance.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other.

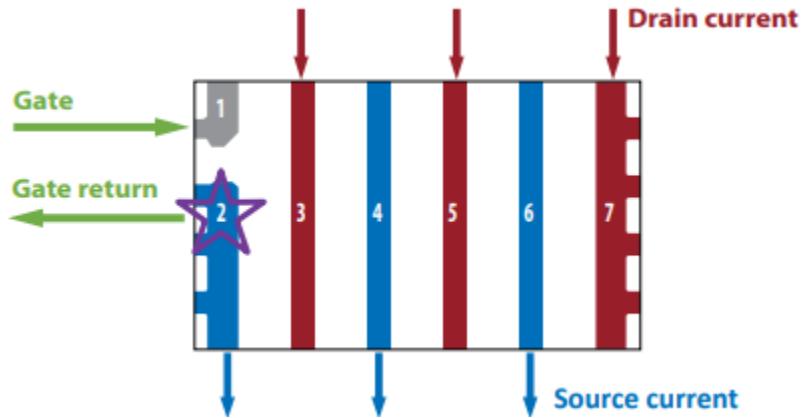


Fig: 28 EPC2304 QFN Package. [EPC2304 Datasheet](#)

The GaN FET packaging has been engineered to significantly reduce the common source inductance and is no longer the dominant contributor to parasitic inductance. Instead, the loop inductances controlled by the PCB layout become the major contributor to parasitics.

A vertical power loop design where the input capacitors and the GaN FETs are on opposite sides of the board was implanted for this revision. The power loop travels perpendicular to the board plane using vias. It is important to minimize the volume enclosed by the power loop, shown below, because the inductance is proportional to the cross-sectional area ($h * l$) and inversely proportional to the width (w). Hence, the PCB thickness must be minimized, and traces should be as short as possible.

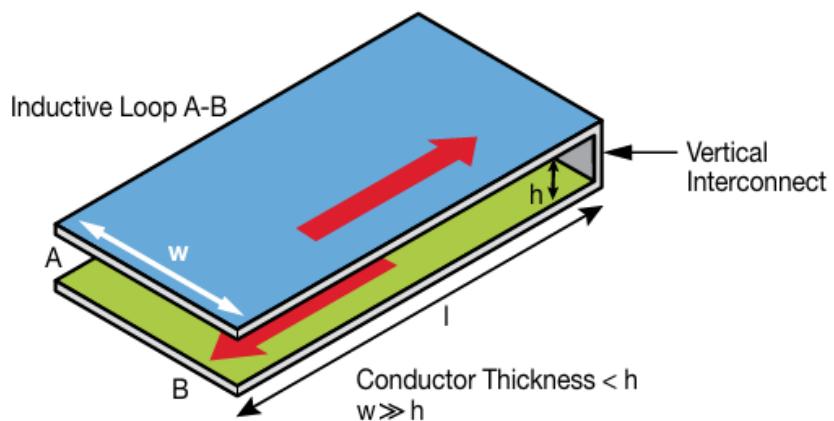


Fig. 29: Theoretical Parallel Plate Transmission Line Forming an Inductive Loop. Lidow, A., De Rooij, M., Strydom, J., Reusch, D., & Glaser, J. (2020). GAN transistors for Efficient Power Conversion. Wiley.

$$(16) L_{A-B} = \frac{\mu_R * \mu_0 * h * l}{w}$$

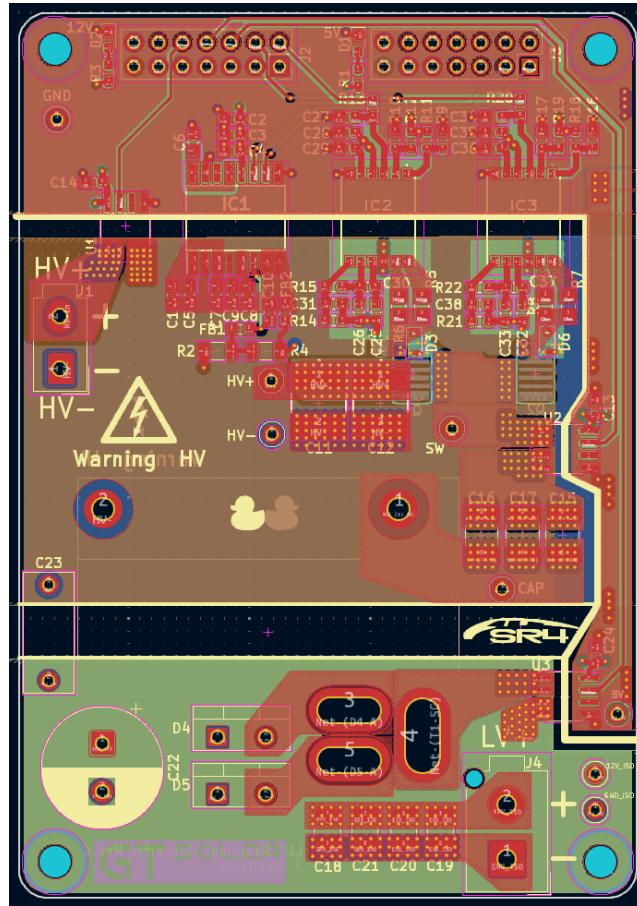
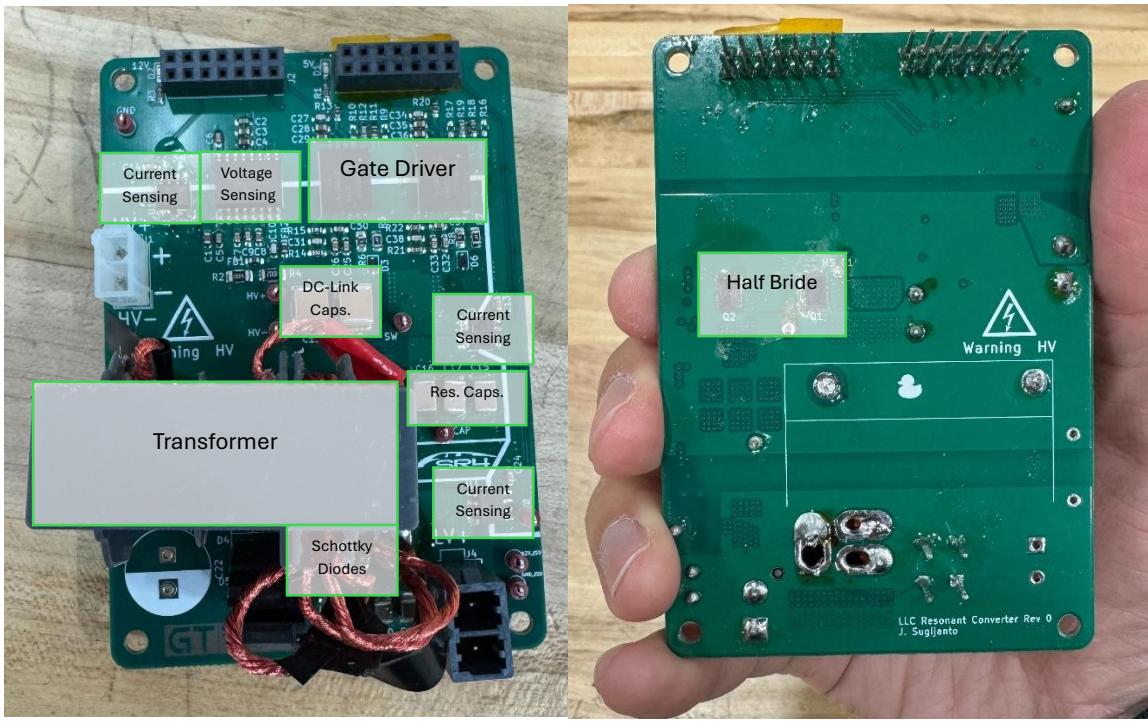


Fig. 30: PCB Layout

7 Benchtop Testing and Validation

The components were soldered to the PCB in-house using a reflow oven. After solder bridges were fixed and resistance tests were completed, the board was ready to be tested. Firmware for the microcontroller was written with C on the STM32 Cube IDE. The firmware has implemented ADC readings for current and voltage sensing and PWM generation with adjustable frequency, duty cycle, and dead time.



Fig. 31: PWM Outputs for High Side (HS) and Low Side (LS) Gate Driver. 100 kHz, 45ns dead time, and 50% duty cycle

Additional firmware was created for a Pulse Mode where only a specific number of PWM periods is output. Pulse Mode is first utilized to verify operation of converter components.



Next, a 100 ns dead time was verified to prevent shoot-through across the half bridge. Since the author does not have access to differential probes, this test was verified by probing the LS Drain to Source (which is HV-) voltage and the HS Gate to HV- Voltage.



Fig. 33: High Side FET V_{G_HV} (yellow) and Low Side FET V_{DS} (green)

With 5V supplied to the HV input and no output load, the HS gate is turned off before the LS FET stops blocking, as shown in Figure 34.



Fig. 34: Zoomed In High Side FET V_{G_HV} (yellow) and Low Side FET V_{DS} (green). LS FET stops blocking approximately 100ns after the HS Gate is turned off, as expected.

First, only a purely resistive load was connected between the switch node and HV-, without any of the resonant components connected.



Fig. 35: High Side Logic Signal (yellow) and Current Sensing Analog Output

Next, a series combination of the resonant capacitor (300nF) and a resistor (100Ω) is connected between the switch node and HV-. 30V supplied to HV input.



Fig. 36: Voltage Across Resistor for 9 Cycles. Waveform follows LTSpice Simulation.



The 100Ω resistor is removed and the primary winding of the transformer is connected to the resonant capacitor and HV-, while the secondary windings are left open. 10V supplied to HV input.



The ringing after the 25 cycles seems to be the Resonant Capacitance (C_r) and the Resonant Inductance (L_r) resonating with each other. The lower frequency oscillation during the 25 switching cycles seems to be the Resonant Capacitance (C_r) resonating with the Magnetizing Inductance (L_m).

Next, the secondary windings are connected to the rectification diodes, and the center tap wire is connected to a 30uF output bulk capacitance with no output load.



Fig. 38: Voltage Across Output Bulk Capacitance.10V supplied to HV input, unloaded output. Voltage level follows LTSpice simulation.



Fig. 39: Voltage Across Output Bulk Capacitance.20V supplied to HV input, unloaded output. Voltage level follows LTSpice simulation.

7.1 Steady State and ZVS Measurements

After progressively verifying all of the converter components, an Electronic Load with constant resistance can finally be connected to the output. The firmware is set to output the PWM signal continuously, so that steady state operations can be measured.

The LS V_{DS} (yellow), LS V_{GS} (green), and Transformer Current (blue) are measured for Figures 40 – 45. 60V supplied to HV and 1.7Ω load was connected to the output.



Fig. 40: Oscilloscope Capture at 100 kHz Switching Frequency and 100ns Dead Time.

Figure 40 shows the converter operating at the resonant frequency (100 kHz) of the LLC tank. In each switching half cycle, a resonant half cycle is completed and power is delivered to the secondary. The inductor current forms an almost perfect sinusoid.



Fig. 41: 100 kHz Switching Frequency, Turn On and Turn Off Events of LS FET

As seen in Figure 41, ZVS was not achieved when operating at 100 kHz with 100ns Dead Time. During Turn On, the V_{DS} of the LS FET starts to decrease, but does not reach 0V by the time the gate voltage is applied. This causes considerable overshoot and noise on the V_{DS} and V_{GS} readings. At the time of writing, the author needs to do further research as to why ZVS is not achieved at resonant frequency operation to improve the design for the next revision.

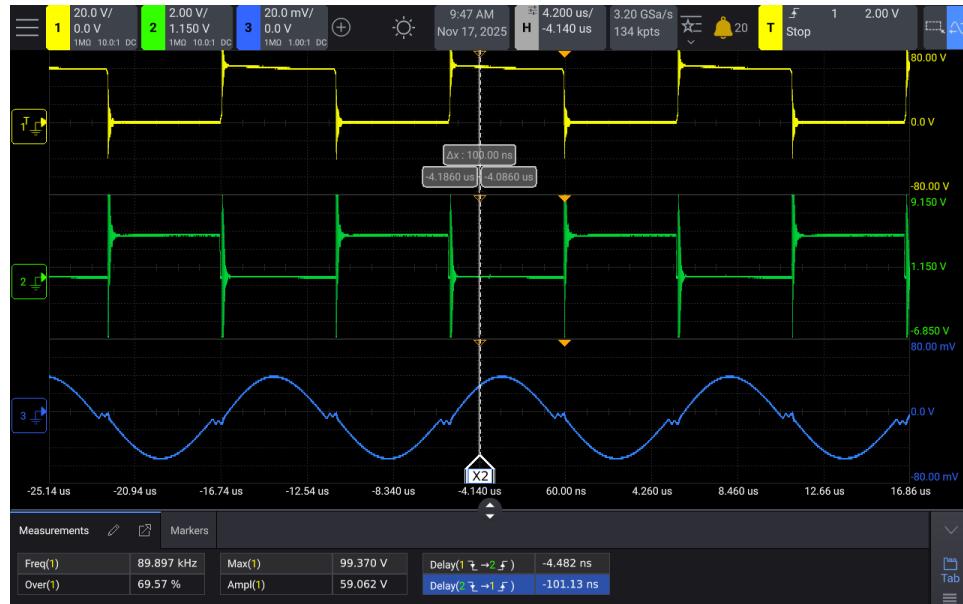


Fig. 42: Oscilloscope Capture at 90 kHz Switching Frequency and 100ns Dead Time.

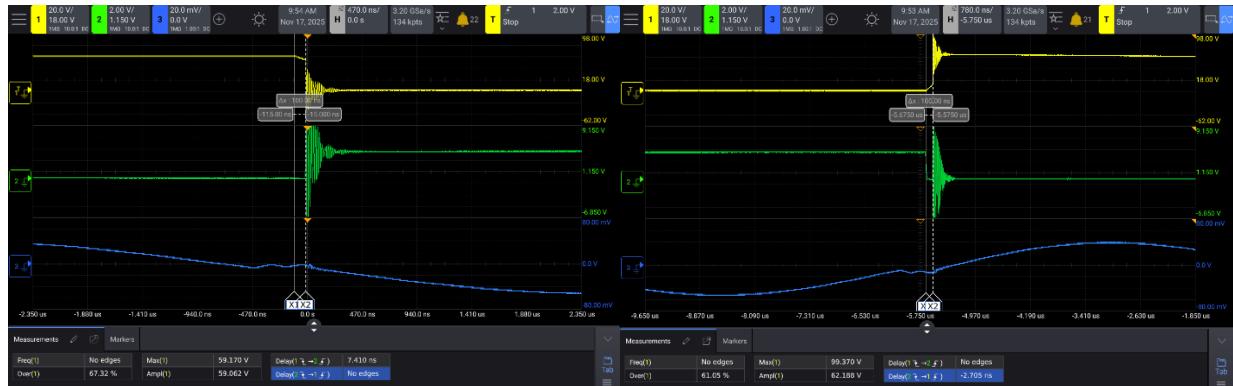


Fig. 43: 90 kHz Switching Frequency, Turn On and Turn Off Events of LS FET

At 90 kHz, the converter switches below the resonant frequency of the LLC tank. Each half of the switching cycle contains a full power delivery and freewheeling operation. When the inductor current reaches the magnetizing current, the freewheeling operation starts, signified by the flat portions in the inductor current (blue) waveforms. ZVS is also not achieved here.



Fig. 44: Oscilloscope Capture at 120 kHz Switching Frequency and 100ns Dead Time.



Fig. 45: 120 kHz Switching Frequency, Turn On and Turn Off Events of LS FET

At 120 kHz, the converter operates above the resonant frequency. In each switching half cycle, only a portion of the resonant half cycle is completed as it is interrupted by the start of the next half cycle, shown by the current waveform. ZVS is finally achieved in this operation; this can be seen as the V_{DS} reaches 0V before the gate voltage is applied during the turn on event. There is very little overshoot and noise on the voltage waveforms, as there is virtually zero dv/dt and very little EMI is produced.

7.2 Results

A DC Power supply (SL 160-9) and an Electronic Load (EL34243A) were used to perform steady state testing. The converter was supplied with 60V, and the Electronic Load was set on constant resistance mode. As the input voltage was held constant, the output resistance was swept between 24Ω to 1.3Ω .

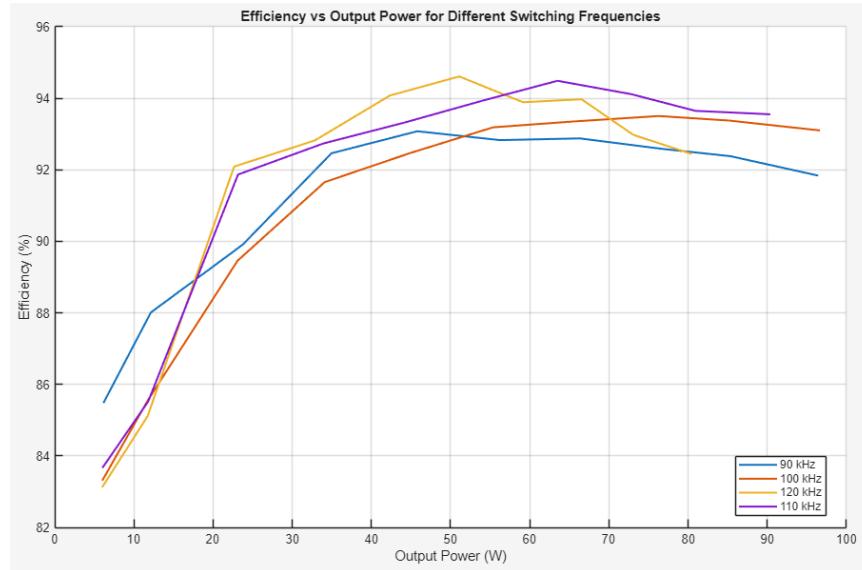


Fig. 46: Efficiency vs Output Power for Different Switching Frequencies

A peak efficiency of 94.6% was achieved while switching at 120 kHz while outputting 50W. The converter starts inefficient at lower output power, then start to increase until its peak, then gradually decreases again at high output power.

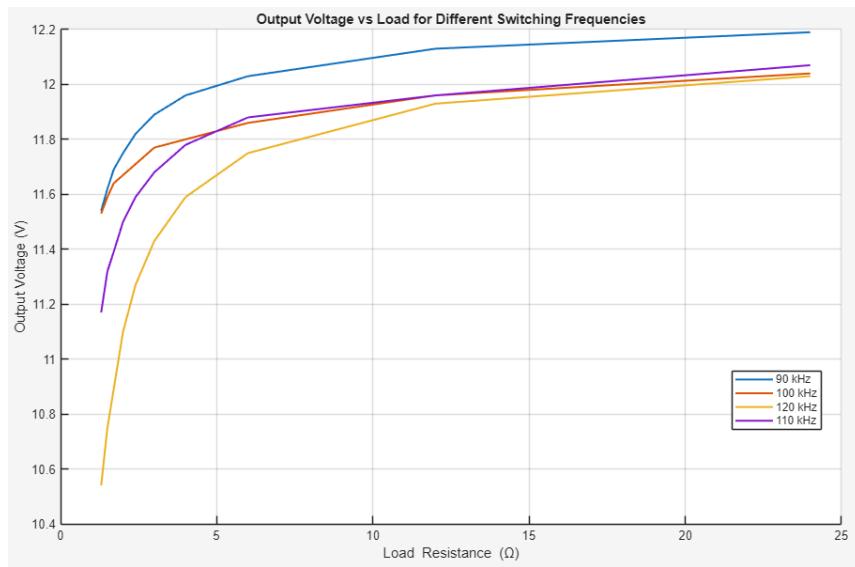


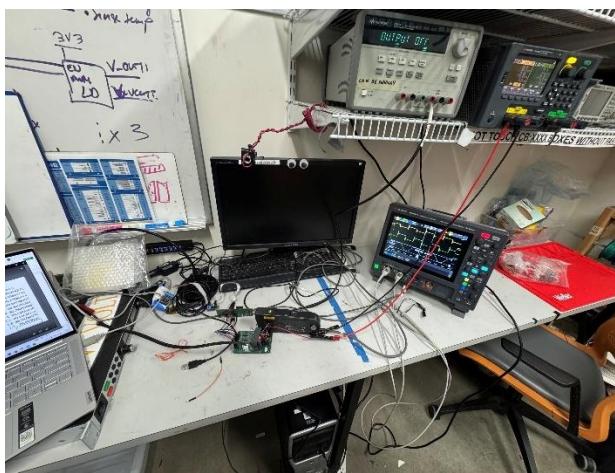
Fig. 47: Output Voltage vs Load Resistance for Different Switching Frequencies

At heavier loads (lower load resistance), the gain of the LLC tank significantly decreases, lowering output voltage. The effect is more significant the further the operation is from the resonant frequency, as shown with the 120 kHz curve (yellow). At lighter loads, the output voltage is more stable and at unity gain, so the output is around 12V. Lastly, operating at 90 kHz increases the LLC gain above 1, as it is in the “boost mode”. All of these observations agree with the gain vs frequency graph in Figure 3.

8 Miscellaneous Photos



Power Stage Board



Benchtop Test Setup