Yield, Overall Test Environment Timing Accuracy, and Defect Level Trade-offs for High-Speed Interconnect Device Testing

Baosheng Wang[1], Yong B. Cho[2], Sassan Tabatabaei[3], and André Ivanov[1]

[1]*SOC Lab, Department of Electrical & Computer Engineering, The University of British Columbia, Vancouver V6T 1Z4, Canada, 1-604-822-5333, {baosheng, ivanov}@ece.ubc.ca*

[2]*Department of Electronics Engineering, Konkuk University, Seoul Korea, ybcho@konkuk.ac.kr*

[3]*Vector 12 Corporation, stabatabaei@vector12.com*

Abstract

This paper extends the model in [4] to be more realistic by including the effects of the test fixtures between a device under test and a tester. The paper enables analyzing the trade-offs that arise between the predicted yield and the required overall test environment timing accuracy (OTETA) which involves the tester overall timing accuracy (OTA) and the test fixtures' impacts. We specifically focus on the application of the extended model to predict the test yield of standard high-speed interconnects, such as PCI Express, RapidIO, and HyperTransport. The extended model reveals that achieving an actual yield of 80% with a defect level of 300 DPM (Defects Per Million) requires an equivalent OTETA that is about half the acceptable absolute limit of the tested parameter.

Keywords: *Timing specifications testing, Test Environment, Yield analysis, Tester OTA and yield, High-speed interconnect testing*

1. Introduction

Four important factors that affect the quality of tests aimed at verifying device timing specifications are (i) yield; (ii) overall test environment timing accuracy (OTETA) which includes tester *overall timing accuracy (OTA)* [1] and the test fixtures' effects [2] [3]; (iii) defect level; and (iv) timing parameters. OTETA is a critical test parameter that directly impacts device yield and defect level [4]. Obviously, as device under test (DUT) speeds increase and associated timing specifications tighten, the criticality of OTETA increases. Increasing tester OTA and/or improving the test fixtures are two of the required trends to adequately test devices expected to run at ever increasing speeds [5].

Previous work on yield and device timing test mainly focus on relating the yield with device timing parameters either considering defect level [4] [6] or without considering defect level [7] [8] [9]. In [6], by using the delay fault coverage, a defect level model is proposed as a function of the yield of a manufacturing process and delay parameters. Statistical analysis models are applied to estimate the yield when testing timing skew in [7] and the delay at the output in [8]. By using static timing analysis techniques in PowerPC microprocessor timing tests, the authors of [9] estimate the yield for each path delay test and the total timing test yield for a given number of paths. However, all these related methods fail to relate the four factors stated earlier, like in [6] [7] [8] [9], or simply fail to consider the effects of the test fixtures that connect the DUT with a tester, like in [4]. This is compounded by the general lack of understanding of the relationships between realistic OTETA, timing specifications under test, yield and defect level. We conjecture that this obviously causes inaccurate test quality evaluations for timing parameter tests.

Currently, one emerging technology for which timing specifications are particularly important is the *high speed interconnect technology*, e.g., PCI Express [10], Rapid IO [11] and HyperTransport [12]. Testers used for verifying that devices dedicated to supporting such standards indeed meet their timing specifications must in turn possess sufficient timing accuracy. Misjudgments due to insufficient OTETA can cause considerable yield loss, and therefore corresponding economic loss. To the best of our knowledge, the application of such yield vs. OTETA predictions as they pertain to high speed interconnects has not yet been reported in the open literature. This causes a challenge in designing and testing the growing high speed interconnects applications.

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This paper presents an extension to the model used in [4], rendering the latter more realistic and thereby allowing a better estimation of the trade-offs between actual yield, OTETA, defect levels and DUT's timing specifications. Three applications of our extended model are discussed in this paper: (1) predicting actual device yields or defect levels (DPMs) for given OTETA and timing specification under test; (2) defining OTETA to guarantee an acceptable test quality; and (3) checking the device timing testability under test quality constraints in terms of defect level and expected yield. As the application examples, we predict the yield vs. device speed as in the future projections of the Test and Test Equipment Working Group of the International Technology Roadmap of Semiconductors 2001 (ITRS'01) and also apply our extended model to specific standard high speed interconnects to achieve better trade-offs during timing tests of their applications.

2. Review of Previous Work

We begin by briefly reviewing the basics of the timing test model and yield calculations developed in [4]. For a given timing parameter test through functional patterns, the device under test (DUT) is expected to produce a timing event (edge) according to a normal distribution with mean μ_{DUT} and a tester strobe edge is also assumed to be normally distributed. This is shown in Figure 1, where PS (program strobe) refers to mean timing value for which a tester edge strobe is programmed and AL (absolute limit) corresponds to the maximum limit from which a DUT's timing specification can vary away from the mean for the device to be considered acceptable.

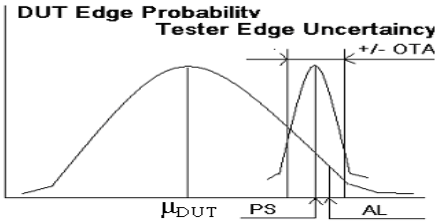

Figure 1. Timing parameter definitions

Several other yield-related terms are defined in [4]:

- The *ideal yield (IY)* is the expected yield before test;
- The *actual yield (AY)* is the measured yield after test;
- The *defect level (DL),* quantified as Defects per Million (DPM), is a measure of how many "bad" devices are incorrectly binned as "good" due to tester inaccuracy;
- The *yield loss (YL)* is a measure of how many "good" devices are incorrectly binned as "bad" due to tester inaccuracy.

The YL and DPM are illustrated in Figure 2.

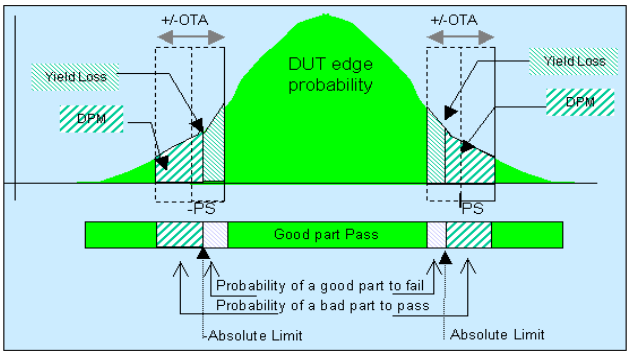

Figure 2. Yield Relationships

We assume a perfect process and therefore that IY = 1 (100%). From Figure 2, because bad devices may escape as good devices, thus contributing to the actual yield, IY = (AY – DPM/10^6) + YL.

Moreover, according to [4], the actual yield (*AY*) is a function of a DUT's absolute limit (AL) on a timing parameter, tester OTA, and Defect Level (DPM). Given AL, OTA and DPM, AY can be calculated from the model equations reported in [4]. Thus, the model in [4] can be considered as a yield estimator. Furthermore, if any three of four parameters AL, OTA, DPM or AY are specified, the fourth can be deduced. Applications of this model are summarized in Table 1.

Table 1. Model Applications

Application	Known Parameters	Calculated Parameter
Yield Estimation	OTA, DPM, AL	AY
OTA Requirement	DPM, AL, AY	OTA
Device Timing Testability Check	DPM, AY, OTA	AL

3. Extension of the Timing Test Model

In practice, tester channel probes are not directly connected the DUTs' pins. A device interface (fixturing) that typically includes connectors, PCBs, capacitors, cables, sockets and contactors, etc., applies. It is common not to include test fixturing effects (measurement error) when specifying testers OTA specifications, as in [1]. It is expected that such fixturing would still impact test accuracy, especially when dealing with higher speed devices although this type of errors can be calibrated in the first stage by using the TDR [13] (Time Domain Reflectrometry) and partly compensated for each pin-to-pin paths (both ATE-to-DUT and DUT-to-ATE). A realistic test environment, i.e., a realistic ATE that

includes a test fixture and a stand-alone ATE is illustrated in Figure 3.

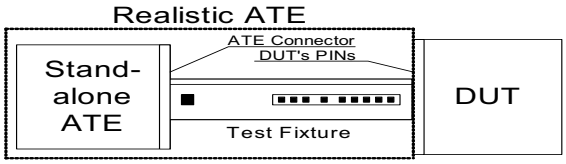

Figure 3. Timing Test Environment

To extend the realism of the timing test model used in [4], as illustrated in Figure 3, we model a realistic ATE as one that includes a stand-alone ATE as well as the test fixturing, in order to capture the overall test environment impact on signals reaching the DUT pins. Thus, in applications like those summarized in Table 1, the corresponding ATE's OTA is extended to OTETA.

Normally, the bandwidth of the test fixture path is much higher than the frequency of the signals applied to the DUT for the purpose of testing the latter's timing specifications. Under this assumption, two timing parameters, TPD and TS, can be applied to model the test fixture performance in all the channels and evaluate their effects on yield and/or other related parameters (as in Table 1).

Test Fixture Propagation Delay (TPD): the delay across the test fixtures from tester ports to DUT pins and/or vice versa. In an ideal setting or low-speed test, TPD is assumed to be negligible.

Test Fixture Skew (TS): the maximum magnitude of the difference in the TPD of different test fixture channels. Again, ideally or for low-speed tests, TS=0.

Regarding a single-ended serial interface, only the TPD parameter will affect the tester accuracy. Therefore, the corresponding OTETA can be expressed as

$$\text{OTETA} = \pm (\text{OTA} + \text{TPD}) \quad (1)$$

For parallel single-ended bus timing tests, TS is factor that affects tester accuracy because the timing tests depend on both the tested data signal and the reference signal which is normally a clock signal. Therefore, for such cases, OTETA can be expressed according to the following:

$$\text{OTETA} = \pm (\text{OTA} + \text{TS}) \quad (2)$$

The test fixture impact on differential I/Os is potentially worse. A differential I/O timing example is shown in Figure 4, where TS still denotes test fixture skew, and "plus" and "minus" denote the high and low signal values, respectively.

With differential I/Os, all the single-ended terminals are replaced by differential ports. These ports will be affected by the relative test fixture channel skew. Therefore, complementary signals' intersection point, which is usually used as the reference point for timing measurements, will shift left or right in time due to the test fixture. Thus, the realistic OTETA for differential serial I/O can be expressed as

$$\text{OTETA} = \pm (\text{OTA} + \text{TS}/2 + \text{TPD}) \quad (3)$$

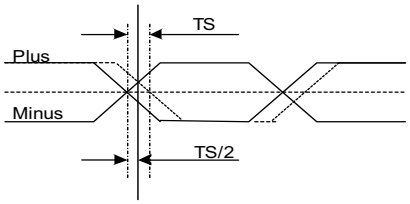

Figure 4. A Differential I/O Timing Diagram

According to Figure 4, due to the possibility that the measured differential signal itself and the reference differential signal itself can be delayed in opposite direction by the test fixtures and the potential test fixture channel skew between the measured differential signal and the reference signal, the realistic OTETA for parallel differential bus can be expressed as Equation (4):

$$\text{OTETA} = \pm (\text{OTA} + 2 * \text{TS}) \quad (4)$$

4. ITRS'01 Predictions Using the Extended Model

In this section, we determine the yields that our extended model predicts under ideal test fixtures given the OTETAs derived from the OTAs predictions in the ITRS'01 since there are no yield predictions in ITRS'01, as there were in ITRS'99. Assuming that 25% of device period, as predicted in [14], is considered as the absolute limit (AL) on the variation away from of the nominal device clock cycle for the device to be acceptable, and assuming a defect level of 300 DPM, the actual yield for the different technology nodes, assuming ideal test fixtures, is reported in Table 2.

Table 2. Yield Predictions for ITRS'01

	Year	'03	'04	'05	'06	'07	'10	'13	'16
BUS speed	GHz	2.1	2.3	2.5	2.7	3	6.6	14.5	32
DUT Period	ps	486	442	402	365	332	151	69	31
AL	ps	122	111	101	91	83	37	17	8
AY	%	71	67	64	59	54	37	17	14

The entries for AY in Table 2 show that the yield loss challenge will grow significantly over time.

Assuming a requirement of 80% actual yield and 300 DPM, the required OTETA under ideal test fixture conditions is as reported in Table 3 and further illustrated in Figure 5. The latter also compare our OTETA predictions for 80% actual yield and 300 DPM with those predicted as available in the ITRS'99 and ITRS'01. A significant gap between predictions on ITRS'99, ITRS'01 and those from our model exists, further suggesting the need for increased OTETA to achieve acceptable yields.

Table 3. Required OTETA to achieve 80% actual yield and 300 DPM for Devices Predicted by ITRS'01

	Year	'03	'04	'05	'06	'07	'10	'13	'16
BUS Speed	GHz	2.1	2.3	2.5	2.7	3.0	6.6	14.5	32
OTETA of 2001	ps	155	136	120	106	93	63	43	29
OTETA of 1999	ps	130	115	100	100	100	100	100	100
OTETA from our Model	ps	61	56	50	46	42	19	9	4

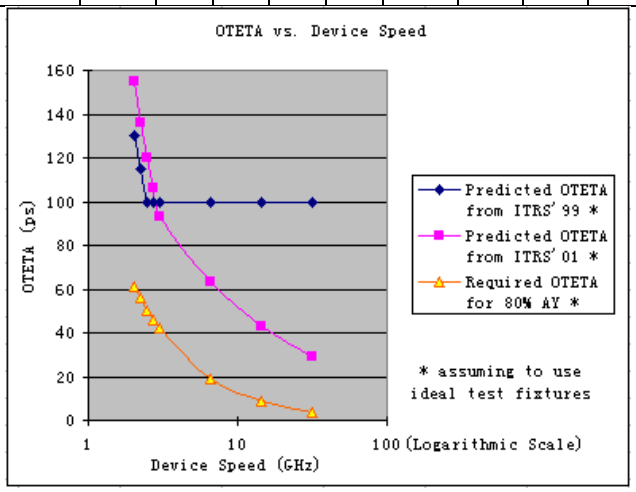

Figure 5. Required OTETA to achieve 80% AY and 300 DPM and predicted OTETA from ITRS documents under Ideal Test Fixture

5. High Speed Interconnect Timing Tests

High performance systems require high-speed interconnects for chip-to-chip or board-to-board connections. Several high-speed interconnect standards are emerging, e.g., RapidIO, HyperTransport, and PCI Express.

5.1 PCI Express Timing Test

For high-speed digital parts, specified timing parameters include propagation delays, setup and hold time, rise and fall time, skew (including clock skew, data to clock skew and data to data skew), and jitter. All of these parameters can be measured by specified functional test patterns if appropriate test environments specified OTETA exist. Test yields are sensitive to test environment accuracy when testing these parameters. PCI Express (formerly 3GIO) is a new differential serial I/O technology that is compatible with the current PCI software environment. Table 4 shows some typical timing parameters of Differential Transmitter (TX) Output Specifications for the PCI Express Standard in [10].

Table 4. PCI Express Differential Transmitter (TX) Output Timing Specifications

Line Speed (embedded clock speed): 2.5Gbps					
Symbol	Parameter	Max (ps)	AL (ps)	AY (%) under the defined test environment below	Required OTETA to achieve 80% AY and 300 DPM (ps)
$T_{TX\text{-}JITTER}$	Transmitter Jitter	120	60	24.5	30
$T_{TX\text{-}RISE}$ $T_{TX\text{-}FALL}$	D+/D- TX Output Rise/Fall Time	200	75	36	37.5
$L_{TX\text{-}SKEW}$	Lane-to-Lane Output Skew	500	500	88	250

As an interconnect with embedded clock interfaces, GHz PCI Express is more difficult to test than synchronous counterparts for which timing parameters can be tested using functional test patterns applied through sufficiently accurate test environments. However, two mandatory DFT features defined by the standard simplify the test of PCI Express interfaces [15]. These are that all the timing parameters of the transmitter can be checked against a special compliance pattern and all the receiver parametric are testable via the device internal Rx to Tx path by executing functional tests on the Tx pins with varying Rx parameters.

In Table 4, AL is defined as half of the difference between the maximum and minimum values for all timing parameters. Ideal minimum value for the transmitter jitter

is 0ps and its absolute limit value for our model is 60ps. Because the transmitter rise/fall time is less than half of the cycle time but exceeds 50ps (from [10]), the AL of the transmitter is taken to be (200 - 50)/2ps. However, we assume skew to be positive or negative, ranging between –500ps and 500ps, and therefore assume its associated absolute limit to be 500ps. Here, by defining a test environment in which an available tester, e.g., from [16], has ±100ps OTA, and characterized test fixtures have ±10ps TPD and TS, the actual yield values are those shown in Table 4. The yields that result for testing the transmitter jitter and rise/fall time by a tester with such accuracy would clearly not be viable. Although an eye diagram width can be used to substitute the testing of the transmitter jitter due to the embedded design-for-test features in the PCI Express protocol, the potential yield under the defined test environment above will remain the same as the eye diagram varies by the same width as that of the jitter which defines AL as the same. According to equation (3), a possible solution to overcome yield loss is using more accurate ATE with considerably greater OTA and/or higher performance test fixtures with less TS and TPD. To achieve an actual yield of 80% and 300 DPM, the required OTETA for testing the typical timing parameters above is determined from our extended model and reported in Table 4.

5.2 RapidIO Timing Test

RapidIO is a high performance low pin count packet-switched system-level interconnect architecture intended primarily as an intra-system interface for chip-to-chip and board-to-board communications at gigabyte-per-second performance levels. Its architecture is specified in a three-layer hierarchy consisting of a logical layer, a common transport layer, and a physical layer. In the RapidIO Physical Layer 8/16 LP-LVDS (Low Voltage Differential Signaling) AC specification, the allowable static skews of data output to associated clock are shown in Table 5 ($t_{skew, pair}$ is the static skew of data output to associated clock defined in [11]).

In Table 5, AL = (Max-Min)/2. By reusing the defined test environment above, the actual yield is as predicted in Table 5. Assuming a 300 DPM requirement, our extended model also predicts the required OTETA shown in Table 5 for 80% actual yield. Results presented in Table 5 suggest the need for OTETAs better than 100ps if adequate testing and yields for such parts are to be achieved.

Table 5. RapidIO Driver AC timing Specifications ($t_{skew, pair}$)

Date Rate	Range (ps)	AL (ps)	AY (%) under the defined test environment above	Required OTETA to Achieve 80% AY and 300 DPM (ps)
(Mbps)	Min Max	(ps)		
500	-180 180	180	74	90
750	-133 133	133	64	67
1000	-100 100	100	50	50
1500	-133 133	133	64	67
2000	-100 100	100	50	50

5.3 HyperTransport Timing Test

HyperTransport technology is another parallel packet-based link implemented on two independent unidirectional sets of wires. Table 6 shows the HyperTransport link skew of transmitter PHY output data to data in [12]. Still assuming the test environment above, and assuming a 300 DPM requirement, our model estimates that the required skew of HyperTransport data to clock absolute limit (AL) is about 240ps to achieve 80% actual yield.

Table 6. HyperTransport Timing Parameters

Data Rate	Skew of transmitter data to clock (ps)		AL	AY under the defined test environment above	Required OTETA to achieve 80% AY and 300 DPM (ps)
(Mbps)	Min	Max	(ps)	(%)	(ps)
400	-283	283	283	83	142
600	-192	192	192	76	96
800	-151	151	151	69	76
1000	-130	130	130	63	65
1200	-111	111	111	56	56
1600	-91	91	91	45	46

In Table 6, the higher the line speeds of the HyperTransport I/O interconnect, obviously the more stringent the test of skew of transmitter output data to data. This is because the absolute limit (AL) from [12] are farther and farther from the required AL when guaranteeing 80% actual yield and 300DPM defect level as the HyperTransport device speeds approach the GHz ranges.

Moreover, the predicted yield assuming the defined test environment above and the required OTETA defined by our extended model, are also reported in Table 6. Due to

the yield loss and the gap between the available and required OTETA, more accurate ATEs and improved test fixtures are obviously needed.

6. Conclusions

In this paper, we introduced a realistic model that relates yield, overall testing environment timing accuracy (OTETA) (an extension to with the standard tester accuracy (OTA)), and defect level, assuming a given timing specification under test. We discussed the model and applications. We compared the values of OTETA requirements from our model with those found in the ITRS documents under ideal test fixtures. We illustrated the application of our model to explore the OTETA requirements for testing timing specification of emerging high-speed interconnects, namely PCI Express, RapidIO, and HyperTransport. The results of our case studies revealed that testing the timing specifications of such standards will require the availability of testers with OTETAs that are much better than those predicted to be available in the ITRS documents. Hence, continued improvements in testing environment accuracies, e.g., specific test methods or Built-in-self-test (BIST) like testing methodologies, are in order if such high speed devices are to be tested for their timing specifications in productions stages and such that acceptable yields and defect levels are to be achieved.

7. Acknowledgements

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