Jacob Betsworth

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Recent Computer Engineering Master's Graduate looking for industry experience in logic design using C/C++/VHDL/Verilog to design ASIC, processor, and GPU designs. Well versed in computer architecture having created processor and GPU designs in hardware design languages and tested them on FPGAs. Capable of performing research that will propel current and future projects to new horizons.

Education

BACHELOR OF SCIENCE | COMPUTER ENGINEERING| IOWA STATE UNIVERSITY

- GPA 3.15/4.00

MASTER OF SCIENCE | COMPUTER ENGINEERING | IOWA STATE UNIVERSITY

- GPA 3.44/4.00
- Focus in storage systems, fault handling, and logic design.

Experience

RESEARCH ASSISTANT | DATA STORAGE LAB, IOWA STATE | SPRING 2023

- Conducted literature reviews over research papers to find relevant information for upcoming projects and to increase personal and group knowledge of a technology or method.
- Experimented with different software and virtual machines to evaluate platforms for project usage.

TEACHING ASSISTANT | IOWA STATE UNIVERSITY | FALL 2021 – FALL 2022

- Fall 2021-Spring 2022: Senior Design Assistant
  - Edited student documents and gave them notes on what to improve in their design documents to make them easier to understand.
- Fall 2022: Embedded Systems Lab Assistant
  - Helped students debug their C code that they would be uploading to a test embedded system provided, Roomba.
  - Gave guidance to students when their understanding of the problem wasn't right or if they were moving in the wrong direction.

LOGIC DESIGN INTERN | MICRON TECHNOLOGY | SUMMER 2022

- Pathfound for a future project using SystemVerilog to model what needed improvements and where to focus efforts.
- Led meetings with relevant engineers to get a full picture of what was wanted and what could be done with what resources there were.

OPERATIONS MANAGER | MR. PICNIC OMAHA | MAY 2016 – CURRENT

- Communicated with customers to deliver according to their schedule so they had everything ready to go for their party.
- Mapped out routes that would be most efficient for drivers to keep drive time to a minimum.

NETWORK SOLUTIONS INTERN | PRIME COMMUNICATIONS, INC. | SUMMER 2019

- Learned about the communication infrastructure in use and being upgraded in schools and businesses.
- Transported equipment efficiently that allowed the upgrade project to advance ahead of schedule allowing for more of a buffer period for stability tests.

Projects

CENOD – CUSTOMIZABLE ENEMY N' OBJECT DETECTION | SPRING 2022

- Using different open detection techniques and OpenCV in Python made an app that would allow users to detect certain enemies or objects in games by using the right filter to find the target.

BASIC GPU DESIGN | SPRING 2021

- Developed a GPU using VHDL for the hardware and C for the drivers.
- Tested with OpenGL programs loaded onto a FPGA running the VHDL code. Done using remote access during COVID.

PROCESSOR DESIGN SIMULATOR | FALL 2020-SPRING 2021

- Senior Design project commissioned by a teacher to help students learn the structure and elements inside a CPU.
- Developed in a five-person team, personal task was creating elements for user interaction such as the switches and different controls.
- Developed as a website page with HTML, CSS, and Javascript.
- https://www.ece.iastate.edu/~alexs/classes/i281/index.html

MIPS PIPELINE PROCESSOR DESIGN | FALL 2019

- Designed different ALUs, registers, multiplexers, and hazard logic and tested for proper functionality in VHDL.
- Created schematics for different design elements to keep the group unified on the design intention.
- Instructions based on ARM assembly

CLUSTERCORE, AN ANDROID APP | FALL 2019

- Designed an android multiplayer game that had a SQL database for account details on the backend and a Java based frontend for the user.
- Oversaw user interface and development of the user experience to make things easy to navigate and understand.

Skills

- Machine Learning, C/C++, VHDL/Verilog/SystemVerilog, Debugging, Logic Design, Assembly, Javascript, HTML, Python, Linux, FPGAs, Git, Microsoft Office, Technical Documentation, Constructive Feedback