#	Name	Details
1	IP_Flow 19-4067	Ignoring invalid widget type specified checkbox.Providing a default widget
2	IP_Flow 19-4067	Ignoring invalid widget type specified checkbox.Providing a default widget
3	Synth 8-3917	design EtchaSketch_TOP has port vgaBlue[1] driven by constant 0
4	Synth 8-3917	design EtchaSketch_TOP has port vgaBlue[0] driven by constant 0
5	Synth 8-3917	design EtchaSketch_TOP has port vgaGreen[0] driven by constant 0
6	Synth 8-3917	design EtchaSketch_TOP has port vgaRed[0] driven by constant 0
7	Synth 8-3917	design EtchaSketch_TOP has port vgaBlue[1] driven by constant 0
8	Synth 8-3917	design EtchaSketch_TOP has port vgaBlue[0] driven by constant 0
9	Synth 8-3917	design EtchaSketch_TOP has port vgaGreen[0] driven by constant 0
10	Synth 8-3917	design EtchaSketch_TOP has port vgaRed[0] driven by constant 0
11	Project 1-486	Could not resolve non-primitive black box cell 'BRAM' instantiated as 'mem' [O:/ENGS31/final/final.srcs/sources_1/imports/sources_1/imports/new/VGA_Controller_top.vhd:225]
12	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port MUX_RST[0]
13	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port MEM_LAT_RST
14	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port MUX_REGCE[0]
15	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port WE
16	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[16]
17	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[15]
18	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[14]
19	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[13]
20	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[12]
21	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[11]

22	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[10]
23	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[9]
24	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[8]
25	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[7]
26	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[6]
27	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[5]
28	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[4]
29	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[3]
30	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[2]
31	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[1]
32	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port ADDR_IN[0]
33	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[63]
34	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[62]
35	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[61]
36	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[60]
37	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[59]
38	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[58]
39	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[57]
40	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[56]
41	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[55]
42	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[54]
43	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[53]

44	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[52]
45	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[51]
46	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[50]
47	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[49]
48	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[48]
49	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[47]
50	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[46]
51	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[45]
52	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[44]
53	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[43]
54	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[42]
55	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[41]
56	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[40]
57	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[39]
58	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[38]
59	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[37]
60	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[36]
61	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[35]
62	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[34]
63	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[33]
64	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[32]
65	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[31]

66	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[30]
67	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[29]
68	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[28]
69	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[27]
70	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[26]
71	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[25]
72	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[24]
73	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[23]
74	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[22]
75	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[21]
76	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[20]
77	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[19]
78	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[18]
79	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[17]
80	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[16]
81	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[15]
82	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[14]
83	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[13]
84	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[12]
85	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[11]
86	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[10]
87	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[9]

88	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[8]
89	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[7]
90	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[6]
91	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[5]
92	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[4]
93	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[3]
94	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[2]
95	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[1]
96	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port SBITERRIN[0]
97	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[63]
98	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[62]
99	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[61]
100	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[60]
101	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[59]
102	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[58]
103	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[57]
104	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[56]
105	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[55]
106	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[54]
107	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[53]
108	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[52]
109	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[51]

110	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[50]
111	Synth 8-3331	design blk_mem_gen_mux__parameterized0 has unconnected port DBITERRIN[49]
112	DRC 23-20	Rule violation (CFGBVS-1) Missing CFGBVS and CONFIG_VOLTAGE Design Properties - Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax: set_property CFGBVS value1 [current_design] #where value1 is either VCCO or GND set_property CONFIG_VOLTAGE value2 [current_design] #where value2 is the voltage provided to configuration bank 0 Refer to the device configuration user guide for more information.