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----------------------------------------------------------------------------------
-- Engineer: Taggart Bonham and Will Chisholm
-- Create Date: 05/23/2017 09:05:13 PM
-- Module Name: vga_sync_tb- Behavioral
-- Project Name: Etch-a-Sketch final project
-- Target Devices: Digilent Basys3 Board
-- Tool Versions: Vivado 2016.1
-- Description: testbench of vga_SYNC
----------------------------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;

entity VGA_tb is
end VGA_tb;

architecture testbench of VGA_tb is

component VGA_SYNC IS
PORT (  clk     :   in  STD_LOGIC; --100 MHz clock
        V_sync  :   out STD_LOGIC;
        H_sync  :   out STD_LOGIC;
        video_on:   out STD_LOGIC;
        pixel_x :   out STD_LOGIC_VECTOR(9 downto 0);
        pixel_y :   out STD_LOGIC_VECTOR(8 downto 0));
end component;



signal  clk     :   STD_LOGIC; --100 MHz clock
signal  V_sync  :   STD_LOGIC;
signal  H_sync  :   STD_LOGIC;
signal  video_on:   STD_LOGIC;
signal  pixel_x :   STD_LOGIC_VECTOR(9 downto 0);
signal  pixel_y :   STD_LOGIC_VECTOR(8 downto 0);


begin

uut : VGA_SYNC PORT MAP(
        clk  => CLK,
        V_sync => V_sync,
        H_sync => H_sync,
        Video_on => video_on,
        pixel_x => pixel_x,
        pixel_y => pixel_y);


clk_proc : process
BEGIN

  CLK <= '0';
  wait for 5 ns;

  CLK <= '1';
  wait for 5 ns;

END PROCESS clk_proc;

stim_proc : process
begin



    wait;
```

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end process stim_proc;
end testbench;
```