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-- Create Date: 05/23/2017 09:05:13 PM
-- Design Name:
-- Module Name: Mux2x1- Behavioral
-- Project Name: Etch-a-Sketch final project
-- Target Devices: Digilent Basys3 Board
-- Tool Versions: Vivado 2016.1
-- Description: A basic mux, used to explicitly show how our clear procedure works

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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux2x1 is --simples 2x1 Mux
  Port ( A : in STD_LOGIC_VECTOR (16 downto 0);
         B : in STD_LOGIC_VECTOR (16 downto 0);
         sel : in STD_LOGIC;
         y: out STD_LOGIC_VECTOR (16 downto 0));
end Mux2x1;

architecture Behavioral of Mux2x1 is


begin

with sel select y<= --Mux logic
     A when '0',
    B when '1';


end Behavioral;
```