Critical Path

Max Delay Paths

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Slack (MET) : 8.744ns (required time - arrival time)

Source: sclkdiv\_reg[0]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: sclkdiv\_reg[0]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 1.252ns (logic 0.580ns (46.336%) route 0.672ns (53.664%))

Logic Levels: 1 (LUT1=1)

Clock Path Skew: 0.000ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.786ns = ( 14.786 - 10.000 )

Source Clock Delay (SCD): 5.086ns

Clock Pessimism Removal (CPR): 0.300ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Our critical path comes from the Clock divider that turns the Board’s 100 MHz clock into a 25 MHz clock in order to interface with the VGA’s output. The route starts at the sclkdiv\_reg (slow clock divider register) and travels through one level of logic, a look up table, before reaching it’s destination, sclkdiv\_reg, the same register. The logic portion of the delay is .580 ns, about 45% of the path, and the route takes .670 ns, or 55%. The maximum estimated time of slack, or MET, is 8.744 ns meaning that the design could be clocked faster. However, based on specifications in the datasheets for VGA Sync we saw in class, and the limits of human speed when interfacing with a debounced knob, there is no incentive to run it faster.