概念题常考

内存

静态动态RAN

Give two advantages and two disadvantages of dynamic RAM over static RAM

Advantages of DRAM:

- Higher Density: Simpler cell structure allows more memory per chip.
- Lower Cost: Cheaper to manufacture per bit.

disadvantages of DRAM:

- Slower Speed: Longer access times compared to SRAM.
- Requires Refreshing: Must be periodically refreshed to retain data, adding complexity.

Differences between ROM types**

- **(i) ROM vs. PROM**: **ROM** is mask-programmed at the factory. **PROM** is programmed once by the user.
- **(ii) PROM vs. EPROM**: **PROM** is one-time programmable. **EPROM** can be erased with UV light and reprogrammed.
- **(iii) EPROM vs. EEPROM**: **EPROM** requires UV light for a full-chip erase. **EEPROM** can be erased and reprogrammed electrically, in-circuit, often byte-by-byte.

磁盘计算题

SSD 与 HDD

Give two advantages and two disadvantages of solid-state drive (SSD) compared to HDD.

Advantages of SSD:

- Greater Durability: More resistant to physical shock and vibration. 更高的耐用性：更能抵抗物理冲击和振动。
- Faster Speed: Much lower latency and higher transfer speeds due to no moving parts. : "更快的速度：由于没有移动部件，延迟显著降低，传输速度更高。

Disadvantages of SSD:

- Limited Lifespan: Flash memory cells have a finite number of write cycles . 有限寿命：闪存单元具有有限的写入周期数。
- Higher Cost: More expensive per gigabyte than HDDs. "更高的成本：每千兆字节的价格比HDD高。

缓存: How caching speeds up execution

Caches (fast SRAM) store frequently used data from slower main memory (DRAM). They work on the principle of locality . When data is found in the cache (a hit), access is very fast. This reduces the average memory access time, speeding up the CPU. 缓存（高速SRAM）存储来自较慢的主内存（DRAM）的常用数据。它们基于局部性原理工作。当数据在缓存中找到时（命中），访问速度非常快。这减少了平均内存访问时间，从而加快了CPU的速度。

汇编概念

What is the main difference between assembler directives and assembly language instructions?

- **Assembly instructions** (`mov`, `add`) are translated into machine code for the CPU to execute at runtime.
- **Assembler directives** (`.MODEL`, `.DATA`) are commands for the assembler itself, guiding the assembly process (e.g., memory layout), and do not translate to executable CPU instructions.

命名

Difference between mnemonics and opcodes

- **Mnemonics**: Human-readable instruction names (for programmers).
- **Opcodes**: Machine-readable binary/hex codes (for the CPU).
- An assembler translates mnemonics into opcodes.

大端小端 Big-Endian vs. Little-Endian

- **Big-Endian**: Stores the Most Significant Byte (MSB) at the lowest memory address. "Big end first."
- **Little-Endian**: Stores the Least Significant Byte (LSB) at the lowest memory address. "Little end first." Intel CPUs use this convention.

导体

a)i) Briefly explain how an npn BJT is turned on.

Put a large positive voltage at base of the BJT to remove the depletion region in the narrow base, causing a large current to flow between collector and emitter.

在BJT的基极施加一个大的正电压，以消除窄基极中的耗尽区，从而导致集电极和发射极之间有大电流流动

ii) Briefly explain how an n-channel FET is turned on.

Put a large positive voltage at the gate of the FET to attract electrons to the n-channel allowing for a large current flow between the source and the drain.

在FET的栅极施加一个大的正电压，以吸引电子进入n沟道，从而允许源极和漏极之间有较大的电流流动。

硬件

指令集

Briefly explain the differences between the operation of a complex instruction set computer (CISC) and a reduced instruction set computer (RISC). Give one advantage of each.

CISC uses complex instructions that can perform multiple operations in a single instruction.

Advantage: High code density (smaller program size).

Uses a small set of simple, fixed-length, and fast instructions.

Advantage: Simpler design allows for faster clock speeds and easier instruction pipelining, leading to higher performance and lower power consumption. 更简单的设计使得更高的时钟速度和更容易的指令流水线成为可能，从而提高了性能并降低了功耗。

CPU架构

Give three examples of techniques modern CPUs use to speed up processing time.现代CPU用于加速指令平均处理时间的三种技术及其解释

Pipelining: An instruction is broken into stages (fetch, decode, execute, etc.). The CPU overlaps these stages for different instructions, processing them like an assembly line to increase instruction throughput.流水线：一条指令被分解为多个阶段（取指、解码、执行等）。CPU重叠处理不同指令的这些阶段，像装配线一样处理它们，以增加指令吞吐量。

Caching: A small, fast memory (SRAM) is placed between the CPU and main memory (DRAM). It stores frequently accessed data, reducing the average memory access time based on the principle of locality."translation": "缓存：在CPU和主内存（DRAM）之间放置一小块快速存储器（SRAM）。它存储经常访问的数据，根据局部性原理减少平均内存访问时间。

Superscalar Architecture: The CPU has multiple execution units (e.g., multiple ALUs) allowing it to execute more than one instruction per clock cycle, achieving a higher degree of instruction-level parallelism." 超标量架构：CPU具有多个执行单元（例如，多个算术逻辑单元），使其能够在每个时钟周期内执行多条指令，从而实现更高的指令级并行度。

中断

List the 3 types of interrupts, and briefly explain why they are used.

Hardware Interrupts: Asynchronous signals from external devices (e.g., keyboard). Used for efficient I/O handling without constant polling. 硬件中断：来自外部设备（例如键盘）的异步信号。用于高效处理I/O，而无需持续轮询。

Software Interrupts: Synchronous calls from code via an instruction (e.g., INT n). Used for system calls to request OS services. 软件中断：通过指令（例如，INT n）从代码发出的同步调用。用于系统调用以请求操作系统服务。

Exceptions: Synchronous events caused by errors during instruction execution (e.g., division by zero). Used for error handling. "translation": "异常：由指令执行过程中发生的错误引起的同步事件（例如，除以零）。用于错误处理。

Explain briefly the actions the CPU will take when attending to an interrupt.

Finishes the current instruction.

Saves Context: Pushes the Program Counter and Status Register onto the stack.

Identifies Interrupt: Gets an interrupt number to identify the source.

Finds Handler: Looks up the address of the Interrupt Service Routine (ISR) in the Interrupt Vector Table (IVT).

Jumps to ISR: Loads the ISR address and begins execution.

Returns: After the ISR is done, it restores the context from the stack and resumes the original program.

Why are interrupts necessary for the proper functioning of the CPU? Give one function each for hardware and software interrupts. （为什么中断是必要的）

- **Necessity**: Interrupts are crucial for CPU efficiency. They avoid **polling**, where the CPU wastes time constantly checking device status. Interrupts allow the CPU to perform other tasks and only handle a device when it actually needs service, enabling parallelism and fast system response. "translation": "必要性：中断对于CPU效率至关重要。它们避免了轮询，即CPU浪费时间不断检查设备状态。中断允许CPU执行其他任务，并且仅在设备实际需要服务时处理它，从而实现并行性和快速系统响应。
- **Hardware Interrupt Function**: **Keystroke Handling**. A key press generates an interrupt, causing the CPU to run a routine to read the character from the keyboard. 硬件中断功能：按键处理。按键产生中断，导致CPU运行一个例程从键盘读取字符。
- **Software Interrupt Function**: **File Access**. A program executes `INT 21h` (in DOS) to ask the OS to read a file from the disk on its behalf. : "软件中断功能：文件访问。程序执行`INT 21h`（在DOS中）请求操作系统代表它从磁盘读取文件。

When entering an interrupt service routine (ISR), contents of registers are normally pushed onto the stack, and retrieved only at the end of the ISR. Briefly explain why this is done

程序在恢复运行时，其所有的工作状态都和被中断前一模一样，因此能够无缝、正确地继续运行 When the program resumes execution, all its working states remain exactly the same as before the interruption, allowing it to continue running seamlessly and correctly.

门电路

Edge-triggered vs. Level-triggered D Flip-flop

- **Level-triggered (Latch)**: Output `Q` follows input `D` as long as the clock is at an active *level* (e.g., high).
- **Edge-triggered**: Output `Q` updates to `D` only at the *instant* of a clock's rising or falling *edge*.

The registers in 8086 are 16-bit long, but the address bus is 20-bit long. How does the 8086 generate the addresses for data, code and stack from the 16-bit registers?

cs*16+ip