**SEMESTER 2**
**2021-2022**

# CS253FZ
# Computer Architecture 2

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Time allowed: 2 hours

Answer ***four*** questions
Complete question 1, which is worth 40 marks. Choose 3 from the remaining 4 questions, each of which is worth 20 marks.

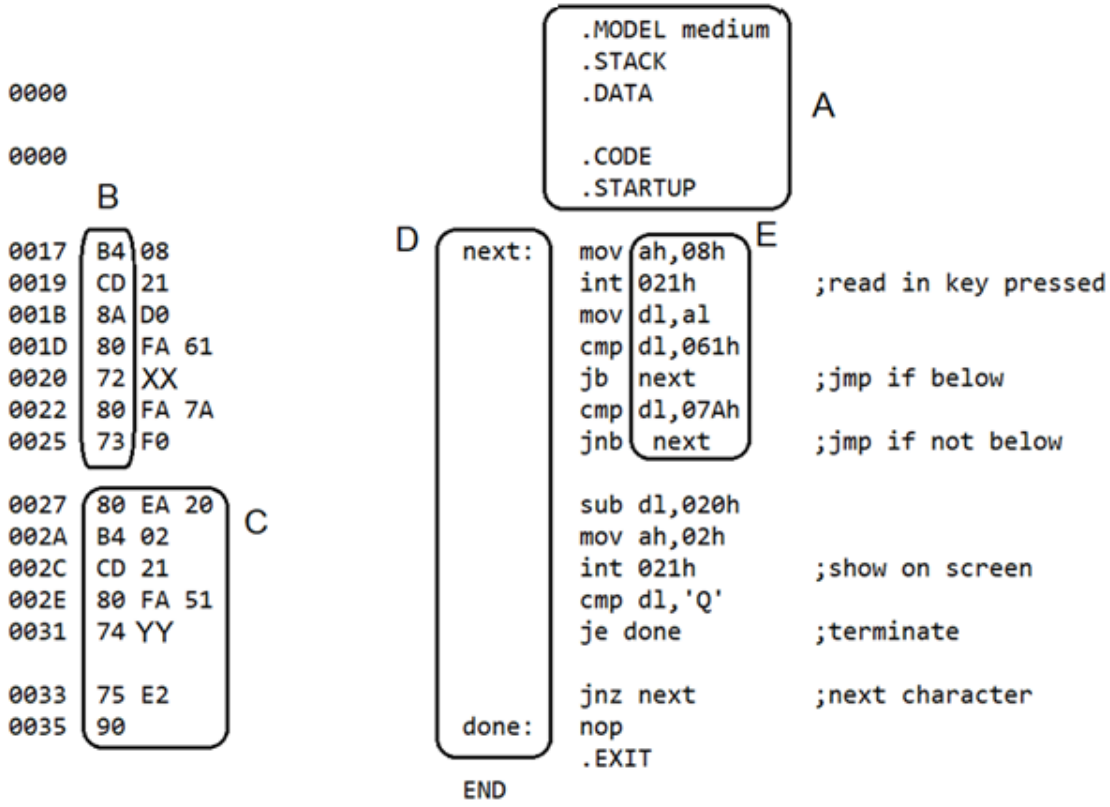
Instructions

| | Yes | No |
|---|---|---|
| Log Books allowed | | X |
| Formula Tables allowed | | X |
| Other allowed *(enter details)* Scientific calculator | X | |

| |
|---|
| General *(Enter Details)*<br><br>An ASCII Table is provided at the end of the paper. |

## QUESTION 1

Parts (a) to (e) refers to the assembly listing shown below.




(a) Match the following: assembler directives, labels, machine instructions, operators, and operands to the items in the boxes (5 marks)
(i) A (ii) B (iii) C (iv) D (v) E

(b) What is the main difference between mnemonics and opcodes? (5 marks)

(c) If the following keys are typed when the programme is running: (5 marks)
abc123PQR@#$pqr
show what will appear on the screen.

(d) The hexadecimal values in locations 21h and 32h have been replaced with XX and YY. Write out these values. (5 marks)

(e) Suppose the CS contains 12EFh. What is the starting address in main memory of the instruction cmp dl, 'Q' ? (5 marks)

(f) Explain the main difference between an edge-triggered and a level-triggered D flip-flop. (5 marks)

(g) (i) Give three differences between static and dynamic memory. (5 marks)
(ii) How does caching help to speed up execution of programmes?

(h) (i) What is the difference between ROM and PROM? (5 marks)
(ii) What is the difference between PROM and EPROM?
(iii) What is the difference between EPROM and EEPROM?

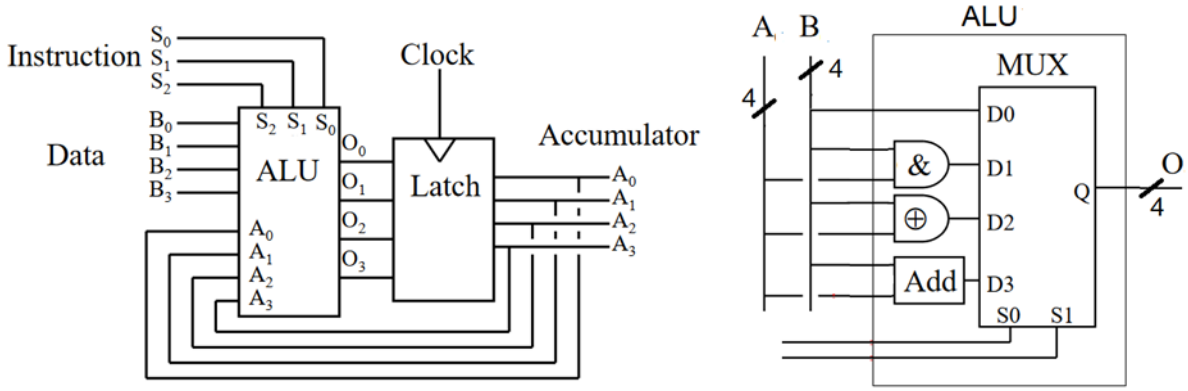
## QUESTION 2

A simple 4-bit CPU consists of an ALU made up of the multiplexer shown below. It uses only one register, the Accumulator A. It can take one operand B using two addressing modes: immediate and direct. Immediate means that the operand follows the opcode and direct means that the operand is pointed out by the address which follows the opcode. The difference is encoded by the bit S2, with 1 meaning immediate and 0 meaning direct.

The 4 actions available are LOAD, which loads the accumulator, ADD which adds operator B to the accumulator A, AND which does a logical 'and' between B and A, XOR, which does a logical 'xor' between A and B and ADD, which adds A and B ignoring any carry. The result is put back into the accumulator.

A load immediate 5 instruction looks like: LOAD 5h

An ADD direct A instruction looks like: ADD @Ah




(a) (i) How many bits does each instruction require? (4 marks)
(ii) How many memory locations can this CPU address directly?

(b) Obtain the machine code in hex for: XOR @8 (4 marks)
AND 9

(c) Suppose the memory locations 0, 1, 2, 3 and 4 contain the values 5, 6, 7, 8, 9 respectively. What is stored in the accumulator after the CPU has executed the following code segment? (6 marks)
LOAD @3
ADD 5
XOR @0

(d) Write a few lines of code that will calculate the two's complement of the number 7. (6 marks)

## QUESTION 3

Intel CPU's can handle different types of data, such as byte, string, integer and floating-point numbers. For numbers, Intel CPU's use the little-endian convention of storing data in memory.

(a) Briefly explain the main difference between big and little-endian conventions of data storage. (3 marks)

(b) Determine how the 8086 stores the real value 6.75 in short real format. (5 marks)

(c) The following block of code is used to provide data to an 8086 assembly language programme. The offset address pointed to by the label 'num' is 1000h. (8 marks)

```
        .DATA
num     dw      1025
num2    dd      6.75
num3    byte    77o
str     byte    '123abCD$'
```

| Memory contents | Offset address |
|---|---|
| | FFFFh |
| | …. |
| | 1001h |
| | 1000h |
| | 0FFFh |
| | …. |
| | 0000h |

Fill in the contents of the memory from location 1000h.

(d) The registers in 8086 are 16-bit long, but the address bus is 20-bit long. How does the 8086 generate the addresses for data, code and stack from the 16-bit registers? (4 marks)

## QUESTION 4

The 8086 CPU has three types of interrupts, hardware, software and exceptions.

(a) What is the difference between these three types of interrupts? (6 marks)

(b) Why are interrupts necessary for the proper functioning of the CPU? Give one function each for hardware and software interrupts. (4 marks)

(c) When an interrupt occurs, explain briefly the actions taken by the CPU. (5 marks)

(d) There are only 2 pins on the 8086 for hardware interrupts, namely NMI and INTR. Explain how the 8086 can allow for interrupts from more than two external sources, for example, from the keyboard, the printer, and the serial communication port. (5 marks)

## QUESTION 5

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are used in the fabrication of most semiconductor devices.

(a) Sketch the structure of an n-channel MOSFET, marking clearly metal, oxide, n-doped, p-doped and silicon parts. (5 marks)

(b) Explain how well each of the following materials support the flow of current in terms of charge carriers and energy bands: (10 marks)
(i) metal
(ii) oxide
(iii) n-doped silicon
(iv) p-doped silicon
(v) pure silicon

(c) Tri-state devices made from CMOS inverters are needed to connect input and output lines to data buses. Explain how these tri-state devices function, and what can happen if they are not used. (5 marks)

## ASCII Table

| Hex | Value | Hex | Value | Hex | Value | Hex | Value | Hex | Value | Hex | Value | Hex | Value | Hex | Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | NUL | 10 | DLE | 20 | SP | 30 | 0 | 40 | @ | 50 | P | 60 | ` | 70 | p |
| 01 | SOH | 11 | DC1 | 21 | ! | 31 | 1 | 41 | A | 51 | Q | 61 | a | 71 | q |
| 02 | STX | 12 | DC2 | 22 | " | 32 | 2 | 42 | B | 52 | R | 62 | b | 72 | r |
| 03 | ETX | 13 | DC3 | 23 | # | 33 | 3 | 43 | C | 53 | S | 63 | c | 73 | s |
| 04 | EOT | 14 | DC4 | 24 | $ | 34 | 4 | 44 | D | 54 | T | 64 | d | 74 | t |
| 05 | ENQ | 15 | NAK | 25 | % | 35 | 5 | 45 | E | 55 | U | 65 | e | 75 | u |
| 06 | ACK | 16 | SYN | 26 | & | 36 | 6 | 46 | F | 56 | V | 66 | f | 76 | v |
| 07 | BEL | 17 | ETB | 27 | ' | 37 | 7 | 47 | G | 57 | W | 67 | g | 77 | w |
| 08 | BS | 18 | CAN | 28 | ( | 38 | 8 | 48 | H | 58 | X | 68 | h | 78 | x |
| 09 | HT | 19 | EM | 29 | ) | 39 | 9 | 49 | I | 59 | Y | 69 | i | 79 | y |
| 0A | LF | 1A | SUB | 2A | * | 3A | : | 4A | J | 5A | Z | 6A | j | 7A | z |
| 0B | VT | 1B | ESC | 2B | + | 3B | ; | 4B | K | 5B | [ | 6B | k | 7B | { |
| 0C | FF | 1C | FS | 2C | , | 3C | < | 4C | L | 5C | \ | 6C | l | 7C | \| |
| 0D | CR | 1D | GS | 2D | - | 3D | = | 4D | M | 5D | ] | 6D | m | 7D | } |
| 0E | SO | 1E | RS | 2E | . | 3E | > | 4E | N | 5E | ^ | 6E | n | 7E | ~ |
| 0F | SI | 1F | US | 2F | / | 3F | ? | 4F | O | 5F | _ | 6F | o | 7F | DEL |