CS253Architectures III

Lecture 15

Buses

Buses

A bus is a shared set of communication lines that connect different components of the computer and the standard to use it.

Intrasystem communication: Connection of various components inside the computer distances less than a meter.

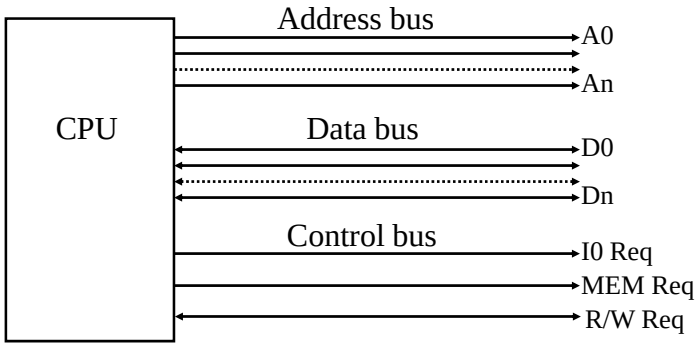
Implement by large groups of parallel data lines called buses.

Intersystem communication: Connection between computer and distant hardware.

Normally achieved using a serial link.

Serial is chosen for cost and reliability.

Typical Computer Bus



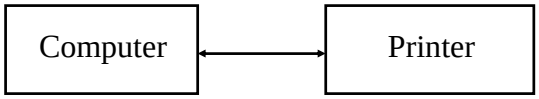
Address Bus: When the computer wishes to read/write to memory or an IO device the address bus specifies the location to be accessed. It is output only.

Data Bus: A bi-directional bus that carries data to and from the CPU.

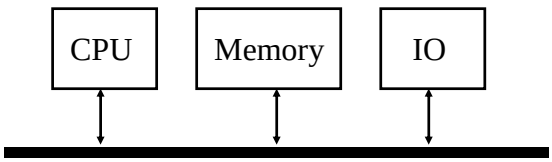
Control Bus: A group of input/output lines that control the sequence of events during the read/write operations.

Interconnection Structure

Dedicated bus structures connect just two devices together



Shared bus structures use the same data path at different times.



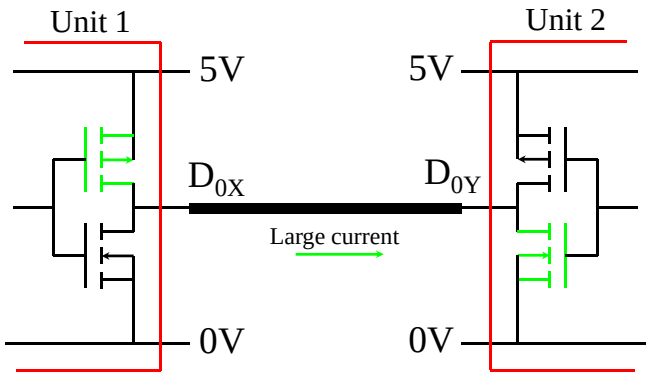
Contention

Unidirectional buses such as the address bus on the computer are simple to implement. The CPU produces the address all devices monitor the address lines.

Some buses such as the data bus are required to carry data in both directions. For example the data bus connects memory to the CPU, that data flow is in both directions (Read/Write).

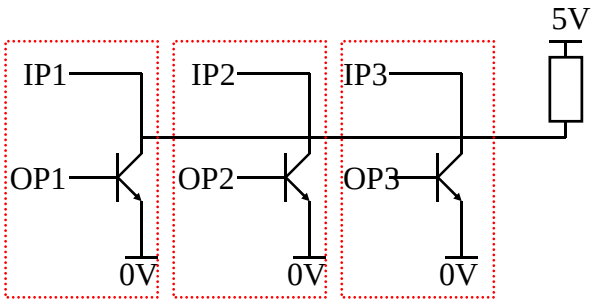
If two outputs are ever connected together the result is known as contention. At best this will cause ambiguous data to be produced at worst it could damage the bus or memory.

Contention and CMOS



If ever D_{0X} is not equal to D_{0Y} then large currents start flowing through transistors and failure can occur.

Current sinking logic



The outputs of the devices are effectively ORed together.

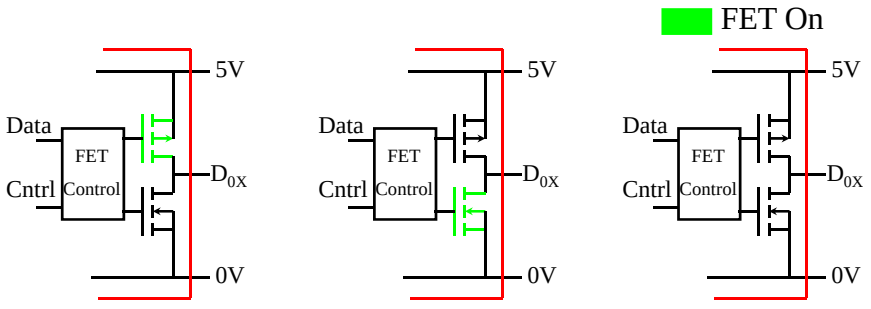
Each unit can read the data line.

If there is contention no damage occurs since resistor limits the current.

Problems: Very slow (no active pull high)

Wastes power.

Tri-State



Logic High Logic Low Disconnected

Tri-state devices use a second control line to disconnect the unit from the bus. The disconnected state has a high input impedance preventing contention.

Bus Timing

At any one moment in time only one device can send data, all others must listen or ignore the data. The sending the control information is known as the master other units are known a slave.

Buses create bottlenecks.

Synchronous buses contain a clock signal that allows each item to be transferred in a time slot known in advance to both master and slave. Very fast data rates possible. However system becomes as slow as the slowest device on the bus.

Asynchronous bus contain no clock signal, each item to be transferred is accompanied by a set of control signal that sequence the transfer. This sometimes involves handshaking.

Bus Arbitration Hardware

Different devices may wish to use the bus at the same time.

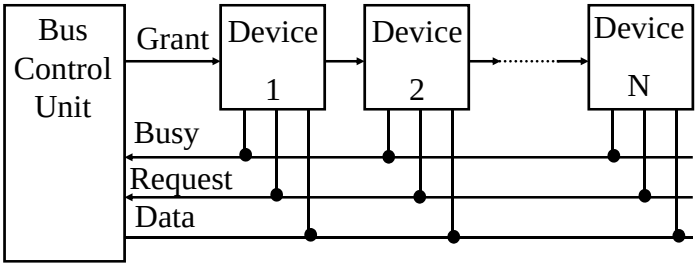
Bus Arbitration is used to avoid conflicts or contention on the bus.

Daisy Chaining

Polling

Independent Requesting

Daisy Chaining



When Request is high one of the devices wishes to use the bus.

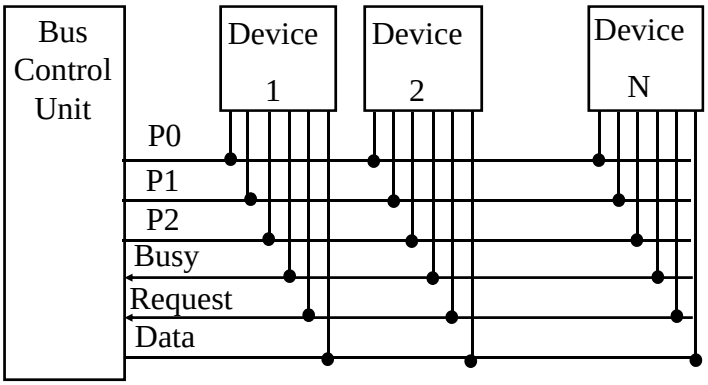
If Busy is high the controller ignores the request.

If Busy is low the controller sends a Grant signal to a specific device.

The device sets busy high and puts data on the Bus.

Examples: Parallel Printer Port used with ZIP drive.

Polling



Grant lines are replaced by poll count lines

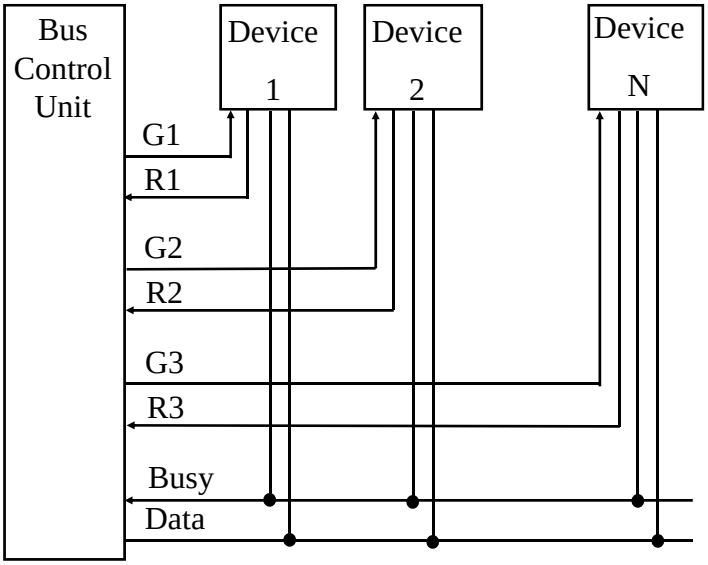
On receiving a request.

Control unit cycles through poll lines, looking for active unit.

Busy busy signal goes high and the data lines are connected.

Priority set by polling sequence.

Independent requesting



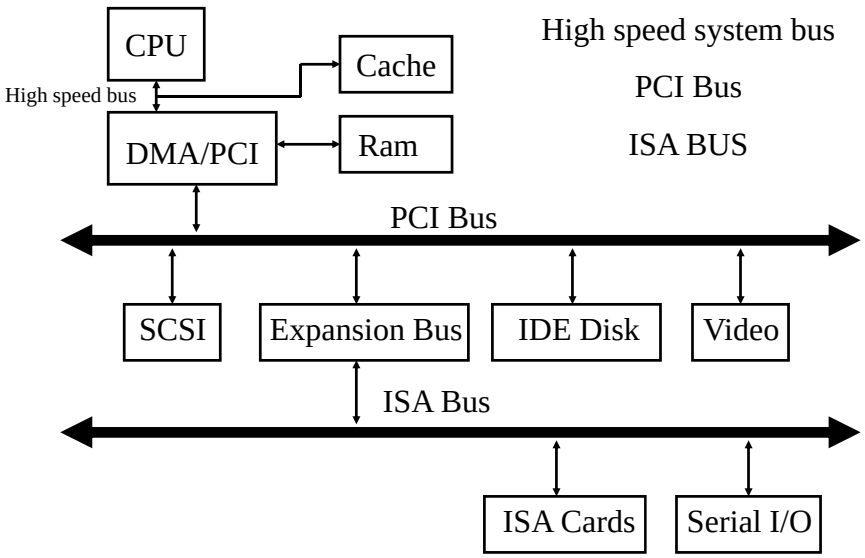
Independent requesting

Separate Bus lines for Request and Grant on each peripheral unit.

Priority controlled by the bus control unit.

Disadvantage is the complexity, requires separate request and grant lines for each unit.

PC Buses



PC Buses

ISA: Industry Standard Architecture, released in 1984 it is still popular due to the large number of peripheral available that use it.

Originally an 8 bit bus that ran at 4.77MHz.

Expanded to 16bit 8MHz.

16 bit peripheral make use of the full ISA connector.

8 bit peripheral use only the first half.

PC Buses

PCI: Peripheral Component Interconnect Bus was released in 1993 and is now the most popular I/O bus.

It is 32 bits wide and runs at 33MHz. The PCI controller manages bus arbitration and control.

The PCI standard extends beyond the PC world.

PCI has been used to implement Plug and Play.