Lab 1: Introduction to Verilog HDL

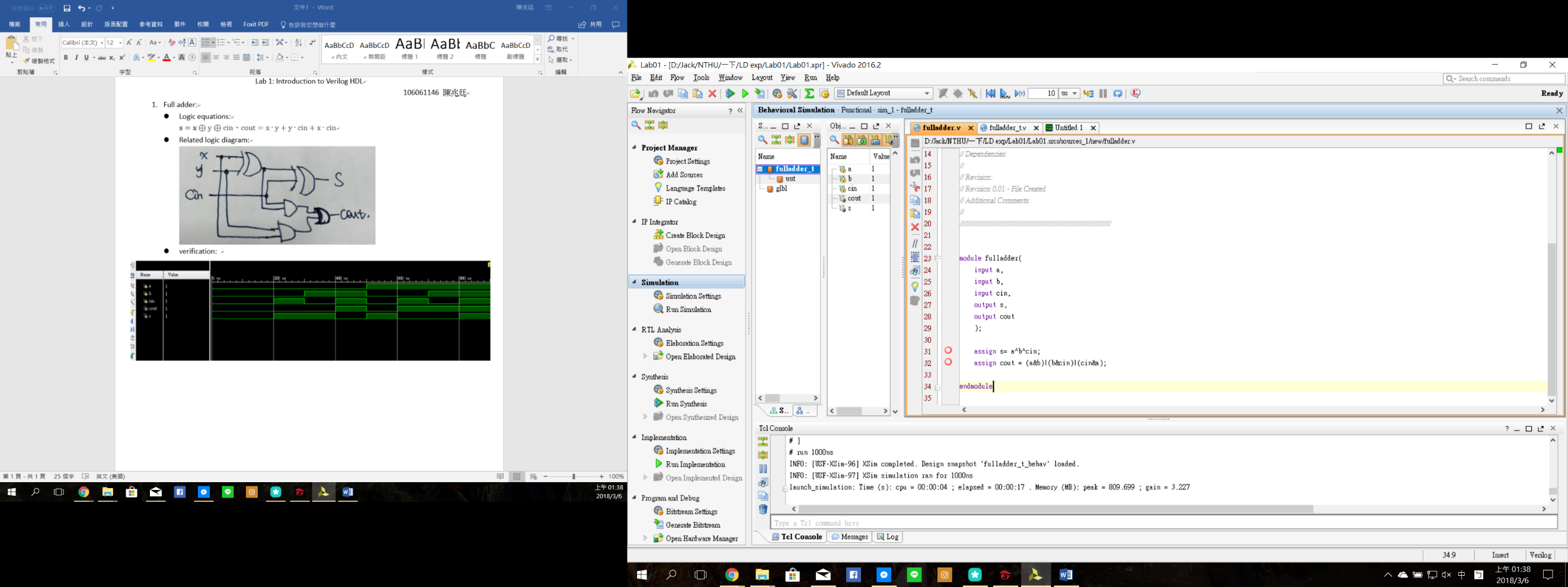
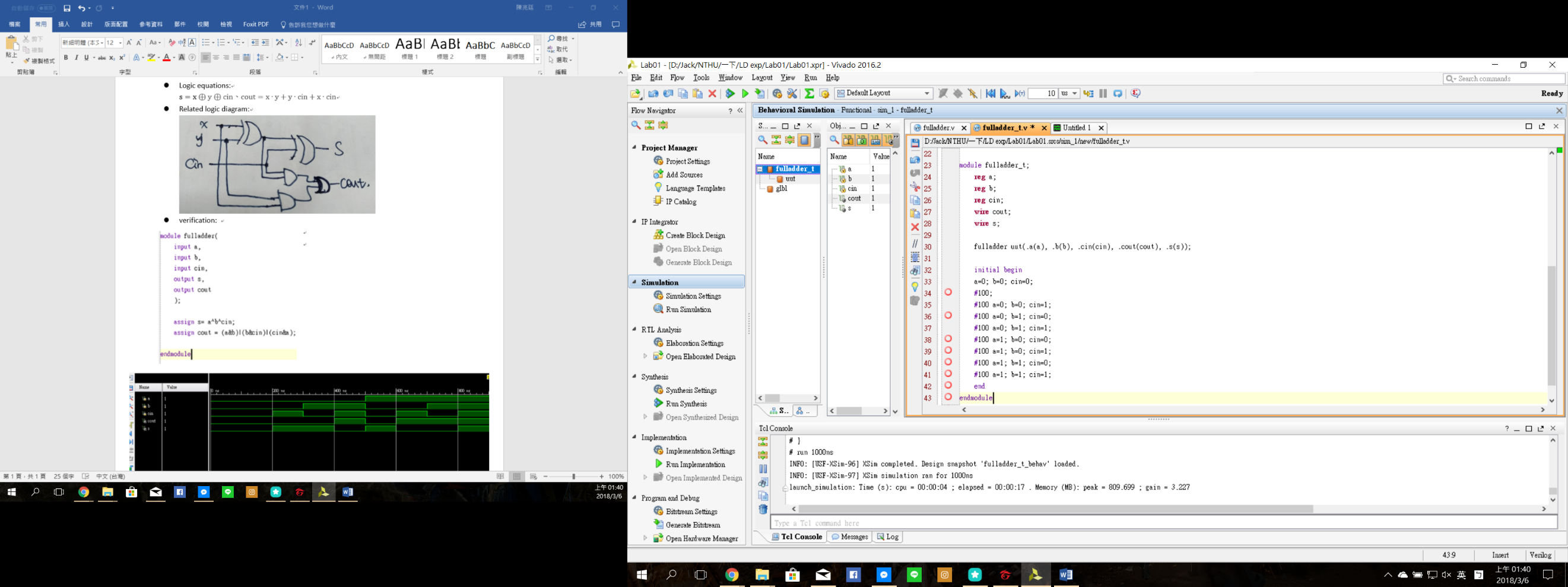
106061146 陳兆廷

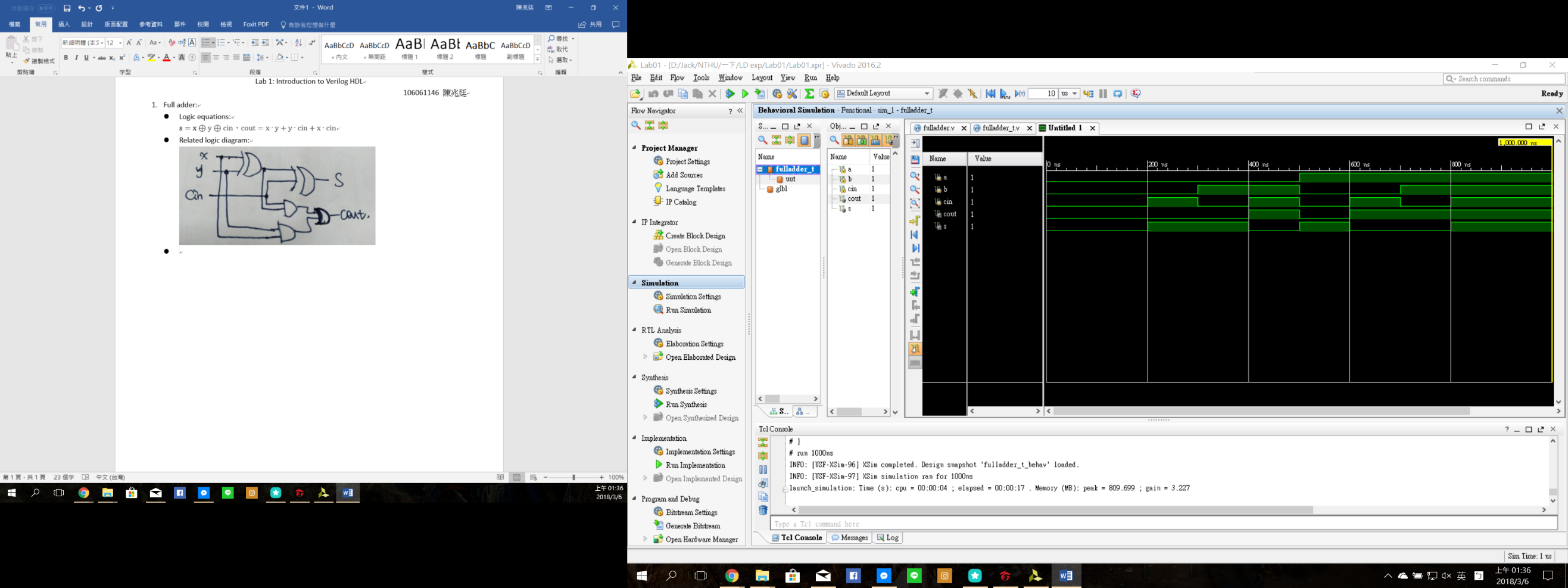
1. Full adder:

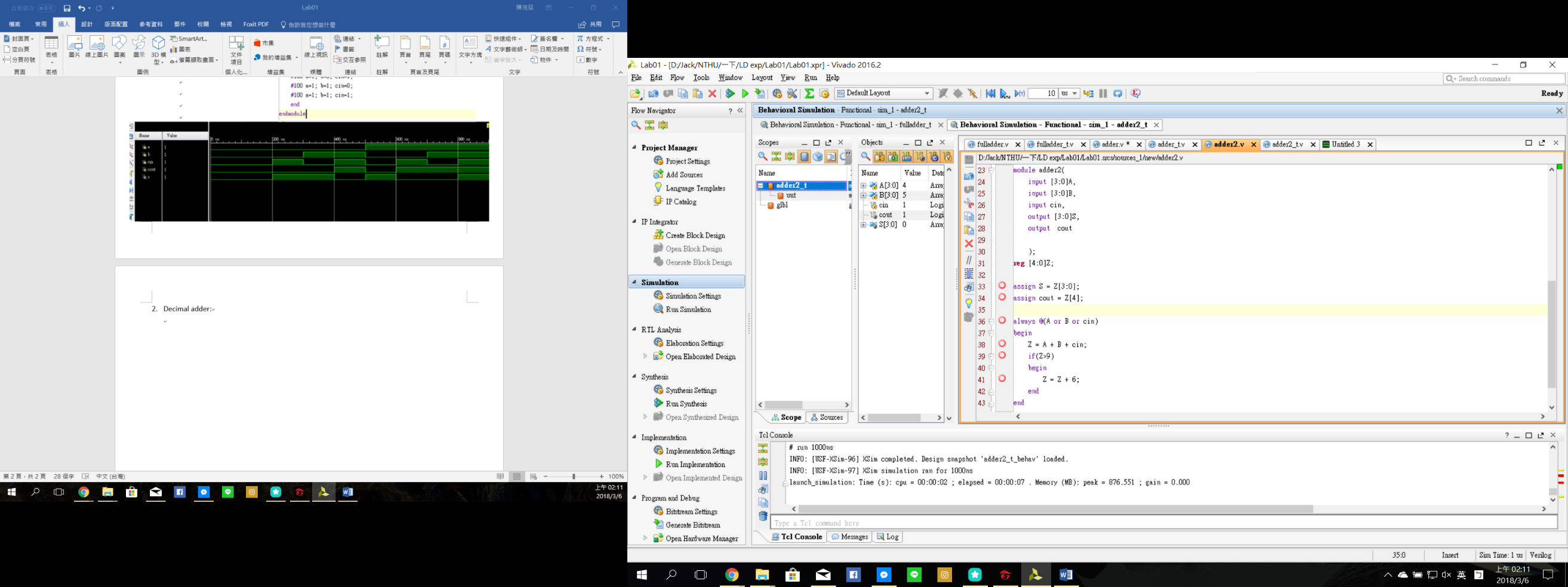
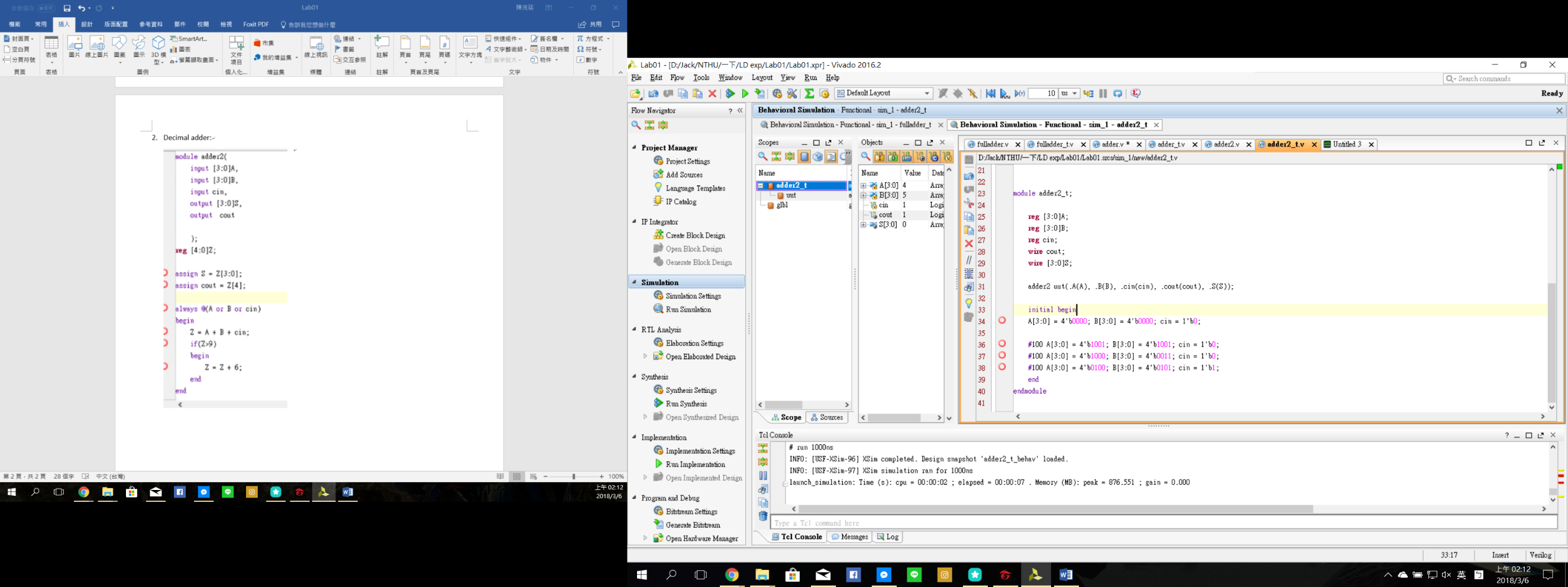
* Logic equations:

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* 一張含有 文字, 白板 的圖片

  描述是以非常高的可信度產生Related logic diagram:
* verification:

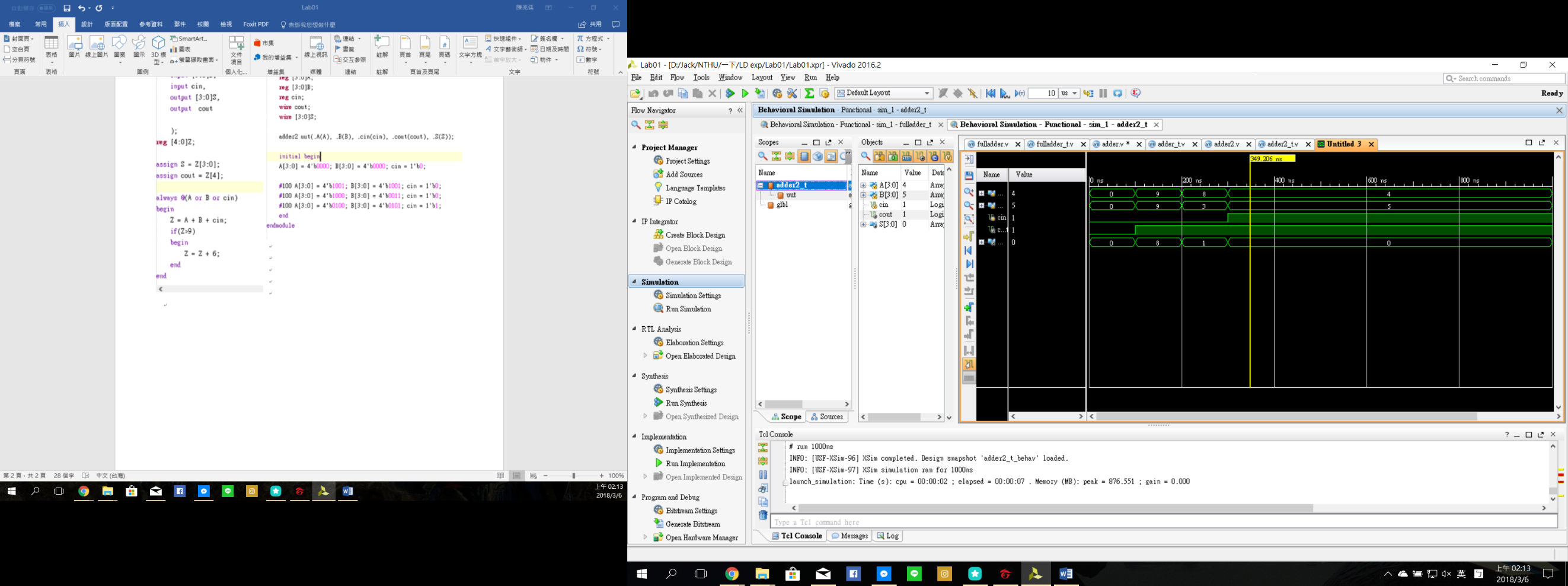


1. Decimal adder:

測試值：9+9=18

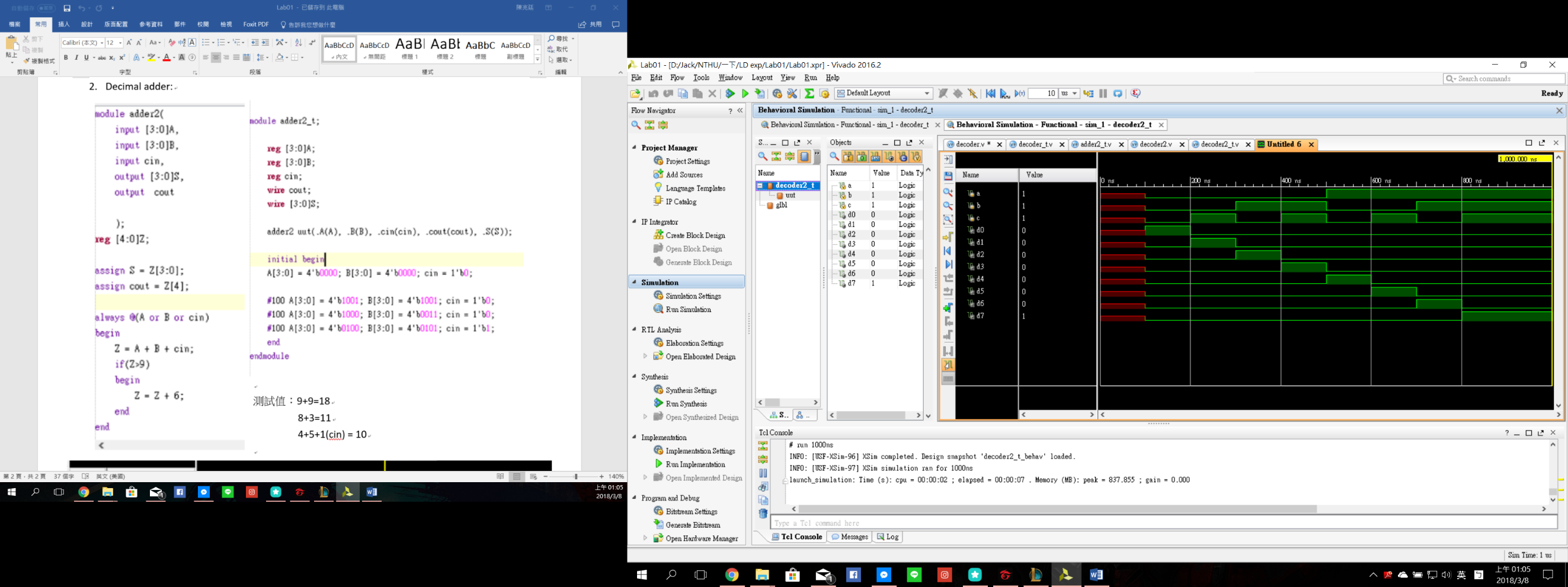
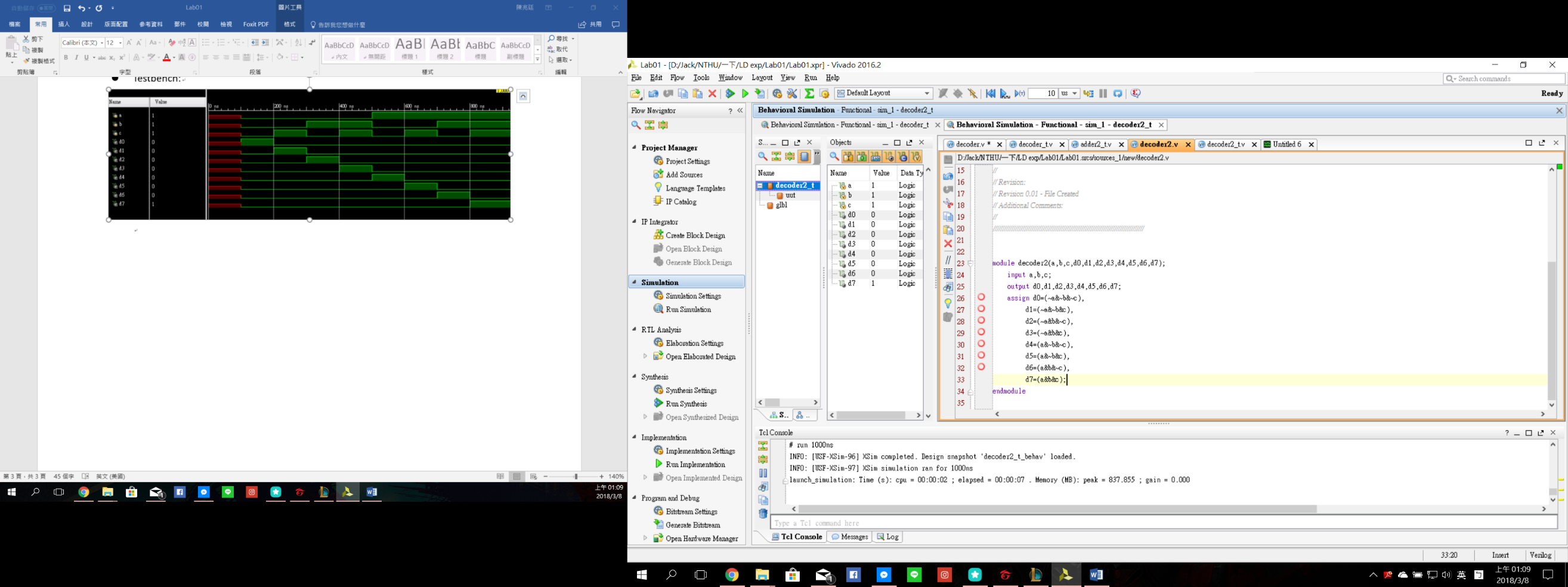
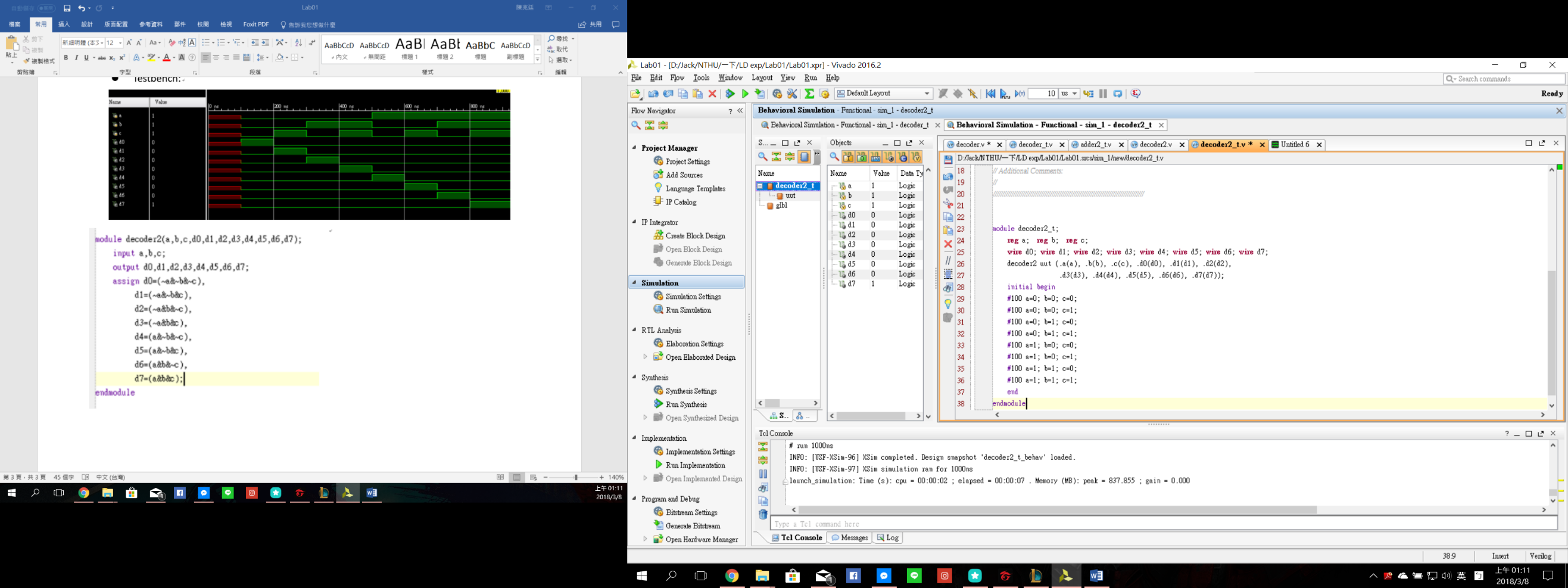
8+3=11

4+5+1(cin) = 10



Bonus:

* 一張含有 文字, 白板 的圖片

  描述是以非常高的可信度產生Logic equations and diagrams:
* Testbench: