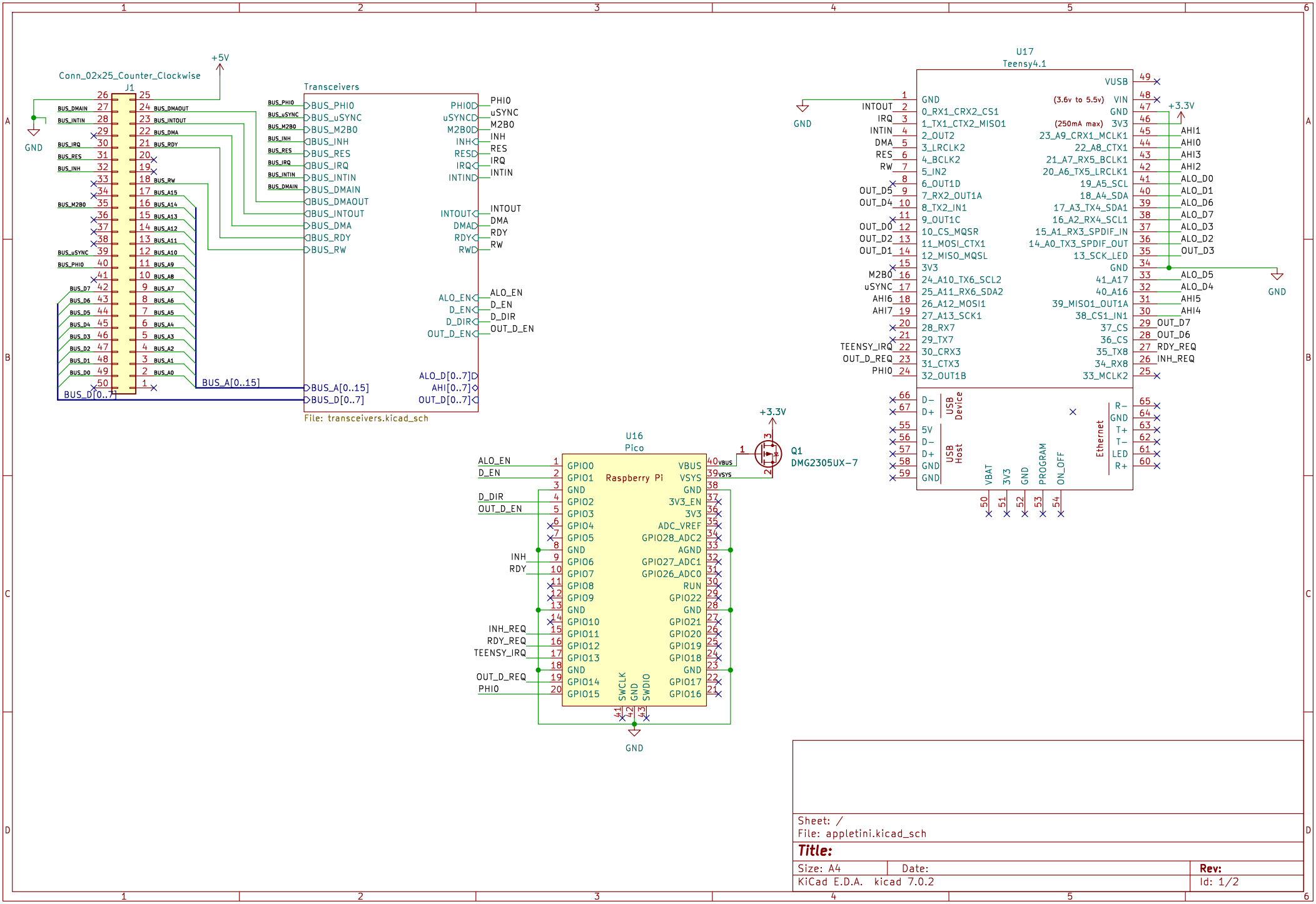

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We don't do DMA, so we run DMAIN directly to DMAOUT.

BUS_DMAOUT — BUS_DMAIN

Low byte of address. This gets muxed onto the same Teensy pins as data.

High byte of address. This doesn't get muxed so it is always enabled.

BUS_uSYNC

BUS_A[0..15]

U1 74LS245 — ALO_D[0..7]

U2 74LS245 — AHI[0..7]

R5 10K — ALO_EN

U5 74LVC1G07 — R1 10K — INTOUT — BUS_INTOUT

U6 74LVC1G07 — R2 10K — INH — BUS_INH

U7 74LVC1G07 — R3 10K — IRQ — BUS_IRQ

U8 74LVC1G07 — R4 10K — RDY — BUS_RDY

Data transceiver, which is bidirectional. This either brings the data byte in, muxed on the same pins as the high address byte, or writes the contents of the OUT data transceiver onto the bus.

OUT data transceiver. When a data byte write happens, the byte is put onto this transceiver and enabled out onto the bus.

BUS_D[0..7] — U3 74LS245 — ALO_D[0..7] — U4 74LS245 — OUT_D[0..7]

D_DIR — R7 10K — D_EN

R9 10k — R8 10K — OUT_D_EN

U9 74LS245 — BUS_INTIN, BUS_DMA, BUS_RES, BUS_RW, BUS_M2B0, BUS_uSYNC, BUS_PHI0 — INTIN, DMA, RES, RW, M2B0, uSYNC, PHI0

C1 0.1uF, C2 0.1uF, C3 0.1uF, C4 0.1uF, C5 0.1uF

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