ECE 363

Logic and Computer Design

ECE 363: LOGIC AND COMPUTER DESIGN

Design Project V: Pipelined Controller

Due: March 25

For this project, you will design a Controller for a Pipelined Processor.

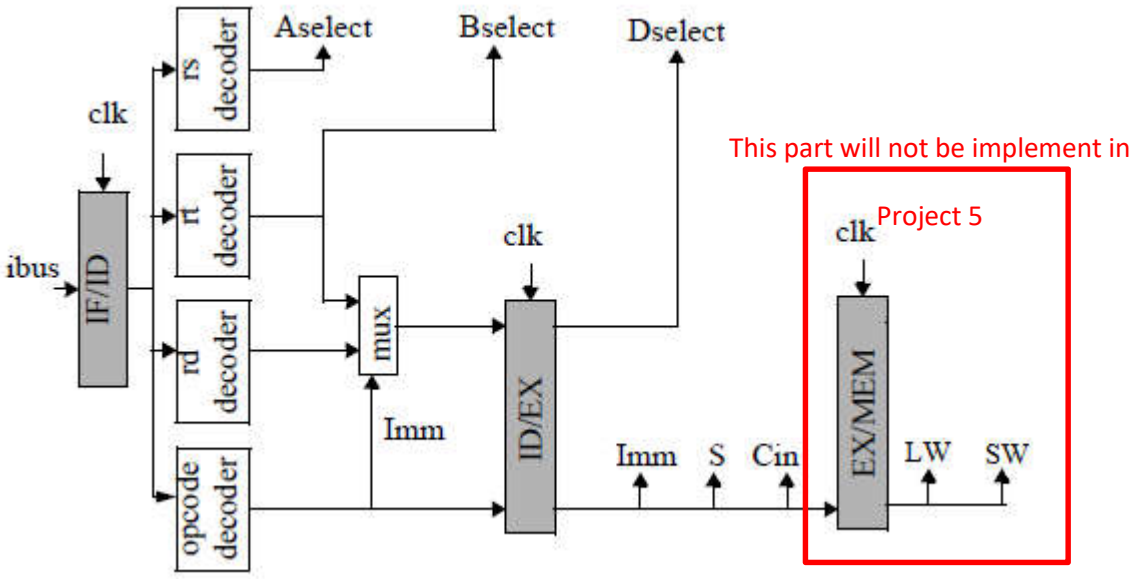

Fig 1.

R-Type

op	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

I-Type

op	rs	rt	imm
6 bits	5 bits	5 bits	16 bits

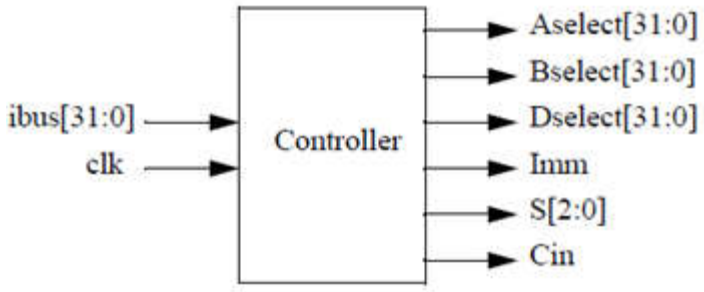

Fig 2.

Subset of instruction codes to be implemented.

Code	Function	Name	Format
000011		ADDI	I
000010		SUBI	I
000001		XORI	I
001111		ANDI	I
001100		ORI	I
011110		LW	I
011111		SW	I
000000	000011	ADD	R
000000	000010	SUB	R
000000	000001	XOR	R
000000	000111	AND	R
000000	000100	OR	R

S[2:0]	ALU FUNCTION
000	A XOR B
001	A XNOR B
010	**A ADD B**
011	**A SUB B**
100	A OR B
101	A NOR B
110	A AND B
111	0

The contents of the instruction register must be decoded to provide all of the control inputs. Binary decoders can be used to produce the Aselect, Bselect and Dselect inputs for the register file from the operand fields in the instruction register. Write the logic equations for the opcode decoder logic so that the control lines are correct for each instruction. Make sure that the control lines go through the appropriate pipeline registers before connecting to the control points. The controller design should be similar to Fig. 1.

The mux is needed because the destination register is in the rd field for R format, but in the rt field for I format. The mux control is the "Imm". To facilitate testing of your design, the IF/ID register inputs will be connected to the instruction bus which will be made available as an external terminal. Your highest level should be named **Project5** and should have the terminals shown in Figure 2.