ECE 363

Logic and Computer Design

ECE 363: LOGIC AND COMPUTER DESIGN

Design Project 6: 3 Stages 32 Bit Pipelined CPU

Due: April 8

For this project, you will design a complete 3 stage, 32 bit pipelined CPU.

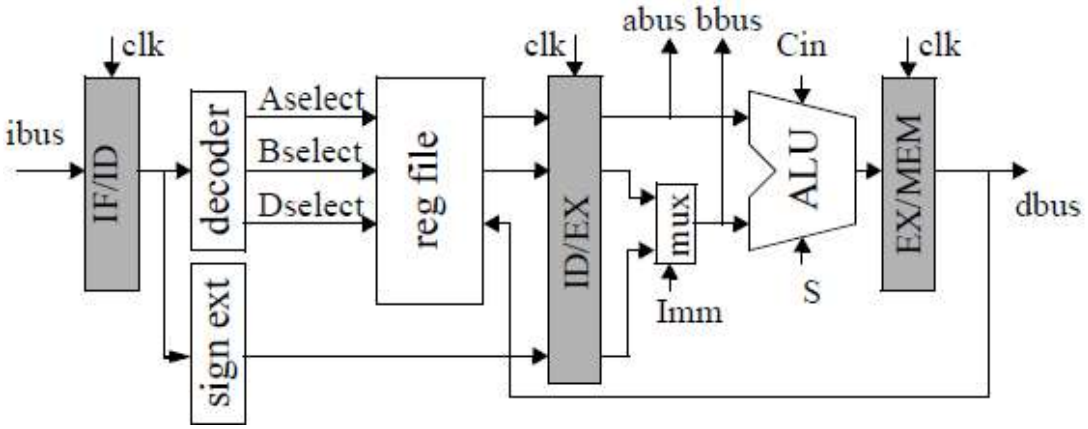

Fig 1: 3 Stage Pipeline Block Diagram

Very Important: Make sure that the **opcode decoder** has the same delay i.e. Imm, S and Cin all are inside the same always block.

Connect the ***controller from Project 5 or design a new pipeline*** as shown in Figure. 1. The ***controller*** should include Aselect, Bselect and Dselect decoders. The controller also provides the control inputs, Imm, S and Cin.

The data path consists of a register file and ALU. You will also need to add:

1. The sign extension logic which extends the lower order 16-bits of the instruction to 32 bits, and
2. A MUX on the ALU B-input such that the sign extension output is selected for I format.

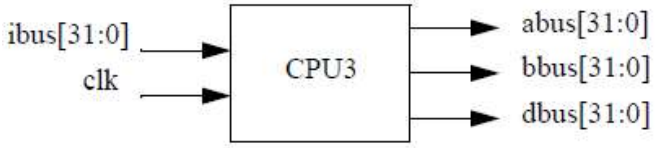

Fig 2: Controller Design

Each instruction will stay on the ibus for one clock cycle. It is acceptable for all of the registers in the register file to remain undefined until something is clocked into them. To facilitate testing of your design, the IF/ID register inputs will be connected to the instruction bus which will be made available as an external terminal. Your design should have terminals as shown in Figure 2.