

CSCE 312 Lab manual

Lab-2 - Combinational logic design

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Chapter 3: Combinational logic design

In the last chapter we understood the usefulness of basic logic gates (example – TTL gates) in designing simple digital applications. In this chapter, we focus on the designing combinational digital circuits for similar applications. The idea is to learn how to apply Boolean logic theories in designing digital circuits to solve real-life problems.

1. Learning duration: 1 week. **Required Tools:** Logisim 2.5.x

2. Objective:

To learn -

Primary topics

1. How to design combinational digital circuits using logic gates.
2. What are the basic design considerations in designing combinational circuits.
3. How to identify and choose the required chips to implement the designed circuits.
4. How to test combinational circuits.
5. How to optimize the design using larger gates.

Secondary topics

6. To get familiar with TTL chips and their data sheets.
7. Develop of an engineering understanding about which data sheet parameter to use.
8. Familiarity of a simple GUI based digital circuit design and simulation tool

3. Instructions:

The following instructions are good for next few chapters and labs -

1. You will use the freeware software tool named “Logisim” to design and verify the digital circuits.
2. This tool is available for download from <http://ozark.hendrix.edu/~burch/logisim/> . Documentation for Logisim is available on the same website. See <http://ozark.hendrix.edu/~burch/logisim/docs/> for the documentation. You should have already installed the tool during the first lab session. If you haven't please do so at this time.
3. Use the Logisim tool to do all the problems of this chapter. You will have all the required gates, LED, 7 segment display, push button switch, memory, clock, sequence generator, etc. in the tool. Explore the tool by yourself to see what all circuit components are available and how to use them. If you get stuck using the software, contact your TA.
4. You can print the drawn circuits from this tool. For electronic submission of the circuit submit the completed Logisim file in itself.
5. Logisim does not at this moment create timing diagrams. To create timing diagrams you can use software such as Microsoft Visio or even Powerpoint. Also ask your TA if he/she

has better recommendations for software to create timing diagrams. Submit timing diagrams by inserting the appropriate figure into your report.

6. Use push button switches and attach them to the input lines whose logical states you want to change for testing. Logic states of the input lines can be changed simply by pushing the corresponding switches. Use LED's to monitor the logic states of individual lines. A glowing LED indicates 1/true state.
7. As a good design practice run parallel wires (called a bus) of all the input variables and their inverses (NOT of the variables) and then tap these to feed the input of the gates. It is possible to mark the wires, switches with names typed beside them.
8. Some problems are similar to home work 1, submit these at both places (as your HW1 and also as your Lab 2) separately.

4. Useful resources:

1. Chapter 1, 2 of Frank Vahid's "Digital Design" or the first few chapters of any digital circuit/design/architecture book by Morris Mano (available in TAMU library).
2. About TTL logic – http://en.wikipedia.org/wiki/Transistor-transistor_logic
3. About 74xx series logic family - http://en.wikipedia.org/wiki/7400_series
4. List of all 74xx series logic gates (this would be useful to identify which gates you would like to use) - http://en.wikipedia.org/wiki/List_of_7400_series_integrated_circuits or <http://rabbit.eng.miami.edu/info/datasheets/>
5. To obtain data sheets for the logic gates use - <http://rabbit.eng.miami.edu/info/datasheets/> or <http://www.alldatasheet.com/> . You can also google for the required data sheet if you know the 74xx series chip name.
6. 7 segment display data sheet is available here - <http://rocky.digikey.com/WebLib/Panasonic/Web%20data/LN516GA,GK,RA,RK.pdf>

5. Exercises to do

5.1 Problem 1:

Activities to do-

1. Using one and two input gates draw and verify the digital circuit for the functions. Do not simplify/reduce the equations.
 - a. $F = abc + ab + a + b + c$
 - b. $G = a'b'c + ab'c + abc$
2. What are the names of the 74xx series logic gates that you should use to do the above problem in real-life situation?
3. Calculate the delay performance (time delay between change of any input which leads to change of the output) of the two circuits designed above. Assume that you have used 74Fxx or 74LSxx series gates to implement the circuit. Use respective data sheets for the required chips.
4. Which data sheet parameter(s) did you use to calculate the delay performance and why?

Notes:

1. Circuit delay is the delay of the longest path in the circuit from input to output. If your longest path had 3 gates, then the sum of the individual delays make up the delay of the circuit.
2. In the data sheet, the delays reported are for individual gates. It does not matter if the package has 4 gates in it or 6 gates in it- the delay reported in the datasheet is for one gate.

5.2 Problem 2:

New York's Metropolitan Transport Authority (MTA) operates the subway transport facility in New York. Each subway train consists of 6 subway cars all chained together and pulled by a motored subway car at the front end. (6 + 1 motor car in total) To improve the security of passengers, MTA decided to install a switch inside every subway car. A passenger can press this emergency switch which is there in his/her car to signal the driver that an emergency situation has happened in his/her car. In response the driver will then dispatch security personnel to that particular car, when the car stops at the next station. You are recruited by MTA to develop a digital system to achieve this. MTA's chief wants that when the emergency button is pressed in a particular car, that car's number should be displayed in the driver's dash board. If no button is pressed, the display remains off. You decided to use a **7 segment LED display**, an encoder and a decoder built by TTL chips, to design and implement this system. The functional diagram of the system is given below –

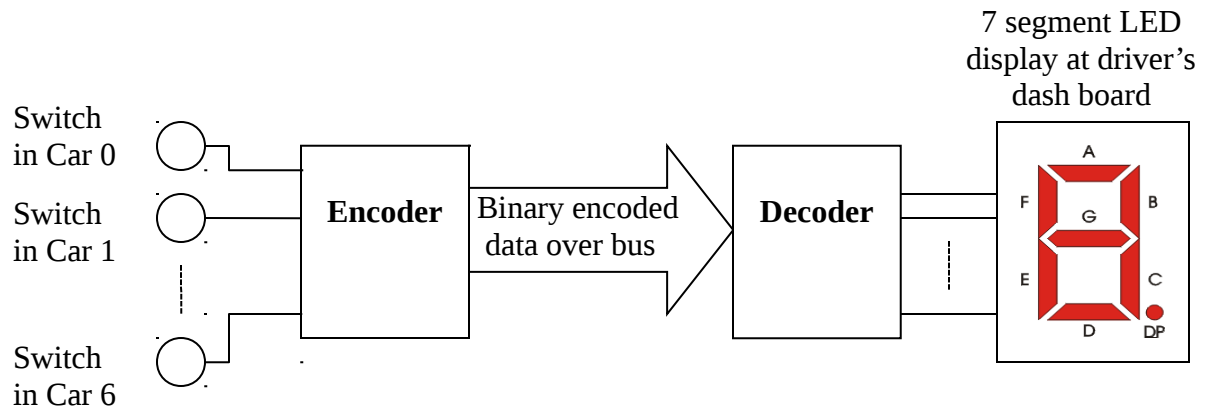


Fig. 1: The functional block level diagram of the proposed digital system

Activities to do-

1. Identify the following design parameters –
 - a. Number of switches that will be required.
 - b. Number of the bits/wires required in the data bus.
 - c. Size of the encoder and decoder.
2. Read one of the 7 segment LED display data sheet, try to understand how to use it.
3. Design the encoder and decoder blocks with basic logic gates then incorporate the same into a complete digital system on Logisim.
4. **Submit your design with a brief text explanation/description on how it will actually work. You must explain the working of your system to get full credit.**