BELOW IS A CHART SHOWING WHEN THE i-DESIGNATOR AND THE 3 BITS OF THE FUNCTION CODE ARE SENT TO THE AR MODULE FOR THESE INSTRUCTIONS 2, 20-7, 40-4, 6.

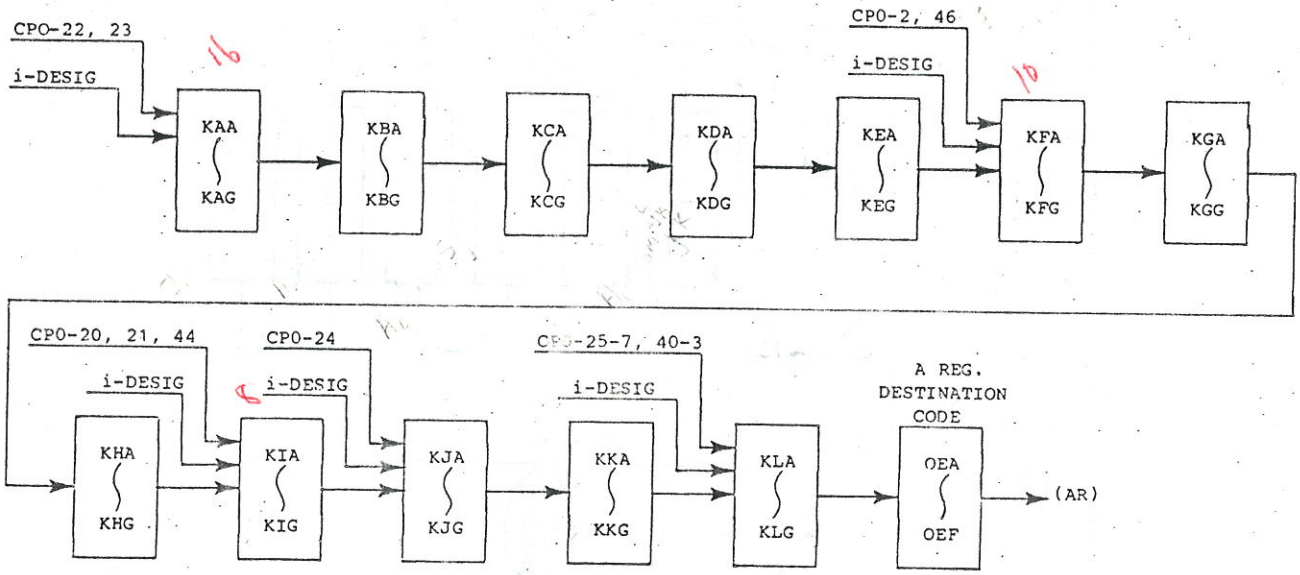
	CP13	CP8		CP5		CP4	CP2	
	22,23	2	46	20,1	44	24	25	26,7 40-3
OEA	X	X	X	X	X	X	X	X
OEB	X	X	X	X	X	X	X	X
OEC	X	X	X	X	X	X	X	X
OED	1	1	0	0	0	1	1	0
OEE	0	0	1	1	1	1	0	0
OEF	1	1	0	1	0	0	0	1

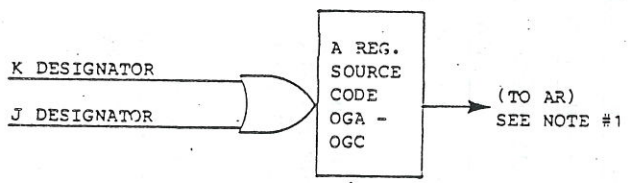
2^0, 2^1, 2^2 } i-DESIG

2^0, 2^1, 2^2 } AR FUNCTION CODE

Delay for Chain how long it takes to do instruction.

A REGISTER SOURCE PATH TRANSLATION -
0 - NO ENTRY
1 - L DATA
2 - LOCAL MEMORY DATA
3 - S REGISTER DATA
4 - CONSTANT DATA
5 - AM MODULE DATA
6 - ADDER DATA
7 - NOT USED





A REGISTER CONTROL (JA MODULE)

NOTE #1: THE THREE BIT SOURCE CODE IS SENT OUT FOR ALL INSTRUCTIONS CP1 OF THE INSTRUCTION INDICATES THE K DESIGNATOR. CP2 OF THE INSTRUCTION INDICATES THE J DESIGNATOR.

A REGISTER TAG DELAY CHAIN