I. Module Testing at Machine Speed.

A. Description of Tester Operation and Procedures.

The Cray 2 module tester is designed and built to run at machine speed, rather than at micro speed. This has been accomplished by the use of data buffers which are loaded or read via a micro, then clocked at machine speed (4.0 nsec) to and from a module under test.

The Tester consists of 8 transmitter synch boards to supply inputs to the module under test, 8 receiver synch boards to record the outputs of the module under test, one master synch board to provide "go gates" to transmitters and receivers and synch pulses to the oscilloscope, and one clock driver board to supply a selectable clock rate and clock divider circuitry.

Each transmitter and receiver is 24 bits wide by 64 bits deep, for a total input and output range of 192 bits wide, and 64 bits - or clock periods - deep (receive buffers can be skewed by an additional 64 clocks to increase their length to 128 clock periods). The transmitter and receiver buffers are designed to be run with a 4.0 nsec clock speed to match that of the Cray 2, with enough headroom for clock margin testing.

To initiate a test step, data is dumped from disk by the micro. Included in this data is the transmitter buffer information, master buffer information, and an expected buffer which is to be compared to the data actually received from the module under test.

The transmitter information is then translated, and loaded one buffer at a time to the tester transmitter buffers. When this has been completed, one of two things can happen. If the module is being run under full power, "go gates" are sent to the transmitter boards and data is dumped to the module at a 4.0 ns clock rate. If the module is being run under pulse power (see section II-B) a "go power pulse" must first be sent to the module power supply to start a power cycle and then the data is dumped to the module at a 4.0 nsec rate.

After a delayed programmed time, "go gates" are sent to the receiver boards which start to capture data from the module under test. At the completion of the receiver boards 64 clock period data window, all synch boards stop. (If under pulse power, the power cycle ends at this time also.) Data from the receivers is then translated and sent to the micro.

This received data is then compared to the expected buffer previously loaded from disk, and any differences are flagged as errors. If no errors are detected, the next test step is read from disk, and the cycle is repeated.