KB MODULE DESCRIPTION

Main area on the KB module:

- Local Memory
- Channel Data Registers
- Real Time Clock

Local Memory

This memory is a 4K x 32 bit memory with parity. It is organized on one bank. Access time is 4 clock periods.

The A or B registers are used as source or result data registers for local memory operations. Addressing for local memory also comes from the A or B registers or it may also be an immediate address from the instruction. Parity errors are flaged to the console.

Channel Data Registers

There is a 32 bit data register for each channel. Data is transferred between the channel data register and the A or B register. Data is also transferred to and from the channel loop. (See channel loop write up)

Real Time Clock

The real time clock is a 32 bit register which increments sequentially for every clock period only a dedstart sequence will clear it out. It can only be read into the A or B register.