II. Internal drawn path times

A. Path times should be 3.90 nanoseconds or less , exceptions see this section items 1,2,3, and 4 .

1. Modules with register and storage chips may have lines drawn over 3.90 n.s. but these lines must be verified good by the Design Engineering Group .
2. Channel modules may also contain long path times but again these are to be verified good by the Design Eng. Group .
3. Design Group must use individual module timing diagrams to determine the length allowable for the module to function correctly for storage chips . (See Appendix A and B)
4. Design path times over 3.90 should be evaluated before being sent to artwork . Generally design times are shorter than drawn

B. The main foil path must not be longer than 9" .

C. At most four loads may exist on the path from a transmitter . (SEE EXCEPTIONS UNDER 42.5 TERMINATION)