MODULE MAPS

The module maps are a layout of a module. Each board on a module is divided into three fields. The first board in the module is the ABC board where A, B, and C are the fields, and the last board is VWX. Each field is divided into four columns and eight rows of chip locations. A 3-character designator heads each location. The first character is the field or board identifier, the second character is the location in the field, and the third character is the chip type that is used.

Underneath each designator are spaces for four Boolean terms. Each of those terms is an output. If only one term appears in the location the chip has or is using only one output. The terms are read from left to right, top to bottom. The first term listed corresponds to the first set of outputs off of the chip. If a chip has more than four sets of outputs, and more than four are used, only the first four are listed.

- KAI

MODULE	JKL BOARD)		Y	FIE	ATION A IN LD K					00.00
JAS	JBS	JCS	JDS	(KAI)	KBK	ксх	KDF	LAK	LBJ	FCF	
SAD	SAL	SBD	SBL	daf dan	ZZA ZZA ZZA ZZA	OAD OED	BAD BCD	had hbd	TAA TAC TAE TAG	TMA TMC	
JES	JFS	JGS	JHS	KEI	KFW	KGX	KHF	LEF	LFÇ		LHL
SCD	SCL	SDD	SDL	ean faf	ZZB ZZB ZZB ZZE	OCD	BED BGD	hal hbl	JMA		oká okl
JIS	JJS	JKS	JLS	i KII	KJW	KUE:	KLF	LIT	LJL	LKT	LLF
SED	SEL	SFD	SFL	dbf dbn	ZYE ZYC	OAL OEL	BAL BCL	MAD	TIA TIE	OH}	PDD PET
JMS	JNS	Jos	JPS	ı KMI	KNL	кох	KPF	LML	LNL		LPF
GD	SGL	SHD	SHL	ebn fbf	WAD WBD WCD WDD	OCL	BEL BGL	TED TFD	TJA TJB		KAA KAI
Jos	JRS	JSS	JTS	l KOI	KRL	KSX	KTF	LOT	LRL	LSA	LTM
SID	SIL	SJD	SJL	dcf dcn	wal wbl wcl wdl	OBD OFD	BBD BDD	MAL	tka tkb tkc tkd	JED	PAD QCA QCB
JUS	JVS	JWS	JXS	KUI	KVW	KWX	KXP	LUT	LVO	LWI	LXM
KD	SKL	SLD	SLL	ecn fcf fcn	ZZD ZZD ZZD ZZD	ODD	BFD BHD	MAT	JMC	JDD	0)2
J1S	J2S SML	J3S	J4S	K1I	K2W	кзх	K4P	LIK	L2Q	L3Q	L4L
	3/11	SND	SNL	ddf ddn edf	ZZE ZZE	OBL OFL	BBL BDL	hed hdd	JME	JMG	pbd pcd
J5S	J6S	J75	J8S	K5I	K6W	K7X	K8P	L5K	L6J	L7L	L8L
OD	SOL	SPD	SPL	edn fdf	ZZF ZZF ZZF ZZF	ODL	BFL BHL	hcl hdl	tab tad	TME TMG	nbl

C0001C0617

BOOLEAN TERMS MADE AT THIS CHIP LOCATION

edn - From pin pair I, h of the I chip fdf - From pin pair E, d of the I chip

fdn - From pin pair G, f of the I chip