Single Processor Refresh

The Cray-2 dynamic memory needs to be refreshed. The storage chips that we use need to be fully refreshed every four milliseconds.

A 64K storage chip needs to be hit with a refresh cycle 256 times to refresh the entire chip. 512 refresh cycles are required to fully refresh all the data in a 256K storage chip. A refresh is performed, in the chip, all columns at once, one row at a time. Each chip has an internal counter which advances each time the chip receives a refresh function. This counter then automatically points to the next row to be refreshed. The chip will go into a refresh cycle if it receives the Column Address Strobe (CAS) before it receives the Row Address Strobe (RAS) signal.

Control on the storage module generates the CAS before RAS sequence when it detects that the refresh bit is set in the memory address. All chips on a bank storage module are refreshed at the same time. So in the case of the 64K storage chip the bank has to be hit with a refresh 256 times in four milliseconds.

EB does 4 refreshes for each function 20.

To send a refresh function to the storage modules a foreground function 20 is issued. In our single quadrant systems we do a function 20 with a vector length of 40_8 every 55 nsec (msec). The only valid address bits, in this function, are the set refresh bit and the starting bank address bits. The hardware will do the vector length four times for each function 20. This sends four refresh functions to each bank of the single quadrant for each function 20. Issuing the function 20 every 55 nsec (msec) will result in a full refresh in three and one half milliseconds.

The refresh requests have top priority to do memory requests.

1 Billion Bytes

500,000

32 X 64K X 8