JC MODULE WRITE-UP

The JC module controls vector register accessing. There are two JC modules per processor. One JC controls four vector registers. Below is a list of the main areas on the module.

Addressing for VR Registers.

- Vector Pointers
- Vector Length Counters
- Control

Vector Pointers

There are four vector pointers per JC module. A vector pointer contains the banks select bits (2^0, 2^1), chip address (2^2-2^5), Write mode bit, and go vector step bit.

Each vector register is subdivided into four banks. The reason for the banks is data coming from Common Memory into a vector register may be out of sequence. Common memory quad conflicts will cause the quad to stop outputting data but the other three quads of common memory may continue.

Vector Length Counters

There are four vector length counters on the JC module. One counter per vector regiser. A counter is initially loaded with the vector length value. It will decrement by one for every word inputted or outputted from that vector register. When the counter goes to zero a signal is sent to the JA module to clear out that vector registers reservation flag.

Control

Each vector register has a set of controls. The controls operate independently of one another during vector register transfers.