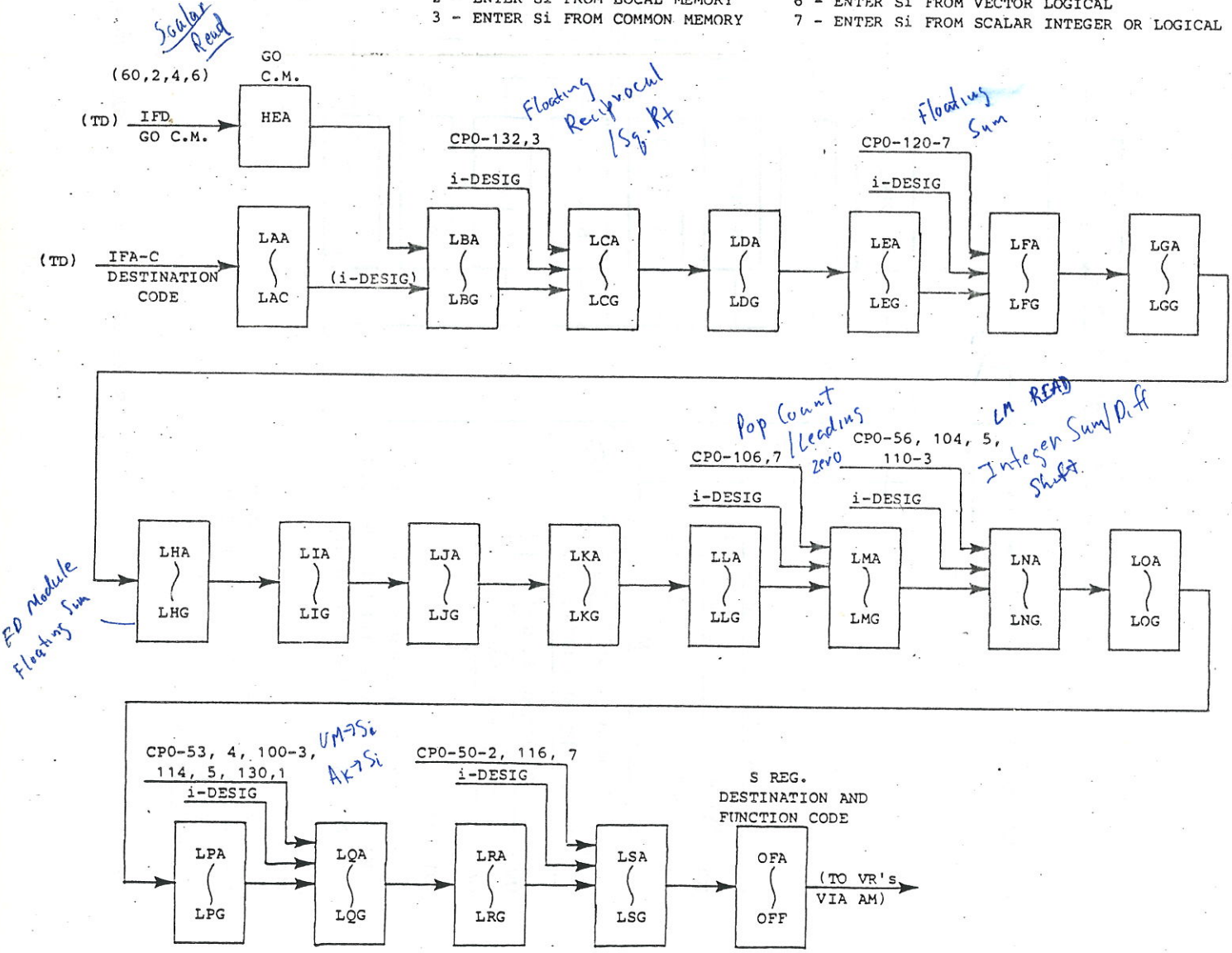
BELOW IS A CHART SHOWING WHEN THE i-DESIGNATOR AND THE 3 BITS OF THE FUNCTION CODE IS SENT TO THE VR MODULE (VIA THE AM) FOR THESE INSTRUCTIONS 50-4, 6, 60, 2, 4, 6, 100-133.

t(CM Ref Time)

	CP20	CP18	CP15		CP8	CP7		CP4						CP2	
	60,2,4,6	132,3	124-7	120-3	106,7	104,5, 110-3	56	130,1	115	114	100-3	54	53	50-2 116,7	
OFA	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2^0
OFB	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2^1 i-DESIG
OFC	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2^2
OFD	1	1	1	0	1	1	0	1	0	0	1	0	1	1	2^0
OFE	1	0	0	0	1	1	1	0	1	1	1	1	0	0	2^1 VR FUNCTION CODE
OFF	0	1	1	1	1	1	0	0	1	1	1	0	0	0	2^2

S REGISTER SOURCE PATH TRANSLATION -
0 - NO SCALAR ENTRY
1 - ENTER Si WITH CONSTANT
2 - ENTER Si FROM LOCAL MEMORY
3 - ENTER Si FROM COMMON MEMORY
4 - ENTER Si FROM FLOATING ADD UNIT
5 - ENTER Si FROM FLOATING MULTIPLY UNIT
6 - ENTER Si FROM VECTOR LOGICAL
7 - ENTER Si FROM SCALAR INTEGER OR LOGICAL



S REGISTER TAG DELAY CHAIN