

VR MODULE LOCATIONS

MODULE	DATA BITS	CPU			
		A	B	C	D
VR0 <i>A</i>	<i>N</i> 0-7	FK	IK	FN	IN
VR1 <i>B</i>	8-15	FJ	IJ	FO	IO
VR2 <i>C</i>	16-23	FI	II	FP	IP
VR3 <i>D</i>	24-31	FH	IH	FQ	IQ
VR4 <i>E</i>	32-39	FF	IF	FS	IS
VR5 <i>F</i>	40-47	FE	IE	FT	IT
VR6 <i>G</i>	48-55	FD	ID	FU	IU
VR7 <i>H</i>	56-63	FC	IC	FV	IV

(COLUMN ROW)

VR MODULE VECTOR REGISTER CHIP LOCATIONS

REG.	DATA BITS	BANK			
		0	1	2	3
V0	N + 0-3	AB-	AJ-	AR-	A2-
	N + 4-7	AF-	AN-	AV-	A6-
V1	N + 0-3	DB-	DJ-	DR-	D6-
	N + 4-7	DF-	DN-	DV-	D6-
V2	N + 0-3	GB-	GJ-	GR-	G2-
	N + 4-7	GF-	GN-	GV-	G6-
V3	N + 0-3	JB-	JJ-	JR-	J2-
	N + 4-7	JF-	JN-	JV-	J6-
V4	N + 0-3	MB-	MJ-	MR-	M2-
	N + 4-7	MF-	MN-	MV-	M6-
V5	N + 0-3	PB-	PJ-	PR-	P2-
	N + 4-7	PF-	PN-	PV-	P6-
V6	N + 0-3	SB-	SJ-	SR-	S2-
	N + 4-7	SF-	SN-	SV-	S6-
V7	N + 0-3	VB-	VJ-	VR-	V2-
	N + 4-7	VF-	VN-	VV-	V6-

16 X 4 CHIP LOCATIONS

Bank = last 2 bits of Elements

8 VR

64 Elements

64 Bits

48-51
52-55