I. Input and Output drawn path times

A. Path times not to exceed 50 picoseconds over the design time .

B. If the output is an unlatched chip the path time may not need to meet the 50 picosecond criteria , engineer must verify .

C. Input and output chips should be located close to the connector . This will help keep the path time between modules as short as possible . The path time between modules should be less than or equal to 3.85 ns. with two inches of slack wire .

D. Try to place the input or output signal on the side of the chip facing the connector .

E. Input signals both true and false should not be jumpered . Input signals shall not be jumpered more than 4 boards and the true and false sides shall not be terminated farther than 4 boards apart .

F. Unused inputs should be padded equal to or up to -10 grids from the used side path length .

G. Output path lengths should be within 10 grids of each other .

H. At most 3 loads may exist on the input pin .

I. The path from a connector pin to its terminator must not be longer than 8.0" .