XVIII. Short2's padded to 144 grids .

Cases:

A. Latch which goes to itself then to another latch .

B. Latch which goes to itself then through a jumper to another latch .

C. Latch which goes to a non latch then through a jumper then to a latch .

D. Latch which goes through a jumper then to a non latch then to a latch .

E. Latch which goes to a jumper then to itself (first latch) then to another latch .

F. 1. Latch which hits a non latch which hits a latch .

2. SPECIAL PADDING pad to 36 grids foil if both latches are on the same chip .

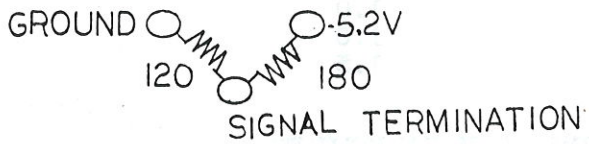
XIX. 180/120 TERMINATIONS All single ended outputs should use them .

A. S chip

B. R chip

C. F chip

DIAGRAM



SIGNAL TERMINATION

XX. PATH LENGTH CALCULATIONS

A. FOIL DELAY

1. 1" of foil is equal to 60 grids .
2. 36 grids is equal to 100 picoseconds .

B. FOIL STUB DELAY

1. All stub lines are doubled .

C. JUMPER DELAY

1. A jumper is given 15 grids of path time between boards .

Example : ABC board to DEF board is 15 grids
ABC board to GHI board is 30 grids
DEF board to MNO board is 45 grids

NOTE : All of our present programs calculate 10 grids a jumper .