

BRANCH SEQUENCE

Items 1-4 are the same for In-stack, Out-of-Stack, and Conditional Branches.

1. The JA issues a branch instruction.
2. The IB receives the branch instruction. It sends "branch preamble", "barrel test," and "field address" (branch address) to the IA. The IB sends "hold issue" to the JA. *Handwritten: $2^{4-2^{27}}$ word address - 2^{0-2^3} parcel address - 2^{1-2^2}*
3. The IA does a barrel check (check if in-stack). The IB does a condition check for the conditional type branch instructions.
4. The IA sends "barrel response" if in-stack. If out-of-stack "barrel response" is a zero.

OUT-OF-STACK

5. The IB sends "go branch" and "parcel pointers" to the JA. The IB sends "branch out" and "word address data" (selects one word of a field) to the IA. IB does a fetch sequence and loads the P register.
6. The JA clears out the instruction queue and waits for instruction data from the instruction stack (IA). IA enters the new field address into the barrel and waits for memory data. IB drops "hold issue" to JA.
7. IA receives data from memory. It sends a "64 bit instruction word" to the JA with a "data ready".
8. JA accepts the data and responds with a "resume" to the IA.