## 11) S Register Tag Delay Chain

This is a 19 clock period delay chain. It controls the S register entry code described on the previous page. S register type instructions will enter the Si designator and entry code at the correct point in the delay. (See A/S Register Tag Delay Chain diagram).

## 12) Control to other modules

The JA module has many outputs which control other modules in the CPU. See definitions of outputs for further descriptions.