S REGISTER BLOCK DIAGRAM (VR MODULE)

A-2778

RELAY outputs:

SCALAR LOGICAL	(VR)
SIGN TEST	(IB)
ZERO TEST	(IB)
SCALAR INTEGER	(GA)
SCALAR SHIFT	(GB)
A REGISTER DATA	(AR)
COMMON MEMORY DATA	(JB)
LOCAL MEMORY DATA	(WA)
VECTOR INTEGER	(VA)
VECTOR MASK	(VL)
FLOATING-POINT ADD	(FA)
FLOATING-POINT MULT.	(M-,RA)

RDOUT SELECT

S REG. 0
S REG. 1
S REG. 2
S REG. 3
S REG. 4
S REG. 5
S REG. 6
S REG. 7

MUX

PATH SELECT

DECODE

(JA VIA AM) S REG. SOURCE CODE   (SEE NOTE #1)

DECODE

(JA VIA AM) S REGISTER DESTINATION CODE   (SEE NOTE #2)

PATH SELECT inputs:

(GA)	SCALAR INTEGER RESULT
(GB)	SCALAR SHIFT RESULT
(JB)	CONSTANT DATA
(TD)	COMMON MEMORY DATA
(VL)	V. LOGICAL RESULT
(FA)	FLOAT.-PT.ADD RESULT
(ME)	FLOAT.-PT.MULT.RESULT
(WA)	LOCAL MEMORY DATA

NOTE #1:

THE S REGISTER SOURCE CODE SELECTS
TWO OF THE S REGISTERS TO BE SENT
TO ALL THE FUNCTIONAL UNITS.

NOTE #2:

THE S REGISTER DESTINATION CODE
IS A SIX BIT CODE WHICH SELECTS
THE CORRECT PATH AND THE CORRECT
S REGISTER TO BE ENTERED.

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