WA MODULE INPUT CONTROL TERMS

GO ISSUE (IHA, IHB) - The WA receives 2 signals called Go Issue from the JA module. Instruction issue time is the clock period when both of these terms are set. The WA is doing a final check to see that all conditions have been met in order for an instruction to issue. IHA and IHB each look at 5 issue conditions on the JA. The final check is done on the WA to get ISSUE to the WA one clock period sooner then if the check were done on the JA. Issue is used in combination with other control signals to start the timing sequence for a Local Memory Reference.

ENABLE CONSTANT WRITE (IIB) - Enable Constant Write is sent from the JA module to condition the WA module for a Write to Local Memory. The second parcel of the current instruction will be used as the Local Memory Address. The reference will write a single word of either Scalar or Address register data into Local Memory. The signal sets for one clock at the start of any write reference using the instruction parcel constant as the Local Memory address.

ENABLE CONSTANT READ (IIA) - Enable Constant Read is sent from the JA module to condition the WA module for a Read from local Memory. The second parcel of the current instruction will be used as the Local Memory Address. The reference will read a single word and send it off to either a Scalar or Address Register. The signal sets for one clock at the start of any read reference using the instruction parcel constant as the Local Memory Address.

Enter AR Address (IJA) - Enter AR Address is sent from the JB module to tell the WA module to gate in the available Address Register value, lower 14 bits, to be used as Local Memory Address for the current reference. The signal sets for one clock at the start of any reference that uses Address Register Data as the Local Memory Address.

Advance Address (IJD) - Advance Address is sent from the JB module to increment the Local Memory Address, plus one, during Vector Register References. The signal sets for the first reference, increments, and stays set throughout the rest of the reference. The duration depends on the Vector Length. Only the bank zero address register has the advance mechanism. The other bank address registers receive the new address by shifting the bank zero address into the other bank address registers.