VECTOR REGISTER CONTROL

VR7 $(2^{63}-2^{56})$
VR6 $(2^{55}-2^{48})$
VR5 $(2^{47}-2^{40})$
VR4 $(2^{39}-2^{32})$
VR3 $(2^{31}-2^{24})$
VR2 $(2^{23}-2^{16})$
VR1 $(2^{15}-2^{8})$
VR0 $(2^{7}-2^{0})$

VECTOR REGS 0-7

AM
WAYSTATION

JC1
JC0
VECTOR 0-3 POINTERS
VECTOR 0-3 LENGTH COUNTERS

VECTOR 4-7 POINTERS
VECTOR 0-3 POINTERS
VECTOR RELEASE 4-7 (JA)
VECTOR RELEASE 0-3 (JA)

BEGIN LOCAL VECTOR WRITE 0-7

JB
INSTRUCTION TRANSLATION
VECTOR WRITE DELAY CHAINS 0-7
FUNCTIONAL UNIT LENGTH COUNTERS

RELEASE FUNCTIONAL UNITS (JA)
FUNCTION UNIT ENABLES (VL,FA,ME)

B-2785
C001C0504

JA
INSTRUCTION TRANSLATION
VECTOR REGISTER RESERVATIONS
FUNCTIONAL UNIT RESERVATIONS

VR MODULE SOURCE CODE
BEGIN VECTOR 0-7
EXPRESS READ/WRITE
GO ISSUE
(TA) BACK UP
(IB) HOLD ADVANCE
(TD) MEM. ARRIVAL CODE
VECTOR LENGTH
(AR via AM)
ADV./RELEASE IOTA (VA)

INSTRUCTION DATE
GO ISSUE

(AR via AM) VECTOR LENGTH
(VA) RELEASE IOTA

(IA) INSTRUCTION DATA
(JC's) VECTOR RELEASE 0-7
(JB) RELEASE FUNCTIONAL UNITS

(writing into vector registers)

DATA

Does not use common memory (sequential data)

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