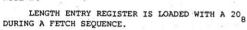
NOTE #1 QQB, QQW HOLD UNTIL A FETCH COMPLETE SIGNAL IS RECEIVED FROM THE IA MODULE (INDICATING ALL WORDS INPUTTED INTO THE INSTRUCTION STACK OR UNTIL ABORT FETCH OCCURS). HOLD QQC, QLP, QLQ UNTIL LENGTH REGISTER EQUALS ZERO OR UNTIL ABORT FETCH IS INDICATED. HOLD QQJ (ENABLE FETCH LATCH) UNTIL LENGTH REGISTER GOES TO ZERO. NOTE #4



NOTE #5 IF A 002 INSTRUCTION (RETURN JUMP).

SEQUENCE WILL BE STOPPED AT CP5 IF THE MEMORY PORT IS BUSY.

NOTE #7

(SEE NOTE #5)

CP1-0,1,3-17 INSTR.

CP4-002 INSTR

START QYD

ABORT FETCH (QQL) AND ENABLE. FETCH (QQJ) WILL BE INDICATED AT CP9.

FETCH WILL BE ABORTED IF THE BRANCH CONDITION IS NOT SATISFIED, OR IF IN-STACK BRANCH CONDITION OCCURS. ABORT FETCH WILL INHIBIT VALID REFERENCE SIGNAL TO TA MODULE.

qql

AQQ

CP3

RAB

NO ABORT FETCH PORT NOT BUSY qlp

CP2

BOUNDRY SEQ

FETCH REQUEST QOA

PORT NOT BUSY glp

(SEE NOTE #6) qqb

FETCH REG. QQA

PORT NOT BUSY alo

NO ABORT FETCH ggl

NO ABORT FETCH qq1

