XXIV. COMMENT SECTION

A) Comments for boolean definitions

B) Special drawing instructions

C) Anything out the ordinary during processing

XXV. CLOCK DISTRIBUTION CIRCUIT

A) There are 90 clock stacks possible per module . Modules with memory chips may have less and may vary from rules stated below .

B) Clock stacks are located in the S jumper location .

C) Raw clock is called IZZ/izz and is feed into two chips at locations KJ and NJ both W chip types .

D) The outputs from these chips ZYA/zya through ZYF/zyf are sent :
ZYA/zya to middle triad B location all 8 boards
ZYB/zyb to middle triad F location all 8 boards
ZYC/zyc to middle triad J location 6 boards , not on K or N boards
ZYD/zyd to middle triad V location all 8 boards
ZYE/zye to middle triad 2 location all 8 boards
ZYF/zyf to middle triad 6 location all 8 boards

E) The outputs from the 6 chip locations per board stated in item 4 are called ZZZ .

F) For each "S" clock jumper stack three ZZZ outputs are wire-anded and four terminations are added .