VI. 42.5 ohm termination placement

A. On circuits with 8 or more loads .

B. On circuits with 4 or more jumpers and at least 5 loads .

VII. All MRN's must be implemented along with open temp evaluation .

VIII. Register and storage chip padding has to be evaluated by the Design Eng. Group and usual strict care must be taken as to not change any line used by the R and S chips .

A. Storage chips are broken into 4 subdivisions called access times . Check appendix A and B for "Usage by module" . Wire-ored outputs must be hand checked , along with any signal drawn on the clock layer . The access program must be run and these values checked ,

1R. (R Register chips) Max. address + 04.000 + max. data_out

a. Times must be under 08.000 for all modules except IA module

b. Times must be under 07.800 for the IA module

1S. (S Storage chips) Max. address + 09.000 + max. data_out ; times must be less than 16.000

2. 04.000 - (max. data_in - write enable) (DATA SETUP)

3. Min. data_in - write enable (DATA HOLD)

4. Min. address - write enable (ADDRESS HOLD)

B. It is best to have all inputs to the storage chips originating on the same board as the storage chip .