FA Module Inputs

Sj, Sk and Vk Data - Scalar data Sj and Sk and vector data Vk share a common path into the FA module. Sj data is latched up on the FA module clock period five of a 120, 121, 170 or 172 instruction. Sj is held for vector length for the 170 and 172, vector-scalar instructions. Sk data is latched up on the FA module clock period six of a 120-123 instruction. Vk data is latched up on the FA module clock period eight on a 170-175 instruction. A new element of the vector stream is latched up on the FA every clock period for vector length time.

Vj Data - Vj data has a unique path into the floating add unit FA module. Vj data is latched up on the FA module clock period eight of a 171 or 173 instruction.

Enable Vector Add - Enable vector add is a single clock period control signal from the JA module. This signal tells the FA module that an instruction in the range 170-175 has issued. The signal is latched up on the FA module clock period two of these instructions.

Enable Scalar Add - Enable scalar add is a single clock period control signal from the JA module. This signal tells the FA module that an instruction in the range 120-123 has issued. The signal is latched up on the FA module clock period two of these instructions.

f Field 2^0-2^2 - The FA module receives the lower order three bits of the f field of an instruction. These three bits are used in combination with the go add signals to tell the unit exactly what instruction has issued. The f field bits are latched up on the FA module clock period two. The j field bits are single clock period signals.

Vector Length Control - Vector length control comes from the JB module during any vector instruction. Vector length control is latched on the FA module clock period four. The signal is set from the JB module for vector length. The signal is used by the FA module to gate through the vector stream and to hold the scalar operand for a scalar-vector type instruction.

Enable Range Check - Enable range check is a static signal from the EA module. The signal reflects the state of a bit in the background port status register on the EA. This register value can be altered by a background processor 035 instruction or by a foreground function. The signal is passed on to the FC module and enables the setting of the range error flag on the FC. The signal is only sampled when an instruction issues to this unit. This allows the state of the bit to be changed on the EA module without having an affect on a previous instruction issued to the floating add unit. The enable is held for vector length during vector instructions.