13. Head Address Register Storage

The head address register storage is found on the WI_ Boolean terms (16x4 chips). It is only used during a DSU read sequence. Only four locations are used within the 16x4 storage chips and a 12 bit value can be read out of or written into them. This 12 bit value is a secondary buffer address. To explain how this circuitry is used let's first take a look at the DSU read sequence.

During a DSU read sequence the four data paths (Head channels) input data from the DSU to the DA module. These four paths are not in sync with each other. Thus the four head channels must be buffered separately. The secondary buffer is subdivided into four separate sections, one section per head channel. The head address storage register contains the four different secondary buffer addresses (one address per secondary buffer section). When one head channel is ready to input data into the secondary buffer a timing chain (QQ_ terms) is started. This timing chain gives all head channel data paths a slot time to enter it's data into it's secondary buffer segment. If the data is not ready to transfer during it's slot time the transfer will not take place. As soon as it is ready to transfer the timing chain is started again and again every head channel has a opportunity to transfer data. The DSU read secondary buffer addresses are read out of the 16x4 chips and presented to the correct secondary buffer segment. If the transfer did take place during that slot time then the address is incremented and stored back into the 16x4 chips.

14. CRC Generation and Clock

There is one CRC generation and check circuit (A_ _, WJ_, WK_, and XE_ terms). It is time shared between the four head channel paths between the DSU and the secondary buffer.

During a DSU read sequence the four head channel paths are inputted from the DSU into the secondary buffer during that head channels' slot time (see number 13, Head Address Register Storage). Also during that time slot the CRC code is being generated for that one head channel. The partial CRC code is loaded into fire code storage (WJ_, WK_). The fire code storage can hold four - 32 bit partial CRC codes (one per head channel). The partial CRC is read out and used when ever it's head channel is going to transfer data into the secondary buffer as described above.

The DSU write sequence is very similar to the DSU read sequence except the data is read out of the secondary buffer and sent to the DSU. After the data is read out and before it is sent to the DSU the CRC generation takes place. Each head channel has it's slot time to generate partial CRC and it is then stored back into the 16x4 storage chips. When the data is done being sent to the DSU the resultant CRC code is sent to the DSU.