(TO DS DSU OUTPUT SIGNALS OA-BUSS/TAG BIT 3 BIT 0 LINES BUSS BIT 1 BIT 2 BUSS BUSS NB-BUSS NBG NBH NBI NBJ (RD EARLY) (PARAM) READ EARLY FUNC DATA) (WRITE (SYNC BITS) PARAMETER 22 PARAMETER 23 PARAMETER 21 WRITE DATA WRITE DATA WRITE DATA SYNC BITS SYNC BITS SYNC BITS MAX OBO MBH YDA MBD OIF max JFII NOTE #1; THE DISASSEMBLY REGISTERS ARE LOADED WITH 4 BITS OF WRITE DATA OR 4 BITS OF CRC. THE REGISTER DISASSEMBLES ONE BIT PER WRITE CLOCK PULSE. (0II) (DIO) (HIÖ)▲ PARAMETER 20 RD GATE ENABLE WRITE. GATE PARAMETERS WRITE DATA SYNC BITS 22 FUNC. (RD EARLY) ENABLE WRITE (TO CRC GENERATION) TO DSU BIT 2 TO DSU BIT 3 TO DSU BIT 1 BIT 0 TO DSU OIF DIĞ PIO CIO HOLD HOLD HOLD HOLD QIK WRITE CLOCK BUFFER DATA TO CRC VG-EAI FAI GAI DAI GAI-GAL DATA FLOW HEAD O DATA OUT DISASSEMBLY REG. HEAD 2 FAI HEAD 3 GAI REG. HEAD 1 EAI (TYPICAL) 212+N FAI-FAL REG. EAI-EAL 20+N 24+N 28+N DAL BIT DAI BIT DAJ BIT DAK BIT (SEE NOTE #1) WEB WEC WED. WF-MG-WII-SECONDARY AAI, ABI, ACI, ADI WE_-WH-BUFFER CRC

SECONDARY BUFFER TO DSU