4. Interrupt Address Register

The interrupt address register (YC_ terms) is loaded from the second parcel of an accepted subfunction. The address remains in the register until the subfunction completes, at which time it will be outputted to the channel during a call sequence. Subfunctions 05, 12, 21, 25 and 37 do not respond to call sequences. (See subfunctions response and call sequence charts).

5. Status Register

The status register on the DA module contains various information depending on what the previous subfunction was.

Example: A subfunction 064 (read disk interlock register) just completed. The DA module will now respond to a call sequence. After responding to a call sequence the foreground will send a subfunction 12 (read disk controller status) to the DA. The DA will send the status register (which contains the disk drives interlock register value) back to the foreground.

Subfunctions 060, 061, 062, 063, 064, and 100 will enter values into the status register. (See subfunctions chart for further description). Once one of these subfuntions completes, a subfunction 12 must be performed to get the status back to the foreground.

After the status has been read back to the foreground the status register will be entered with the controller status. So a subsequent subfunction 12 will report the controller's status.

6. DSU Function Decode

The QC_ Boolean terms decode the various DSU functions (see DSU function chart). They enable the selection of the DSU input and output busses, the DSU tag lines and the Tag/Buss line Controls (M terms). The M terms synchronize the DA module with the DSU and controls when the Buss or Tag lines are to be used.

7. Servo Clock Generation and Control

The SA_ - SG_ terms are the servo control circuits. The SA_ terms generate a psuedo servo clock (see psudeo servo clock generation diagram). It takes a 9.67 MHz DSU clock and converts it to a 806 KHz clock. Positive and negative servo clocks are also generated from this.