JA MODULE

The JA module controls instruction issue and decode for the background processor. Below is a list of the main areas in the JA module.

1) Instruction Queue
2) Instruction Translation
3) Instruction Fanout
4) Issue Control
5) Reservation Flags
6) A Register Readout Code
7) A Register Entry Code
8) A Register Tag Delay Chain
9) VR Module Source Code
10) S Register Entry Code
11) S Register Tag Delay Chain
12) Control to other modules

1) Instruction Queue

The JA module receives a 64 bit word from the instruction field module (IA). The word is disassembled one parcel at a time through the instruction queue. The instruction queue handles instruction translation and fanout. It can stream instruction data in consecutive clock periods.

2) Instruction Translation

The instruction is decoded and used for control.

3) Instruction Fanout

A copy of the instruction data is sent to the IB, JB, and WA modules. These modules will use the data as constants or for decode.

4) Issue Control

The instruction decode determines the resources needed to issue the instruction. If the resources are available then issue will occur. Issue can occur every other clock period, best case.

5) Reservation Flags

Once an instruction issues, reservation flags are set for the registers, functional units, and paths to be used. These flags will determine issue for the <u>next</u> instruction.