Word)	
(Function	
A Register	

_
Word
(Data
Register
m

		Memory					R on EB.				a a .	
i i		Common				h	FAR				2 X	* * * *
Descriptions	Common Memory Refresh	Enter Interrupt Address and status,	Read n words from designated address.	Write n words into designated	Read common memory port status redister data.	Read common memory error address.	Read single word to foreground	Write single word from foreground access register to common memory.	Transmit high-order 32 bits from foreground access register.	Transmit low-order 32 bits from foreground access register.	Load high-order 32 bits into foreground access register	Load low-order 32 bits into foreground access register.
215 20	, C.M.A.	0	C.M.A.	C.M.A.	0	0	215 20	215 20	0	0	Data 247 232	Data 215 20
P-2 20	C.M.A. (see note 1)	0	C.M.A.	C.M.A.	0	0	C.M.A.	C.M.N.	0	0	Data 263 248	Data 231 216
215 20	Refresh Length	Interrupt Address 215 20	Transfer Length 29 20 (see note 3)	Transfer Length 29 20 (see note 3)	0	. 0	0	0	0	. 0 .	0	0
215 20	020000	02100X * (see note 2)	022000	023000	. 024000	025000	026000	027000	030000	031000	032000	033000
Function	20	21	22	23	24	25	. 26	. 27	30	31	32	33

C0001C0408 NOTE 1 - Bit 2^{29} for a four quad memory or bit 2^{26} for a single quad memory has to be set to do a refresh.

NOTE 2 - The lower 2 bits of the subfunction selects interrupt mode. X = 1 - interrupt on single bit error, X = 3 - interrupt on single bit error, X = 3 - interrupt on single or double bit error.

NOTE 3 - A transfer length of 0 will transfer 100g words.