

COMMON MEMORY BACKUP

When a Common Memory reference to a particular quadrant is held off do to a bank conflict, the path to that quadrant is blocked off. Another reference to that quadrant can be made and the information necessary to do these two references will be held until the path to memory reopens. If a third reference is made to that same quadrant from this same processor, the processor goes into memory backup.

A backup condition is confined to the CPU doing the references. A backup condition for any quadrant results in the recirculation of reference information pertaining to all four quadrants. The reference information goes into a ten clock period delay chain. By the end of this ten clock delay the issue of all instructions in the CPU is stopped. A vector stream, if present, is also stopped.

If the reference can be accepted, after the ten clock delay, the data comes out of the delay chain and is sent on its way. The first reference that entered the delay chain is always the first reference to leave the chain. If the request cannot be honored after the ten clock delay the information will enter the delay chain again. Another attempt will occur in another ten clocks.

Another request information may or may not follow the first request into the recycle chain. This depends on whether or not the TA/TE module received another request. There is a flag sent through the chain with each references information which is set if there is valid data in that position of the chain. The flag also says which quadrant the data is for. Sequential positions in the delay chain are for sequential quadrants of memory. Two requests for the same quadrant would be four clock periods apart in the chain.

The information in the recycle delay chain contains a request package, a data valid/quadrant pointer flag, the memory address, and the memory write data. The request package and the data valid/quadrant pointer flag delay chain is found in the P terms on the TA module. The data valid/quadrant pointer flag are used internal to the TA. The request package is entered into the package buffer on the TA, after the ten clock period delay, if the buffer is available. Subsequent references can then come out of the chain. It is sent to the Q? module when the Q? package buffer is available. The request package contains the bank number and a destination code. The bank number is used by the Q? for bank selection. The Q? module does not use the destination code. The Q? simply delays the code and sends it to the TD module. The code is used only during a read. The code tells where the data is going to.

The memory bank address delay chain is found in the S terms on the TA module. This is the 24 bit address packet that is sent to the TC module. The TC module itself has eight 72 bit buffers, two for each memory quadrant. These buffers hold the address and data packets associated with the two request package buffers on the TA and on the Q? module.