

D. Memory Module Testing - Special Procedures.

Memory modules for the Cray 2 are slightly different from the other module types. They contain discrete components for level translation in addition to the standard 16 pin ECL chips. These discrete transistors are difficult to probe when the module is stacked. Also, The MOS memory chips themselves are a leadless chip and are difficult to probe. Therefore, in order to insure that the modules are in good shape before they are ever stacked, a tester was designed to test the boards one at a time. These single board tests insure that all the transistors function, that all memory chips are accessible, and that there are no shorts or opens on the Address, Data, or Control lines. All board levels for memory modules are tested in this manner before stacking.

Failures on a module level are troubleshot on the pulse power tester just as a logic module is. The ECL portion of the module can be probed without difficulty, and certain signals in the MOS memory portion can be probed. The module are laid out well from a troubleshooting standpoint; those signals that can be probed are enough to determine the cause of most failures. Also, the memory module tests have been written to aid troubleshooting; in many cases, the failure cause can be determined from the test step, without probing.

Conclusion:

Using the methods described, to date we have been able to achieve a great deal of success in shipping error free modules from Module Test to System Check-Out. We are continuing to make improvements in our testing process, to further improve on this ability.