

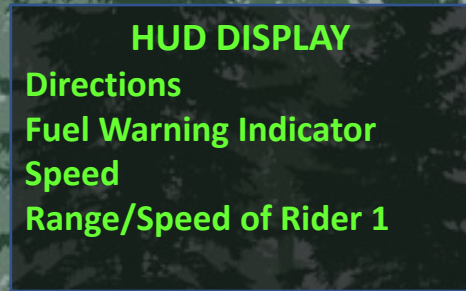


V2X Motorcycle HUD Weekly Updates

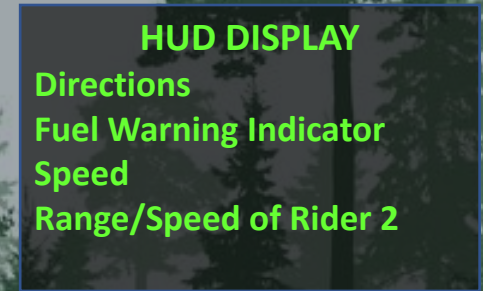
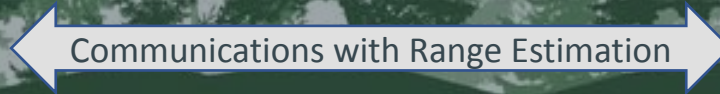
...

Jacob Nguyen, Ryan Hiser, Jorge Pacheco
UCSD MAS WES
14 May 2022

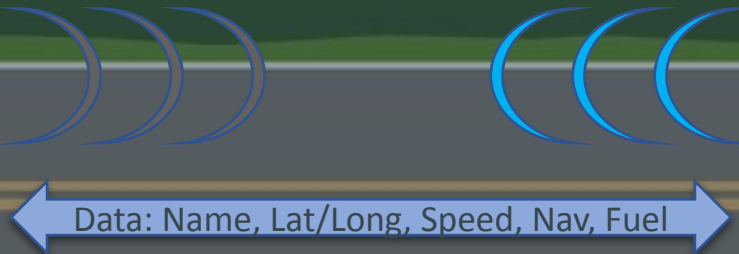
V2X Motorcycle HUD



Rider 2



Rider 1





Motivation and Goal

- Our goal intends to improve the motorcycle group riding experience, by safely providing more information to the riders.
- Final Demonstration:
 - We intend to implement a 2-Node system capable of transmitting various information (range, fuel level, ...) and audio. The audio could eventually be used as a intercom or to stream music from one rider to other (a DJ).
 - The system will be able to display that information via a heads-up display.



Overall Progress

- Waveform Description defined (data defined, QPSK modulated)
- Simulink Model of Waveform (full TX/RX, all code gen except demod)
- RX Demod fully designed in HLS/IP Cores (MATLAB -> HLS workflow)
- OLED and wireless link using arduino (WiFi msg integrated with zed)
- FMComms4 + Zedboard integration with PYNQ



Current Progress



Previous Sprint

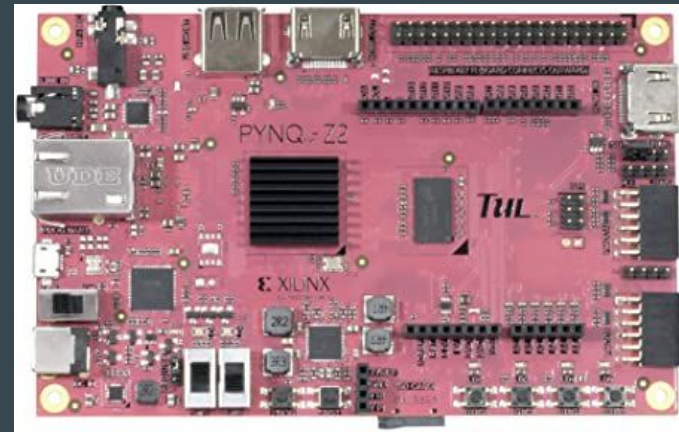
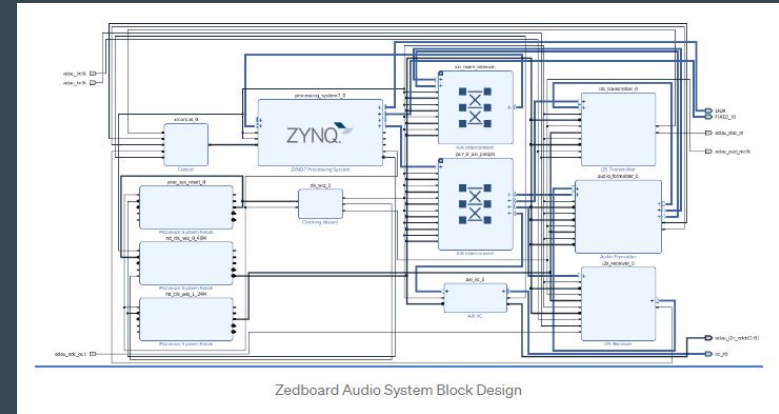
- Integration
 - ~~Integrate audio files with TX modulator SW~~
 - ~~Loopback test with TX/RX~~
- RX
 - ~~Hard decision and store to FIFO~~
 - ~~Finish verification via Verilog testbench~~
 - ~~Package RX IP module and integrate to design~~
 - ~~Integration with PL and RX Baseband software~~
- HUD
 - ~~Update kernel on Pynq for USB (kernel module created and alternative approach)~~
 - Verification and Validation (V&V)

The fun continues...



Integration (audio)

- Audio file (in binary format) being read by the TX baseband code
 - 60 seconds of audio sample
 - 6000 frames of 0.01s audio samples
- Investigation on how to play audio on zedboard
 - <https://yuhei1-horibe.medium.com/zedboard-audio-hardware-design-b19c3a1bf453>
 - Requires zedboard IP core updates in vivado and kernel updates
- Alternatively play audio on the Pynq Z2 board (stream audio from zedboard to Z2)
 - Z2 has some audio support and libraries built in





Integration (loopback SW setup)

- Created UIO Kernel Module and modified device tree.
- Added TX/RX threads that interface with AD9361 and UIO
- TX thread periodically sends data to AD9361:
 - HUD data read from config.txt
 - Audio data read from sample_audio.bin
- RX thread periodically checks for data in UIO
 - UIO used instead of DMA to speed up development.

```
v2x_sdr_xcvr.c
504 static void tx_thread_fn(void* args)
505 {
506     // Loop init
507     printf("TX thread started\n");
508     uint32_t loop_num = 0;
509
510     // Only run if shorts are used
511     int datasize = ((sdr_data*) args)->ini->datasize;
512     if (datasize == 2)
513     {
514         int16_t tx_mod_out[TX_MOD_OUT_SYMS * 2];
515         ssize_t nbytes_tx;
516         char *p_start;
517
518         // Run loop
519         while (!stop)
520         {
521             // WRITE: Get pointers to TX buf and write IQ to TX buf port 0
522             p_start = iio_buffer_first(txbuf, tx0_i);
523             load_frame_txmod(tx_mod_out);
524             memmove(p_start, tx_mod_out, TX_MOD_OUT_SYMS * 2);
525
526             // Schedule TX Buffer
527             nbytes_tx = iio_buffer_push(txbuf);
528         }
529     }
530 }
```




RX

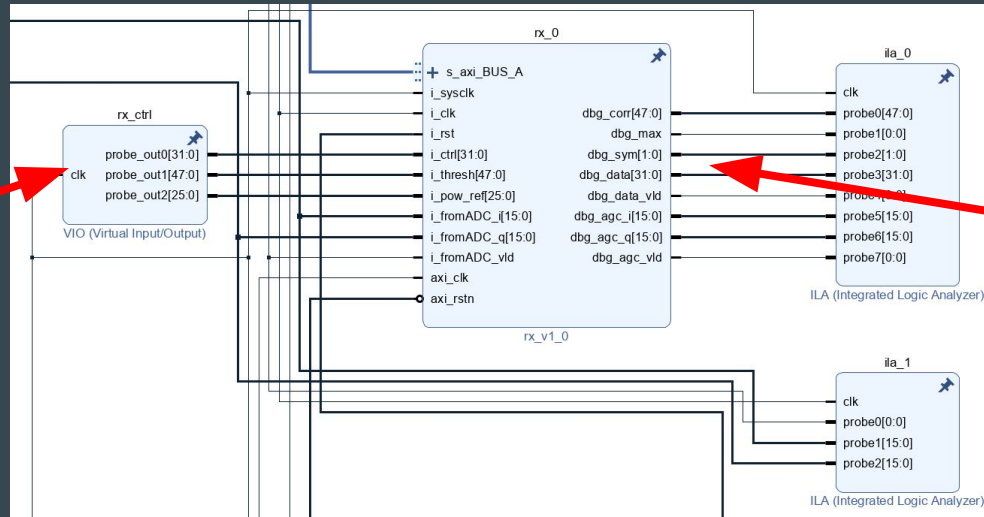
Bram usage
mostly ILA.

Received data
matched sent data!



RX

- Packaged RX IP module and integrated to Analog Devices HDL Project.
 - Currently using a Virtual Input/Output (VIO) to control.
 - Internal Logic Analyzer (ILA) was used to verify DAC input data, AGC, and correlation..



Will replace with a
custom Axi-lite
Interface

Our custom
Demodulator



TX to RX Loopback (Internal Logic Analyzer Output)

ILA Status: Waiting For Trigger (16384 out of 32768 samples)

Name	Value
------	-------

> i_system_wrapper/system_i/rx_0_dbg_agc_i[15:0]	-2048
--	-------

> i_system_wrapper/system_i/rx_0_dbg_agc_q[15:0]	43
--	----

i_system_wrapper/system_i/rx_0_dbg_agc_vld	0
--	---

> i_system_wrapper/system_i/rx_0_dbg_data[31:0]	4fd4a055
---	----------

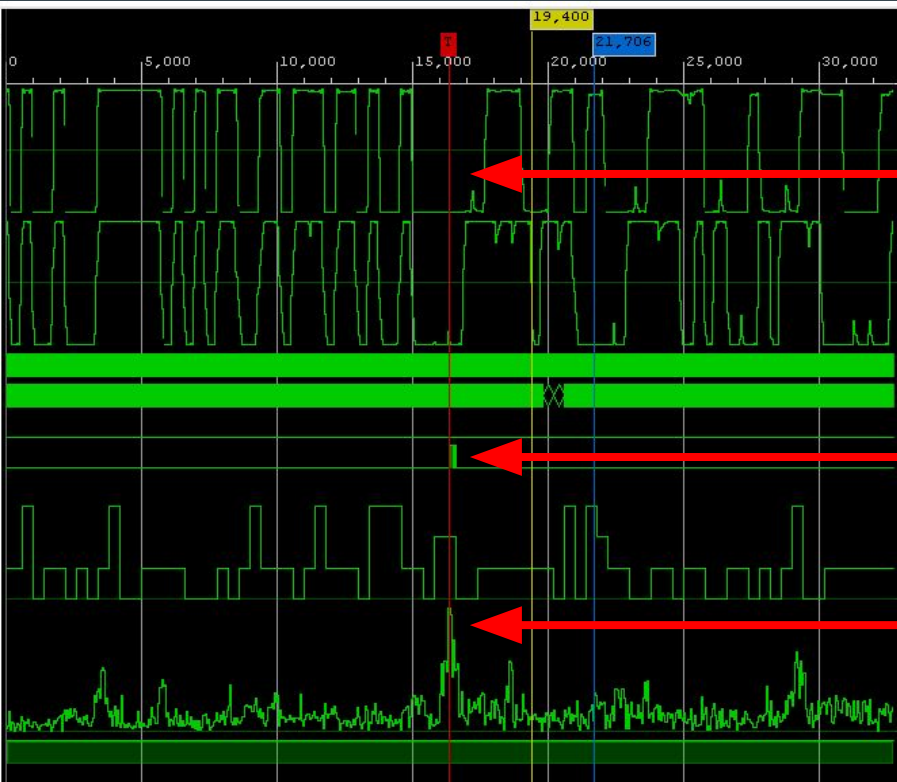
i_system_wrapper/system_i/rx_0_dbg_data_vld	0
---	---

i_system_wrapper/system_i/rx_0_dbg_max	0
--	---

> i_system_wrapper/system_i/rx_0_dbg_sym[1:0]	1
---	---

> i_system_wrapper/system_i/rx_0_dbg_corr[31:0]	000236b9
---	----------

i_system_wrapper/system_i/rx_0_dbg_store	1
--	---



Output of
AGC

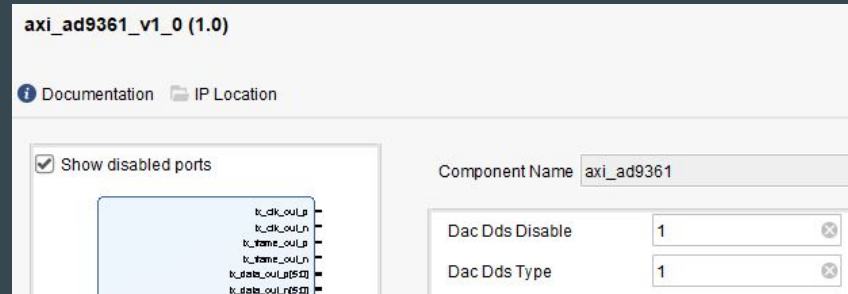
Peak detection

Received Preamble
Detected



TX to RX Loopback V&V (On-going)

- We had to disable the DDS of the axi_ad9361. When you stop filling the DMA it defaults to a DDS tone.

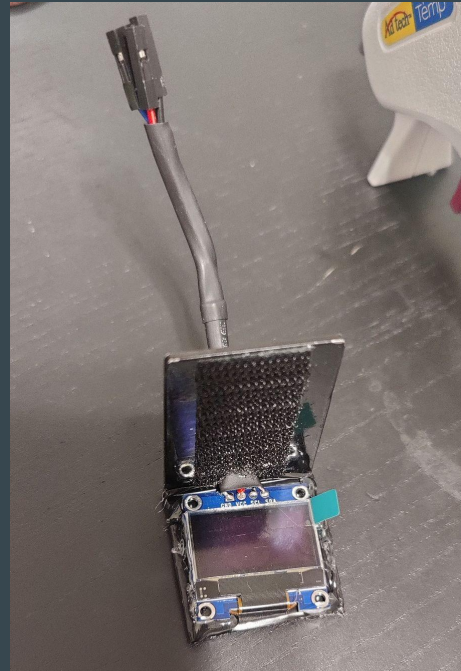


- More debugging required:
 - AD9361 fast-attack AGC seemed to work well for our system.
 - Bad SMA cable or attenuator (stops working if cable gets bumped).
 - TX gain adjustment error needs to be solved to use antennas.

```
* Hardware gain to be set: 15.000000 dB
Failed to set in voltage0_hardwaregain: -95
--- END OF FMCOMMS4 RX CONFIGURATION ---
```

HUD - Progress since last time

- Created “L” bracket out of metal for robust mounting
- Attached OLED to helmet’s sun visor using velcro
- Ran connections through cable sleeve
- Measured clearance so that helmet’s visor still clears





HUD - Progress since last time (Cont.)

- Mounted ESP8266 WiFi module to helmet
- Ran longer jumper cables through cable sleeve
- Attached OLED to WiFi module





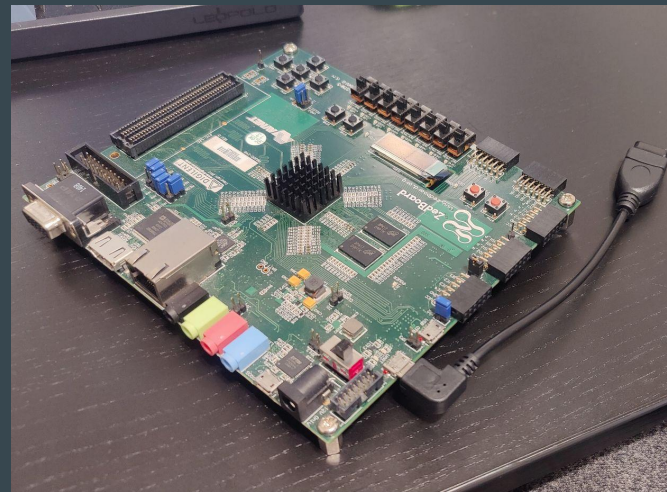
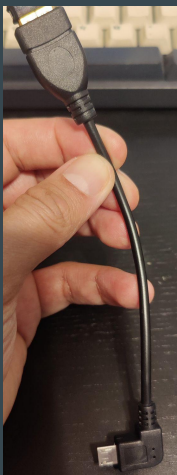
HUD Cont.

- Final Setup



RX Baseband and HUD - Ran into problems!

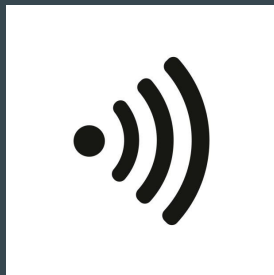
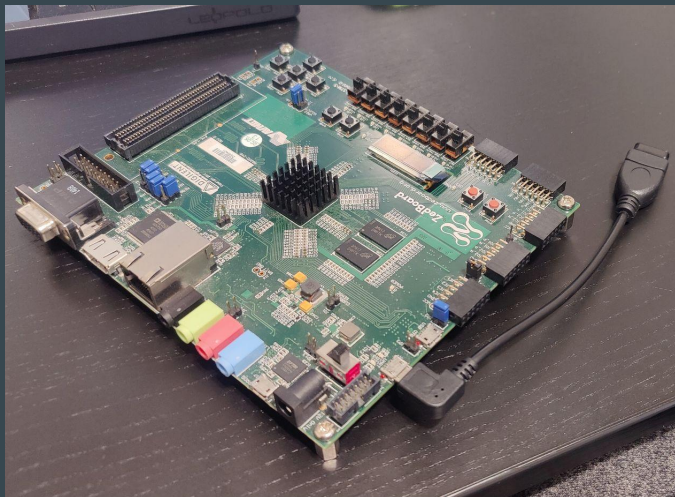
- Sourced USB WiFi adapter for Zedboard
- Could not get Kernel modules to recognize USB WiFi controller...





RX Baseband and HUD - Ran into problems!

Desired Setup:





Demo

- Data generated from reading Config.txt
 - Loaded on zedboards for easy data configuration
 - On the fly updates to data bits transmitted
- Audio bits generated from 60 second audio binary file
 - Audio binary file generated from MATLAB reading 4 kHz .wav file
 - Final demo will save received audio data into binary file, and will be converted to .wav format in MATLAB
- Confirmed that Zedboard compiles with HUD code (libcurl/libev libraries)

```
Config.txt
1 V2X!
2 32.880100
3 -117.234000
4 60
5 3
6 5.3
```

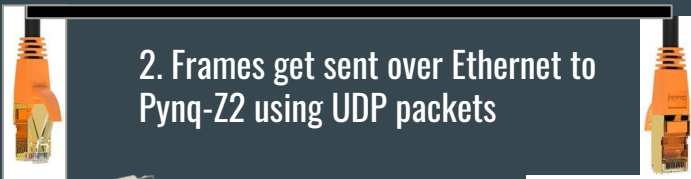
```
Current Folder
Name
audio_gen.m
bin_to_wav.m
play_wav.m

Editor - C:\Users\jacob\Downloads\audio_gen.m
audio_gen.m bin_to_wav.m play_wav.m
1 % Script description:
2 %
3 % Generate an audio file for OTA transmission, with the requirements:
4 % Fs = 4 kHz
5 % Single channel
6 % 16 bits per sample
7
8 %% Choose desired file
9 % Created files using: https://convertio.co/mp3-wav/
10 orig_wav_file = 'latinnova_4000.wav';
11 orig_wav_info = audioread(orig_wav_file);
12
13 %% Read audio from desired file
14 % Choose amount of samples from file
15 num_sec = 60;
16 num_samp = orig_wav_info.SampleRate * num_sec;
17
18 if num_samp > orig_wav_info.TotalSamples
19     num_samp = orig_wav_info.TotalSamples;
20 end
21
22 % Read audio file
23 [orig_y, orig_Fs] = audioread(orig_wav_file, [1, num_samp], 'native');
24
25 % Play audio
26 if 0
27     sound(orig_y, orig_Fs);
28 end
```

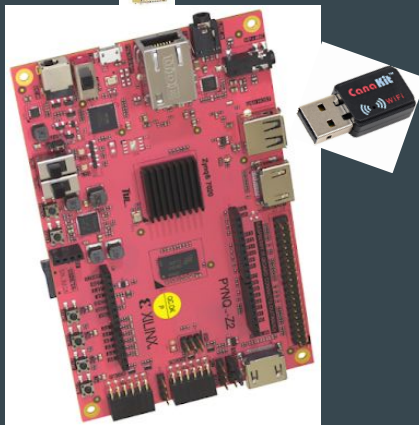
Engineering trickery!

Current Setup (while we sort out kernel drivers...):

2. Frames get sent over Ethernet to Pynq-Z2 using UDP packets



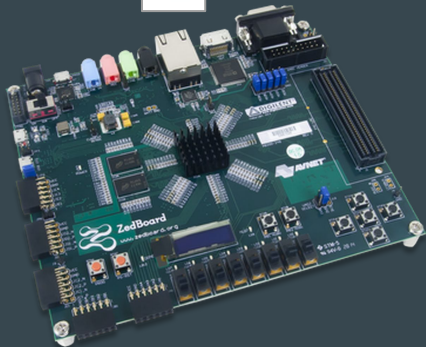
3. Pynq-Z2 acts as a forward link to grab audio and data packets and send over WiFi to HUD



4. HUD packets are displayed in real time!



1. Zedboard produces data

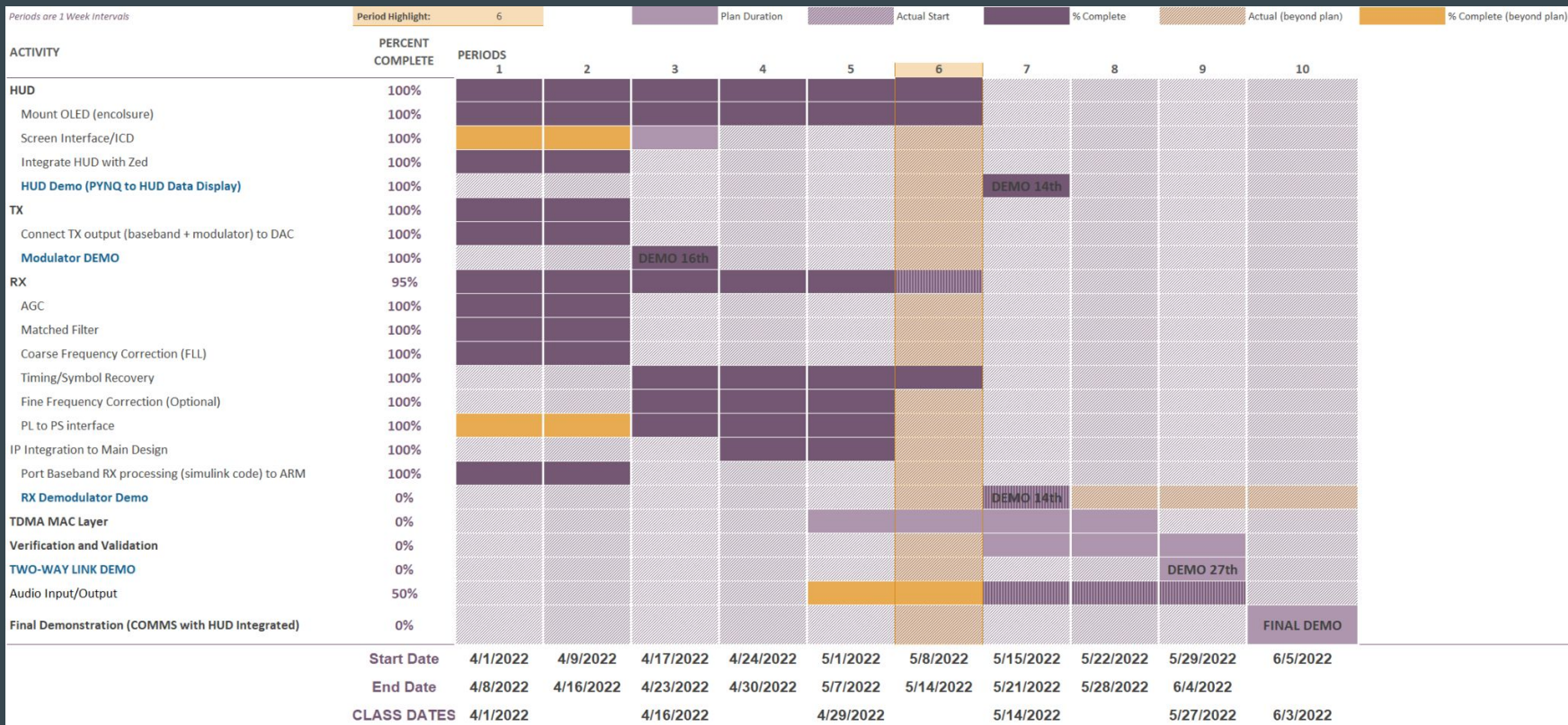




Future Plans



Gantt (timeline)





Next Sprint

- Debug/V&V RX post correlator.
- V&V with antennas.
- Merge all code TX and RX onto one SD Card
 - UIO Kernel Module
 - WIFI/Ethernet code
 - TX
 - RX
- Two-way link
- TDMA protocol investigation and planning
- (Aspirational Tasks) Improve WIFI and Audio approach