V2X Motorcycle HUD Weekly Updates

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UCSD MAS WES
16 April 2022

Motivation and Goal

- Our goal intends to improve the motorcycle group riding experience, by safely providing more information to the riders.

- Final Demonstration:
  - We intend to implement a 2-Node system capable of transmitting various information (range, fuel level, ...) and audio. The audio could eventually be used as a intercom or to stream music from one rider to other (a DJ).
  - The system will be able to display that information via a heads-up display.

Overall Progress

- Waveform Description defined
  - Data packet defined (info + audio)
  - QPSK modulation at WiFi band (2.4 GHz)
- Simulink Model of Waveform
  - Full TX/RX
  - TX Baseband, TX Modulator, RX Baseband generatable
- RX Demod being designed in HLS/IP Cores
  - MATLAB used to demo and verify components
- OLED and wireless link using arduino
  - OLED displays readable text
  - Wireless link integrated with Simulink generated code
- FMComms4 + Zedboard integration with PYNQ

Current Progress

Previous Sprint

- Demo
  - ~~Create data file (name, location, etc) for demo~~
  - ~~Create audio test file for final demo~~
  - ~~Integrate data files with TX modulator SW~~
- RX
  - ~~Insert AGC, SRRC, and Coarse Frequency Correction(CFC) into Vivado design.~~
    - ~~Verilog Test Bench of RX Chain~~
  - ~~Implement Timing Error and Symbol Recovery~~ **(Need to Optimize)**
  - ~~Implement Fine Frequency Correction~~
  - (Start) Integrate with Baseband RX software
- HUD
  - Complete integration with Zed (Code runs on Zed need kernel module for USB)
  - ~~Continue work on Mount/Enclosure~~
- GitHub
  - jtn017/capstone: Capstone (github.com) (We need access to move this)

New Waveform Description

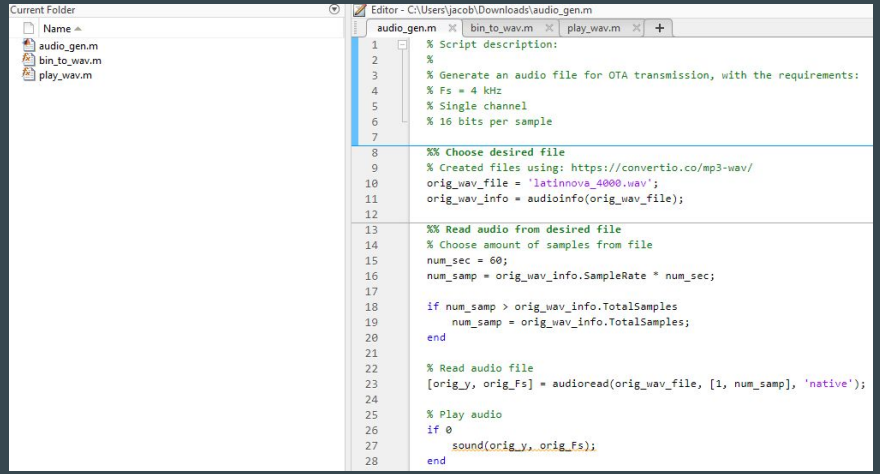
- Changed audio frequency to ease PL timing requirements
  - Original audio frequency: 44.1 kHz
  - New audio frequency: 4 kHz
- New Packet length: 784 bits
  - Data: 144 bits
  - Audio (0.01s): 640 bits
  - Throughput: 784 bits * (1/0.01s) = 78.4 kbps
- Minimum Required Sampling Frequency (before carrier mixer)
  - After TX processing/modulation: 7904 sym
  - Min Fs = 7904 sym * (1/0.01s) * 2 ~= 1.58 Msps

Demo

- Data generated from reading Config.txt
  - Loaded on zedboards for easy data configuration
  - On the fly updates to data bits transmitted
- Audio bits generated from 60 second audio binary file
  - Audio binary file generated from MATLAB reading 4 kHz .wav file
  - Final demo will save received audio data into binary file, and will be converted to .wav format in MATLAB
- Confirmed that Zedboard compiles with HUD code (libcurl/libev libraries)

Config.txt

```
1  V2X!
2  32.880100
3  -117.234000
4  60
5  3
6  5.3
```



RX Data Bits to Data Rate

Data Bits
784

After Coding
$784\frac{7}{3}$=1830

Symbol Mapping
(2 bits per sample)
1830/2=915

Add Preamble
915+32+32=979

x Message Rate
$979\frac{1}{0.01s}=$
$97900\ Symbol\ per\ second$

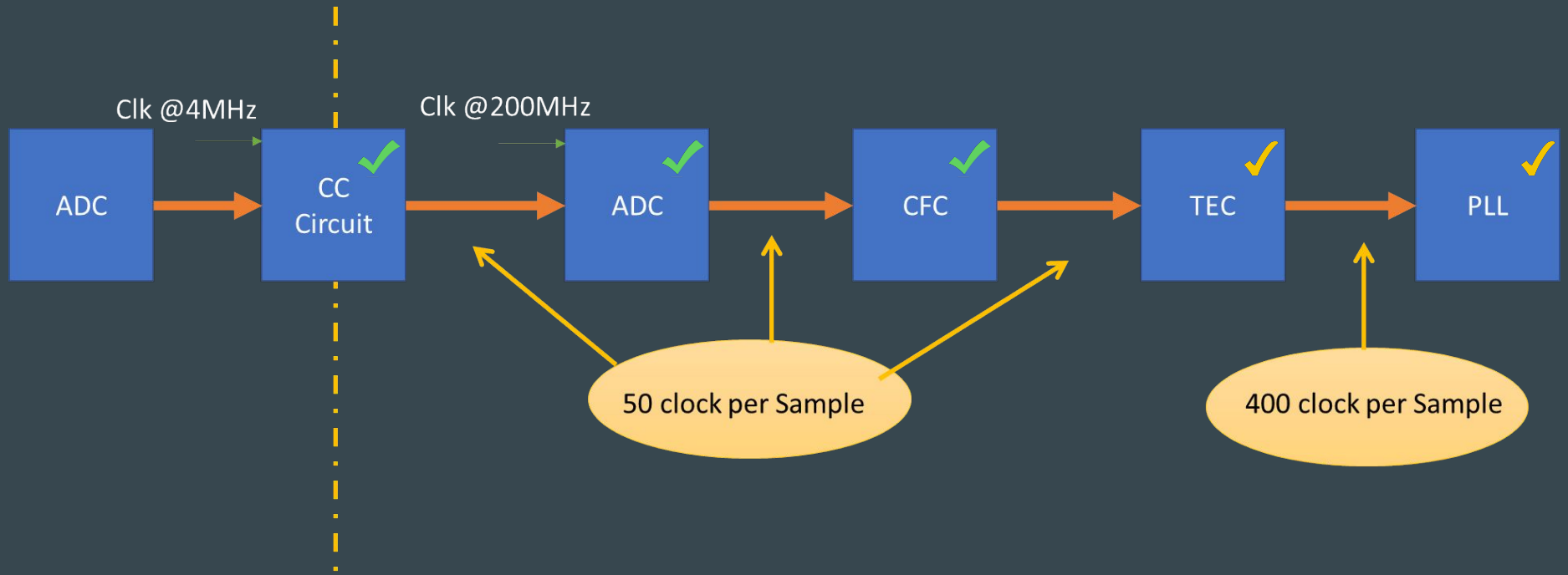
Upsample x8
8(97900)=0.7912 Msps

TDMA
(time Slot allocation)
4(0.7912 Msps)=
3.1648 MSPS

Round Up
4 Msps

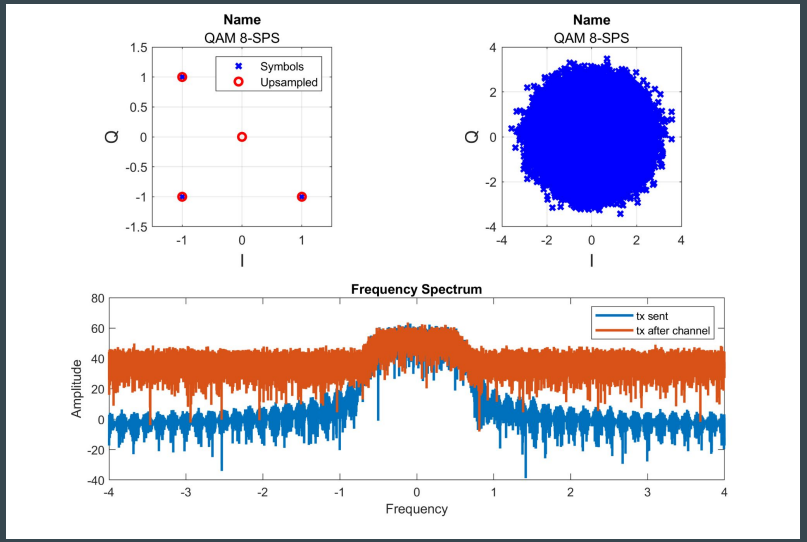
Given a Sample Clock Rate of 4MHz and FPGA System Clock Rate of 200MHZ, then we have about 50 clocks per sample.

Clocking Scheme (Able to Process Real Time)

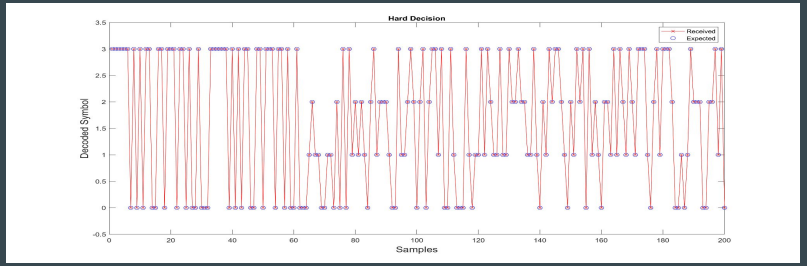


Matlab Model Updated

- Added additional channel effects:
  - Phase offset
  - SNR selection
- Investigated/Implemented
  - Timing Error Correction
  - PLL
  - hard decision decoder
- Model allows us to create test data for our HLS implementations.



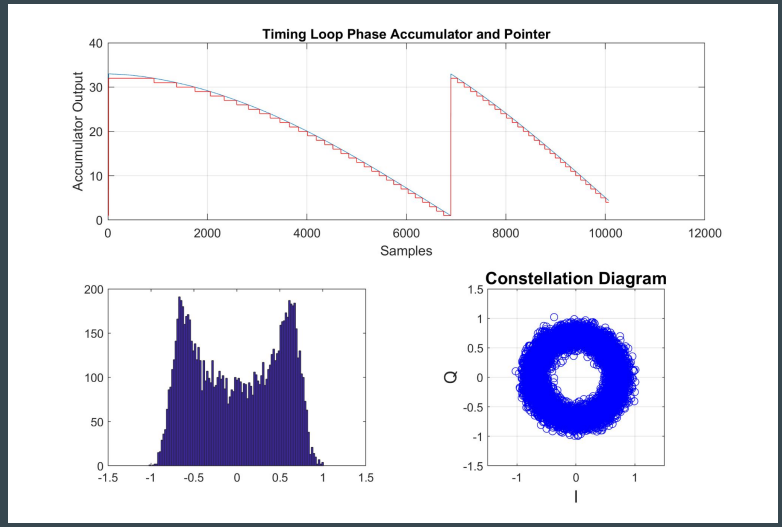
Channel Effects Output



Hard Decision Output

Timing Error Correction

- Uses 2 Polyphase filters (matched and derivative matched) to implement interpolation then selects optimal filter bank for timing.
- Implemented Matlab and HLS version.



Modules & Loops	Issue Type	Latency(cycles)	Latency(ns)	Interval	Pipelined	BRAM	DSP	FF	LUT
tec		54	540.000	50	yes	0	229	48218	17677
mf_pfb		53	530.000	50	yes	0	150	24192	8631
dmf_pfb		52	520.000	50	yes	0	70	23022	8035
tec_loopf		8	80.000	9	yes	0	9	743	670

Uh oh too many DSPs!!

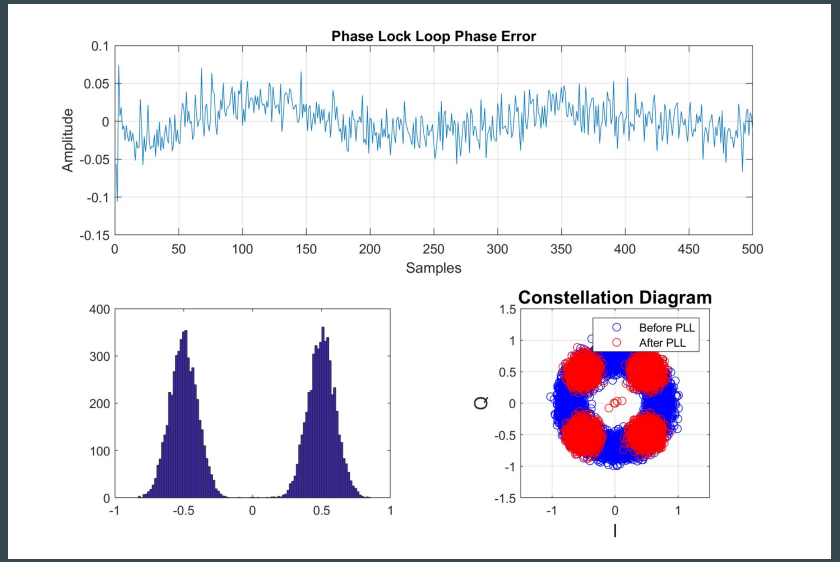
→

Modules & Loops	Issue Type	Latency(ns)	Interval	Pipelined	BRAM	DSP	FF	LUT
tec		430.000	44	no	9	33	11075	12398
tec_Pipeline_shift_loop		150.000	15	no	0	0	210	3110
tec_Pipeline_shift_loop1		150.000	15	no	0	0	210	3110
tec_Pipeline_macloop		190.000	19	no	6	16	1473	2620
tec_Pipeline_macloop2		190.000	19	no	3	8	1375	2620

Sometimes faster is not better

PLL

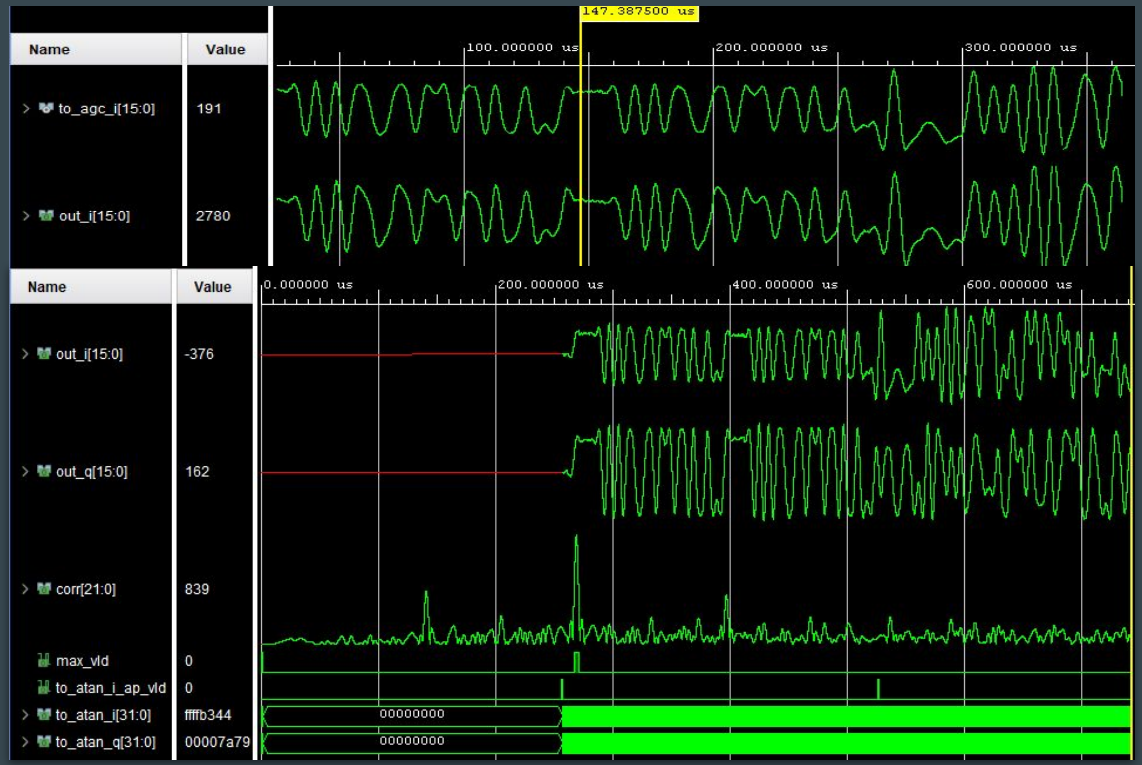
- Matlab and Vivado HLS version implemented.
  - Fixed point version complete.
  - Ready for integration into RX IP.



Modules & Loops	Issue Type	Latency(cycles)	Latency(ns)	Interval	Pipelined	BRAM	DSP	FF	LUT
pll		86	430.000	87	yes	0	8	3588	8510
cordic_circ_apfixed_18_3_0_s		30	150.000	31	yes	0	0	1146	3018
generic_atan2_16_2_s		27	135.000	28	yes	0	0	1747	4384

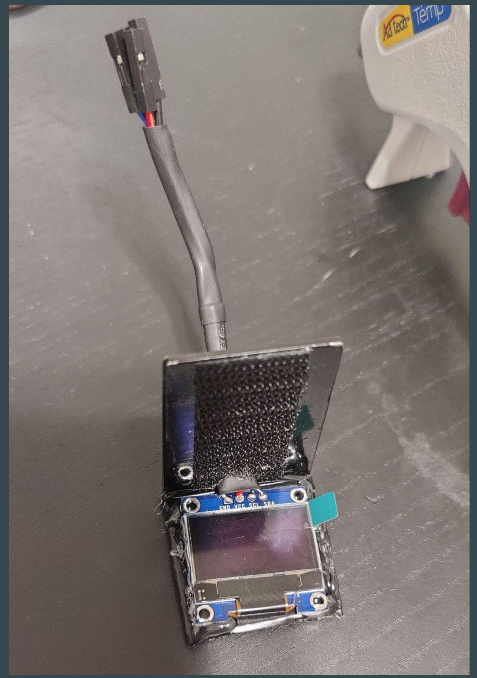
Verilog Testbench Status

- Verilog IP and testbench and currently have the following implemented:
  - Clock Crossing (4MHz → 200MHz)
  - AGC
  - SRRC Filter
  - Correlator (xcorr)
  - Timing Recovery (TEC) - Needs testing
  - Fine Frequency Correction (PLL) - Needs Testing



HUD

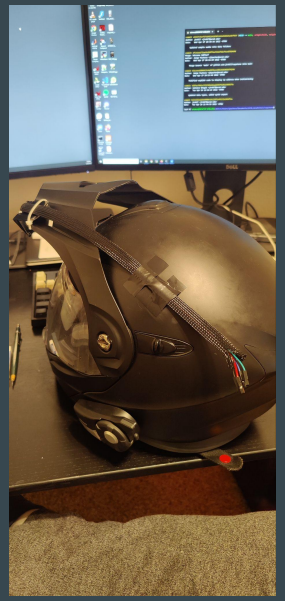
Created Bracket for OLED Display

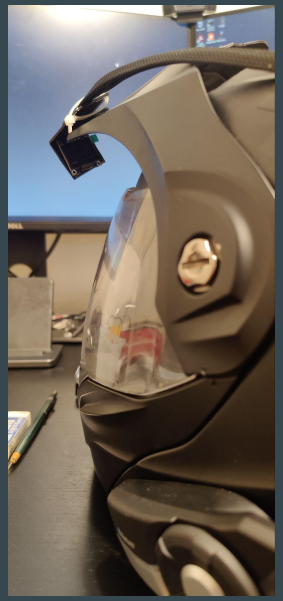


Created enclosure for WiFi Module (ESP8266)

HUD Cont.

- Attached OLED bracket to helmet's sun visor using velcro
- Ran connections through cable sleeve
- Measured clearance so that helmet's visor still clears



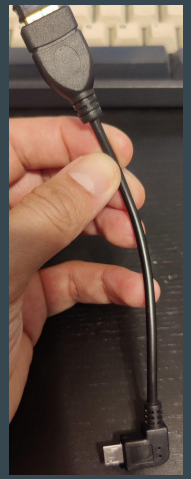


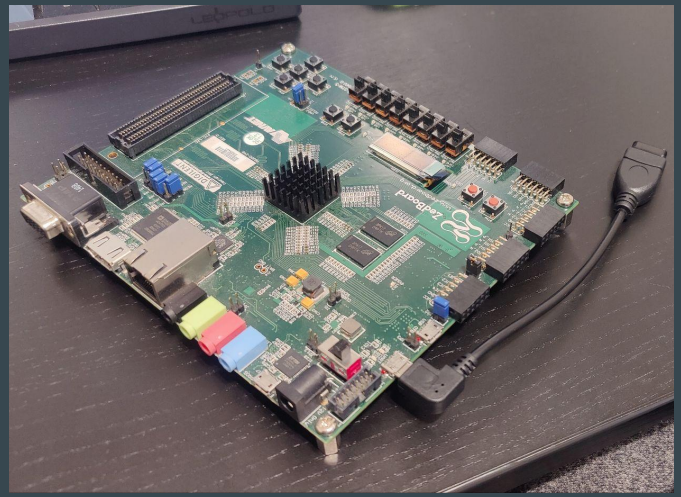
HUD Cont.

- Final Setup

RX Baseband and HUD

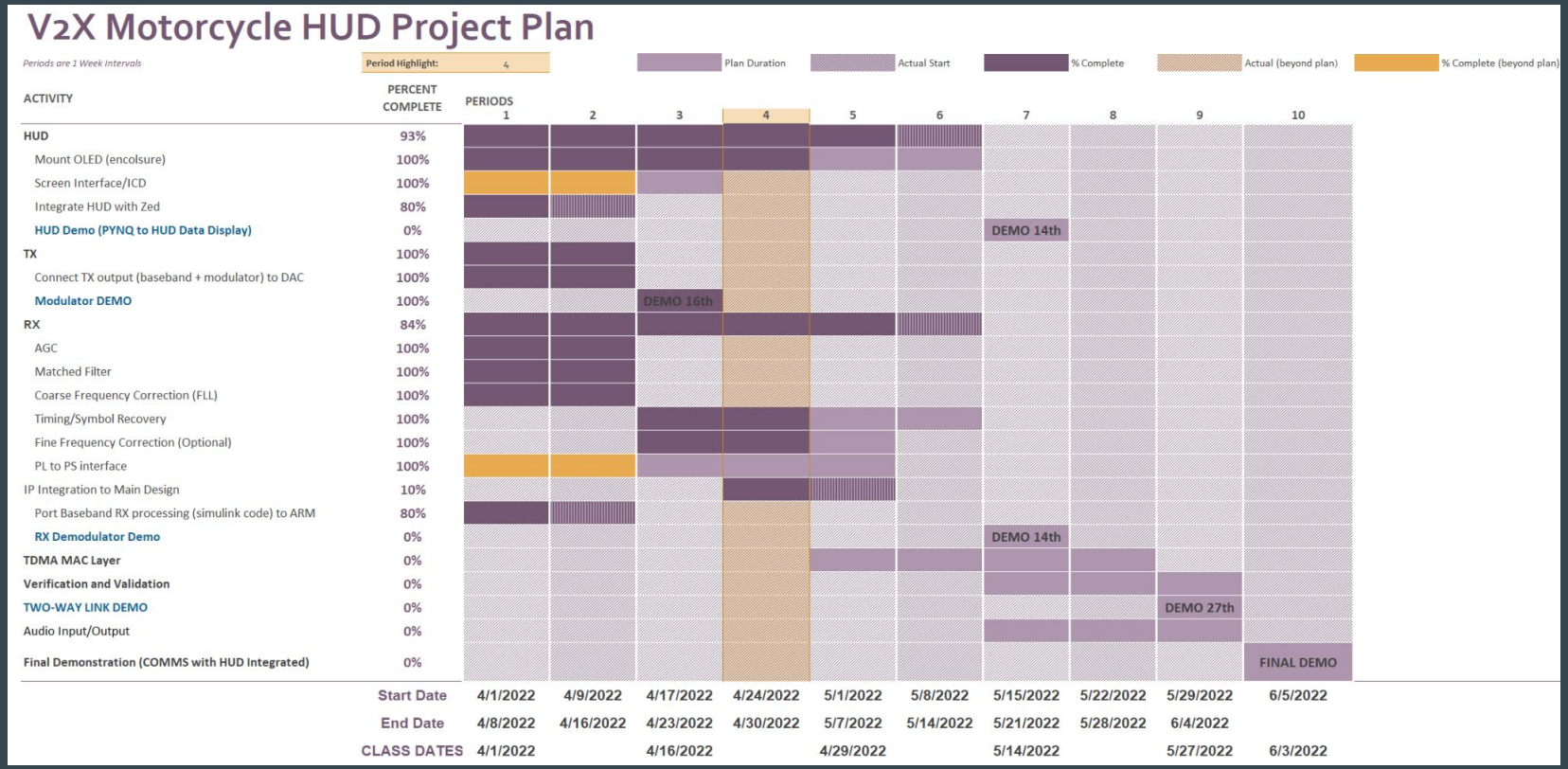
- Sourced USB WiFi adapter for Zedboard
- Still need to recompile kernel to interface with USB module...





Future Plans

Gantt (timeline)



Next Sprint

- Demo
  - Integrate audio files with TX modulator SW
  - Loopback test with TX/RX
- RX
  - Hard decision and store to FIFO
  - Finish verification via Verilog testbench
  - Package RX IP module and integrate to design
  - Integration with PL and RX Baseband software
- HUD
  - Update kernel on Pynq for USB
  - Verification and Validation (V&V)